

CMOS Analog Multiplexers/Demultiplexers*

With Logic-Level Conversion

High-Voltages Types (20-Volt Rating)

- CD4051B – Single 8-Channel
- CD4052B – Differential 4-Channel
- CD4053B – Triple 2-Channel

■ CD4051B, CD4052B, and CD4053B analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if $V_{DD}-V_{SS} = 3$ V, a $V_{DD}-V_{EE}$ of up to 13 V can be controlled; for $V_{DD}-V_{EE}$ level differences above 13 V, a $V_{DD}-V_{SS}$ of at least 4.5 V is required). For example, if $V_{DD} = +4.5$ V, $V_{SS} = 0$, and $V_{EE} = -13.5$ V, analog signals from -13.5 V to $+4.5$ V can be controlled by digital inputs of 0 to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are off.

The CD4051B is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

The CD4051B, CD4052B, and CD4053B are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), and in chip form (H suffix).

Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating

Features:

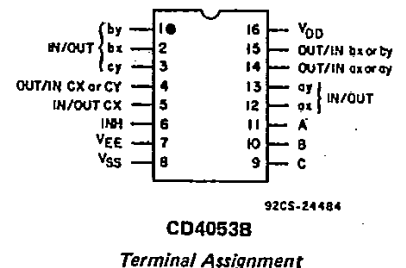
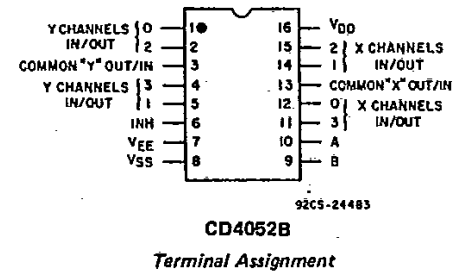
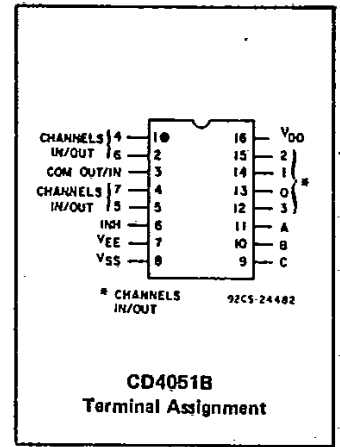
- Wide range of digital and analog signal levels: digital 3 to 20 V, analog to 20 V_{p-p}
- Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for $V_{DD}-V_{EE} = 15$ V
- High OFF resistance: channel leakage of ±100 pA (typ.) @ $V_{DD}-V_{EE} = 18$ V
- Logic-level conversion for digital addressing signals of 3 to 20 V ($V_{DD}-V_{SS} = 3$ to 20 V) to switch analog signals to 20 V p-p ($V_{DD}-V_{EE} = 20$ V); see introductory text
- Matched switch characteristics: $R_{ON} = 5$ Ω (typ.) for $V_{DD}-V_{EE} = 15$ V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μW (typ.) @ $V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10$ V
- Binary address decoding on chip
- 5-, 10-, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package temperature range: 100 nA at 18 V and 25°C
- Break-before-make switching eliminates channel overlap

RECOMMENDED OPERATING CONDITIONS AT T_A = 25°C (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

CHARACTERISTIC	V _{DD}	Min.	Max.	Units
Supply-Voltage Range (T _A = Full Package-Temp. Range)	—	3	18	V
Multiplexer Switch Input Current Capability*	—	—	25	mA
Output Load Resistance	—	100	—	Ω

* In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 3 on the CD4051; terminals 3 and 13 on the CD4052; terminals 4, 14, and 15 on the CD4053.



* When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -85°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 \pm 1/32 Inch (1.59 \pm 0.79mm) from case for 10s max $+265^\circ\text{C}$

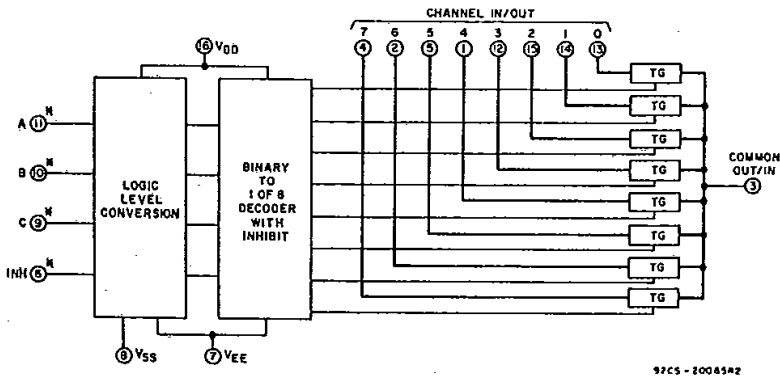


Fig. 1 - Functional diagram of CD4051B.

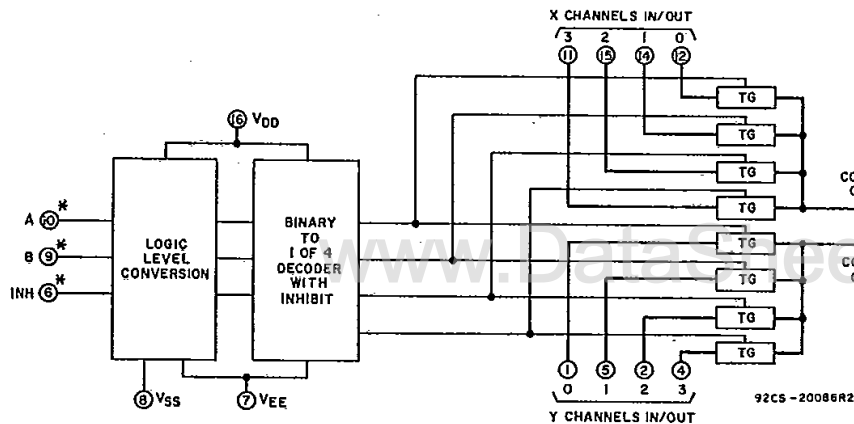


Fig. 2 - Functional diagram of CD4052B.

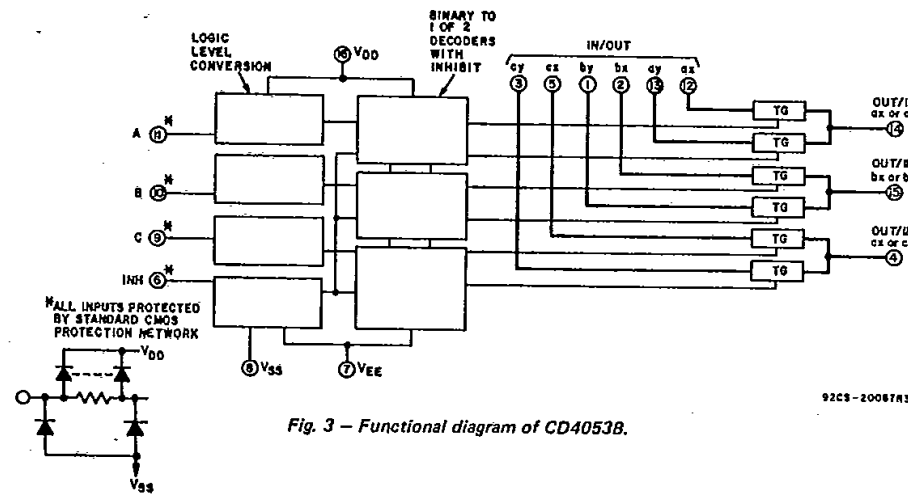


Fig. 3 - Functional diagram of CD4053B.

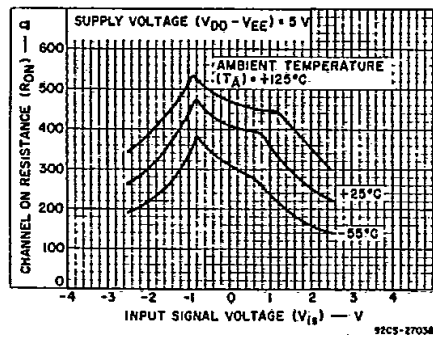


Fig. 4 - Typical channel ON resistance vs input signal voltage (all types).

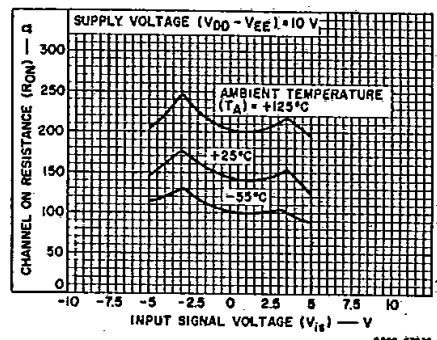


Fig. 5 - Typical channel ON resistance vs input signal voltage (all types).

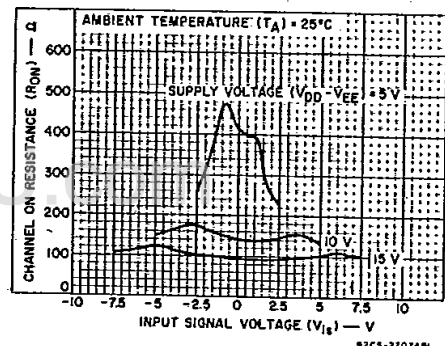


Fig. 6 - Typical channel ON resistance vs input signal voltage (all types).

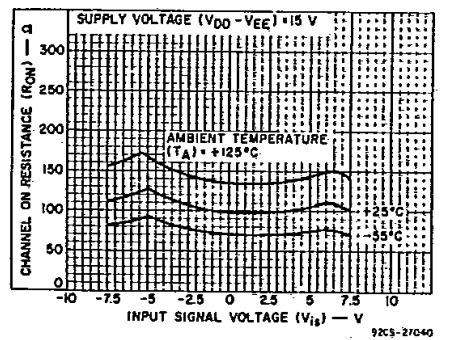


Fig. 7 - Typical channel ON resistance vs input signal voltage (all types).

COMMERCIAL CMOS HIGH VOLTAGE ICs

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS				LIMITS AT INDICATED TEMPERATURES							Units	
	V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	(°C)								
					-55	-40	+85	+125	+25				
											Min.	Typ.	Max.
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})													
Quiescent Device Current, I_{DD} Max.				5	5	5	150	150	-	0.04	5	μ A	
				10	10	10	300	300	-	0.04	10		
				15	20	20	600	600	-	0.04	20		
				20	100	100	3000	3000	-	0.08	100		
On-State Resistance $0 \leq V_{IS} \leq V_{DD}$ r_{on} Max.												Ω	
	0	0	5	800	850	1200	1300	-	470	1050			
	0	0	10	310	330	520	550	-	180	400			
	0	0	15	200	210	300	320	-	125	240			
Change in On-State Resistance (Between Any Two Channels) Δr_{on}												Ω	
	0	0	5	-	-	-	-	-	15	-			
	0	0	10	-	-	-	-	-	10	-			
	0	0	15	-	-	-	-	-	5	-			
OFF Channel Leakage Current: Any Channel OFF Max. or All Channels OFF (Common OUT/IN) Max.												nA	
	0	0	18	$\pm 100^*$	$\pm 1000^*$	-	± 0.01	$\pm 100^*$					
Capacitance: Input, C_{IS} Output, C_{OS} CD4051 CD4052 CD4053										5		pF	
										30			
										18			
										9			
Feedthrough, C_{IOS}										0.2			
Propagation Delay Time (Signal Input to Output)	V_{DD} 	$R_L = 200 \text{ k}\Omega$ $C_L = 50 \text{ pF}$ $t_r, t_f = 20 \text{ ns}$	5	-	-	-	-	-	-	30	60	ns	
			10	-	-	-	-	-	15	30			
			15	-	-	-	-	-	10	20			

* Determined by minimum feasible leakage measurement for automatic testing.

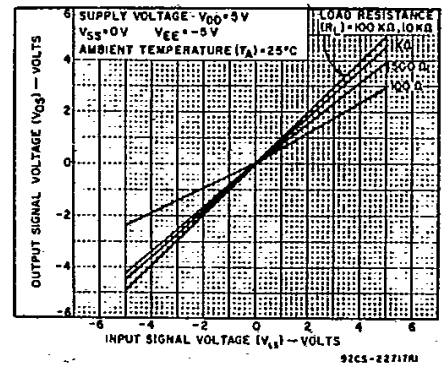


Fig.8 - Typical ON characteristics for 1 of 8 channels (CD4051B).

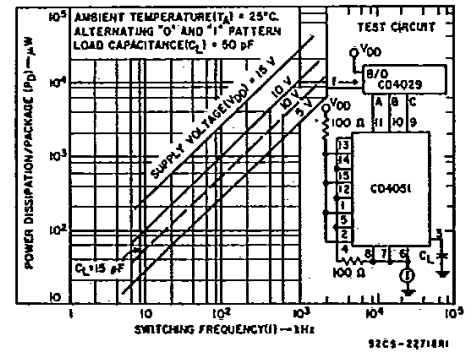


Fig.9 - Typical dynamic power dissipation vs. switching frequency (CD4051B).

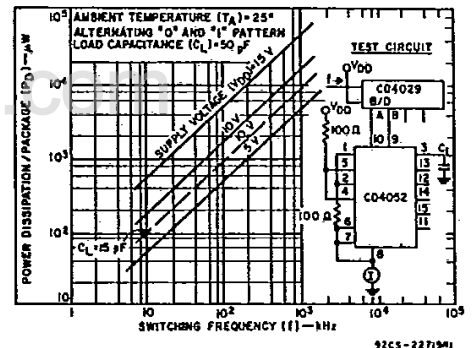


Fig.10 - Typical dynamic power dissipation vs. switching frequency (CD4052B).

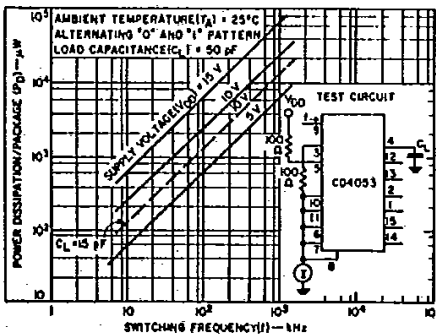
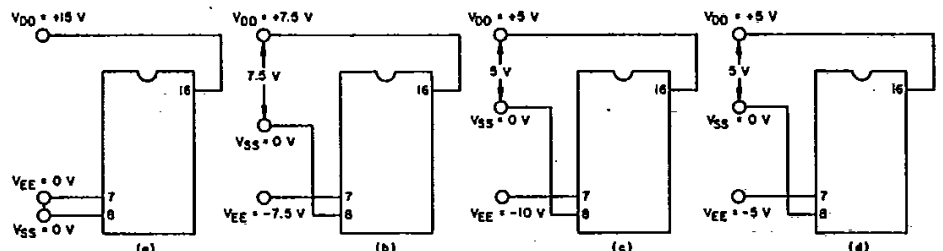


Fig.11 - Typical dynamic power dissipation vs. switching frequency (CD4053B).



The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = V_{SS} and "1" = V_{DD} . The analog signal (through the TG) may swing from V_{EE} to V_{DD} .

Fig.12 - Typical bias voltages.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS				LIMITS AT INDICATED TEMPERATURES							Units	
	V _{IS} (V)	V _{EE} (V)	V _{SS} (V)	V _{DD} (V)	(°C)								
					-55	-40	+85	+125	+25				
											Min.	Typ.	Max.
CONTROL (ADDRESS or INHIBIT) V_C													
Input Low Voltage, V _{IL} Max.	=V _{DD} thru 1 kΩ	V _{EE} =V _{SS} R _L =1 kΩ to V _{SS} I _{IS} < 2 μA on all OFF Channels	5	1.5			-	-	1.5				
			10	3			-	-	3				
			15	4			-	-	4				
			5	3.5			3.5	-	-				
Input High Voltage, V _{IH} Min.			10	7			7	-	-				
			15	11			11	-	-				
Input Current, I _{IN} Max.	V _{IN} = 0,18		18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA		
Propagation Delay Time: Address-to-Signal OUT (Channels ON or OFF) See Figs.14,15,18	t _r , t _f = 20 ns, C _L = 50 pF R _L = 10k Ω												
			0	0	5	-	-	-	-	450	720		
			0	0	10	-	-	-	-	160	320		
			0	0	15	-	-	-	-	120	240		
			-5	0	5	-	-	-	-	225	450		
Inhibit-to-Signal OUT (Channel turning ON) See Fig. 14	R _L = 10k Ω, C _L = 50 pF t _r , t _f = 20 ns												
			0	0	5	-	-	-	-	400	720		
			0	0	10	-	-	-	-	160	320		
			0	0	15	-	-	-	-	120	240		
			-10	0	5	-	-	-	-	200	400		
Inhibit-to-Signal OUT (Channel turning OFF) See Fig. 15	R _L = 1k Ω, C _L = 50 pF t _r , t _f = 20 ns												
			0	0	5	-	-	-	-	200	450		
			0	0	10	-	-	-	-	90	210		
			0	0	15	-	-	-	-	70	160		
			-10	0	5	-	-	-	-	130	300		
Input Capacitance, C _{IN} (Any Address or Inhibit Input)										5	7.5		
											pF		

INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE
CD4052B				
INHIBIT	B	A		
0	0	0	0x, 0y	
0	0	1	1x, 1y	
0	1	0	2x, 2y	
0	1	1	3x, 3y	
1	X	X	NONE	
CD4053B				
INHIBIT	A or B or C			
0	0	ax or bx or cx		
0	1	ay or by or cy		
1	X	NONE		

X = Don't care

Fig. 13 - Truth tables.

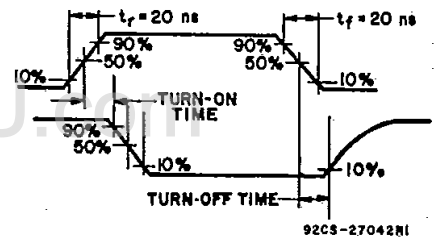


Fig. 14 - Waveforms, channel being turned ON (R_L = 1 kΩ).

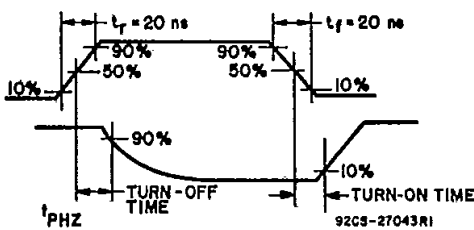


Fig. 15 - Waveforms, channel being turned OFF (R_L = 1k Ω).

TEST CIRCUITS

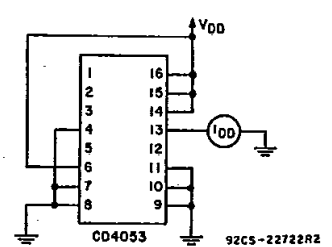
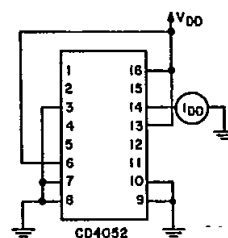
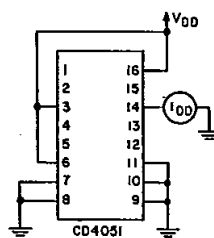


Fig. 16 - OFF channel leakage current - any channel OFF.

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CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS	
	V _{is} (V)	V _{DD} (V)	R _L (kΩ)	TYPICAL VALUE			
Cutoff (-3-dB) Frequency Channel ON (Sine Wave Input)	5*	10	1	CD4053	30	MHz	
	V _{EE} = V _{SS} , 20 log $\frac{V_{os}}{V_{is}} = -3\text{dB}$			V _{os} at Common OUT/IN	CD4052		25
				V _{os} at Any Channel			60
Total Harmonic Distortion, THD	2*	5	10			0.3	%
	3*	10				0.2	
	5*	15				0.12	
	V _{EE} = V _{SS} , f _{is} = 1 kHz sine wave						
-40-dB Feedthrough Frequency (All Channels OFF)	5*	10	1	CD4053	8	MHz	
	V _{EE} = V _{SS} , 20 log $\frac{V_{os}}{V_{is}} = -40\text{dB}$			V _{os} at Common OUT/IN	CD4052		10
				V _{os} at Any Channel			8
-40-dB Signal Crosstalk, Frequency				Between Any 2 Channels		3	MHz
	5*	10	1	Between Sections	Measured on Common	6	
	V _{EE} = V _{SS} , 20 log $\frac{V_{os}}{V_{is}} = -40\text{dB}$			CD4052 Only	Measured on Any Channel	10	
				Between Any 2 Sections	In Pin 2, Out Pin 14	2.5	
				CD4053 Only	In Pin 15, Out Pin 14	6	
Address-or-Inhibit-to Signal Crosstalk	-	10	10#			65	mV (Peak)

* Peak-to-peak voltage symmetrical about V_{DD} - V_{EE}

Both ends of channel

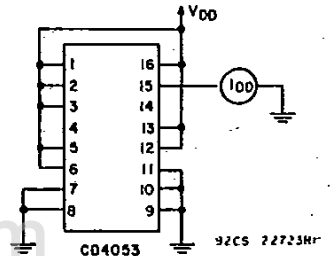
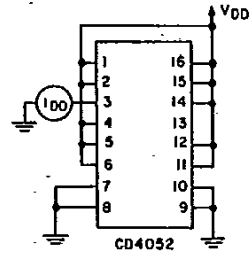
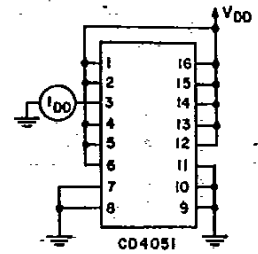


Fig.17 - OFF channel leakage current - all channels OFF.

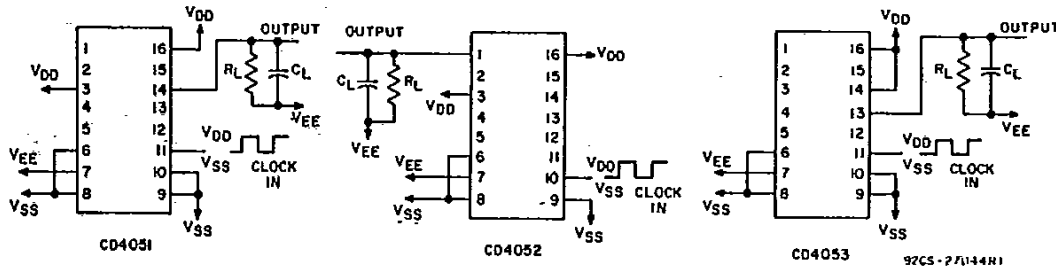


Fig.18 - Propagation delay - address input to signal output.

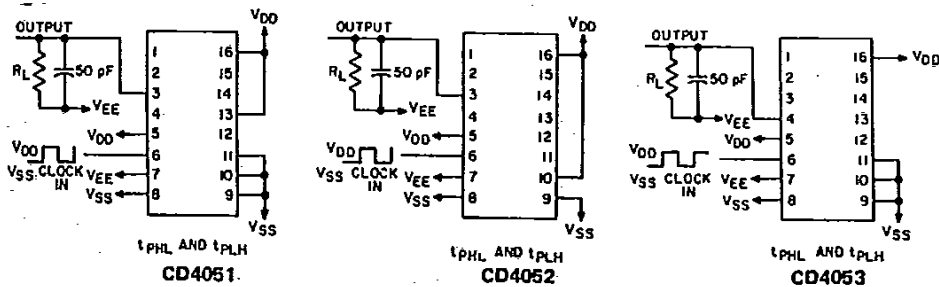
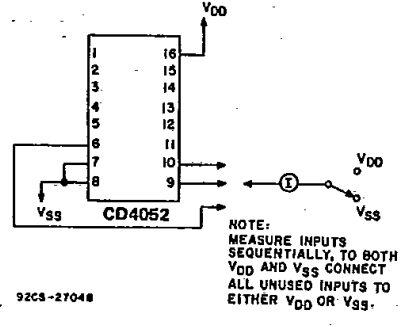
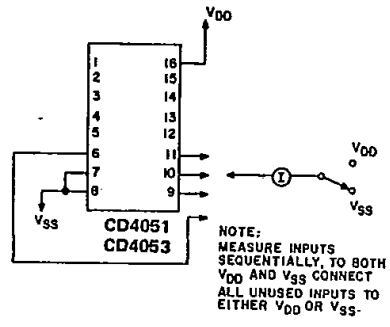
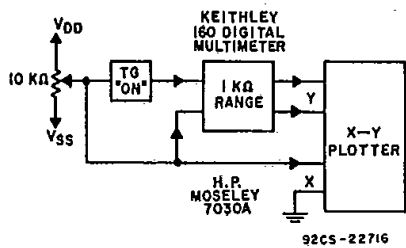
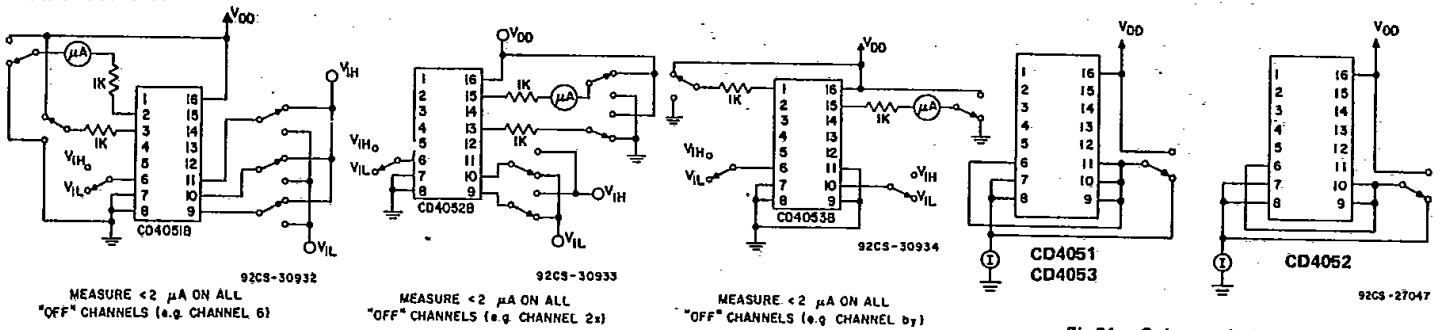
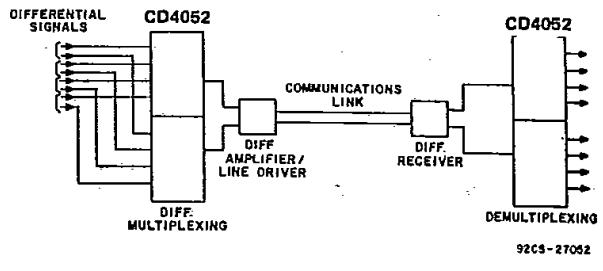
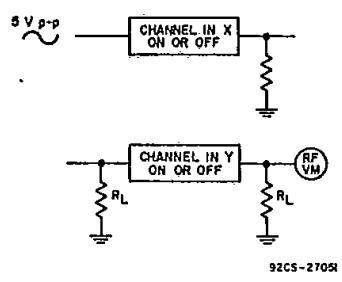
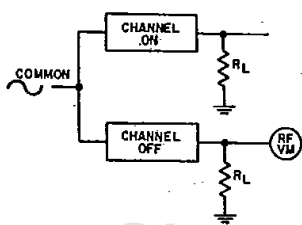
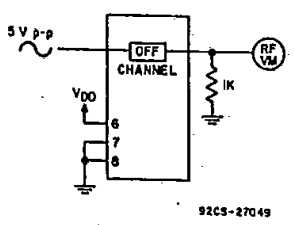


Fig.19 - Propagation delay - inhibit input to signal output.



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SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4051B, CD4052B, or CD4053B.

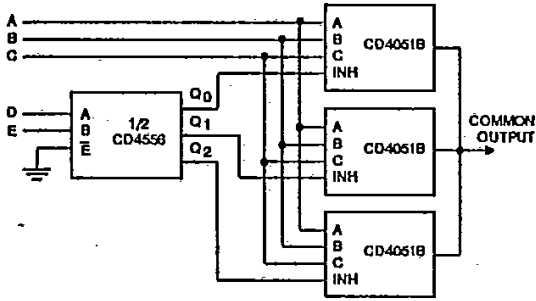
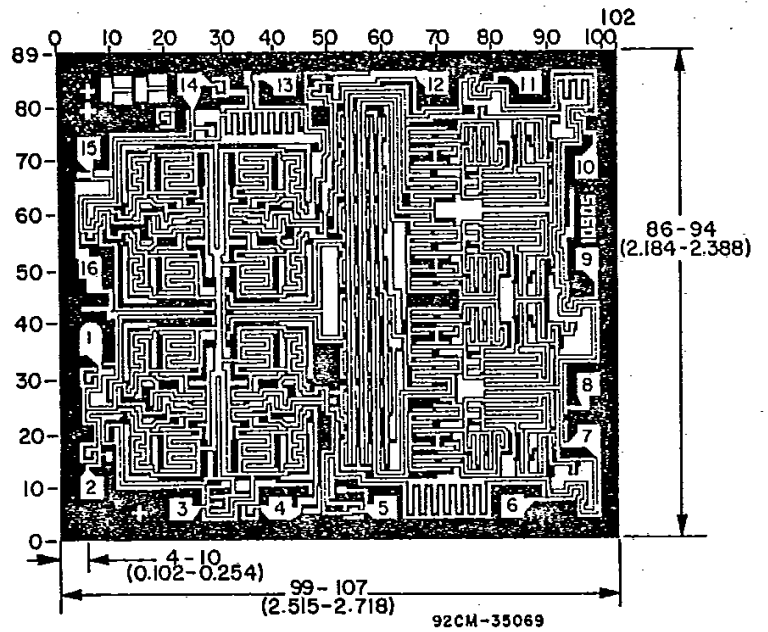
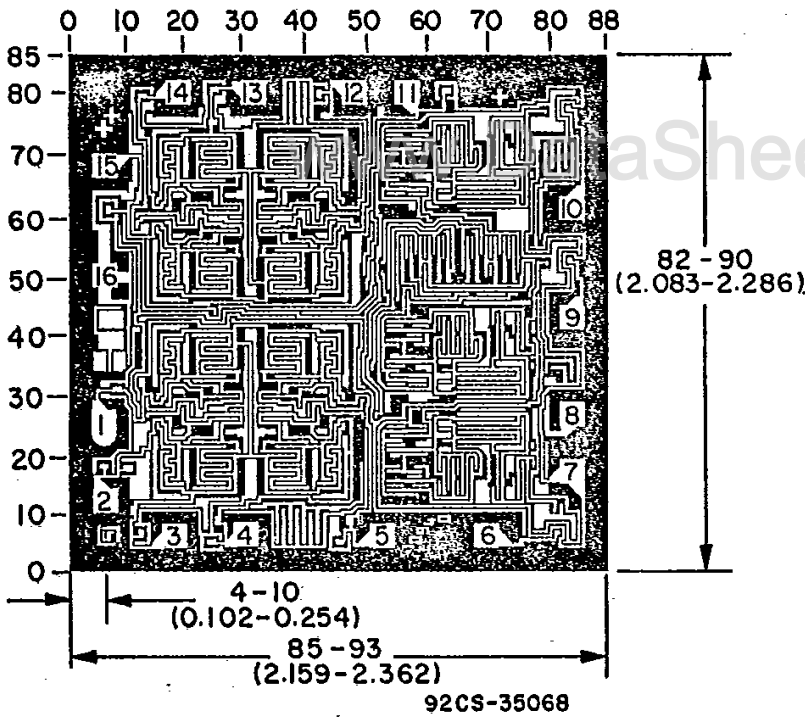


Fig.28 - 24-16-1 MUX Addressing

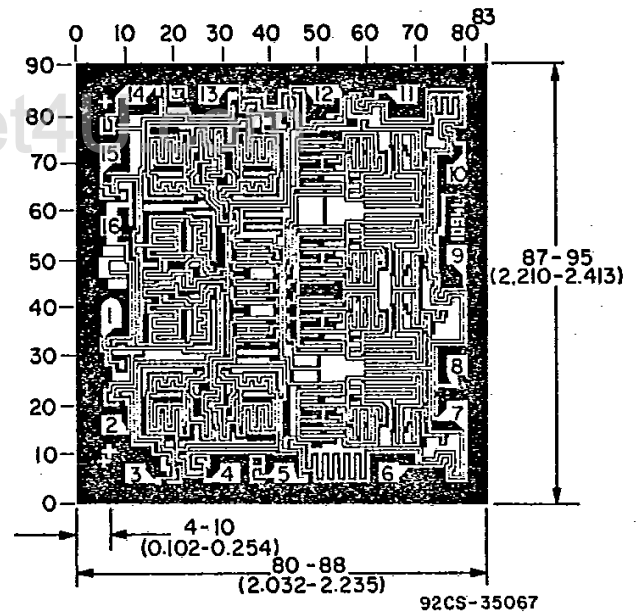


Dimensions and pad layout for CD4051BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid Graduations are in Mils (10^{-3} inch).



Dimensions and pad layout for CD4052BH.



Dimensions and pad layout for CD4053BH.