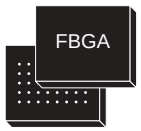
M69AR024B

16 Mbit (1M x16) 1.8V Supply, Asynchronous PSRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE: 1.7 to 2.25V
- ACCESS TIME: 70ns, 80ns
- LOW STANDBY CURRENT: 110µA
- DEEP POWER DOWN CURRENT: 10µA
- COMPATIBLE WITH STANDARD LPSRAM
- TRI-STATE COMMON I/O

Figure 1. Package



TFBGA48 (ZB)
6x8mm

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SUMMARY DESCRIPTION

The M69AR024B is a 16 Mbit (16,777,216 bit) CMOS memory, organized as 1,048,576 words by 16 bits, and is supplied by a single 1.7V to 2.25V supply voltage range.

M69AR024B is a member of STMicroelectronics 1T/1C (one transistor per cell) memory family. These devices are manufactured using dynamic random access memory cells, to minimize the cell size, and maximize the amount of memory that can be implemented in a given area.

However, through the use of internal control logic, the device is fully static in its operation, requiring no external clocks or timing strobes, and has a standard Asynchronous SRAM Interface.

The internal control logic of the M69AR024B handles the periodic refresh cycle, automatically, and without user involvement.

Write cycles can be performed on a single byte by using Upper Byte Enable ($\overline{UB}$) and Lower Byte Enable ($\overline{LB}$).

The device can be put into standby mode using Chip Enable ($\overline{E1}$) or in deep power down mode by using Chip Enable (E2).

Power-Down mode achieves a very low current consumption by halting all the internal activities. Since the refresh circuitry is halted, the duration of the power-down should be less than the maximum period for refresh, if the user has not finished with the data contents of the memory.

Figure 2. Logic Diagram

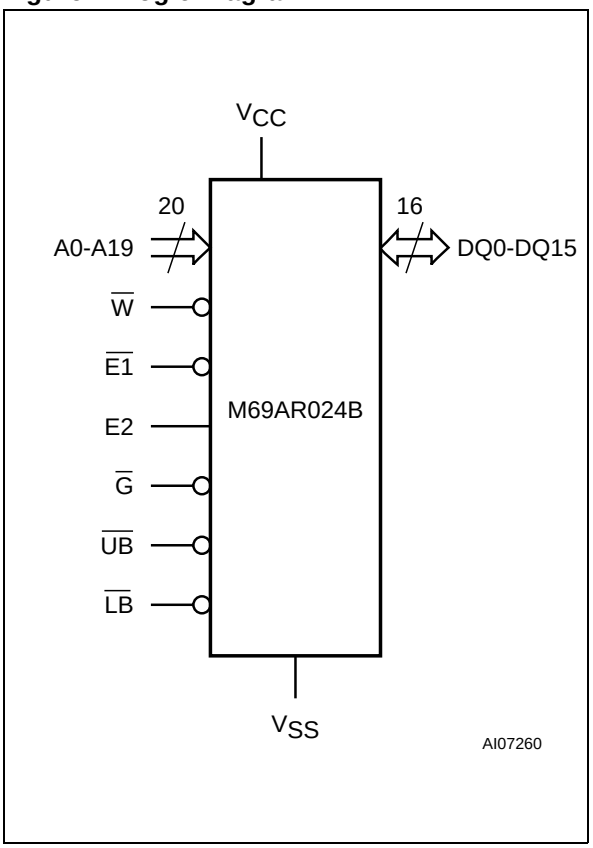
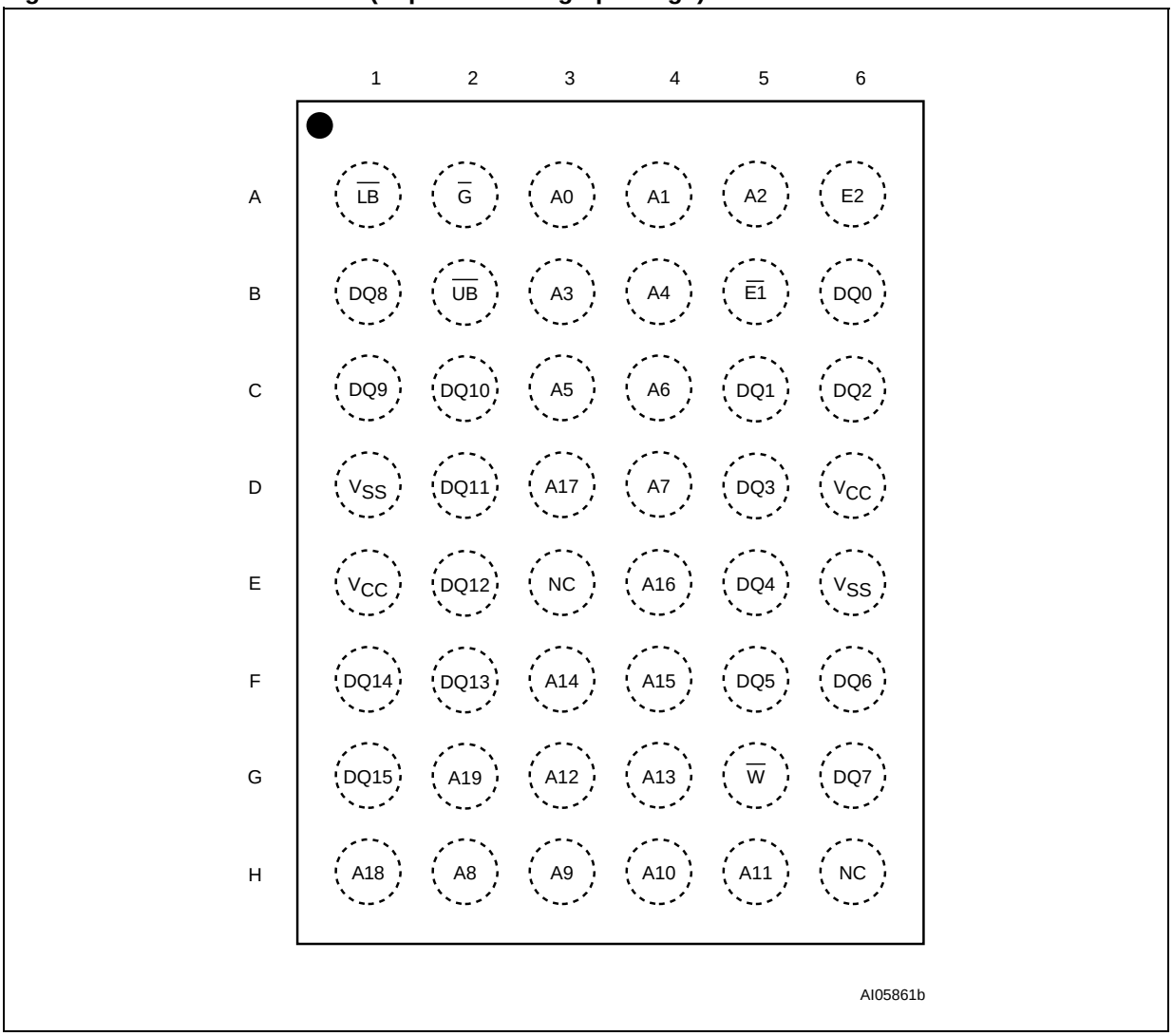


Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected (no internal connection)

Figure 3. TFBGA Connections (Top view through package)



SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram, and Table 1., Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A19). The Address Inputs select the cells in the memory array to access during Read and Write operations.

Data Inputs/Outputs (DQ8-DQ15). The Upper Byte Data Inputs/Outputs carry the data to or from the upper part of the selected address during a Write or Read operation, when Upper Byte Enable ($\overline{UB}$) is driven Low.

Data Inputs/Outputs (DQ0-DQ7). The Lower Byte Data Inputs/Outputs carry the data to or from the lower part of the selected address during a Write or Read operation, when Lower Byte Enable ($\overline{LB}$) is driven Low.

Chip Enable ($\overline{E1}$). When asserted (Low), the Chip Enable, $\overline{E1}$, activates the memory state machine, address buffers and decoders, allowing Read and Write operations to be performed. When de-asserted (High), all other pins are ignored, and the device is put, automatically, in low-power Standby mode.

Chip Enable (E2). The Chip Enable, E2, puts the device in Deep Power-down mode when it is driven Low. This is the lowest power mode.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the device.

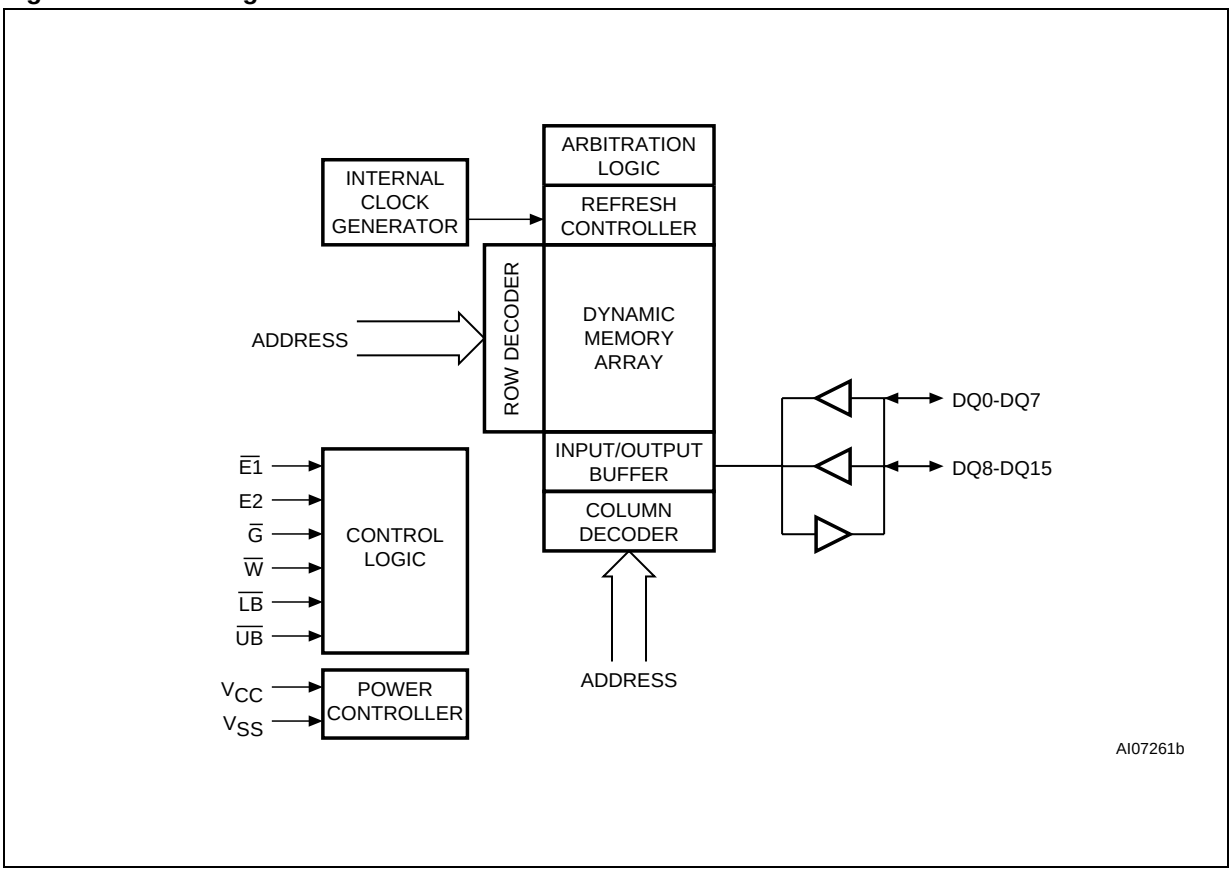
Upper Byte Enable ($\overline{UB}$). The Upper Byte Enable, $\overline{UB}$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

Lower Byte Enable ($\overline{LB}$). The Lower Byte Enable, $\overline{LB}$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

V_{CC} Supply Voltage. The V_{CC} Supply Voltage supplies the power for all operations (Read or Write) and for driving the refresh logic, even when the device is not being accessed.

V_{SS} Ground. The V_{SS} Ground is the reference for all voltage measurements.

Figure 4. Block Diagram



OPERATION

Operational modes are determined by device control inputs $\overline{W}$, $\overline{E1}$, E2, $\overline{LB}$ and $\overline{UB}$ as summarized in the Operating Modes table (see Table 2., Operating Modes).

Power Up Sequence

Because the internal control logic of the M69AR024B needs to be initialized, the following power-on procedure must be followed before the memory is used:

- Apply power and wait for V_{CC} to stabilize
- Wait 300µs while driving both Chip Enable signals ($\overline{E1}$ and E2) High

Read Mode

The device is in Read mode when:

- Write Enable ($\overline{W}$) is High and
- Output Enable ($\overline{G}$) Low and
- Upper Byte Enable ($\overline{UB}$) or Lower Byte Enable ($\overline{LB}$) is Low, or both
- the two Chip Enable signals are asserted ($\overline{E1}$ is Low, and E2 is High).

The time taken to enter Read mode (t_{ELQV}, t_{GLQV} or t_{BLQV}) depends on which of the above signals was the last to reach the appropriate level.
Data out (DQ15-DQ0) may be indeterminate during t_{ELQX}, t_{GLQX} and t_{BLQX}, but data will always be valid during t_{AVQV}.

Write Mode

The device is in Write mode when

- Write Enable ($\overline{W}$) is Low and
- Upper Byte Enable ($\overline{UB}$) or Lower Byte Enable ($\overline{LB}$) is Low, or both
- the two Chip Enable signals are asserted ($\overline{E1}$ is Low, and E2 is High).

The Write cycle begins just after the event (the falling edge) that causes the last of these conditions to become true (t_{AVWL} or t_{AVEL} or t_{AVBL}).
The Write cycle is terminated by the earlier of a rising edge on Write Enable ($\overline{W}$) or Chip Enable ($\overline{E1}$).
If the device is in Write mode (Chip Enable ($\overline{E1}$) is Low, Output Enable ($\overline{G}$) is Low, Upper Byte Enable ($\overline{UB}$) or Lower Byte Enable ($\overline{LB}$) is Low), then Write Enable ($\overline{W}$) will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable ($\overline{W}$), for t_{DVEH} before the rising edge of Chip Enable ($\overline{E1}$), or for t_{DVBH} before the rising edge of Byte Enable ($\overline{LB}$,$\overline{UB}$), whichever occurs first, and remain valid for t_{WHDZ}, t_{EHDZ} or t_{BHDZ}.

Standby Mode

The device is in Standby mode when:

- Chip Enable ($\overline{E1}$) is High and
- Chip Enable (E2) is High

The input/output buffers and the decoding/control logic are switched off, but the dynamic array continues to be refreshed. In this mode, the memory current consumption, I_{SB}, is reduced, and the data remains valid.

Deep Power-down Mode

The device is in Deep Power-down mode when:

- Chip Enable (E2) is Low

Table 2. Operating Modes

Operation	E2	$\overline{E1}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	A0-A19	DQ0-DQ7	DQ8-DQ15	I_{CC}	Data Retention
Standby (Deselect)	V_{IH}	V_{IH}	X (1)	X (1)	X (1)	X (1)	X (1)	Hi-Z	Hi-Z	I_{SB}	Yes
Output Disabled	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X (1)	X (1)	Note (4)	Hi-Z	Hi-Z	I_{CC}	Yes
Output Disabled (No Read) (2)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Valid	Hi-Z	Hi-Z	I_{CC}	Yes
Upper Byte Read (2)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Valid	Hi-Z	Output Valid	I_{CC}	Yes
Lower Byte Read (2)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Valid	Output Valid	Hi-Z	I_{CC}	Yes
Word Read (2)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Valid	Output Valid	Output Valid	I_{CC}	Yes
No Write (2)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Valid	Invalid	Invalid	I_{CC}	Yes
Upper Byte Write (2)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Valid	Invalid	Input Valid	I_{CC}	Yes
Lower Byte Write (2)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Valid	Input Valid	Invalid	I_{CC}	Yes
Word Write (2)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Valid	Input Valid	Input Valid	I_{CC}	Yes
Power-down (3)	V_{IL}	X (1)	X (1)	X (1)	X (1)	X (1)	X (1)	Hi-Z	Hi-Z	I_{PD}	Yes/No

Note: 1. X = V_{IH} or V_{IL}.
2. Should not be kept in this logic condition longer than 1µs. Please contact your local ST sales office for the relaxation of 1µs limitation.
3. Power-down mode can be entered from the Standby state, and all DQ pins are in High-Z state.
4. Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

MAXIMUM RATING

Stressing the device above the rating listed in the “Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
I_O	Output Current	–50	50	mA
T_A	Ambient Operating Temperature	–30	85	°C
T_{STG}	Storage Temperature	–55	125	°C
V_{CC}	Core Supply Voltage	–0.2	3.3	V
V_{IO} (1,2)	Input or Output Voltage	–0.2	3.3	V

Note: 1. The minimum DC voltage on input or I/O pins is –0.3V. During voltage transitions, inputs may undershoot V_{SS} by 1.0V for periods of up to 5ns.
2. The maximum DC voltage on input and I/O pins is V_{CC}+0.2V. During voltage transitions, inputs may overshoot V_{CC} by 1.0V for periods of up to 5ns.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter	M69AR024B		Unit
	Min	Max	
V_{CC} Supply Voltage[1]	1.7	2.25	V
Ambient Operating Temperature	–30	85	°C
Load Capacitance (C_L)	50		pF
Output Circuit Protection Resistance (R_1)	50		Ω
Input Pulse Voltages	0 to V_{CC}		V
Input and Output Timing Ref. Voltages	$V_{CC}/2$		V
Output Transition Timing Ref. Voltages	$V_{RL} = 0.3V_{CC}$; $V_{RH} = 0.7V_{CC}$		V

Note: 1. All voltages are referenced to V_{SS}.

Figure 5. AC Measurement I/O Waveform

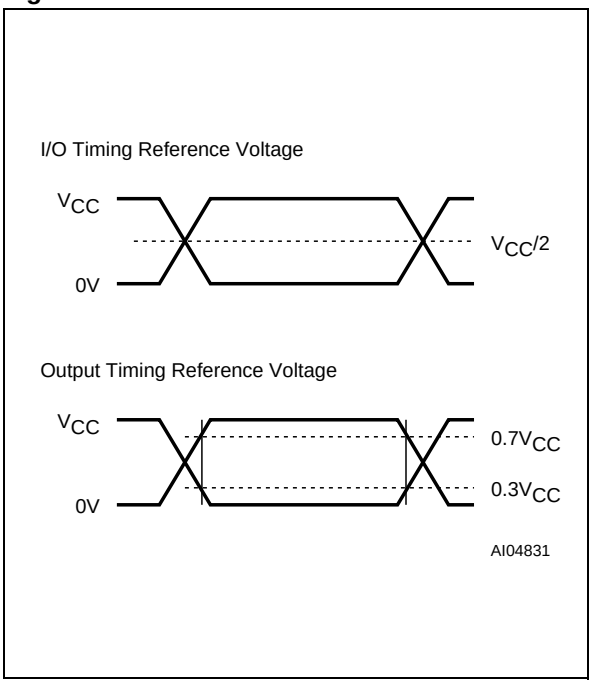


Figure 6. AC Measurement Load Circuit

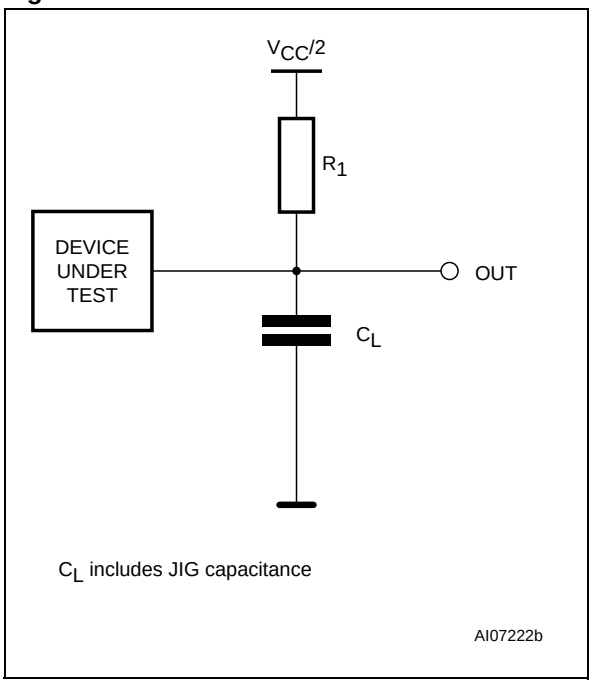


Table 5. Capacitance

Symbol	Parameter[1,2]	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		5	pF
C_{OUT} [2]	Output Capacitance	V_{OUT} = 0V		8	pF

Note: 1. Sampled only, not 100% tested.
2. Outputs deselected.

Table 6. DC Characteristics

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{CC1}	V_{CC} Active Current	V_{CC} = 2.25V, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{E1} = V_{IL}$ and E2 = V_{IH}, I_{OUT} = 0mA	t_{AVAV} Read / t_{AVAV} Write = minimum		20	mA
I_{CC2}			t_{AVAV} Read / t_{AVAV} Write = maximum		3	mA
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		–1	1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		–1	1	µA
I_{PD}	Deep Power Down Current	V_{CC} = 2.25V, $\overline{E1} \ge V_{CC} - 0.2V$ or $\overline{E1} \le V_{IL}$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$			10	µA
I_{SB}	Standby Supply Current CMOS	V_{CC} = 2.25V, $\overline{E1}$ = E2 ≥ V_{CC} – 0.2V, I_{OUT} = 0mA			110	µA
V_{IH} [1]	Input High Voltage			$0.8V_{CC}$	V_{CC} + 0.2	V
V_{IL} [2]	Input Low Voltage			–0.3	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.5mA		V_{CC} – 0.2		V
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.2	V

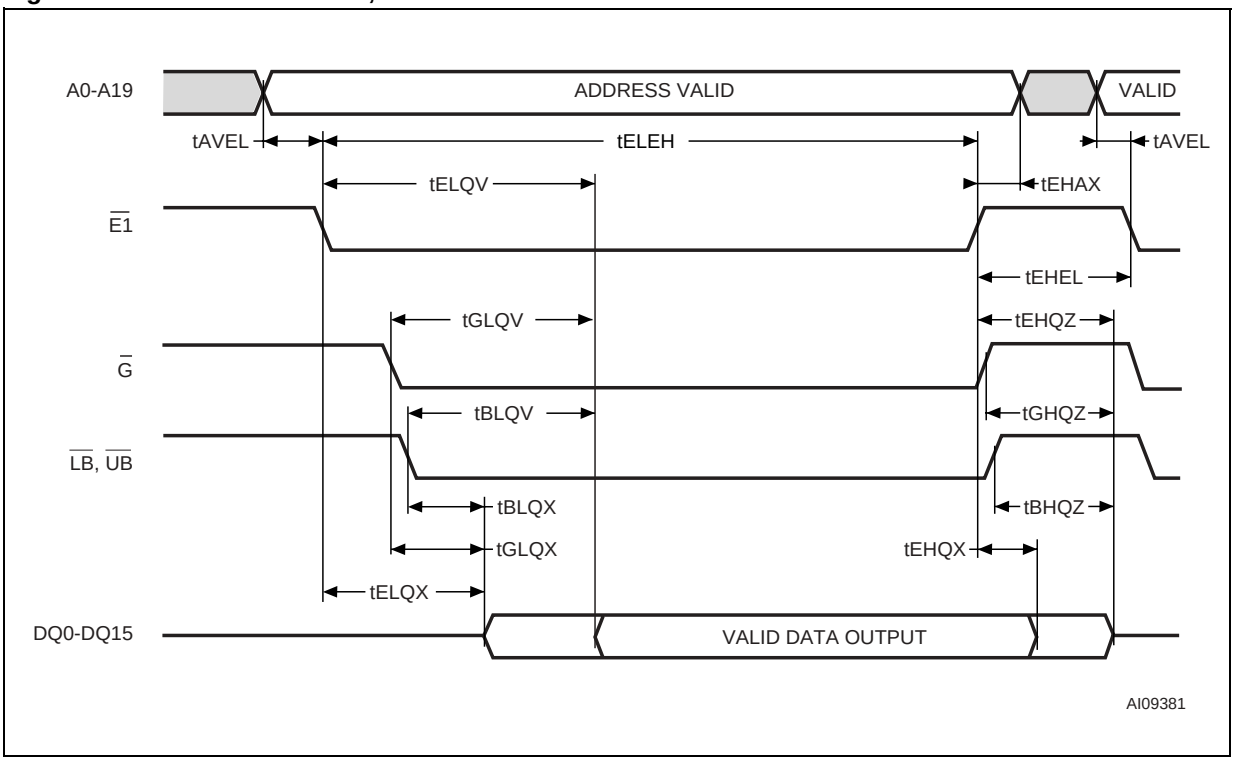
Note: 1. The maximum DC voltage on input and I/O pins is V_{CC}+0.2V. During voltage transitions, inputs may overshoot V_{CC} by 1.0V for periods of up to 5ns.
2. The minimum DC voltage on input or I/O pins is –0.3V. During voltage transitions, inputs may undershoot V_{SS} by 1.0V for periods of up to 5ns.

Table 7. Read Mode AC Characteristics

Symbol	Alt.	Parameter		M69AR024B				Unit
				-70		-80		
				Min	Max	Min	Max	
t_{AVAX} (1,2)	t_{RC}	Address Valid Time	V_{CC} = 1.7V to 2.25V	80	1000	80	1000	ns
			V_{CC} = 1.8V to 2.25V	70		70		
t_{AVEL}	t_{ASC}	Address Valid to Chip Enable Low		–5		–5		ns
t_{AVGL}	t_{ASO}	Address Valid to Output Enable Low		10		10		ns
t_{AVQV} (3,5)	t_{AA}	Address Valid to Output Valid			70		80	ns
t_{AXAV} (5,8)	t_{AX}	Address Invalid Time			10		10	ns
t_{AXQX} (3)	t_{OH}	Data hold from address change		10		10		ns
t_{BHQX} (3)	t_{OH}	Upper/Lower Byte Enable High to Output Transition		10		10		ns
t_{BHQZ} (4)	t_{BHZ}	Upper/Lower Byte Enable High to Output Hi-Z			20		20	ns
t_{BLQV} (3)	t_{BA}	Upper/Lower Byte Enable Low to Output Valid			70		80	ns
t_{BLQX} (4)	t_{BLZ}	Upper/Lower Byte Enable Low to Output Transition		5		5		ns
t_{EHAX} (9)	t_{CHAH}	Chip Enable High to Address Invalid		–5		–5		ns
t_{EHEL}	t_{CP}	Chip Enable High to Chip Enable Low		15		15		ns
t_{EHQX} (3)	t_{OH}	Chip Enable High to Output Transition		10		10		ns
t_{EHQZ} (4)	t_{CHZ}	Chip Enable High to Output Hi-Z			20		20	ns
t_{ELAX} (1,2)	t_{RC}	Read Cycle Time		80	1000	80	1000	ns
t_{ELEH} (1,2)	t_{RC}	Read Cycle Time		80	1000	80	1000	ns
t_{ELQV} (3)	t_{CE}	Chip Enable Low to Output Valid			70		80	ns
t_{ELQX} (4)	t_{CLZ}	Chip Enable Low to Output Transition		10		10		ns
t_{GHAX}	t_{OHAH}	Output Enable High to Address Invalid		–5		–5		ns
t_{GHQX} (3)	t_{OH}	Output Enable High to Output Transition		10		10		ns
t_{GHQZ} (4)	t_{OHZ}	Output Enable High to Output Hi-Z			20		20	ns
t_{GLQV} (3)	t_{OE}	Output Enable Low to Output Valid			45		45	ns
t_{GLQX} (4)	t_{OLZ}	Output Enable Low to Output Transition		5		5		ns

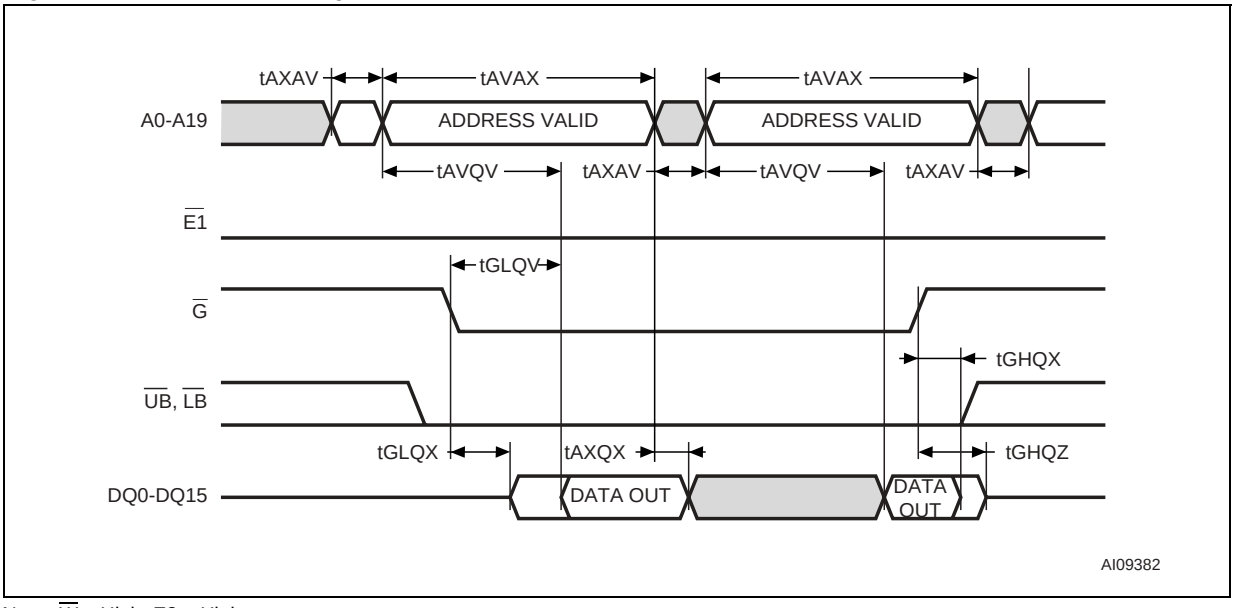
Note: 1. Maximum value is applicable if $\overline{E1}$ is kept at Low without change of address input of A3 to A19. If needed by system operation, please contact local ST sales office for the relaxation of 1µs limitation.
2. Address should not be changed within t_{AVAX}(min).
3. The output load 50pF with 50Ω termination to V_{CC}*0.5 V.
4. The output load C_L = 5pF without any other load.
5. Applicable to A3 to A19 when $\overline{E1}$ is kept at Low.
6. Applicable only to A0, A1 and A2 when $\overline{E1}$ is kept at Low for the page address access.
7. In case Page Read Cycle is continued with keeping $\overline{E1}$ stays Low, $\overline{E1}$ must be brought to High within 4µs. In other words, Page Read Cycle must be closed within 4µs.
8. Applicable when at least two of address inputs among applicable are switched from previous state.
9. t_{AVAX}(min) must be satisfied.

Figure 7. Address Controlled, Read Mode AC Waveforms



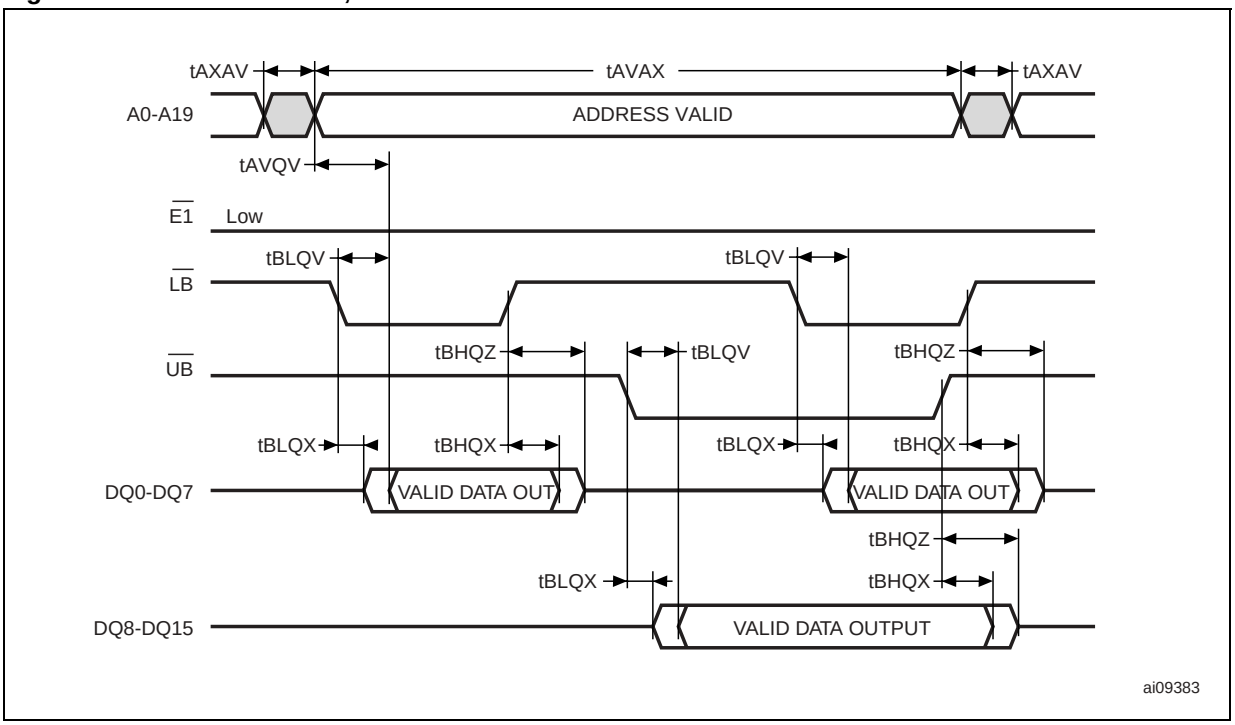
Note: E2 = High, $\overline{W}$ = High.

Figure 8. Address and Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High, E2 = High.

Figure 9. $\overline{LB}$/$\overline{UB}$ Controlled, Read Mode AC Waveforms



Note: $\overline{E1}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{W}$ = High.

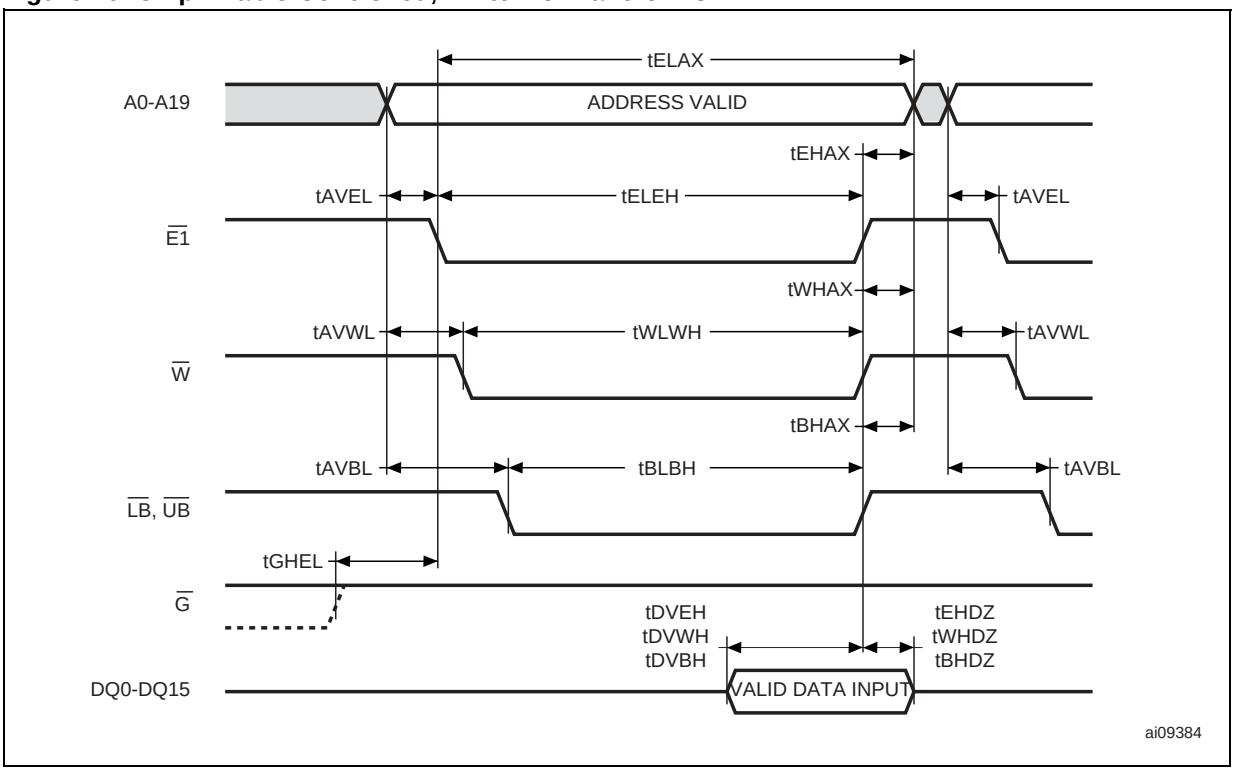
Table 8. Write Mode AC Characteristics

Symbol	Alt.	Parameter		M69AR024B		Unit
				-70, -80		
				Min	Max	
t_{AVAX} (1,2)	t_{WC}	Write Cycle Time	V_{CC} = 1.7V to 2.25V	80	1000	ns
			V_{CC} = 1.8V to 2.25V	70		
t_{AVBL} (2)	t_{AS}	Address Valid to $\overline{LB}$, $\overline{UB}$ Low		0		ns
t_{AVEL} (2)	t_{AS}	Address Valid to Chip Enable Low		0		ns
t_{AVWL} (2)	t_{AS}	Address Valid to Write Enable Low		0		ns
t_{AXAV} (5)	t_{AXW}	Address Invalid Time for Write			10	ns
t_{BHAX} (4)	t_{BR}	$\overline{LB}$, $\overline{UB}$ High to Address Transition		15	1000	ns
t_{BHDZ}	t_{DH}	$\overline{LB}$, $\overline{UB}$ High to Input Hi-Z		0		ns
t_{BLBH} (3)	t_{BW}	$\overline{LB}$, $\overline{UB}$ Low to $\overline{LB}$, $\overline{UB}$ High		45		ns
t_{BLBH2}	t_{BWO}	$\overline{LB}$, $\overline{UB}$ Low to $\overline{LB}$, $\overline{UB}$ High, Pulse Overlap		20		ns
t_{BLWH} (3)	t_{BW}	$\overline{LB}$, $\overline{UB}$ Low to Write Enable High		45		ns
t_{BHWL}, t_{BHEL} (8)	t_{BS}	$\overline{LB}$, $\overline{UB}$ Byte Mask Setup Time		–5		ns
t_{WHBL}, t_{EHBL} (9)	t_{BH}	$\overline{LB}$, $\overline{UB}$ Byte Mask Hold Time		–5		ns
t_{DVBH}	t_{DS}	Input Valid to $\overline{LB}$, $\overline{UB}$ High		30		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High		30		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High		30		ns
t_{EHAX} (4)	t_{WRC}	Chip Enable High to Address Transition		15		ns
t_{EHDZ}	t_{DH}	Chip Enable High to Input Hi-Z		0		ns
t_{EHEL}	t_{CP}	Chip Enable High to Chip Enable Low		15		ns
t_{ELAX} (1,2)	t_{WC}	Write Cycle Time		80	1000	ns
t_{ELEH} (3)	t_{CW}	Chip Enable Low to Chip Enable High		75		ns
t_{GHAV} (7)	t_{OES}	Output Enable High to Address Valid		0		ns

Symbol	Alt.	Parameter	M69AR024B		Unit
			-70, -80		
			Min	Max	
t_{GHEL} (6)	t_{OHCL}	Output Enable High to Chip Enable Low	–5		ns
t_{WHAX} (4)	t_{WR}	Write Enable High to Address Transition	15	1000	ns
t_{WHDZ}	t_{DH}	Write Enable High to Input Hi-Z	0		ns
t_{WLBH} (3)	t_{WP}	Write Enable Low to $\overline{LB}$, $\overline{UB}$ High	65		ns
t_{WLWH} (3)	t_{WP}	Write Enable Low to Write Enable High	65	1000	ns

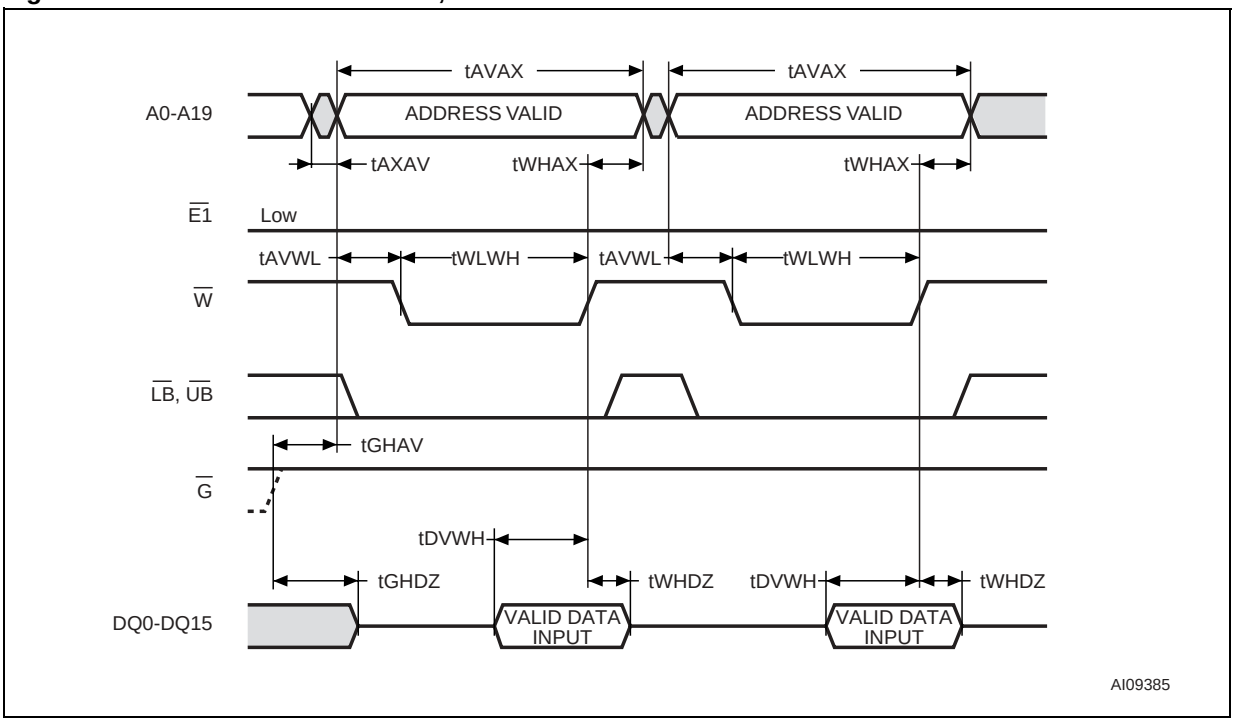
Note: 1. Maximum value is applicable if $\overline{E1}$ is kept at Low without any address change. If needed by system operation, please contact your local ST representative for relaxation of the 1000ns limitation.
2. Minimum value must be equal to or greater than the sum of write pulse (t_{ELEH}, t_{WLWH} or t_{BLBH}) and write recovery time (t_{WRC}, t_{WR} or t_{BR}).
3. Write pulse is defined from the falling edge of $\overline{E1}$, $\overline{W}$, or $\overline{LB}$/$\overline{UB}$, whichever occurs last.
4. Write recovery is defined from Write pulse is defined from the rising edge of $\overline{E1}$, $\overline{W}$, or $\overline{LB}$/$\overline{UB}$, whichever occurs first.
5. Applicable to any address change when $\overline{E1}$ stays Low.
6. If $\overline{G}$ is Low after minimum t_{GHEL}, the read cycle is initiated. In other words, $\overline{G}$ must be brought High within 5ns after $\overline{E1}$ is brought Low. Once the read cycle is initiated, new write pulse should be input after minimum Read Cycle Time is met.
7. If $\overline{G}$ is Low after new address input, the read cycle is initiated. In other words, $\overline{G}$ must be brought High at the same time or before new address valid. Once the read cycle is initiated, new write pulse should be input after minimum Read Cycle Time is met.
8. Applicable for Byte mask only. Byte mask setup time is defined to the High to Low transition of $\overline{E1}$ or $\overline{W}$ whichever occurs last.
9. Applicable for Byte mask only. Byte mask hold time is defined from the Low to High transition of $\overline{E1}$ or $\overline{W}$ whichever occurs first.

Figure 10. Chip Enable Controlled, Write AC Waveforms



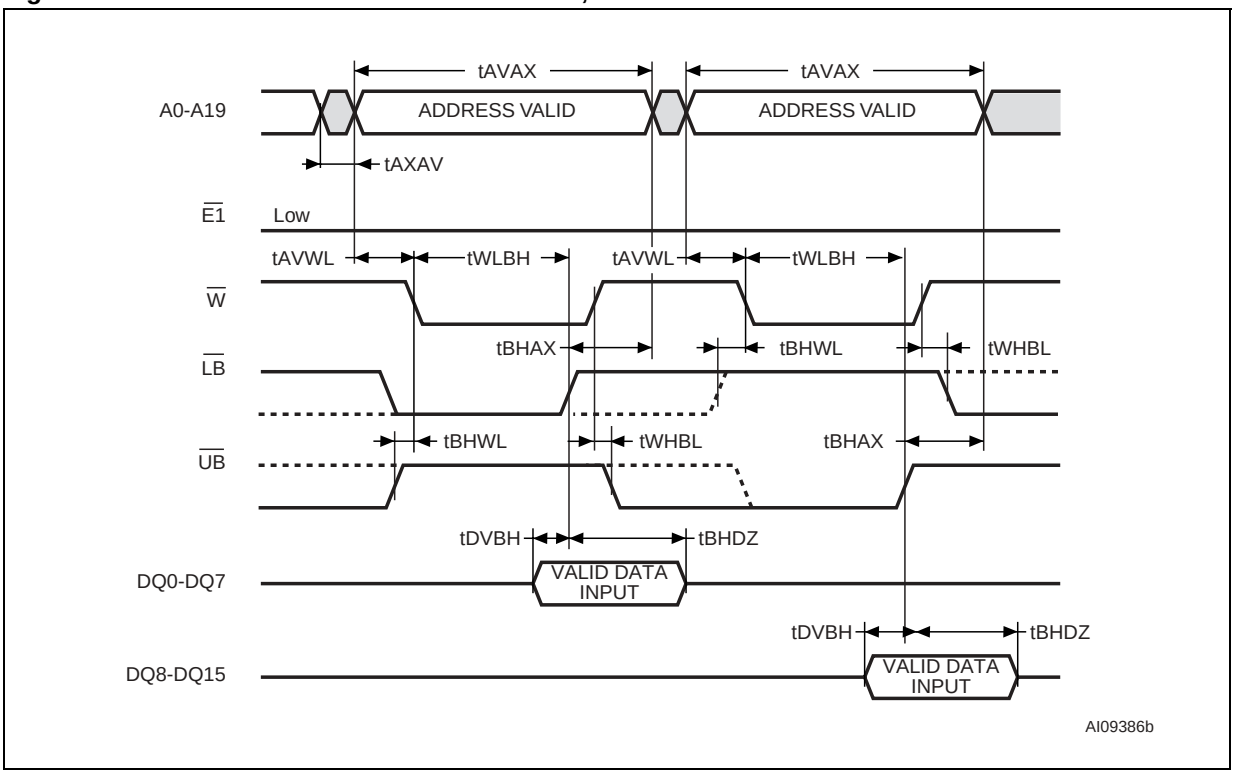
Note: E2 = High.

Figure 11. Write Enable Controlled, Write AC Waveforms



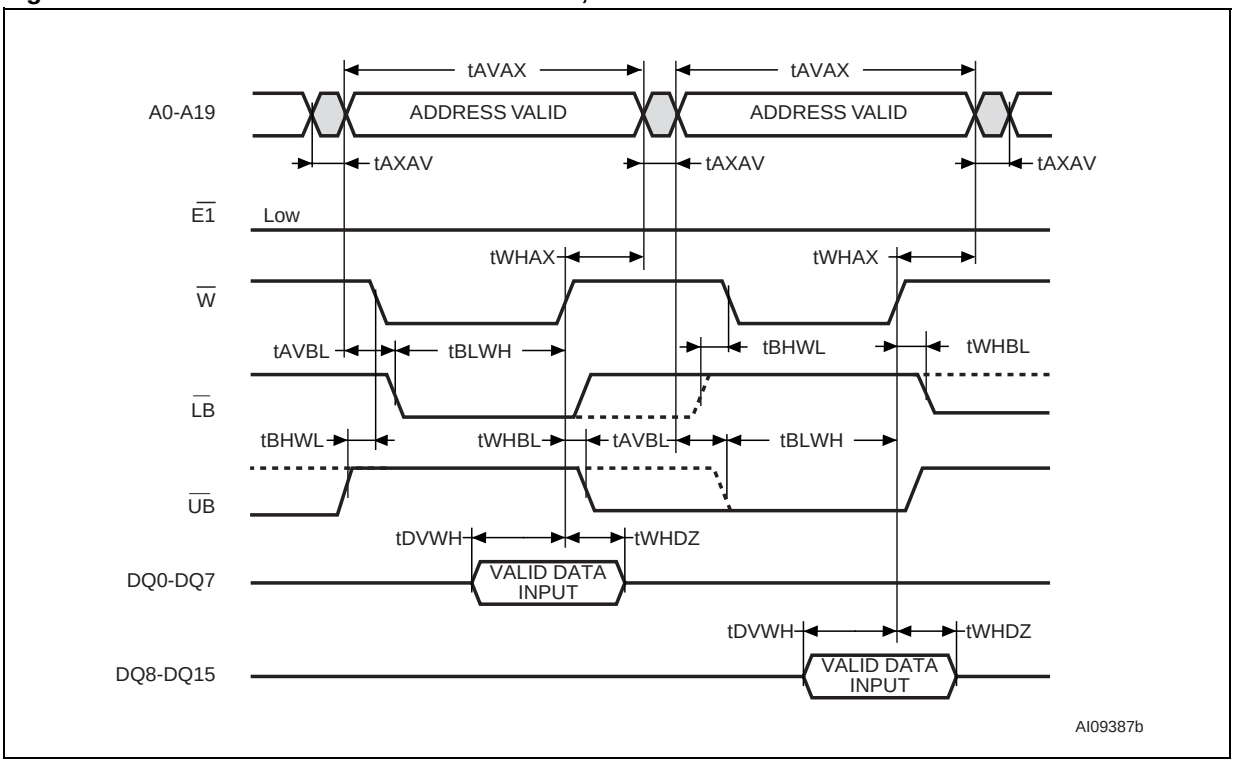
Note: E2 = High.

Figure 12. Write Enable and $\overline{UB}$/$\overline{LB}$ Controlled, Write AC Waveforms 1



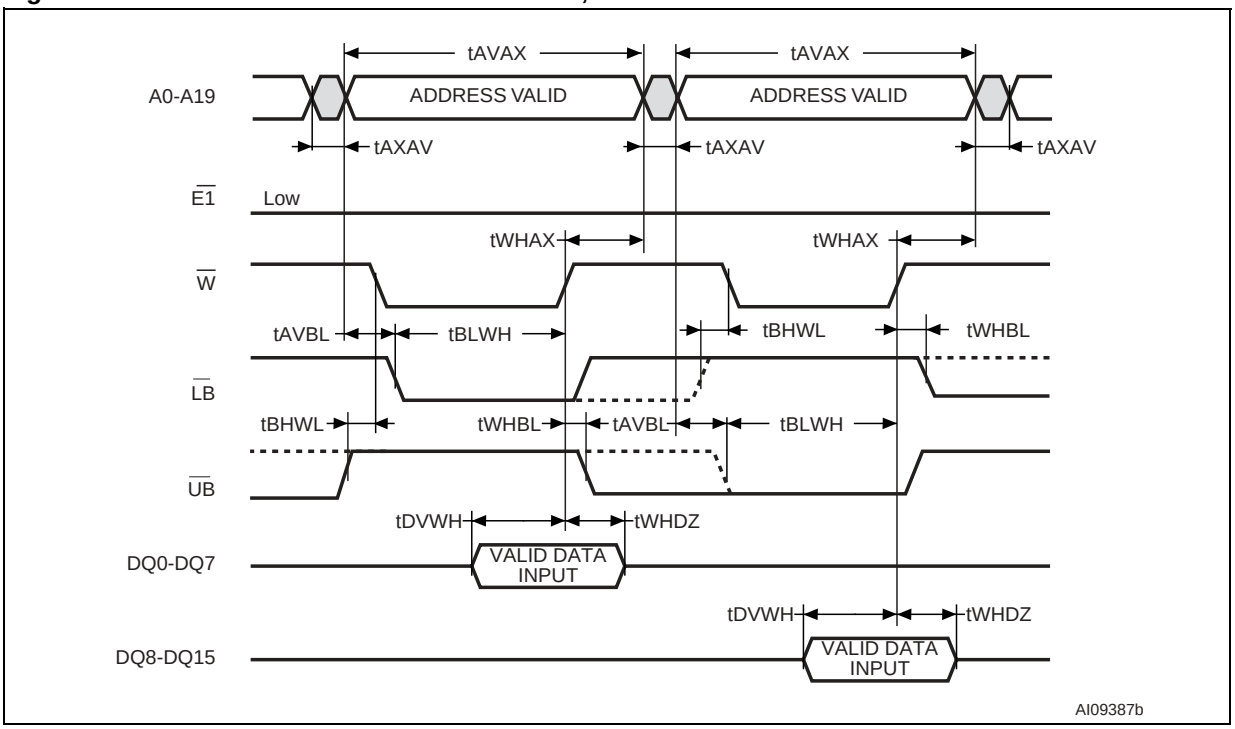
Note: E2 = High.

Figure 13. Write Enable and $\overline{UB}$/$\overline{LB}$ Controlled, Write AC Waveforms 2



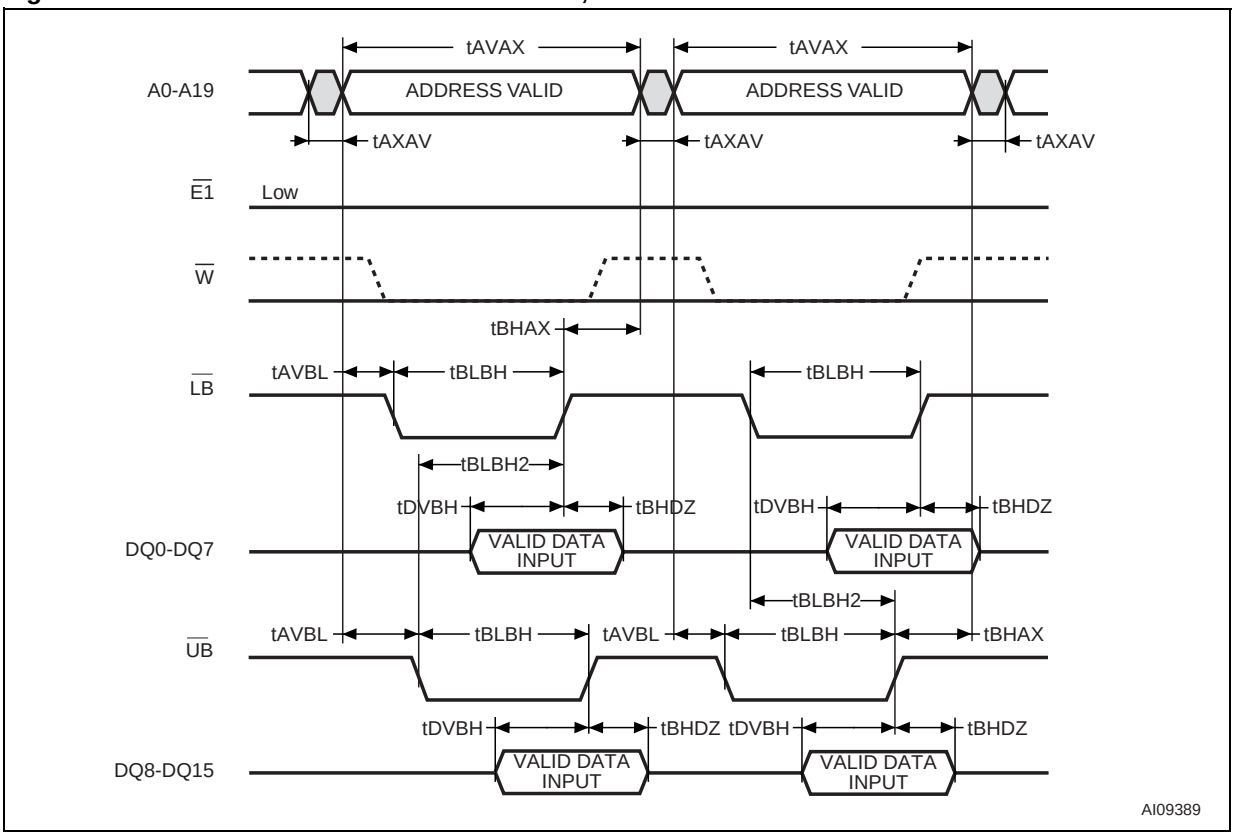
Note: E2 = High.

Figure 14. Write Enable and $\overline{UB}$/$\overline{LB}$ Controlled, Write AC Waveforms 3



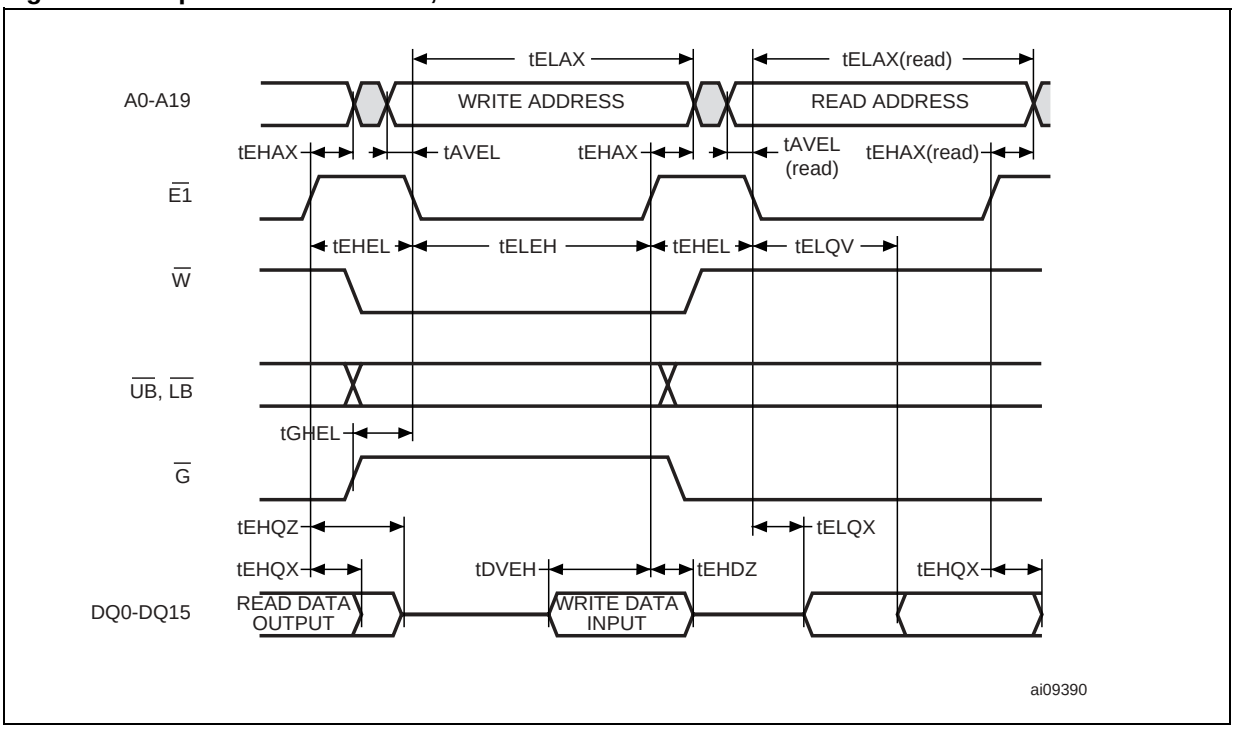
Note: E2 = High.

Figure 15. Write Enable and $\overline{UB}$/$\overline{LB}$ Controlled, Write AC Waveforms 4



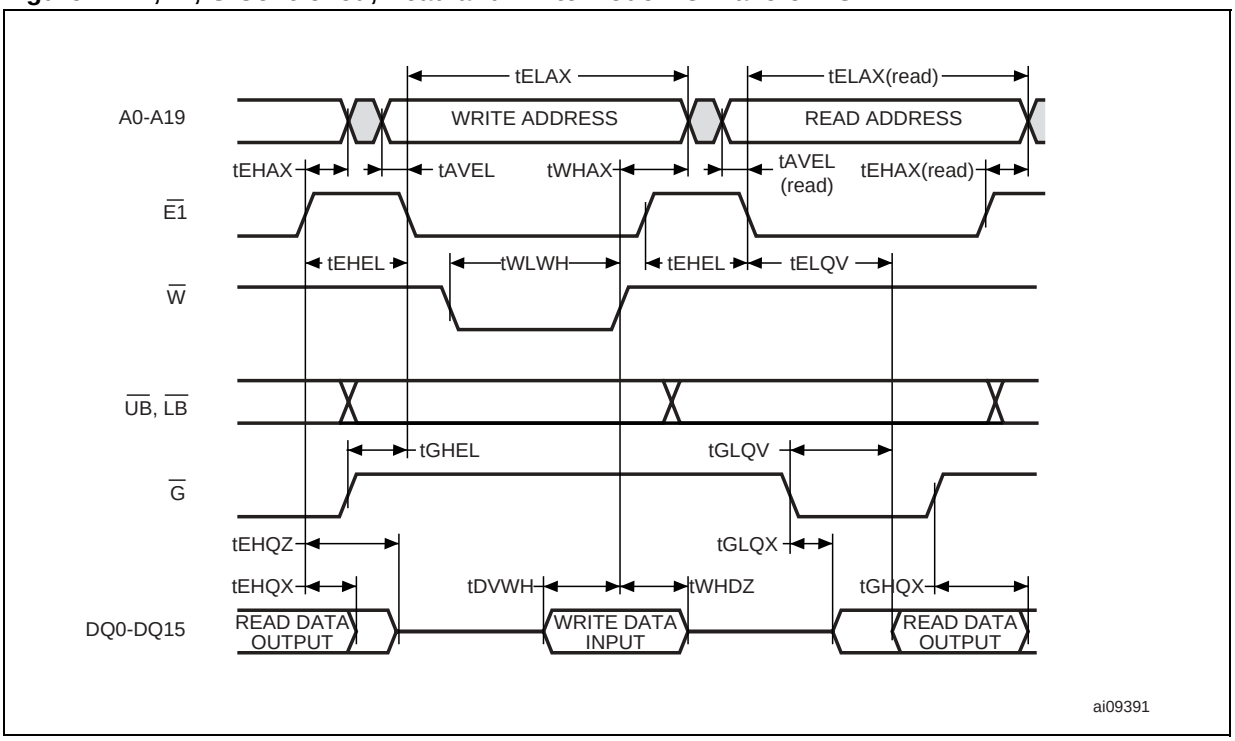
Note: E2 = High.

Figure 16. Chip Enable Controlled, Read and Write Mode AC Waveforms



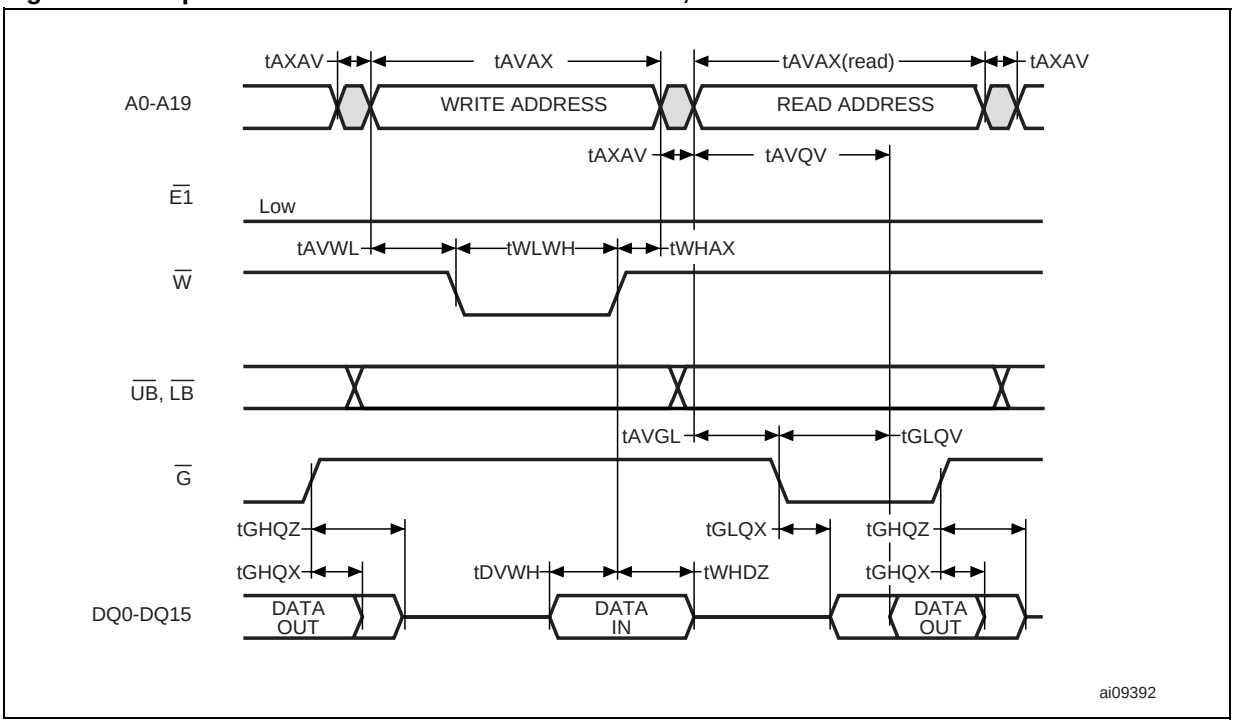
Note: Write address is valid from last falling edge of either $\overline{E1}$ or $\overline{W}$.

Figure 17. $\overline{E}$, $\overline{W}$, $\overline{G}$ Controlled, Read and Write Mode AC Waveforms



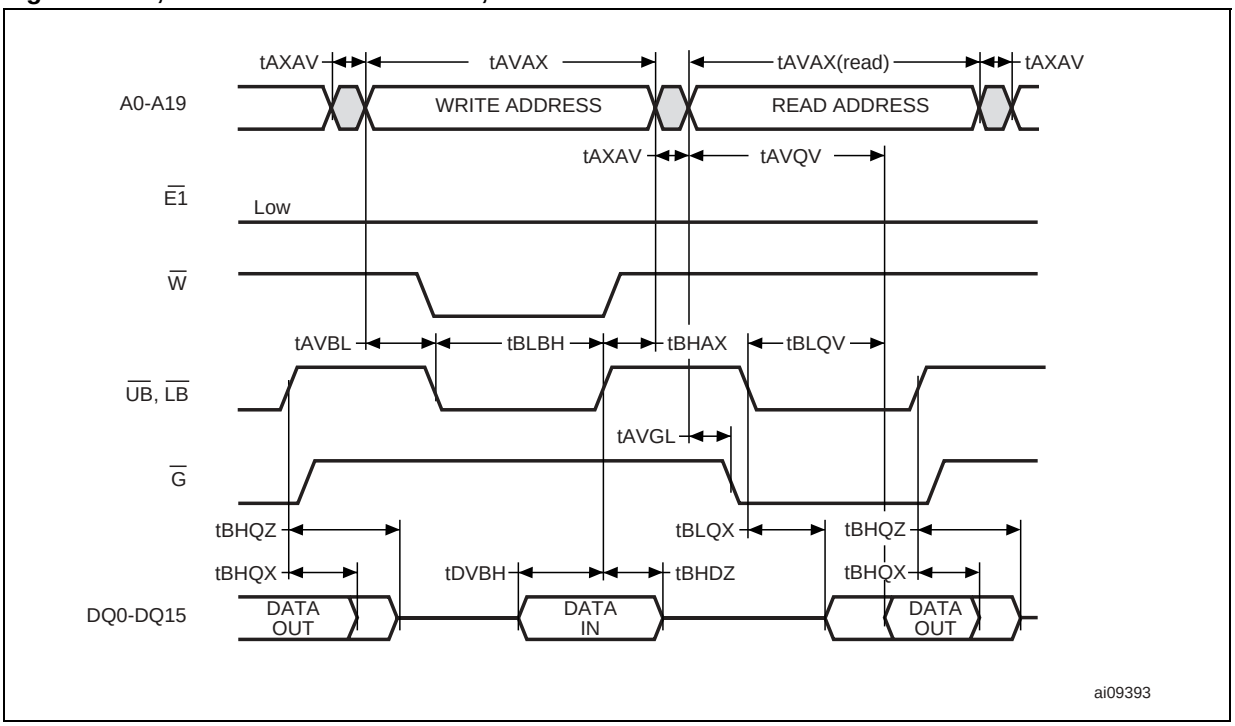
Note: $\overline{G}$ can be fixed Low during the write part of a read-write-read operation that is under $\overline{E1}$ control.

Figure 18. Output Enable and Write Enable Controlled, Read and Write Mode AC Waveforms



Note: $\overline{E1}$ can be tied Low for a $\overline{W}$ and $\overline{G}$ controlled operation.
When $\overline{E1}$ is tied Low, the output is exclusively controlled by $\overline{G}$.

Figure 19. $\overline{G}$, $\overline{W}$ and $\overline{UB}$/$\overline{LB}$ Controlled, Read and Write Mode AC Waveforms



Note: $\overline{E1}$ can be tied Low for a $\overline{W}$ and $\overline{G}$ controlled operation.
When $\overline{E1}$ is tied Low, the output is exclusively controlled by $\overline{G}$.

Table 9. Standby Mode AC Characteristics

Symbol	Alt.	Parameter	M69AR024B		Unit
			-70, -80		
			Min	Max	
t_{CLEX}	t_{CSP}	E2 Low Setup Time for Power Down Entry	10		ns
t_{EXCH}	t_{C2LP}	E2 Low Hold Time after Power Down Entry	70		ns
t_{EHEV} (1)	t_{CHH}	$\overline{E1}$ High Hold Time following E2 High after Power-Down Exit (Sleep Mode only)	300		µs
t_{CHEL}	t_{CHH}	$\overline{E1}$ High Hold Time following E2 High after Power-Down Exit (not in Sleep Mode)	300		µs
t_{EHCH}	t_{CHS}	$\overline{E1}$ High Setup Time following E2 High after Power-Down Exit	0		µs
t_{EHGL}	t_{CHOX}	$\overline{E1}$ High to $\overline{G}$ Invalid Time for Standby Entry	10		ns
t_{EHWL} (2)	t_{CHWX}	$\overline{E1}$ High to $\overline{W}$ Invalid Time for Standby Entry	10		ns
t_τ (3)	t_τ	Input Transition Time	1	25	ns

Note: 1. Applicable also to Power-up.
2. Some data might be written into any address location if t_{EHWL} (min) is not satisfied.
3. The Input Transition Time (t_τ) at AC testing is 5ns as shown below. If actual t_τ is longer than 5ns, it may violate AC specification of some timing parameters.

Figure 20. Power Down Mode AC Waveforms

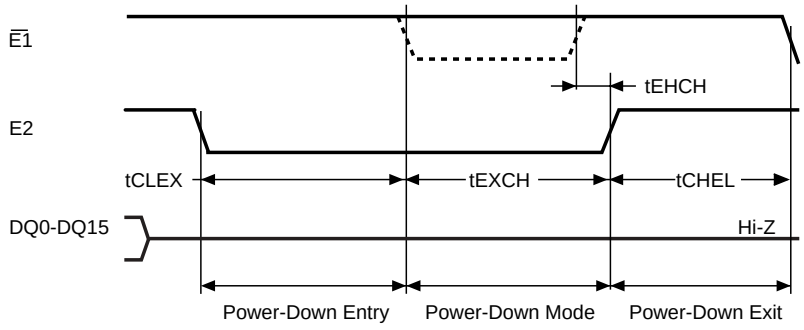


Figure 21. Power-Up Mode AC Waveforms

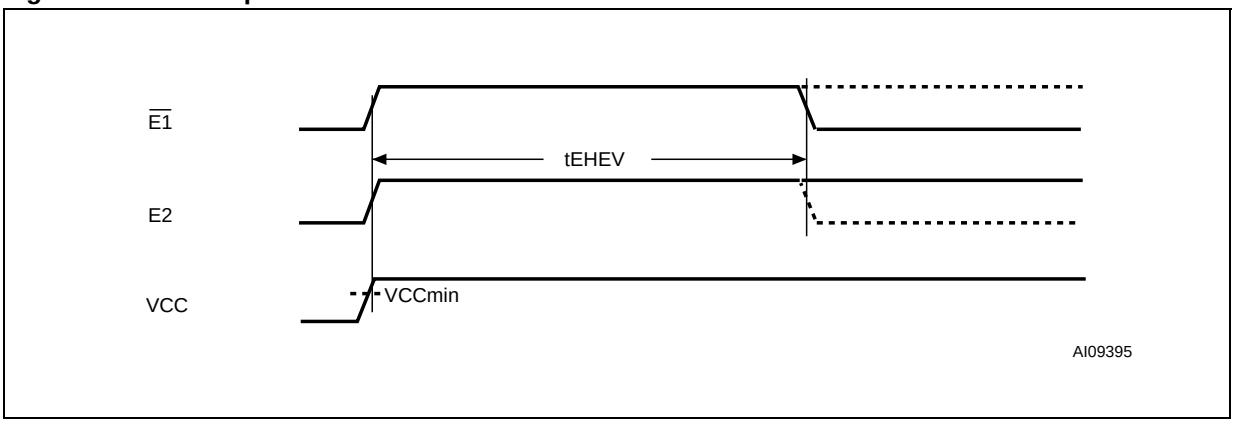
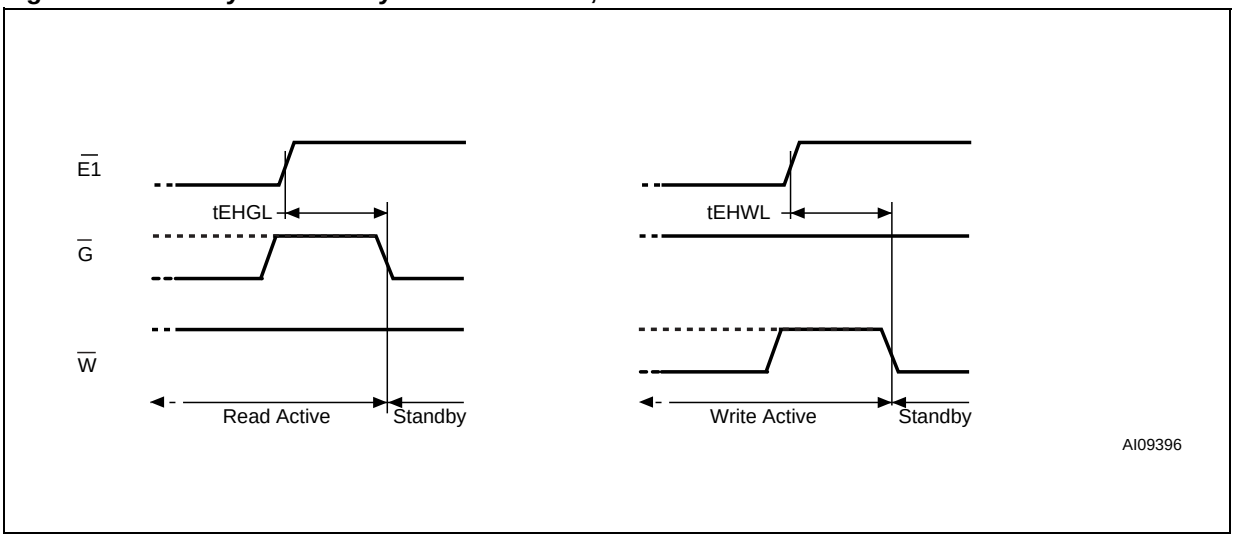


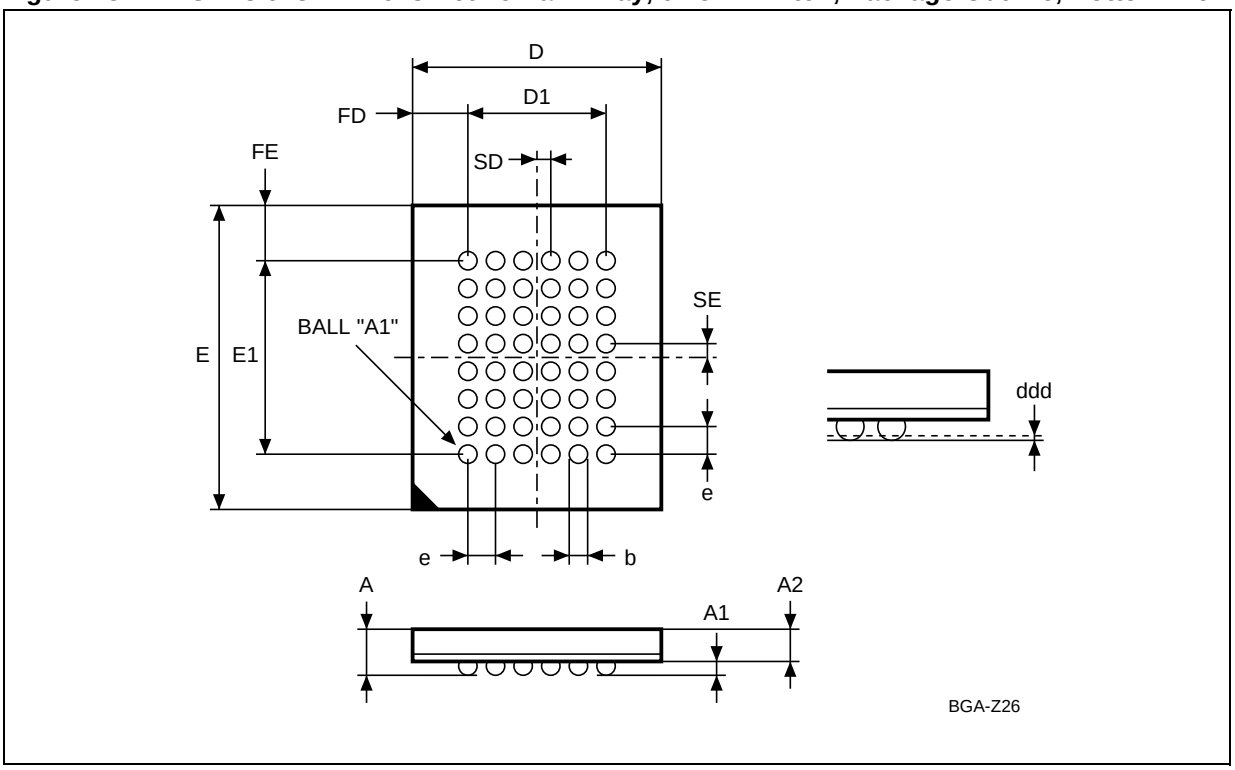
Figure 22. Standby Mode Entry AC Waveforms, After Read



Note: E2 = High.

PACKAGE MECHANICAL

Figure 23. TFBGA48 6x8mm - 6x8 Active Ball Array, 0.75mm Pitch, Package Outline, Bottom View



Note: Drawing is not to scale.

Table 10. TFBGA48 6x8mm - 6x8 Active Ball Array, 0.75mm Pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	3.750	–	–	0.1476	–	–
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.250	–	–	0.2067	–	–
e	0.750	–	–	0.0295	–	–
FD	1.125	–	–	0.0443	–	–
FE	1.375	–	–	0.0541	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

PART NUMBERING

Table 11. Ordering Information Scheme

Example: M69AR024 B L 70 ZB 8 T

Device Type
M69 = 1T/1C Memory Cell Architecture

Mode
A = Asynchronous

Operating Voltage
R = 1.7 to 2.25V

Array Organization
024 = 16 Mbit (1M x16)

Option 1
B = 2 Chip Enable

Option 2
L = L-Die

Speed Class
70 = 70ns
80 = 80ns

Package
ZB = TFBGA48, 6x8mm, 0.75mm pitch

Operative Temperature
8 = –30 to 85°C

Shipping Method
T = Tape & Reel Packing

The notation used for the device number is as shown in Table 11., Ordering Information Scheme. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest STMicroelectronics Sales Office.

REVISION HISTORY

Table 12. Document Revision History

Date	Version	Revision Details
09-Oct-2002	1.0	First Issue
17-Feb-2003	2.0	Document completely revised
14-Mar-2003	2.1	AC Measurement Load Circuit revised. A19-A3 address line labelling corrected
04-Apr-2003	2.2	Correction to signal description in Write Mode section; t_{BLQZ}, t_{ELQZ}, t_{GLQZ} renamed as t_{BLQX}, t_{ELQX}, t_{GLQX} in Read Mode AC Characteristics; a minor label correction in a timing diagram; and value of t_{EXCH}(min) changed
04-Jun-2003	2.3	ZH (8x10mm) package removed. Access time changed to 80ns, with many consequent changes to timing parameters in AC Characteristics tables. Ambient Operatings changed. Some DC Characteristics (and their Test Conditions) changed
17-Jun-2003	2.4	Standby current changed
25-Jul-2003	2.5	Power-on sequence described, and values for t_{EHEV}(min) and t_{CHEL}(min) revised.
21-Oct-2003	2.6	70ns and 80ns access times offered as two options
11-Mar-2004	3.0	t_{AVAX} modified in Table 7., Read Mode AC Characteristics and Table 8., Write Mode AC Characteristics.
16-Apr-2004	4.0	Timing diagrams brought to ST standards and timing names modified. Write Enable (W). signal description changed, Write Mode paragraph clarified and title of Figure 10. modified. t_{BLBH}, t_{BLWH} minimum values updated in Table 8., Write Mode AC Characteristics.
25-May-2004	5.0	Voltage ranged changed to 1.7 to 2.25V. Maximum Standby current updated to 110µs. Ambient temperature changed to -30 to 85°C. Note 3. below Table 2., Operating Modes updated. Maximum values of I_{CC1} and I_{SB}, minimum value of V_{IL}, test conditions for V_{OH}, V_{OL} and I_{SB} updated in Table 6., DC Characteristics. t_{BHWL} and t_{WHBL} added in Table 8., Write Mode AC Characteristics, and Figures 12, 13 and 14, Write Enable and UB/LB Controlled, Write AC Waveforms.
29-Sep-2004	6.0	Minor modification in first paragraph of Summary Description.