

TENTATIVE

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

128-MBIT (16M × 8 BITS) CMOS NAND E²PROM**DESCRIPTION**

The TC58128 is a single 3.3-V 128-Mbit (138,412,032) bit NAND Electrically Erasable and Programmable Read-Only Memory (NAND E²PROM) organized as 528 bytes × 32 pages × 1024 blocks. The device has a 528-byte static register which allows program and read data to be transferred between the register and the memory cell array in 528-byte increments. The Erase operation is implemented in a single block unit (16 Kbytes + 512 bytes: 528 bytes × 32 pages).

The TC58128 is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization
 - Memory cell array 528 × 32K × 8
 - Register 528 × 8
 - Page size 528 bytes
 - Block size (16K + 512) bytes
- Modes
 - Read, Reset, Auto Page Program
 - Auto Block Erase, Status Read
- Mode control
 - Serial input/output
 - Command control
- Power supply
 - V_{CC} = 3.3 V ± 0.3 V
- Access time
 - Cell array-register 25 μs max
 - Serial Read cycle 50 ns min
- Operating current
 - Read (50-ns cycle) 10 mA typ.
 - Program (avg.) 10 mA typ.
 - Erase (avg.) 10 mA typ.
 - Standby 100 μA
- Packages
 - TSOP I 48-P-1220-0.50
 - (Weight : 0.53g typ.)

PIN ASSIGNMENT (TOP VIEW)

| | | | |
|-----------------|----|----|-----------------|
| NC | 1 | 48 | NC |
| NC | 2 | 47 | NC |
| NC | 3 | 46 | NC |
| NC | 4 | 45 | NC |
| NC | 5 | 44 | I/O8 |
| GND | 6 | 43 | I/O7 |
| R/B | 7 | 42 | I/O6 |
| RE | 8 | 41 | I/O5 |
| CE | 9 | 40 | NC |
| NC | 10 | 39 | NC |
| NC | 11 | 38 | NC |
| V _{CC} | 12 | 37 | V _{CC} |
| V _{SS} | 13 | 36 | V _{SS} |
| NC | 14 | 35 | NC |
| NC | 15 | 34 | NC |
| CLE | 16 | 33 | NC |
| ALE | 17 | 32 | I/O4 |
| WE | 18 | 31 | I/O3 |
| WP | 19 | 30 | I/O2 |
| NC | 20 | 29 | I/O1 |
| NC | 21 | 28 | NC |
| NC | 22 | 27 | NC |
| NC | 23 | 26 | NC |
| NC | 24 | 25 | NC |

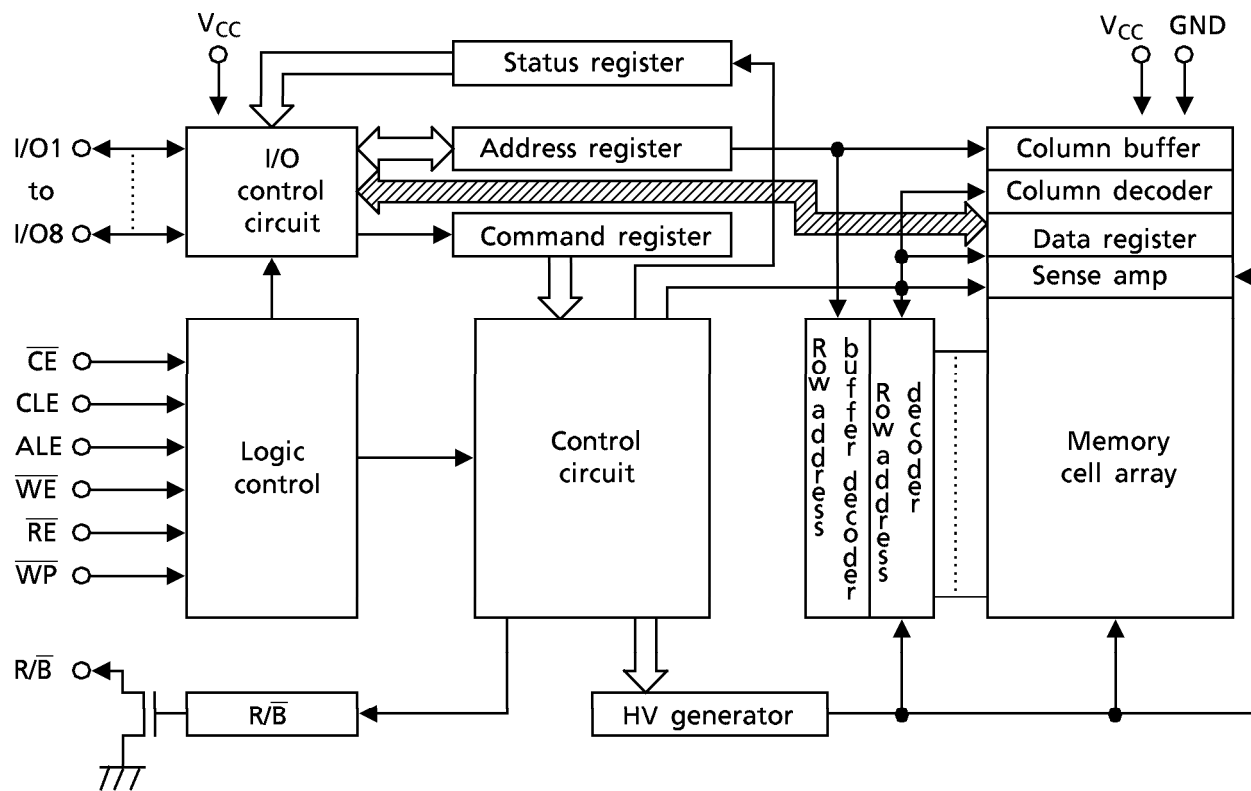
PIN NAMES

| I/O1 to 8 | I/O Port |
|-----------------|----------------------|
| CE | Chip Enable |
| WE | Write Enable |
| RE | Read Enable |
| CLE | Command Latch Enable |
| ALE | Address Latch Enable |
| WP | Write Protect |
| R/B | Ready/Busy |
| GND | Ground input |
| V _{CC} | Power Supply |
| V _{SS} | Ground |

961001EBA1

- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

2000-02-24 1/33

BLOCK DIAGRAM**ABSOLUTE MAXIMUM RATINGS**

| SYMBOL | ITEM | RATING | UNIT |
|--------------|------------------------------|--|-------------|
| V_{CC} | Power Supply Voltage | -0.6 to 4.6 | V |
| V_{IN} | Input Voltage | -0.6 to 4.6 | V |
| $V_{I/O}$ | Input / Output Voltage | -0.6 V \sim $V_{CC} + 0.3$ V (≤ 4.6 V) | V |
| P_D | Power Dissipation | 0.3 | W |
| T_{SOLDER} | Soldering Temperature (10 s) | 260 | $^{\circ}C$ |
| T_{STG} | Storage Temperature | -55 to 150 | $^{\circ}C$ |
| T_{OPR} | Operating Temperature | -40 to 85 | $^{\circ}C$ |

CAPACITANCE *($T_a = 25^{\circ}C$, $f = 1$ MHz)

| SYMBOL | PARAMETER | CONDITION | MIN | MAX | UNIT |
|-----------|-----------|-----------------|-----|-----|------|
| C_{IN} | Input | $V_{IN} = 0$ V | - | 10 | pF |
| C_{OUT} | Output | $V_{OUT} = 0$ V | - | 10 | pF |

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS (1)

| SYMBOL | PARAMETER | MIN | TYP. | MAX | UNIT |
|----------|------------------------|------|------|------|--------|
| N_{VB} | Number of Valid Blocks | 1004 | – | 1024 | Blocks |

(1) The TC58128 occasionally contains unusable blocks. Refer to Application Note (14) toward the end of this document.

RECOMMENDED DC OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN | TYP. | MAX | UNIT |
|----------|--------------------------|-------|------|----------------|------|
| V_{CC} | Power Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| V_{IH} | High Level Input Voltage | 2.0 | – | $V_{CC} + 0.3$ | V |
| V_{IL} | Low Level Input Voltage | -0.3* | – | 0.8 | V |

* -2 V (pulse width \leq 20 ns)

DC CHARACTERISTICS

($T_a = -40^\circ$ to 85°C , $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$)

| SYMBOL | PARAMETER | CONDITION | MIN | TYP. | MAX | UNIT |
|--------------------------|--|---|-----|------|----------|---------------|
| I_{IL} | Input Leakage Current | $V_{IN} = 0\text{ V to }V_{CC}$ | – | – | ± 10 | μA |
| I_{LO} | Output Leakage Current | $V_{OUT} = 0.4\text{ V to }V_{CC}$ | – | – | ± 10 | μA |
| I_{CCO1} | Operating Current (Serial Read) | $\overline{CE} = V_{IL}$, $I_{OUT} = 0\text{ mA}$, $t_{cycle} = 50\text{ ns}$ | – | 10 | 30 | mA |
| I_{CCO3} | Operating Current (Command Input) | $t_{cycle} = 50\text{ ns}$ | – | 10 | 30 | mA |
| I_{CCO4} | Operating Current (Data Input) | $t_{cycle} = 50\text{ ns}$ | – | 10 | 30 | mA |
| I_{CCO5} | Operating Current (Address Input) | $t_{cycle} = 50\text{ ns}$ | – | 10 | 30 | mA |
| I_{CCO7} | Programming Current | – | – | 10 | 30 | mA |
| I_{CCO8} | Erasing Current | – | – | 10 | 30 | mA |
| I_{CCS1} | Standby Current | $\overline{CE} = V_{IH}$ | – | – | 1 | mA |
| I_{CCS2} | Standby Current | $\overline{CE} = V_{CC} - 0.2\text{ V}$ | – | – | 100 | μA |
| V_{OH} | High Level Output Voltage | $I_{OH} = -400\ \mu\text{A}$ | 2.4 | – | – | V |
| V_{OL} | Low Level Output Voltage | $I_{OL} = 2.1\text{ mA}$ | – | – | 0.4 | V |
| $I_{OL}(R/\overline{B})$ | Output Current of R/\overline{B} Pin | $V_{OL} = 0.4\text{ V}$ | – | 8 | – | mA |

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS(Ta = -40° to 85°C, V_{CC} = 3.3 V ± 0.3 V)

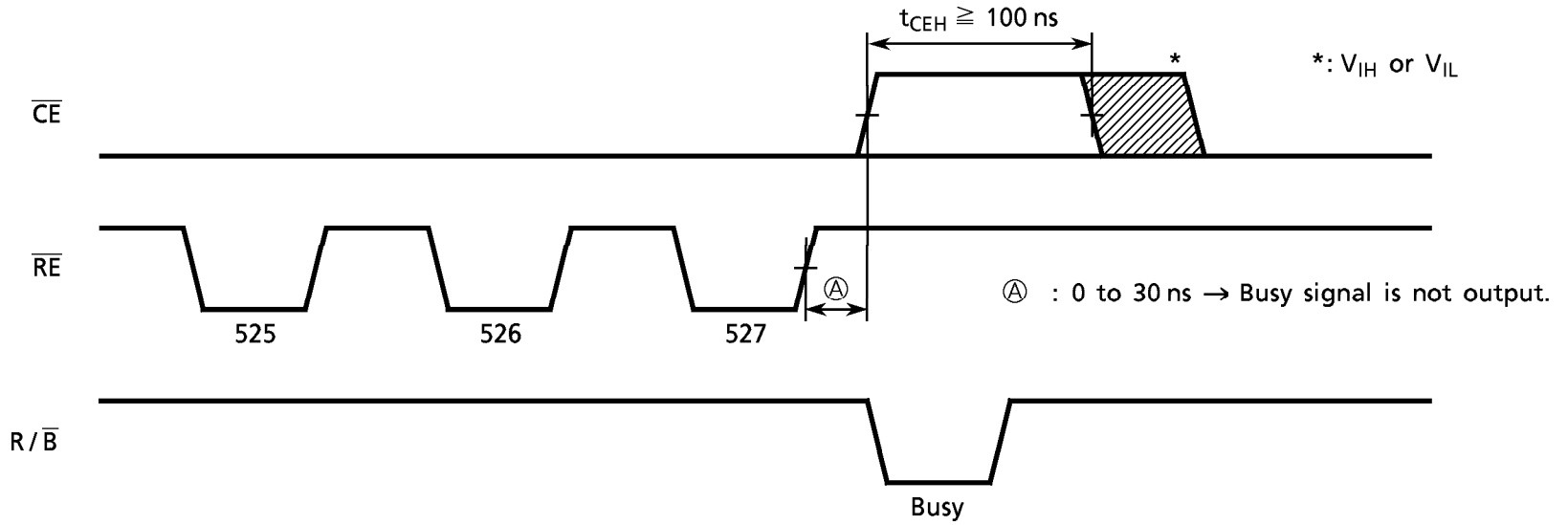
| SYMBOL | PARAMETER | MIN | MAX | UNIT | NOTES |
|-------------------|--|-----|----------------|------|-------|
| t _{CLS} | CLE Setup Time | 0 | – | ns | |
| t _{CLH} | CLE Hold Time | 10 | – | ns | |
| t _{CS} | $\overline{\text{CE}}$ Setup Time | 0 | – | ns | |
| t _{CH} | $\overline{\text{CE}}$ Hold Time | 10 | – | ns | |
| t _{WP} | Write Pulse Width | 25 | – | ns | |
| t _{ALS} | ALE Setup Time | 0 | – | ns | |
| t _{ALH} | ALE Hold Time | 10 | – | ns | |
| t _{DS} | Data Setup Time | 20 | – | ns | |
| t _{DH} | Data Hold Time | 10 | – | ns | |
| t _{WC} | Write Cycle Time | 50 | – | ns | |
| t _{WH} | $\overline{\text{WE}}$ -High Hold Time | 15 | – | ns | |
| t _{WW} | $\overline{\text{WP}}$ High to $\overline{\text{WE}}$ Low | 100 | – | ns | |
| t _{RR} | Ready-to- $\overline{\text{RE}}$ Falling Edge | 20 | – | ns | |
| t _{RP} | Read Pulse Width | 35 | – | ns | |
| t _{RC} | Read Cycle Time | 50 | – | ns | |
| t _{REA} | $\overline{\text{RE}}$ Access Time (Serial Data Access) | – | 35 | ns | |
| t _{CEH} | $\overline{\text{CE}}$ -High Time for Last Address in Serial Read Cycle | 100 | – | ns | (2) |
| t _{REAI} | $\overline{\text{RE}}$ Access Time (ID Read) | – | 35 | ns | |
| t _{OH} | Data Output Hold Time | 10 | – | ns | |
| t _{RHZ} | $\overline{\text{RE}}$ -High-to-Output-High Impedance | – | 30 | ns | |
| t _{CHZ} | $\overline{\text{CE}}$ -High-to-Output-High Impedance | – | 20 | ns | |
| t _{REH} | $\overline{\text{RE}}$ -High Hold Time | 15 | – | ns | |
| t _{IR} | Output-High-Impedance-to- $\overline{\text{RE}}$ Rising Edge | 0 | – | ns | |
| t _{RSTO} | $\overline{\text{RE}}$ Access Time (Status Read) | – | 35 | ns | |
| t _{CSTO} | $\overline{\text{CE}}$ Access Time (Status Read) | – | 45 | ns | |
| t _{RHW} | $\overline{\text{RE}}$ High to $\overline{\text{WE}}$ Low | 0 | – | ns | |
| t _{WHC} | $\overline{\text{WE}}$ High to $\overline{\text{CE}}$ Low | 30 | – | ns | |
| t _{WHR} | $\overline{\text{WE}}$ High to $\overline{\text{RE}}$ Low | 30 | – | ns | |
| t _{AR1} | ALE Low to $\overline{\text{RE}}$ Low (ID Read) | 100 | – | ns | |
| t _{CR} | $\overline{\text{CE}}$ Low to $\overline{\text{RE}}$ Low (ID Read) | 100 | – | ns | |
| t _R | Memory Cell Array to Starting Address | – | 25 | μs | |
| t _{WB} | $\overline{\text{WE}}$ High to Busy | – | 200 | ns | |
| t _{AR2} | ALE Low to $\overline{\text{RE}}$ Low (Read Cycle) | 50 | – | ns | |
| t _{RB} | $\overline{\text{RE}}$ Last Clock Rising Edge to Busy (in Sequential Read) | – | 200 | ns | |
| t _{CRY} | $\overline{\text{CE}}$ High to Ready (When interrupted by $\overline{\text{CE}}$ in Read Mode) | – | 600 + tr (R/B) | ns | (1) |
| t _{RST} | Device Reset Time (Read/Program/Erase) | – | 6/10/500 | μs | |

AC TEST CONDITIONS

Input level : 2.4 V / 0.4 V
 Input pulse rise and fall time : 3ns
 Input comparison level : 1.5 V / 1.5 V
 Output data comparison level : 1.5 V / 1.5 V
 Output load : 1 TTL + C_L (100 pF)

Note : (1) \overline{CE} High to Ready time depends on the pull-up resistor tied to the R/\overline{B} pin. (Refer to Application Note(7) toward the end of this document.)

(2) Sequential Read is terminated when t_{CEU} is greater than or equal to 100ns.
If the \overline{RE} to \overline{CE} delay is less than 30 ns, R/\overline{B} signal stays Ready.



PROGRAMMING AND ERASING CHARACTERISTICS

($T_a = -40^\circ$ to 85°C , $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$)

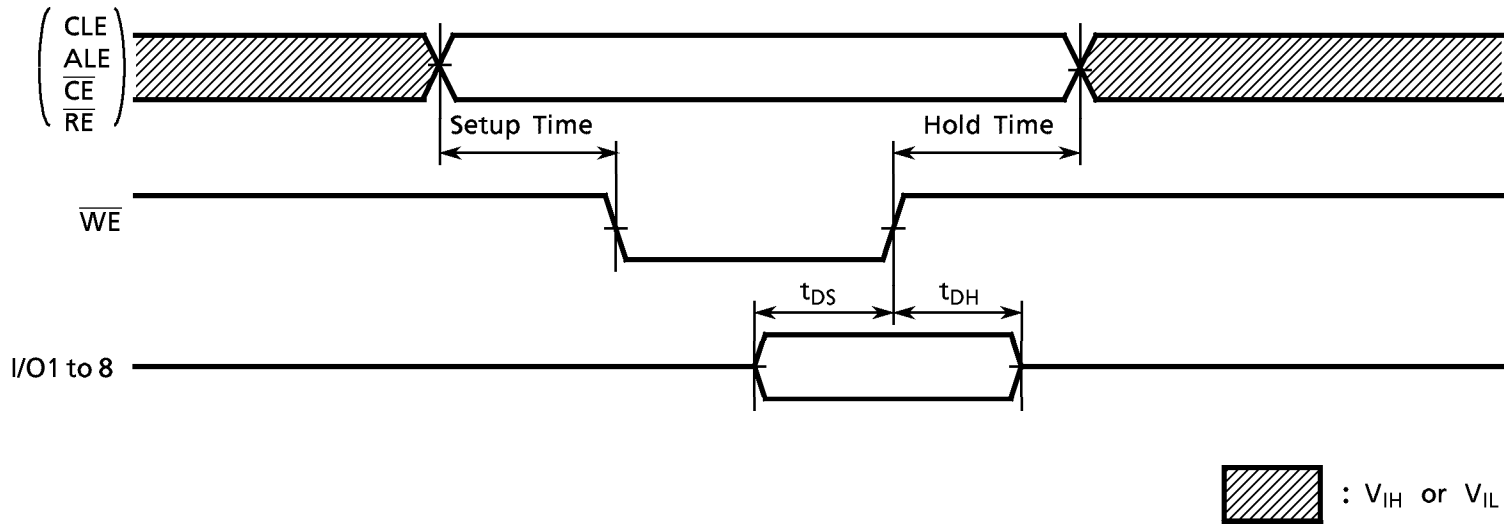
| SYMBOL | PARAMETER | MIN | TYP. | MAX | UNIT | NOTES |
|---------------------|---|-----|------|-------------------|---------------|-------|
| t_{PROG} | Average Programming Time | | 200 | 1000 | μs | |
| N | Number of Programming Cycles on Same Page | | | 10 | | (1) |
| t_{BERASE} | Block Erasing Time | | 3 | 5 | ms | |
| P/E | Number of Program/Erase Cycles | | | 2.5×10^5 | | (2) |

(1) Refer to Application Note (12) toward the end of this document.

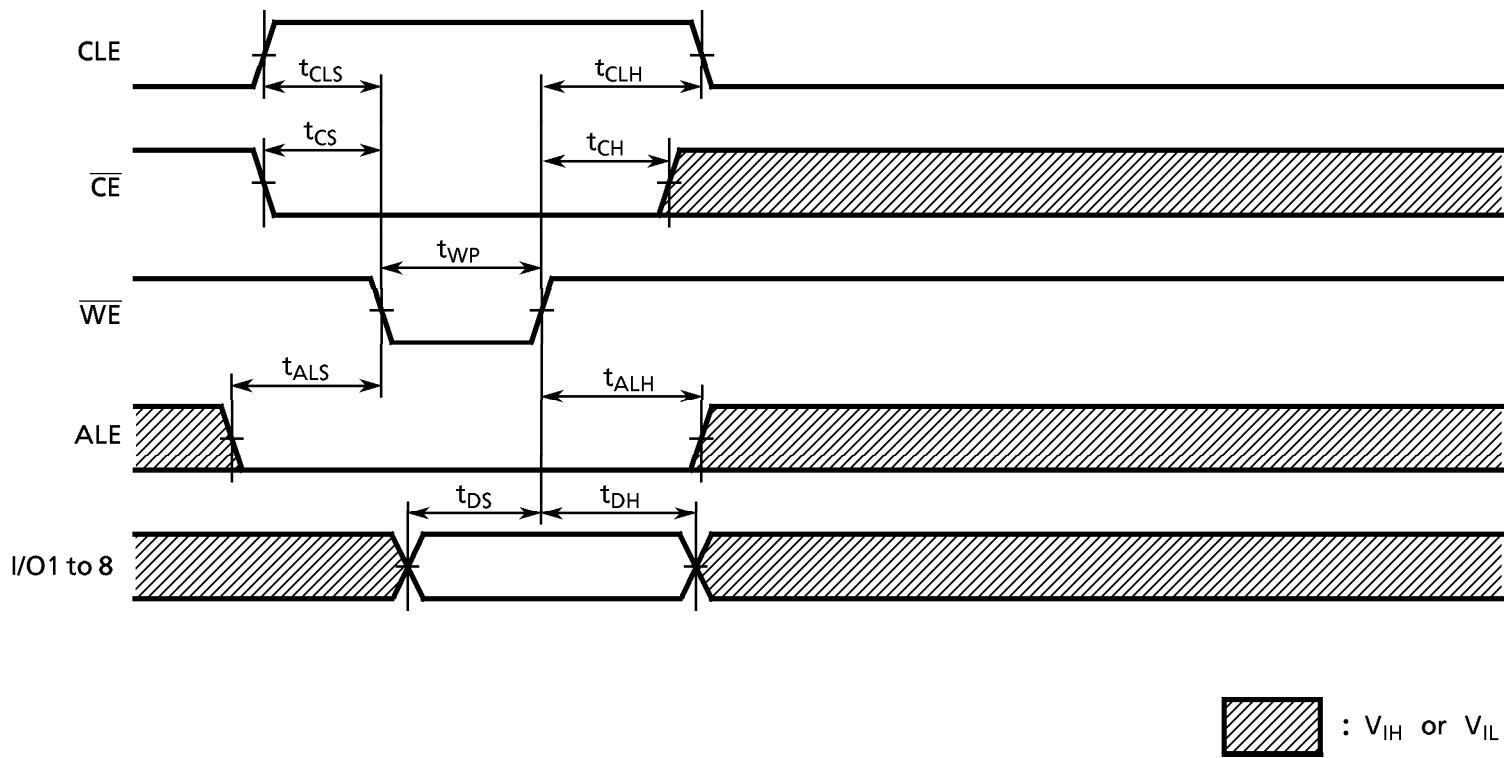
(2) Refer to Application Note (15) toward the end of this document.

TIMING DIAGRAMS

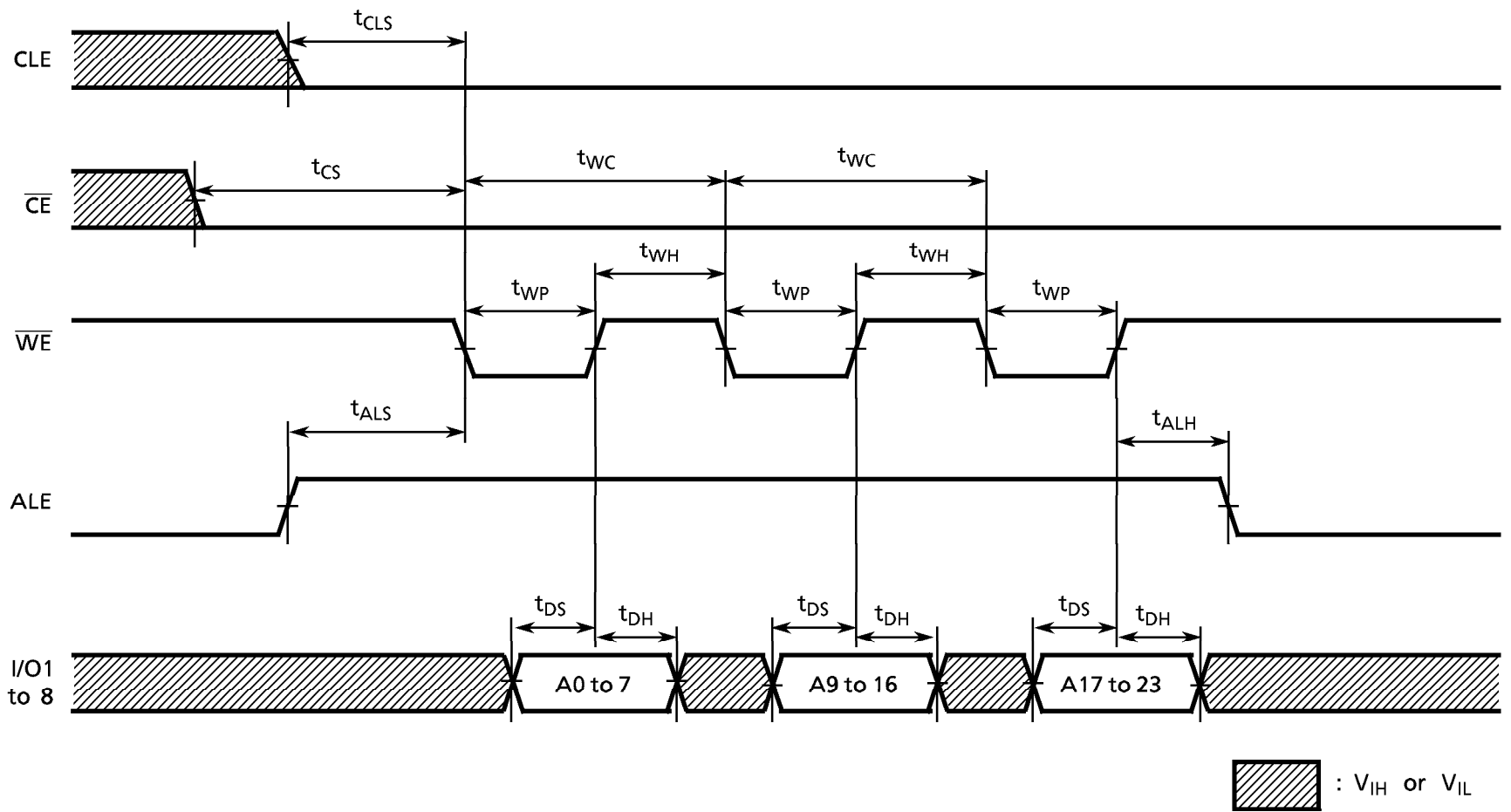
Latch Timing Diagram for Command/Address/Data



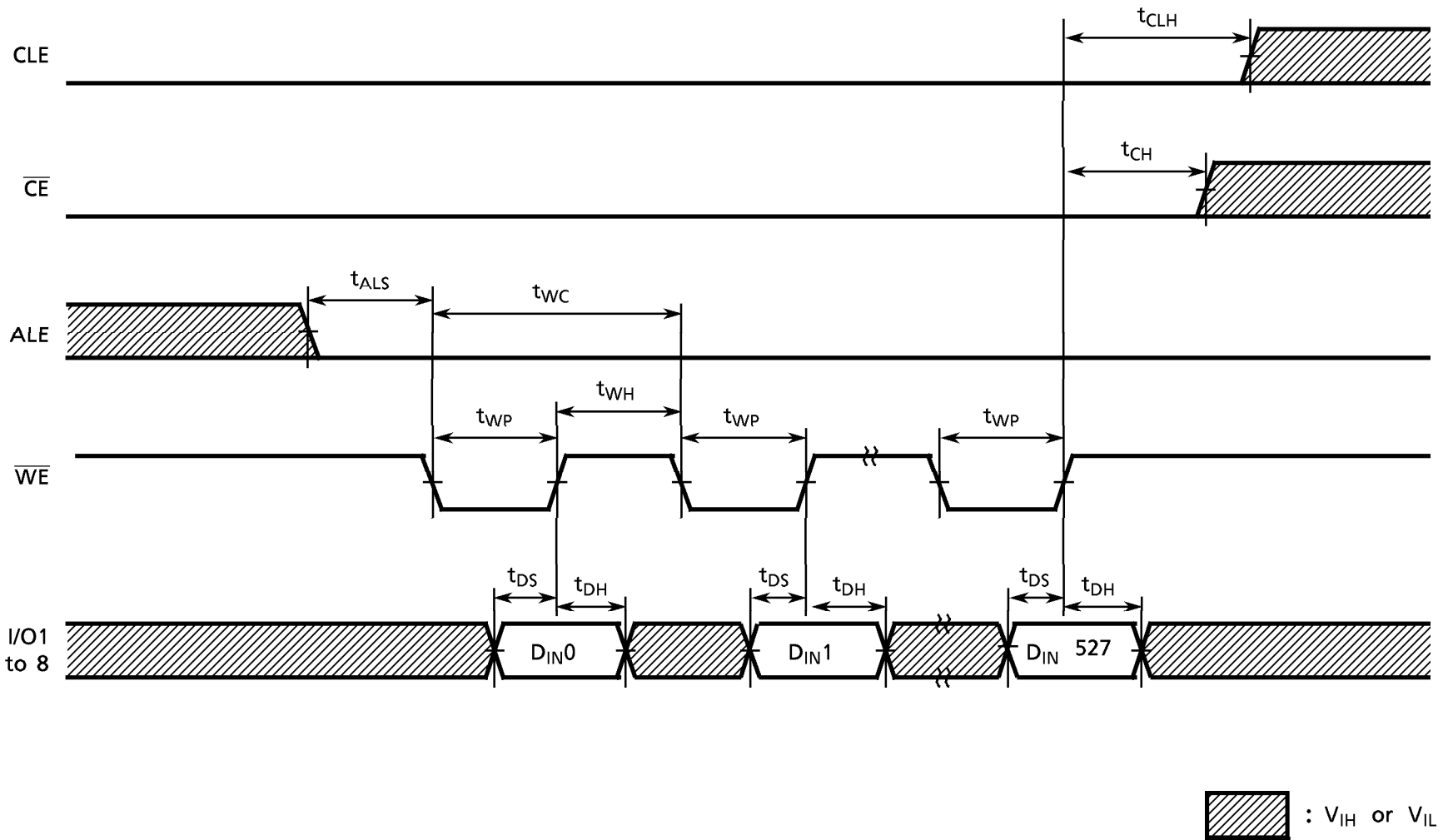
Command Input Cycle Timing Diagram



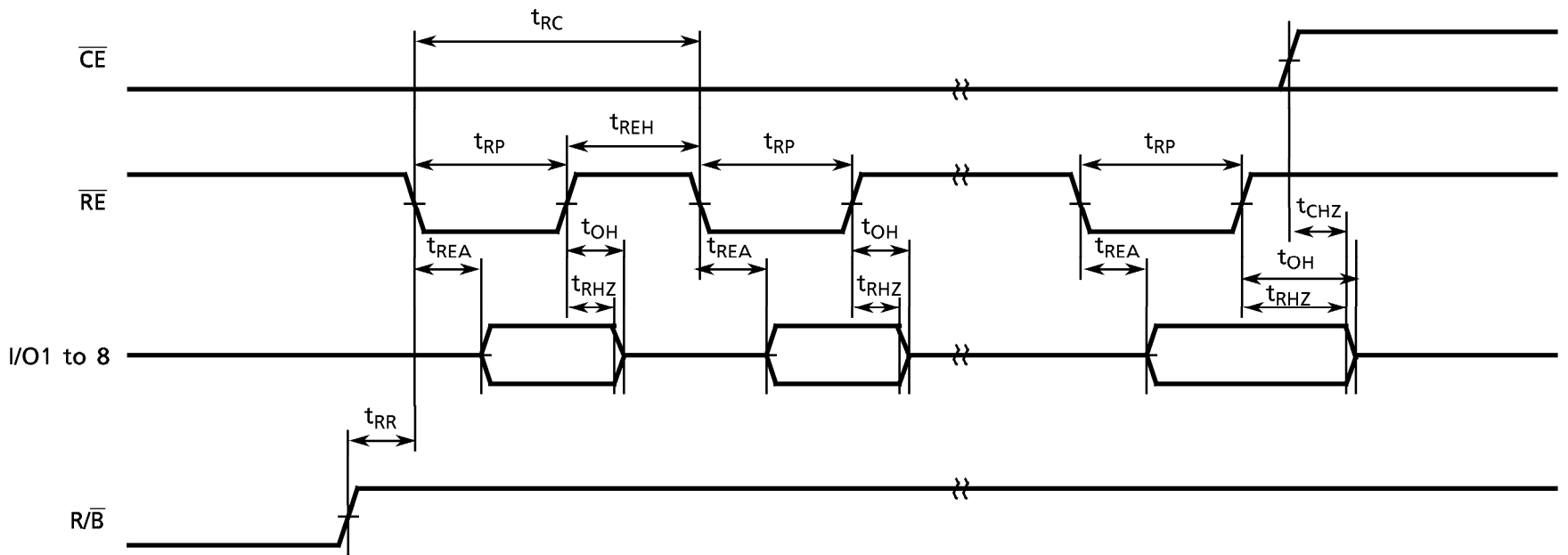
Address Input Cycle Timing Diagram



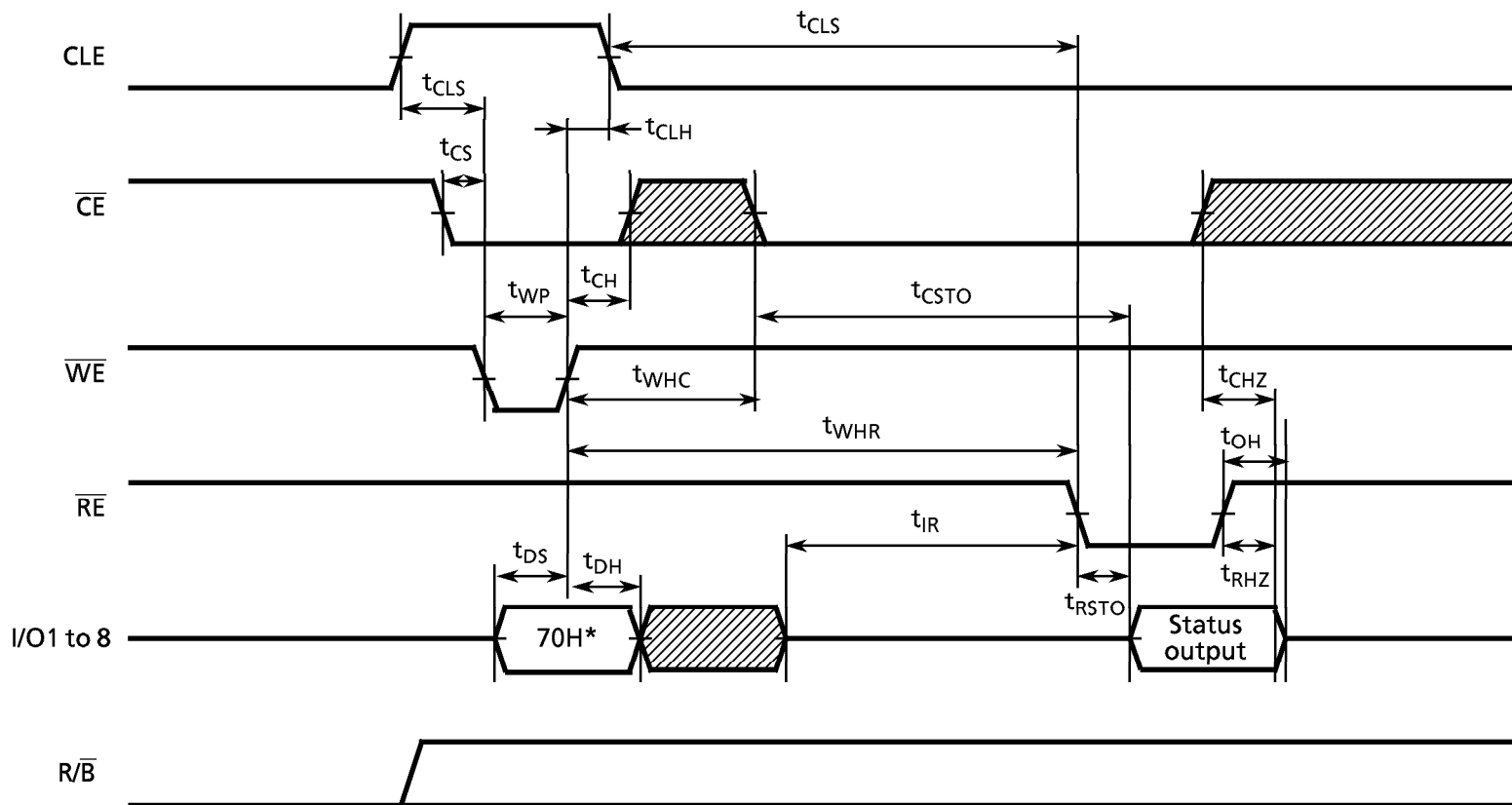
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram



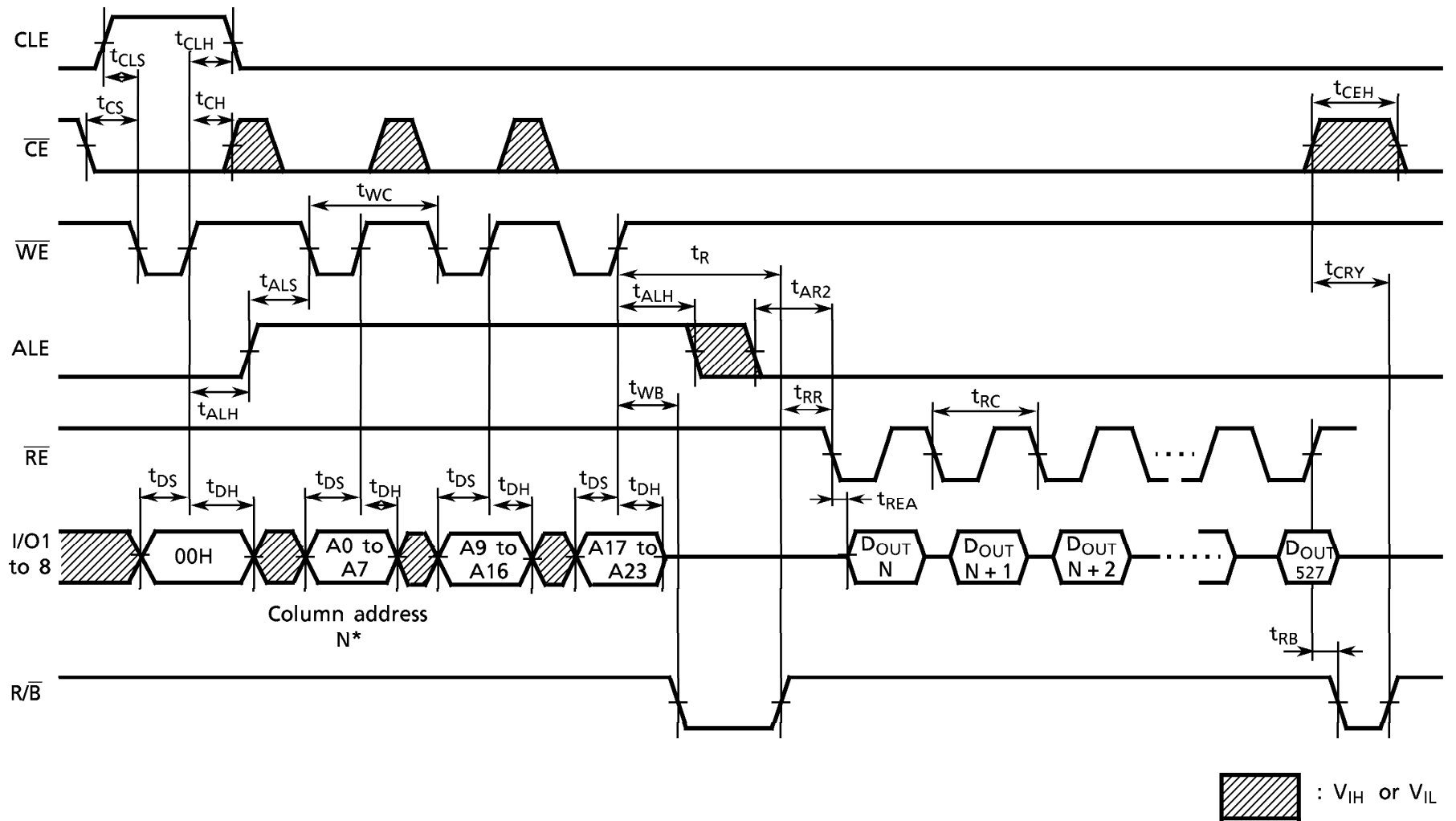
Status Read Cycle Timing Diagram



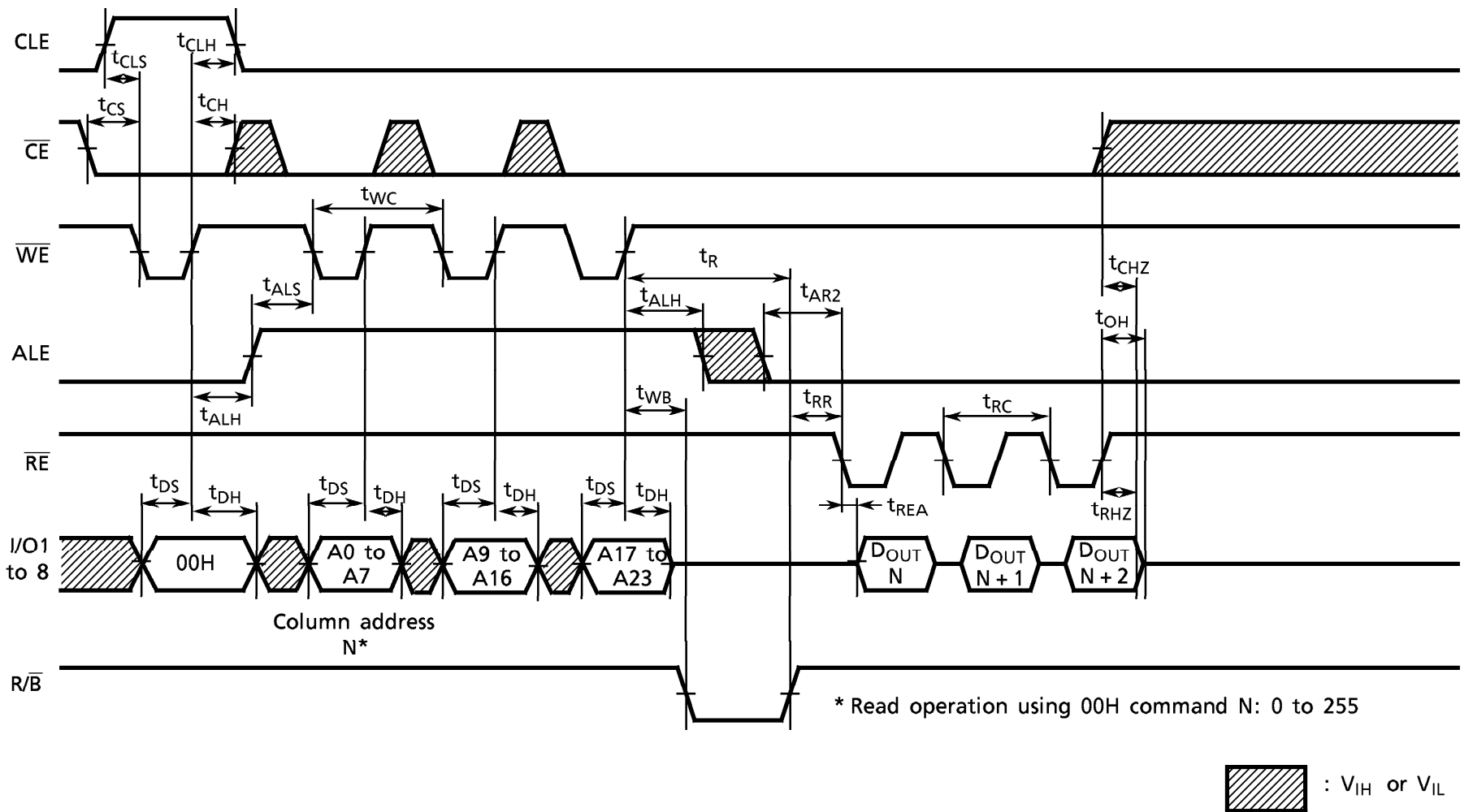
* 70H represents the hexadecimal number 70.

 : V_{IH} or V_{IL}

Read Cycle (1) Timing Diagram

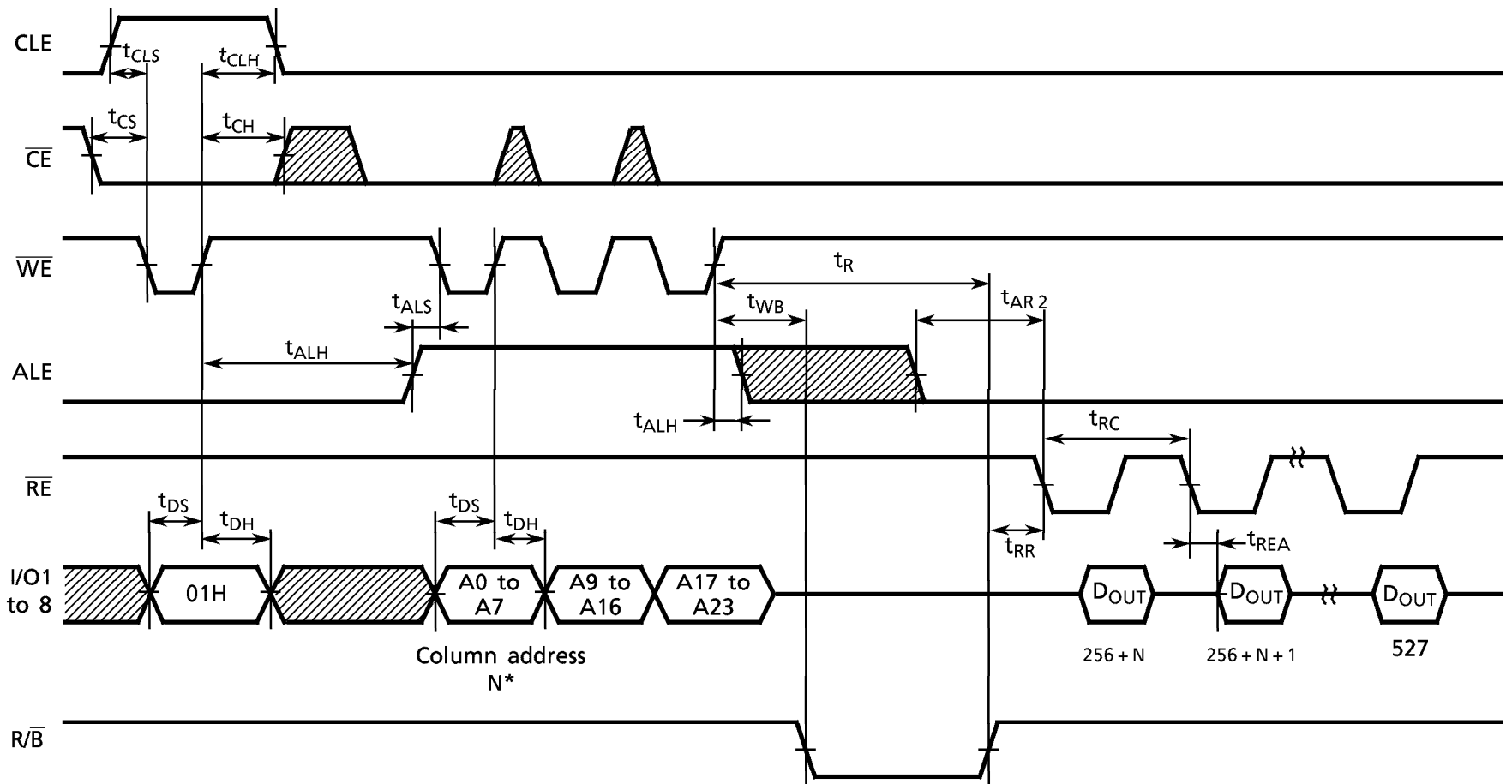


Read Cycle (1) Timing Diagram: When Interrupted by \overline{CE}



* Read operation using 00H command N: 0 to 255

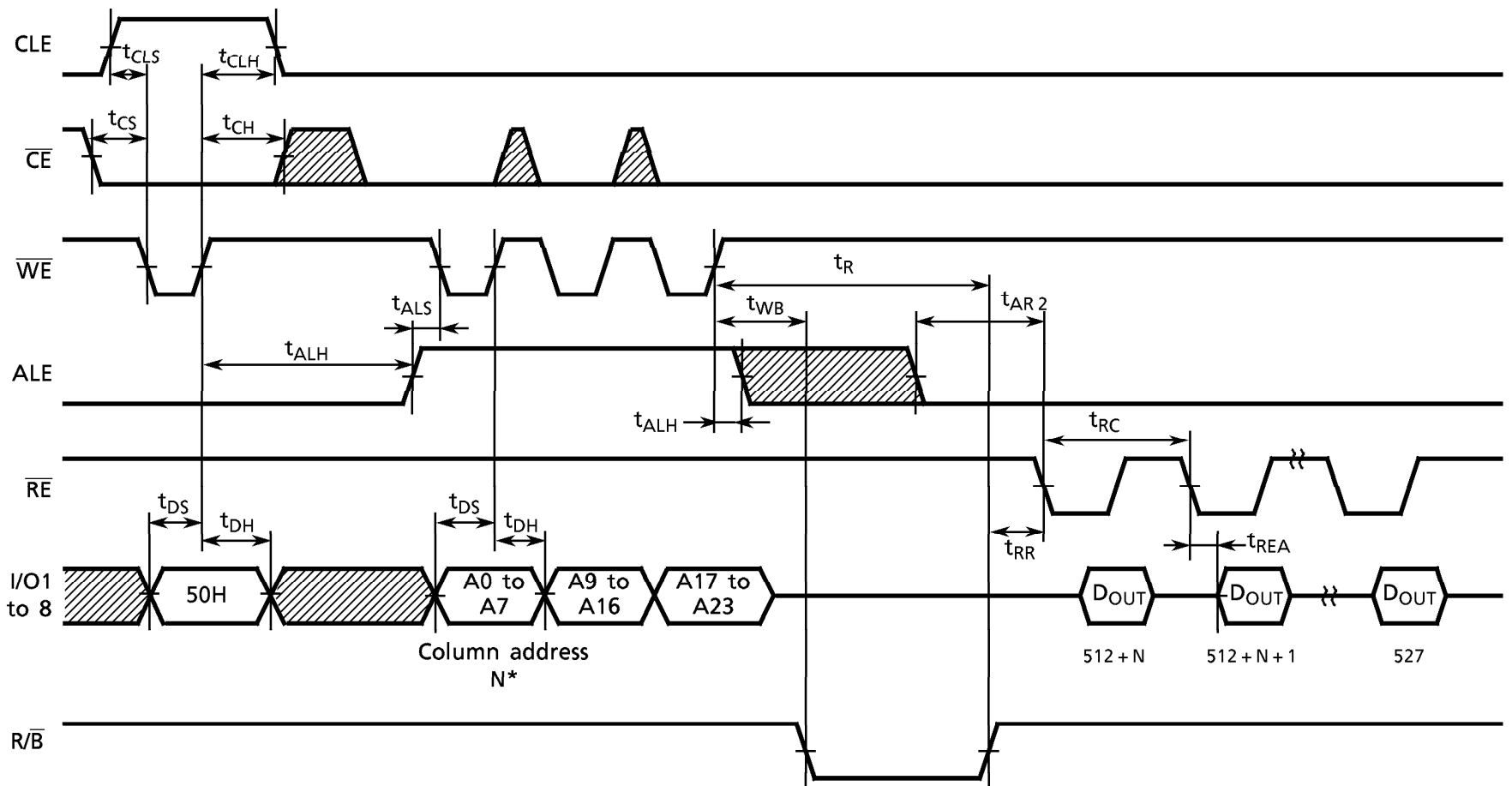
Read Cycle (2) Timing Diagram



* Read Operating using 01H command N : 0 to 255

: V_{IH} or V_{IL}

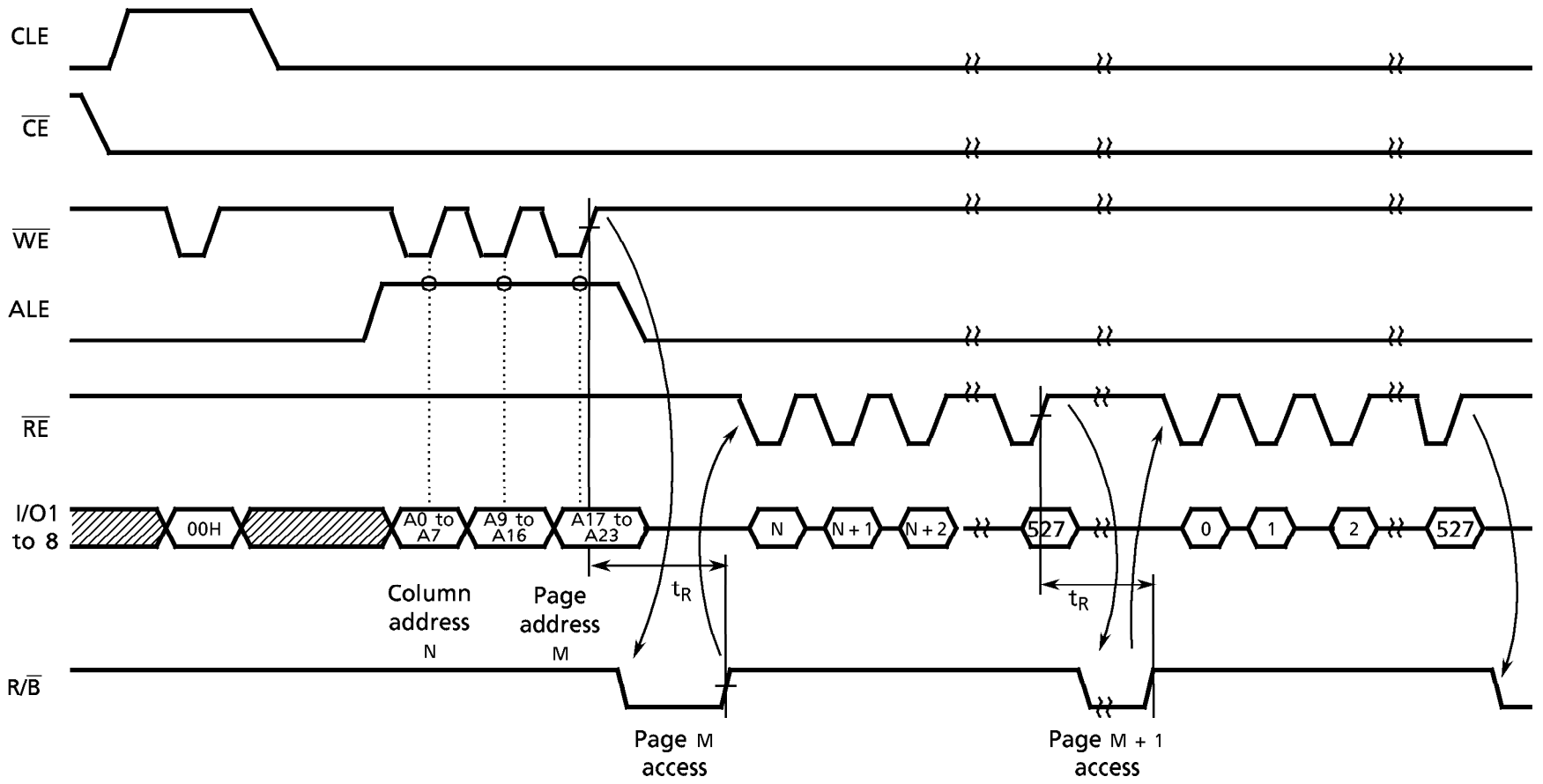
Read Cycle (3) Timing Diagram




* Read Operating using 01H command N : 0 to 15

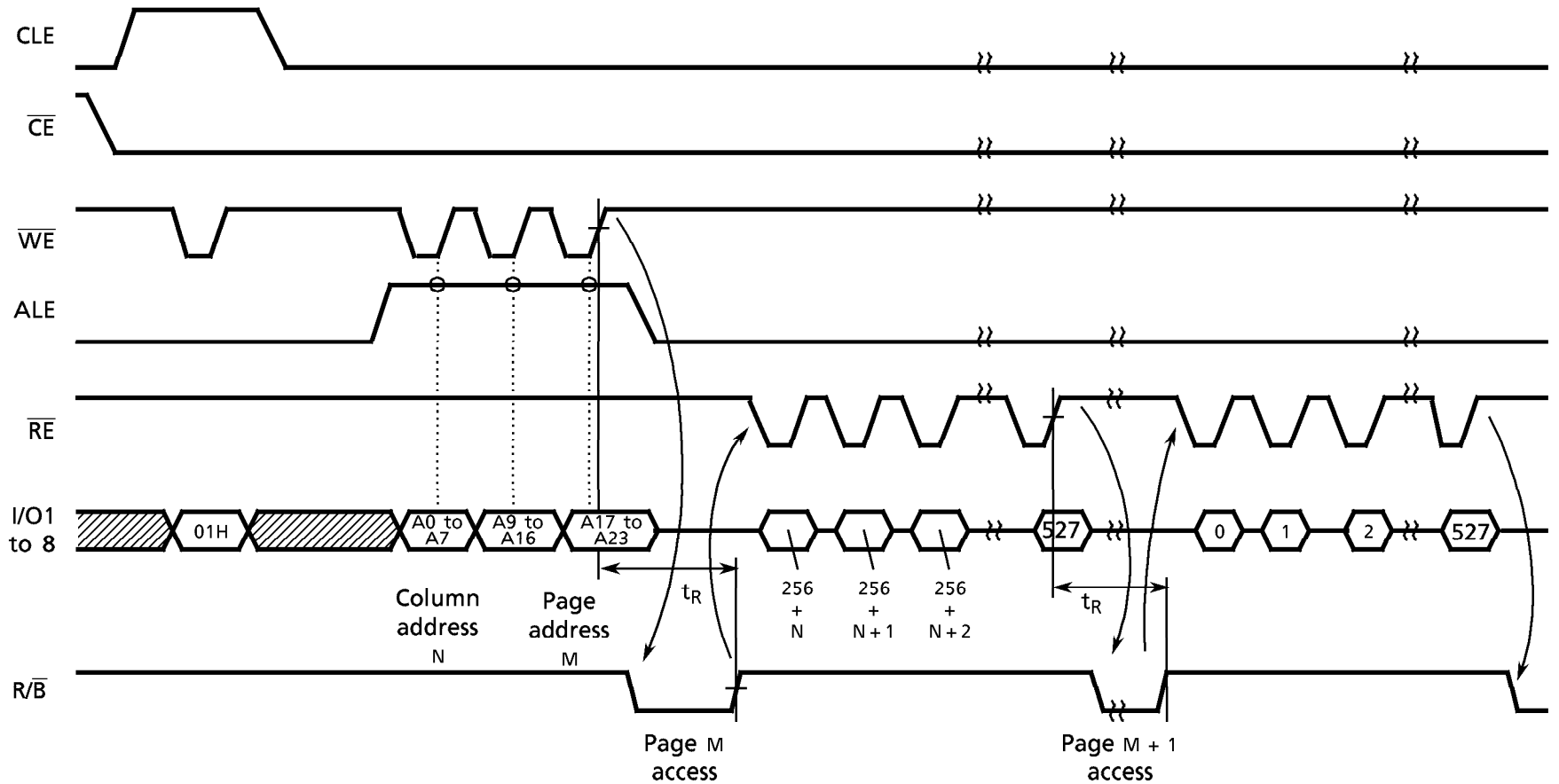
: V_{IH} or V_{IL}


Sequential Read (1) Timing Diagram



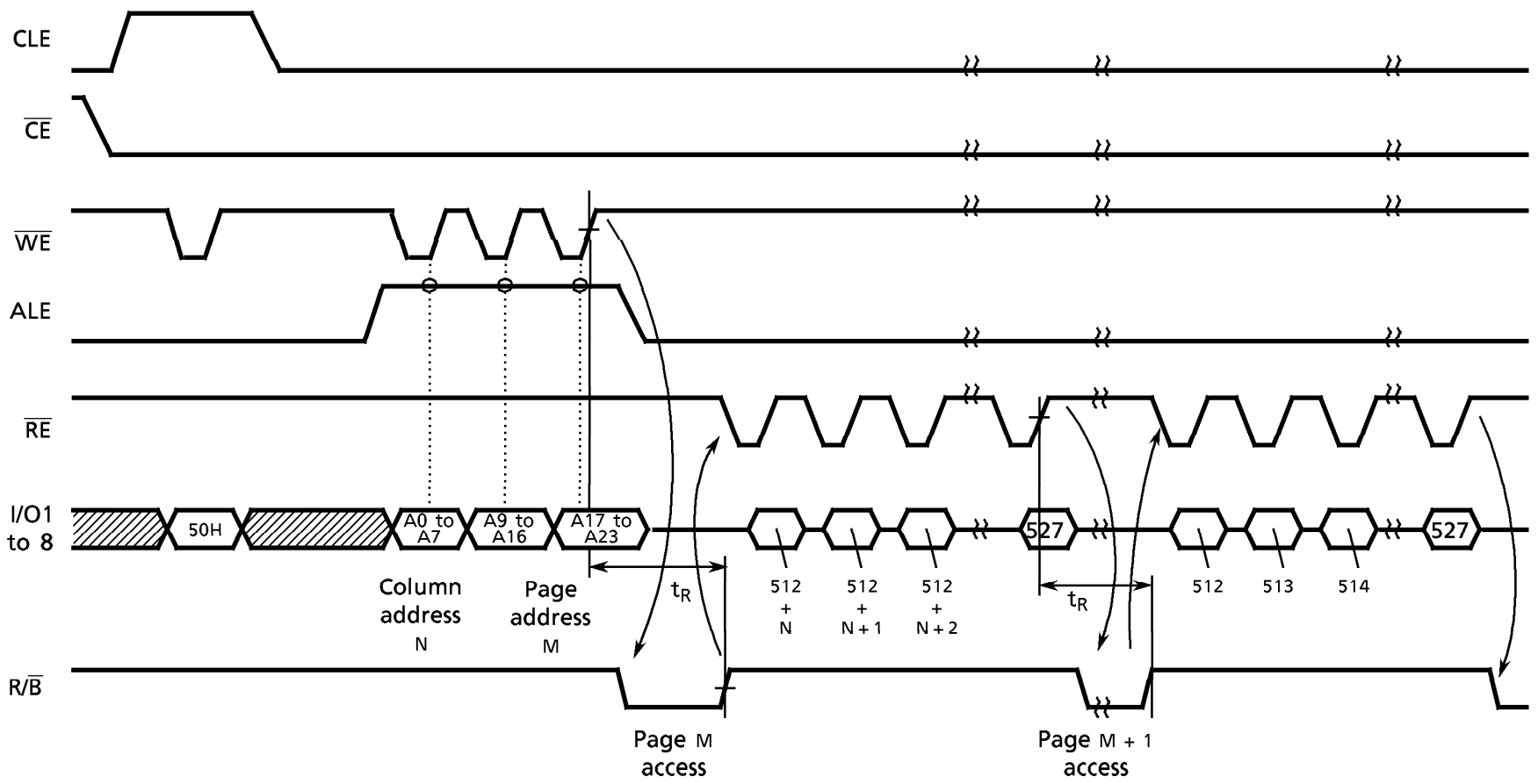
 : V_{IH} or V_{IL}

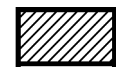
Sequential Read (2) Timing Diagram



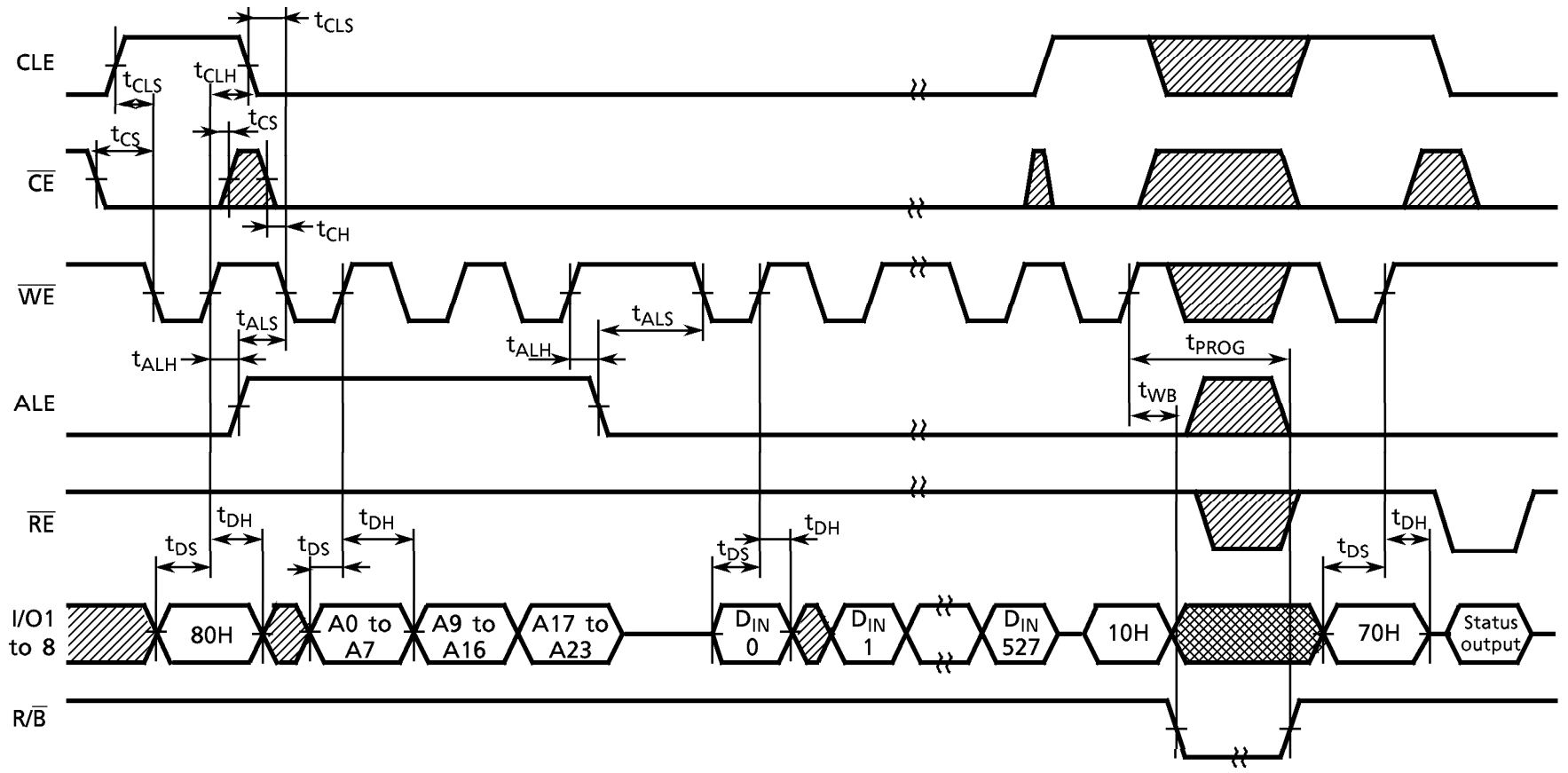
 : V_{IH} or V_{IL}

Sequential Read (3) Timing Diagram



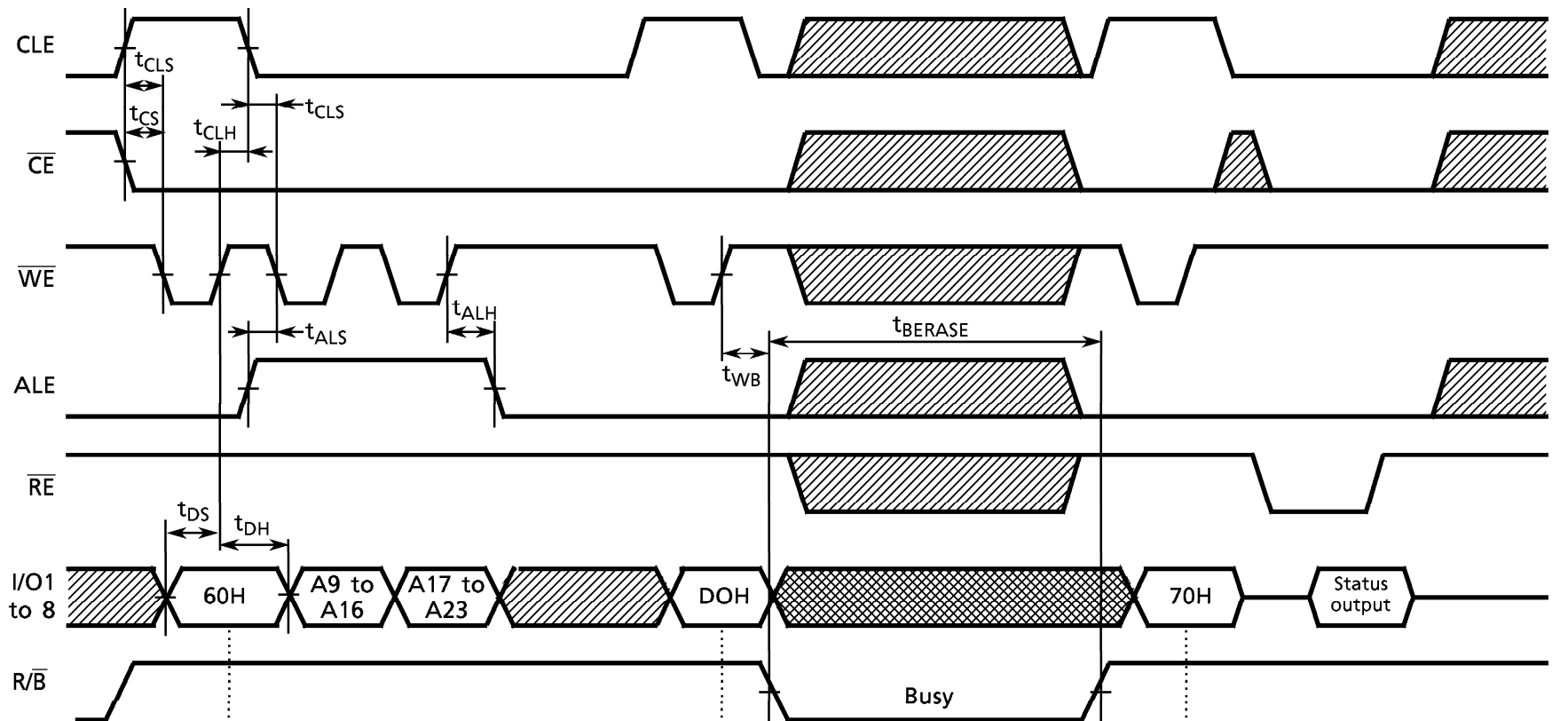
 : V_{IH} or V_{IL}

Auto-Program Operation Timing Diagram



: V_{IH} or V_{IL} : Do not input data while data is being output.

Auto Block Erase Timing Diagram



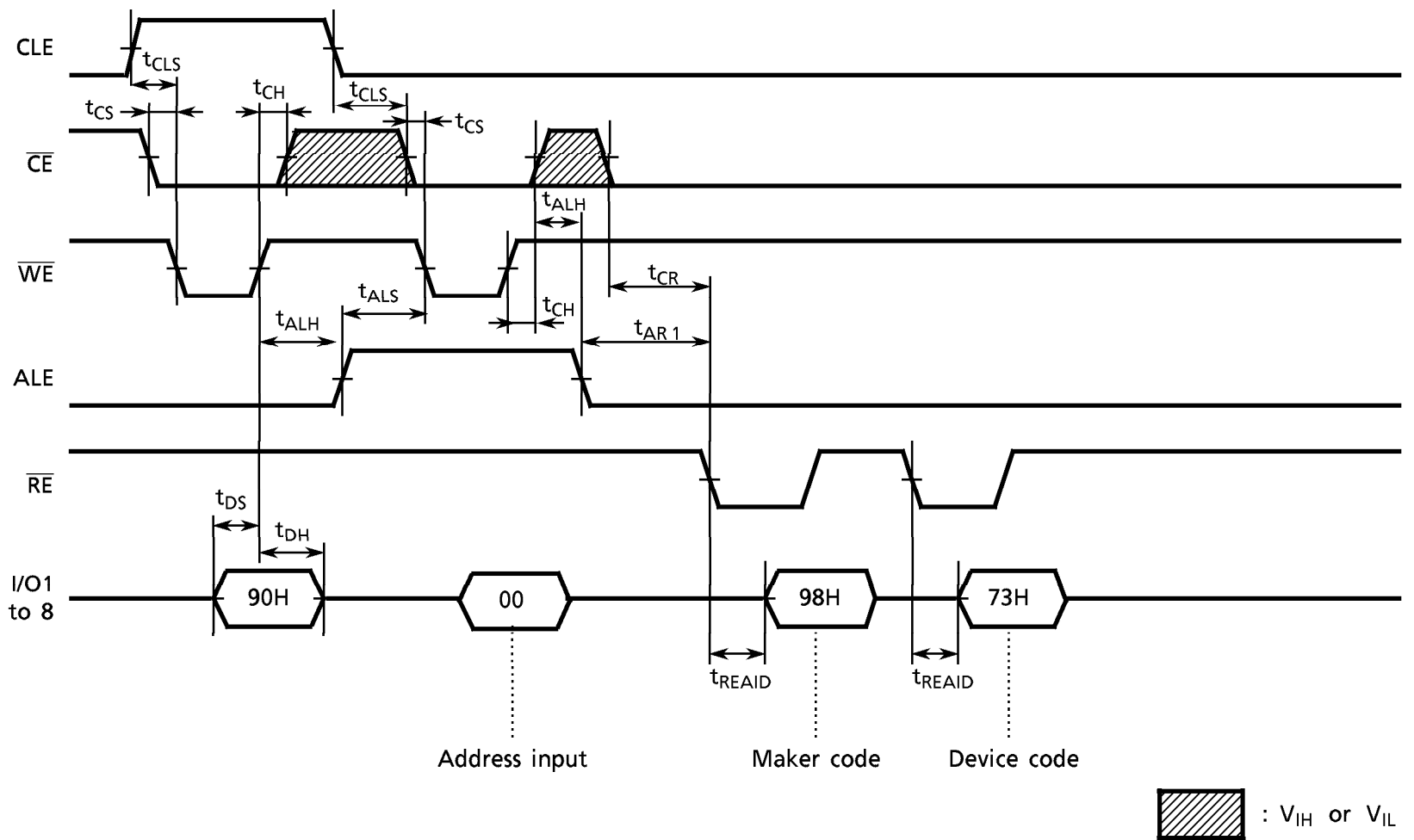
Auto Block Erase Setup command

Erase Start command

Status Read command

: V_{IH} or V_{IL} : Do not input data while data is being output.

ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information. The device pin-outs are configured as shown in Figure 1.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the \overline{WE} signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register. Address information is latched on the rising edge of \overline{WE} if ALE is High. Input data is latched if ALE is Low.

Chip Enable: \overline{CE}

The device goes into a low-power Standby mode when \overline{CE} goes High during a Read operation. The \overline{CE} signal is ignored when device is in Busy state ($R/\overline{B} = L$), such as during a Program or Erase operation, and will not enter Standby mode even if the \overline{CE} input goes High. The \overline{CE} signal must stay Low during the Read mode Busy state to ensure that memory array data is correctly transferred to the data register.

Write Enable: \overline{WE}

The \overline{WE} signal is used to control the acquisition of data from the I/O port.

Read Enable: \overline{RE}

The \overline{RE} signal controls serial data output. Data is available t_{REA} after the falling edge of \overline{RE} . The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: \overline{WP}

The \overline{WP} signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when \overline{WP} is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: R/\overline{B}

The R/\overline{B} output signal is used to indicate the operating condition of the device. The R/\overline{B} signal is in Busy state ($R/\overline{B} = L$) during the Program, Erase and Read operations and will return to Ready state ($R/\overline{B} = H$) after completion of the operation. The output buffer for this signal is an open drain.

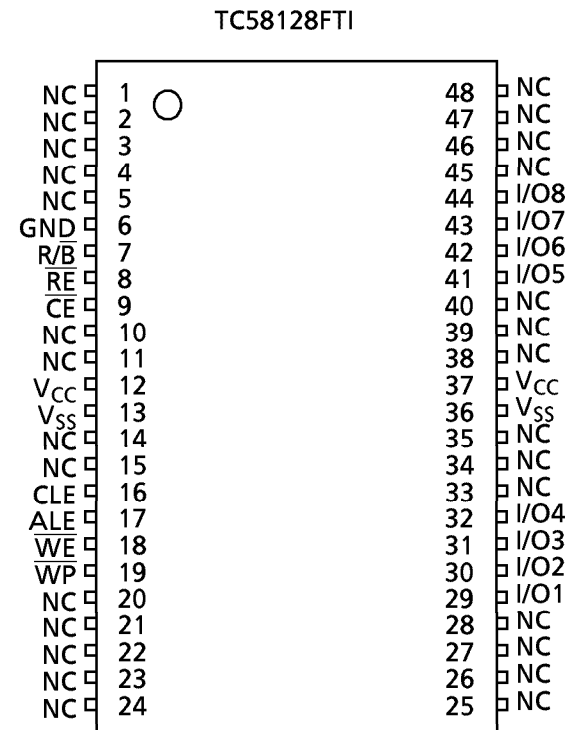


Figure 1. Pinout

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

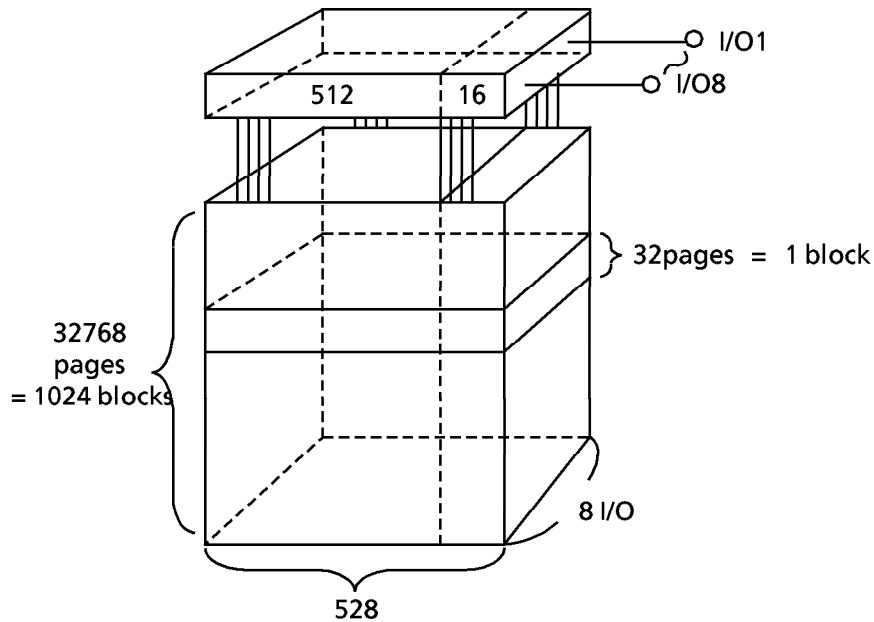


Figure 2. Schematic Cell Layout

A page consists of 528 bytes in which 512 bytes are used for main memory storage and 16 bytes are for redundancy or for other uses.

1 page = 528 bytes

1 block = 528 bytes × 32 pages = (16K + 512) bytes

Capacity = 528 bytes × 32 pages × 1024 blocks

An address is read in via the I/O port over three consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

| | I/O8 | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 |
|--------------|------|------|------|------|------|------|------|------|
| First cycle | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Second cycle | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 |
| Third cycle | *L | A23 | A22 | A21 | A20 | A19 | A18 | A17 |

A0 to A7: Column address
A9 to A23: Page address
(A14 to A23: Block address
A9 to A13: NAND address in block)

*: A8 is automatically set to Low or High by a 00H command or a 01H command.

*; I/O8 must be set to Low in the third cycle.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the eleven different command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{\text{CE}}$, $\overline{\text{WE}}$, $\overline{\text{RE}}$ and $\overline{\text{WP}}$ signals, as shown in Table 2.

Table 2. Logic Table

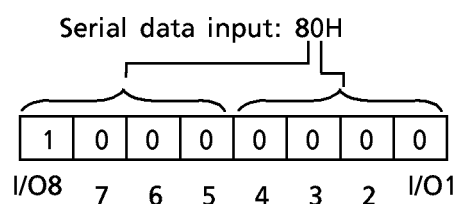
| | CLE | ALE | $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | $\overline{\text{RE}}$ | $\overline{\text{WP}}$ |
|---------------------------|-----|-----|------------------------|------------------------|------------------------|------------------------|
| Command Input | H | L | L | | H | * |
| Data Input | L | L | L | | H | * |
| Address Input | L | H | L | | H | * |
| Serial Data Output | L | L | L | H | | * |
| During Programming (Busy) | * | * | * | * | * | H |
| During Erasing (Busy) | * | * | * | * | * | H |
| Program, Erase Inhibit | * | * | * | * | * | L |

H: V_{IH} , L: V_{IL} , *: V_{IH} or V_{IL}

Table 3. Command table (HEX)

| | First Cycle | Second Cycle | Acceptable while Busy |
|-------------------|-------------|--------------|-----------------------|
| Serial Data Input | 80 | – | |
| Read Mode (1) | 00 | – | |
| Read Mode (2) | 01 | – | |
| Read Mode (3) | 50 | – | |
| Reset | FF | – | ○ |
| Auto Program | 10 | – | |
| Auto Block Erase | 60 | D0 | |
| Status Read | 70 | – | ○ |
| ID Read | 90 | – | |

HEX data bit assignment
(Example)



Once the device has been set to Read mode by a 00H, 01H or 50H command, additional Read commands are not needed for sequential page Read operations. Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

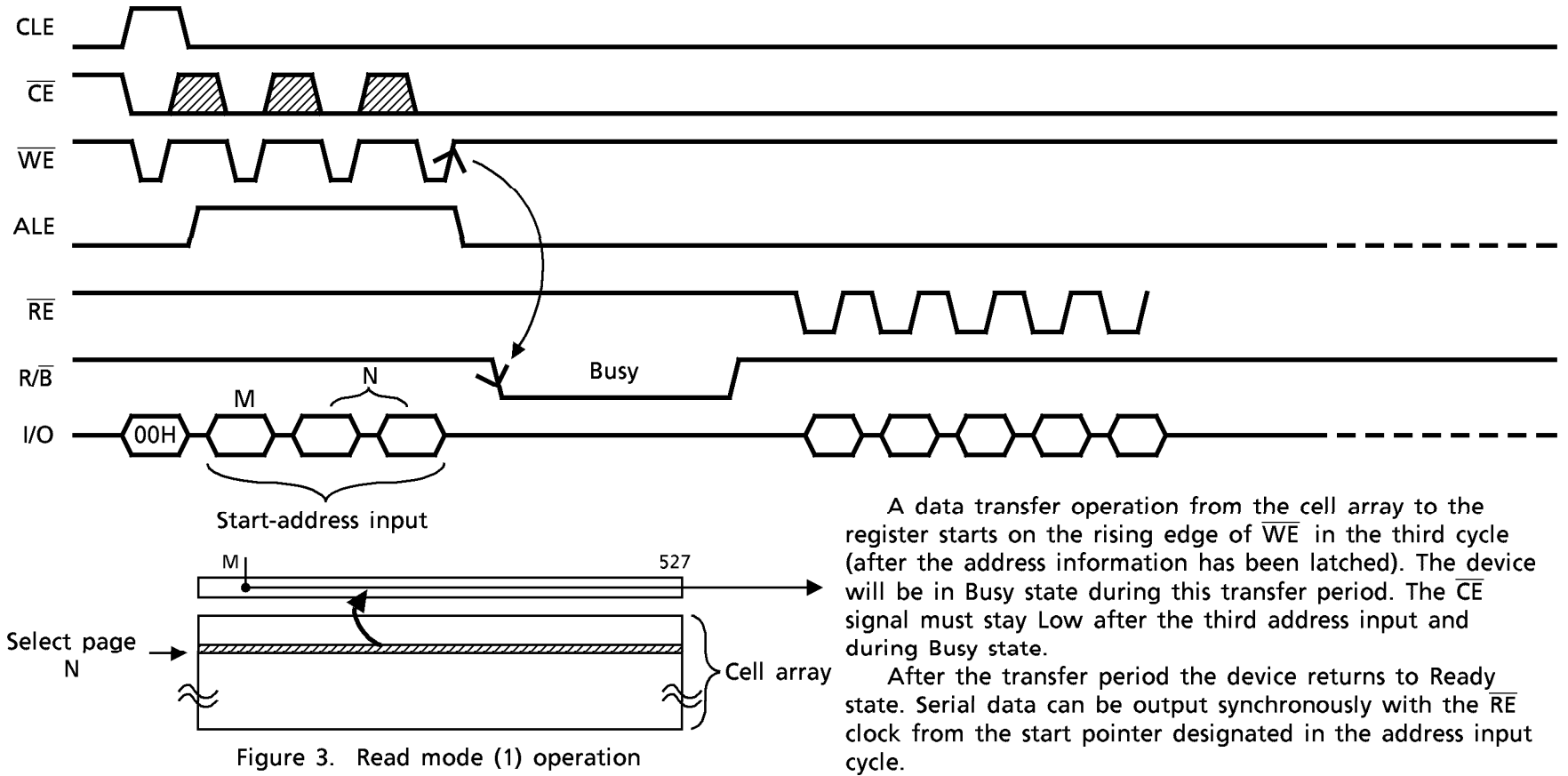
| | CLE | ALE | \overline{CE} | \overline{WE} | \overline{RE} | I/O1 TO I/O8 | Power |
|-----------------|-----|-----|-----------------|-----------------|-----------------|----------------|---------|
| Output Select | L | L | L | H | L | Data output | Active |
| Output Deselect | L | L | L | H | H | High impedance | Active |
| Standby | L | L | H | H | * | High impedance | Standby |

H: V_{IH} L: V_{IL} *: V_{IH} or V_{IL}

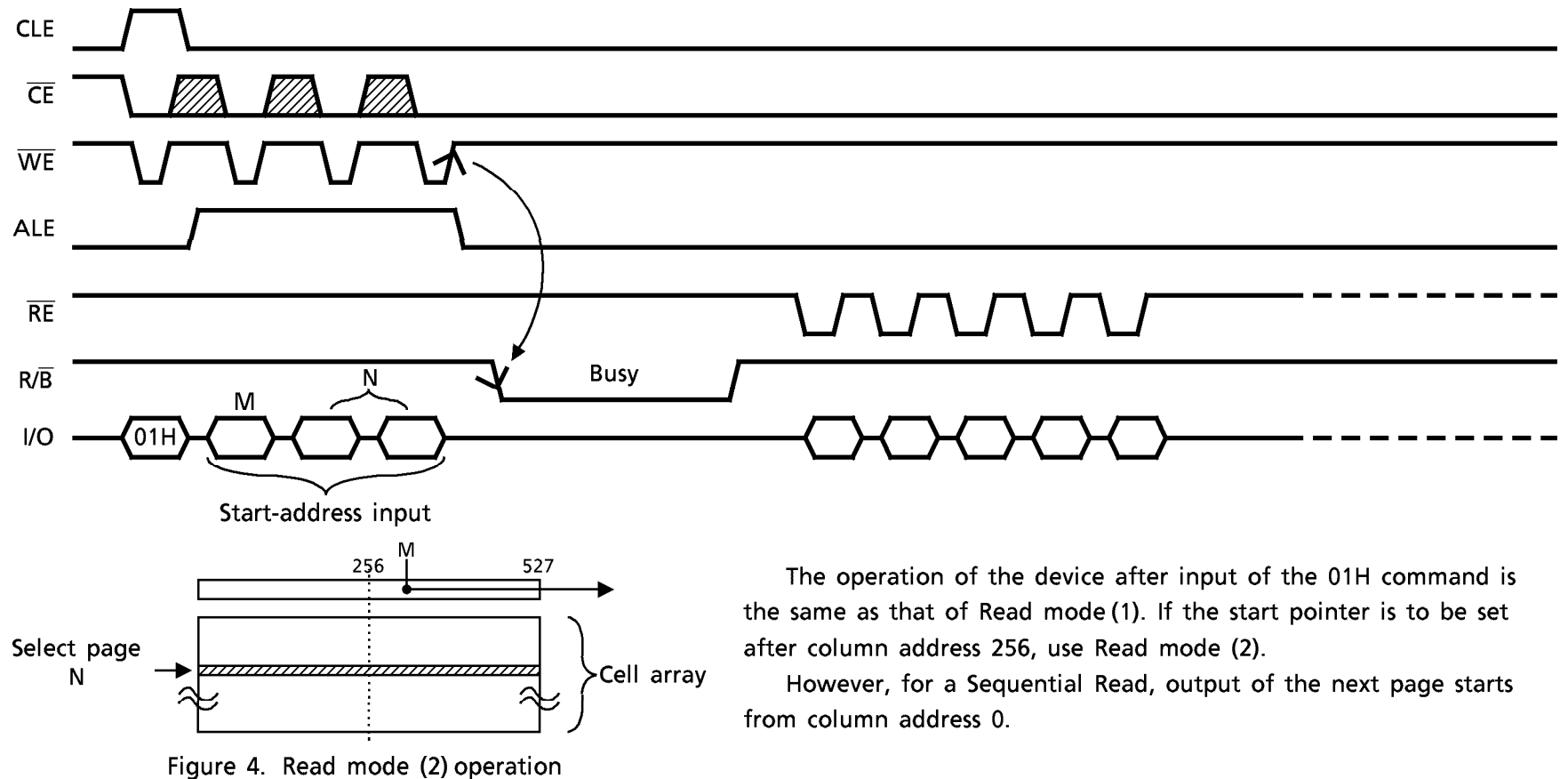
DEVICE OPERATION

Read Mode (1)

Read mode (1) is set when a "00H" command is issued to the Command register. Refer to Figure 3 below for timing details and the block diagram.



Read Mode (2)



Read Mode (3)

Read mode (3) has the same timing as Read modes (1) and (2) but is used to access information in the extra 16-byte redundancy area of the page. The start pointer is therefore set to a value between byte 512 and byte 527.

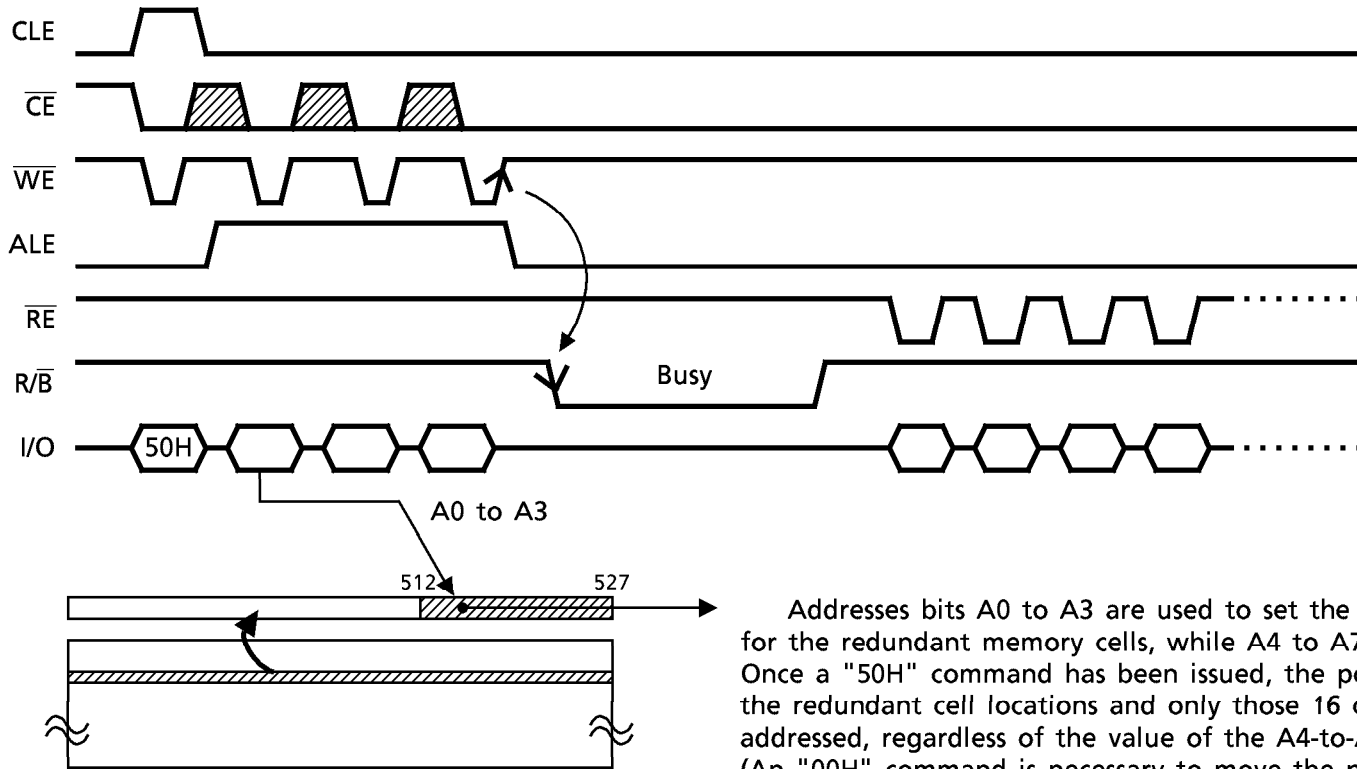
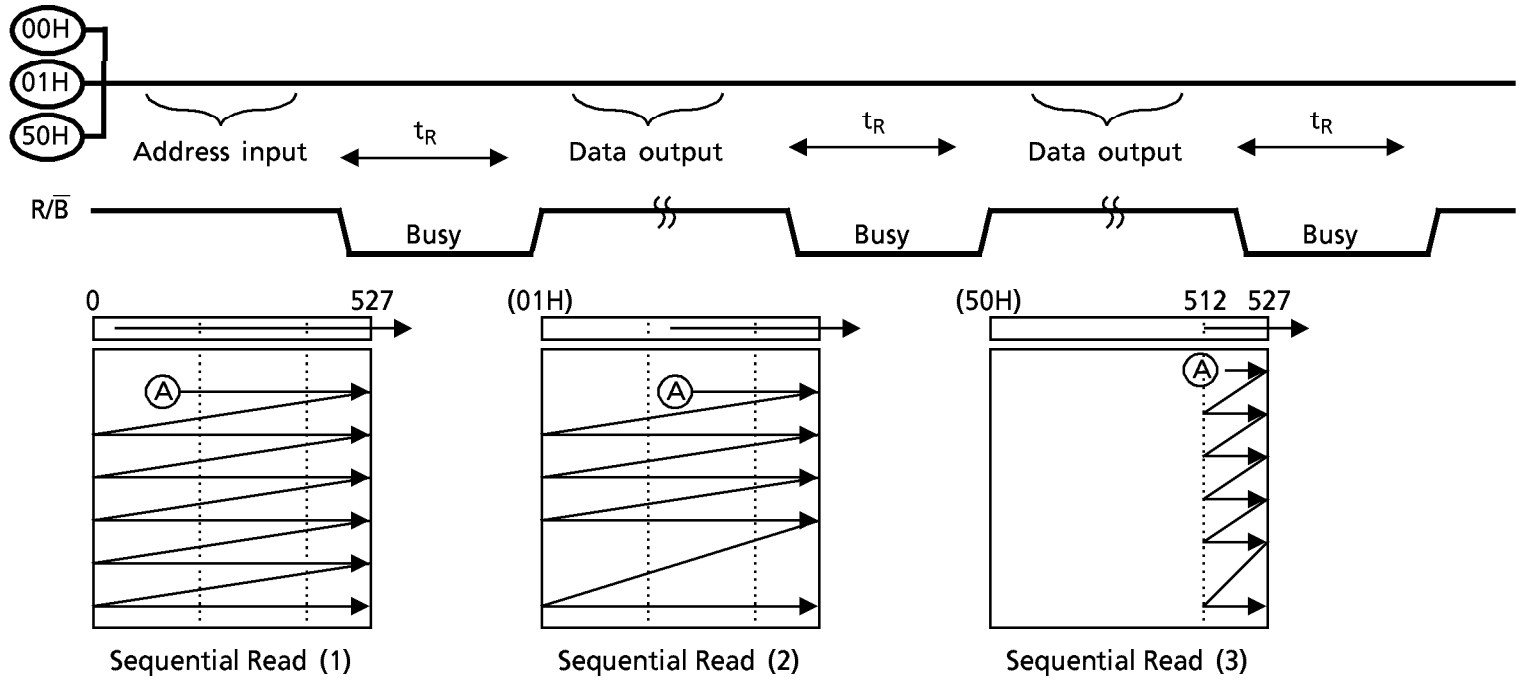


Figure 5. Read mode (3) operation

Addresses bits A0 to A3 are used to set the start pointer for the redundant memory cells, while A4 to A7 are ignored. Once a "50H" command has been issued, the pointer moves to the redundant cell locations and only those 16 cells can be addressed, regardless of the value of the A4-to-A7 address. (An "00H" command is necessary to move the pointer back to the 0-to-511 main memory cell location.)

Sequential Read (1)(2)(3)

This mode allows the sequential reading of pages without additional address input.



Sequential Read modes (1) and (2) output the contents of addresses 0 to 527 as shown above, while Sequential Read mode (3) outputs the contents of the redundant address locations only. When the pointer reaches the last address, the device continues to output the data from this address ** on each $\overline{R/E}$ clock signal.

** Column address 527 on the last page

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the $\overline{R\overline{B}}$ clock after a "70H" command input. The resulting information is outlined in Table 5.

Table 5. Status output table

| | STATUS | OUTPUT | |
|------|---------------|------------|------------------|
| I/O1 | Pass/Fail | Pass: 0 | Fail: 1 |
| I/O2 | Not Used | 0 | |
| I/O3 | Not Used | 0 | |
| I/O4 | Not Used | 0 | |
| I/O5 | Not Used | 0 | |
| I/O6 | Not Used | 0 | |
| I/O7 | Ready/Busy | Ready: 1 | Busy: 0 |
| I/O8 | Write Protect | Protect: 0 | Not Protected: 1 |

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state.

An application example with multiple devices is shown in Figure 6.

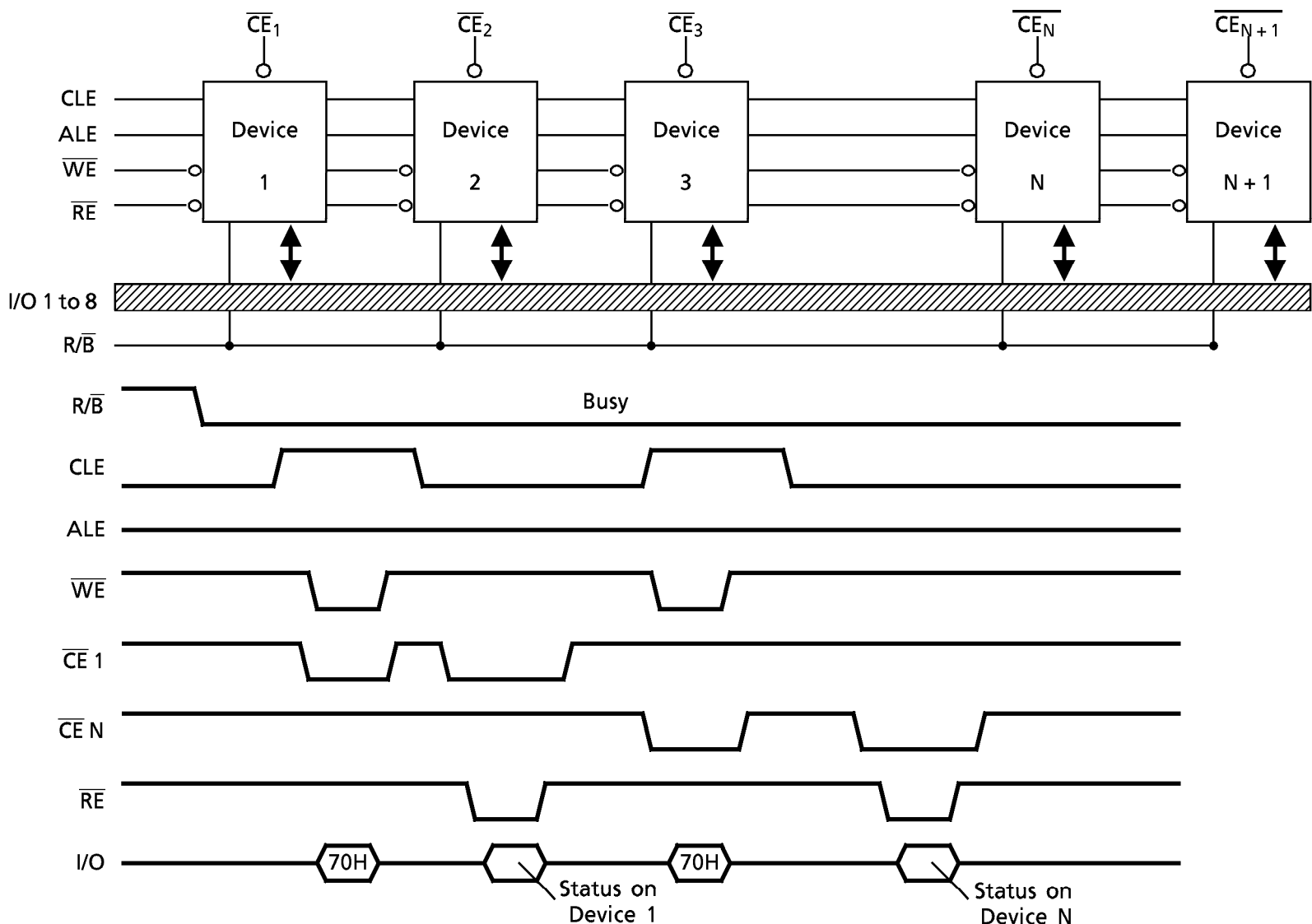


Figure 6. Status Read timing application example

System Design Note: If the $\overline{R\overline{B}}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The device carries out an Automatic Page Program operation when it receives a "10H" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

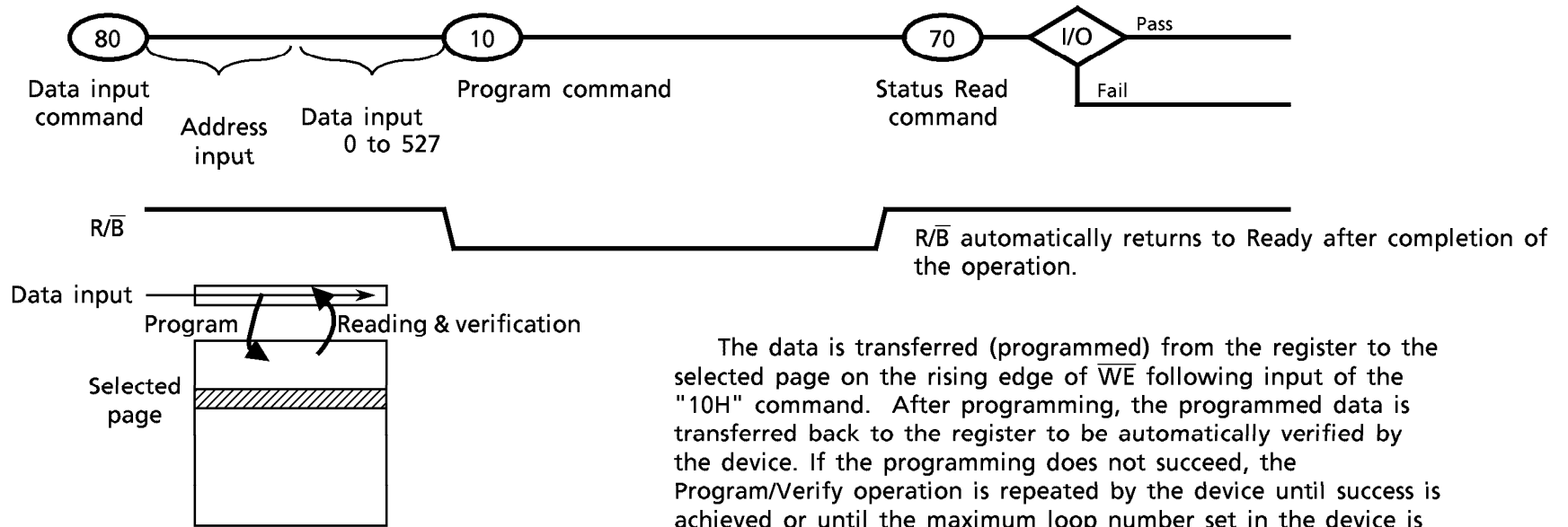
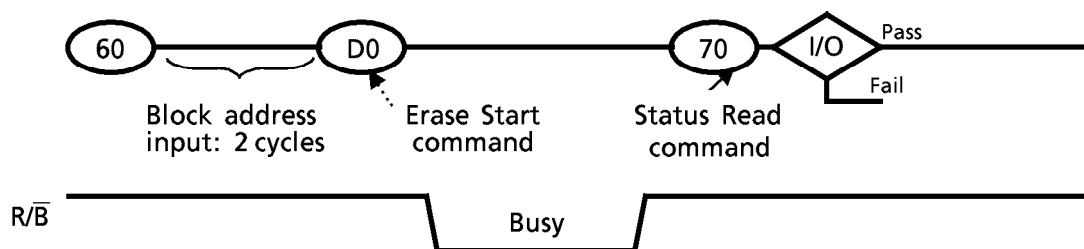


Figure 7. Auto Page Program operation

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of \bar{WE} after the Erase Start command "D0H" which follows the Erase Setup command "60H". This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state. The address and data registers are set as follows after a Reset:

- Address Register: All "0"
- Data Register: All "1"
- Operation Mode: Wait state

The response to an "FFH" Reset command input during the various device operations is as follows:

- When a Reset (FFH) command is input during programming

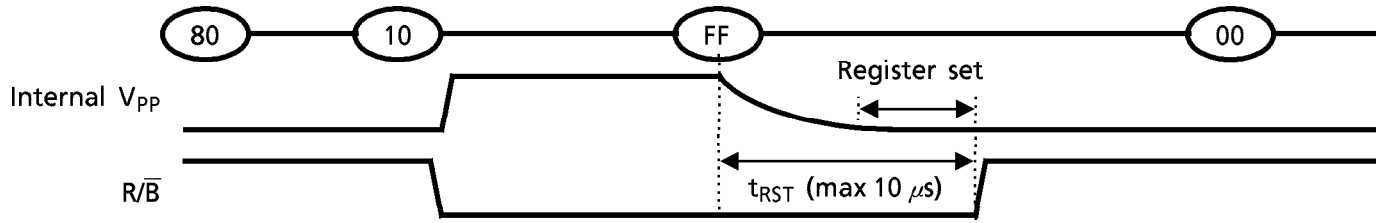


Figure 8.

- When a Reset (FFH) command is input during erasing

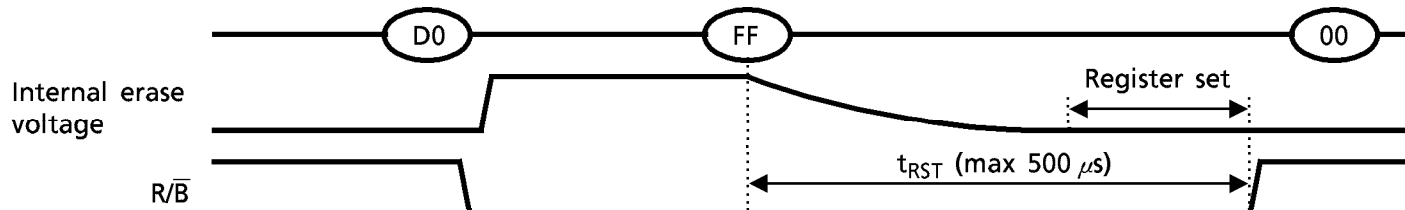


Figure 9.

- When a Reset (FFH) command is input during a Read operation

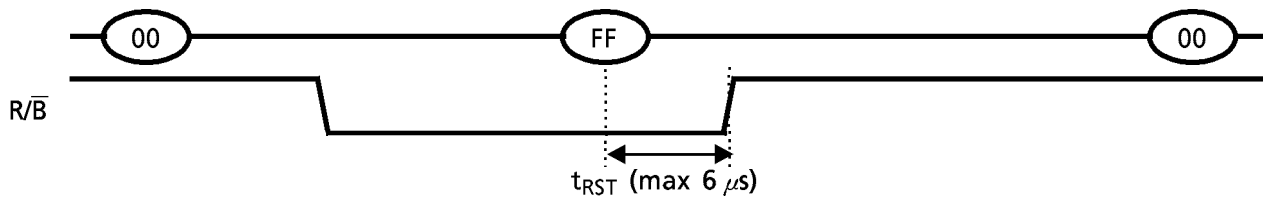


Figure 10.

- When a Status Read command (70H) is input after a Reset

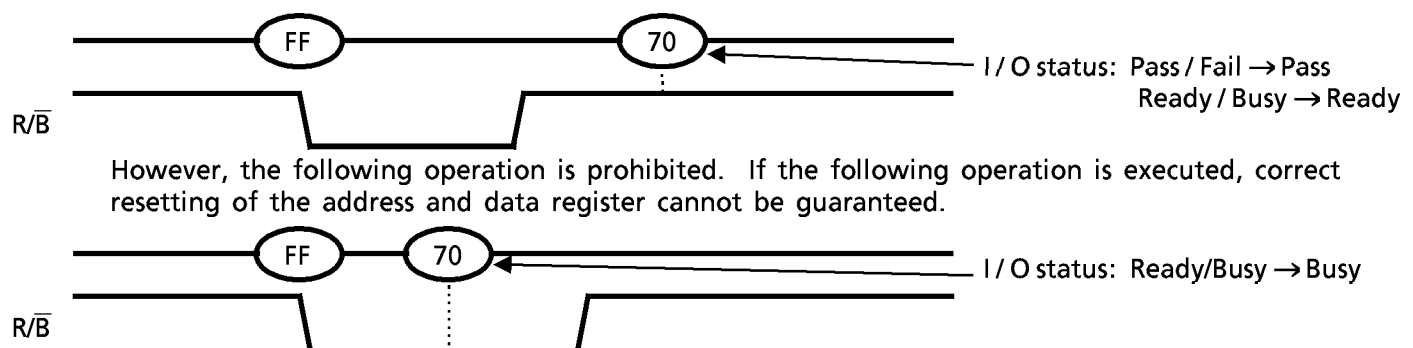


Figure 11.

- When two or more Reset commands are input in succession

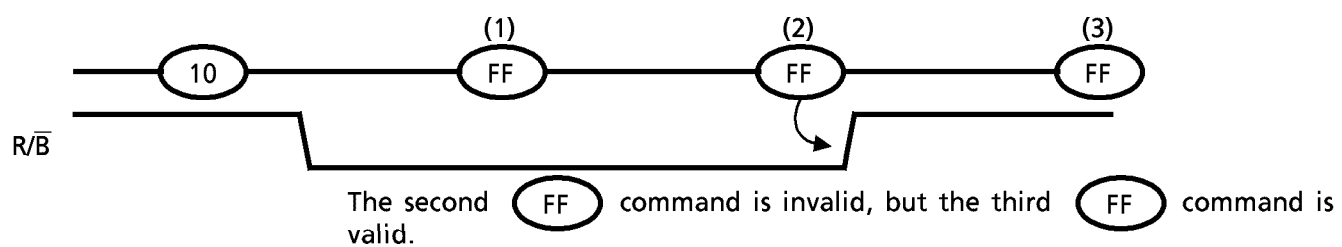
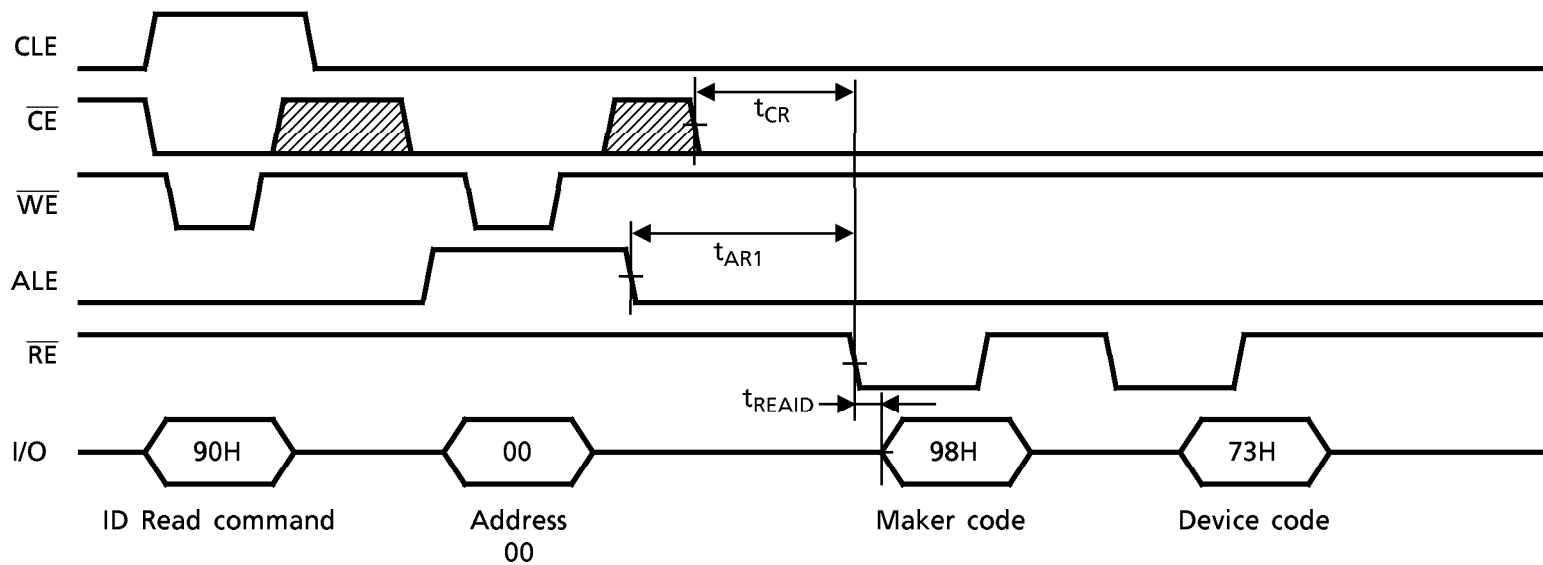


Figure 12.

ID Read

The TC58128 contains ID codes which identify the device type and the manufacturer. The ID codes can be read out under the following timing conditions:



For the specifications of the access times t_{REAID} , t_{CR} and t_{AR1} refer to the AC Characteristics.

Figure 13. ID Read timing

Table 6. Code table

| | I/O8 | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | Hex Data |
|-------------|------|------|------|------|------|------|------|------|----------|
| Maker code | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 98H |
| Device code | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 73H |

APPLICATION NOTES AND COMMENTS

(1) Prohibition of unspecified commands

The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(2) Restriction of command while Busy state

During Busy state, do not input any command except 70H and FFH.

(3) Pointer control for "00H", "01H" and "50H"

The device has three Read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and Figure 14 is a block diagram of their operations.

Table 7. Pointer Destination

| Read Mode | Command | Pointer |
|-----------|---------|------------|
| (1) | 00H | 0 to 255 |
| (2) | 01H | 256 to 511 |
| (3) | 50H | 512 to 527 |

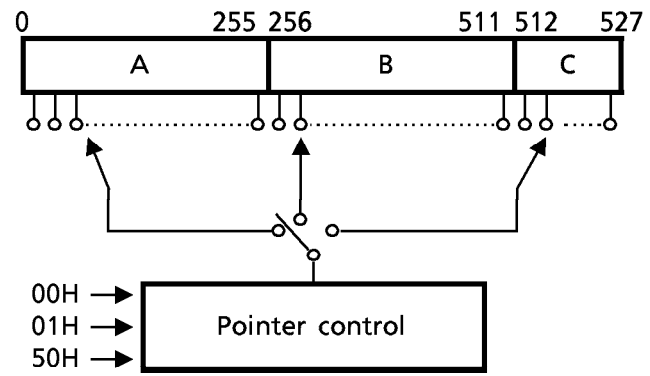
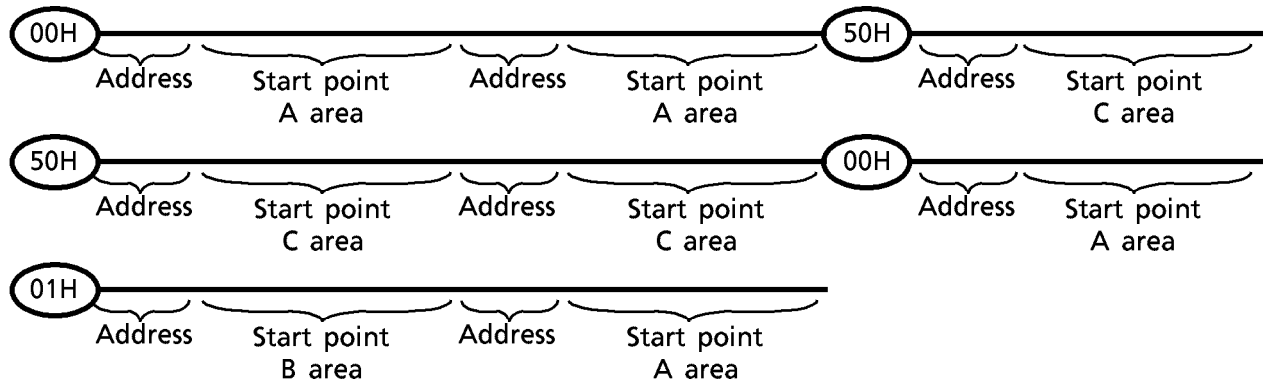


Figure 14. Pointer control

The pointer is set to region A by the "00H" command, to region B by the "01H" command, and to region C by the "50H" command.

(Example)

The "00H" command must be input to set the pointer back to region A when the pointer is pointing to region C.



To program region C only, set the start point to region C using the 50H command.

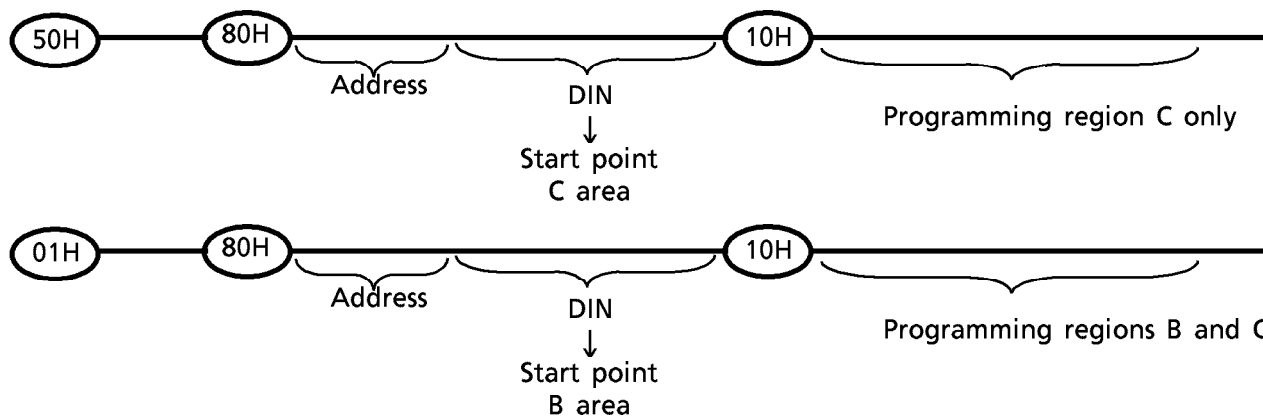


Figure 15. Example of How to Set the Pointer

(4) Acceptable commands after Serial Input command "80H"

Once the Serial Input command "80H" has been input, do not input any command other than the Program Execution command "10H" or the Reset command "FFH".

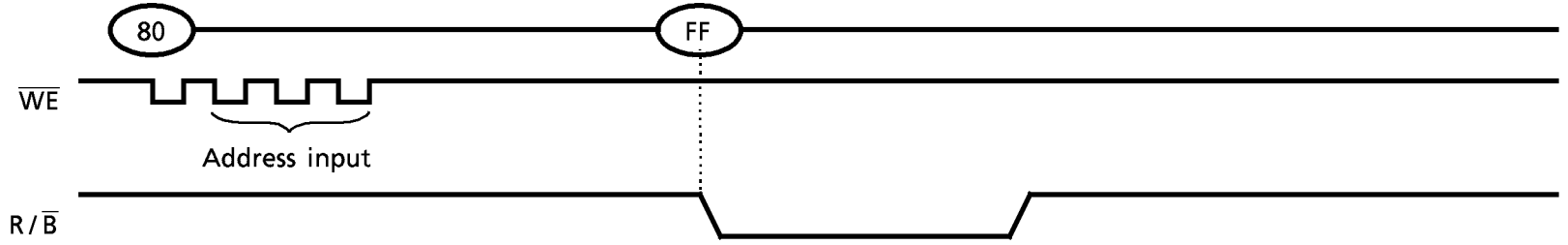
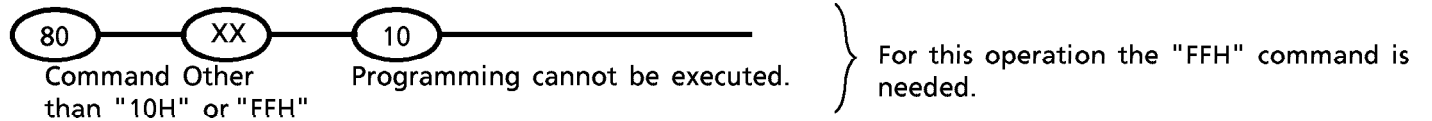


Figure 16.

If a command other than "10H" or "FFH" is input, the Program operation is not performed.



(5) Status Read during a Read operation

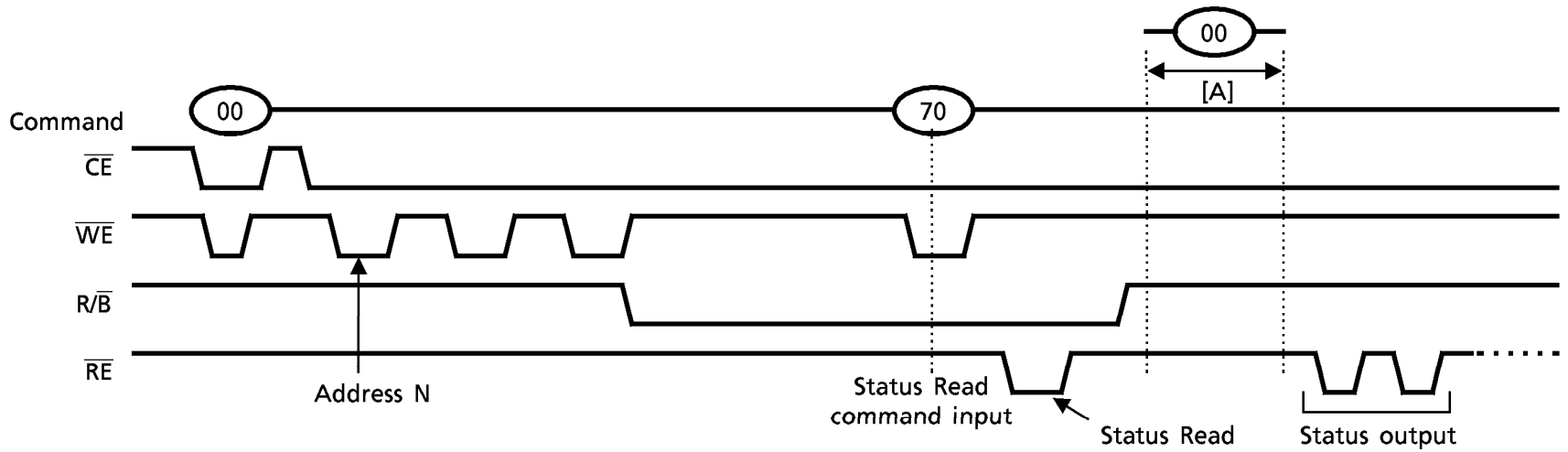


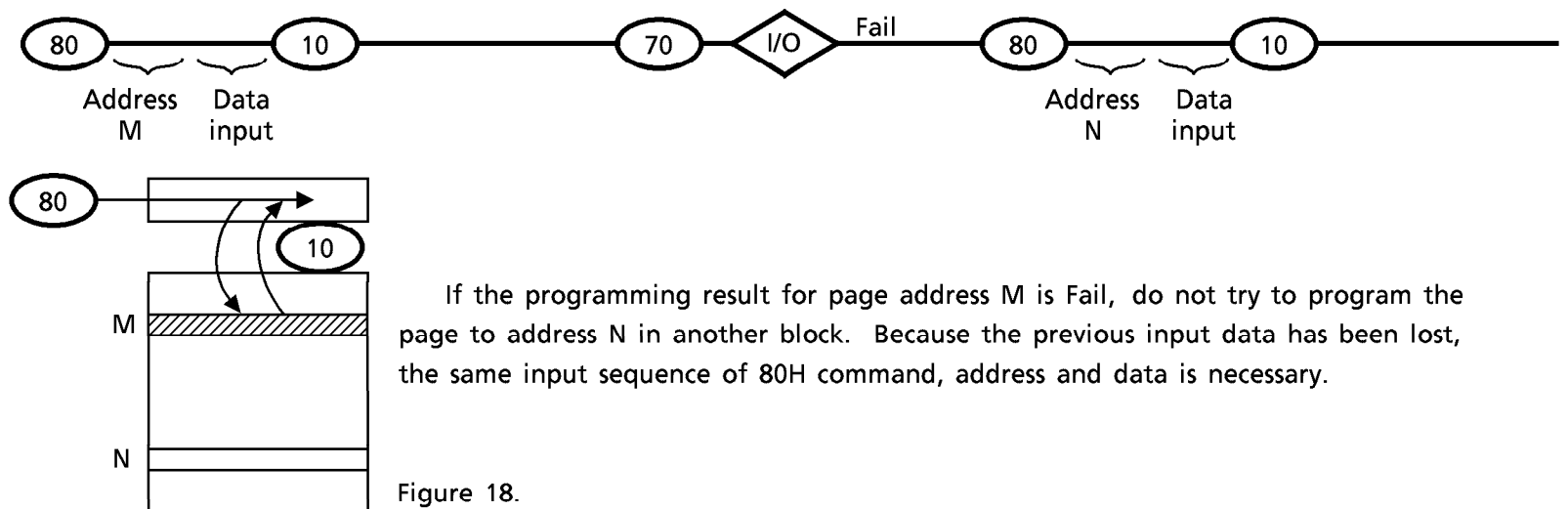
Figure 17.

The device status can be read out by inputting the Status Read command "70H" in Read mode. Once the device has been set to Status Read mode by a "70H" command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command "00H" is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

(6) Auto programming failure



If the programming result for page address M is Fail, do not try to program the page to address N in another block. Because the previous input data has been lost, the same input sequence of 80H command, address and data is necessary.

Figure 18.

(7) R/\bar{B} : termination for the Ready/Busy pin (R/\bar{B})

A pull-up resistor needs to be used for termination because the R/\bar{B} buffer consists of an open drain circuit.

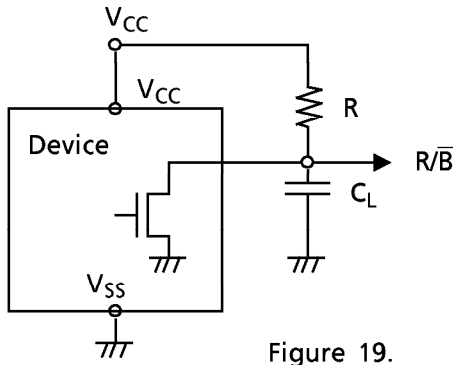
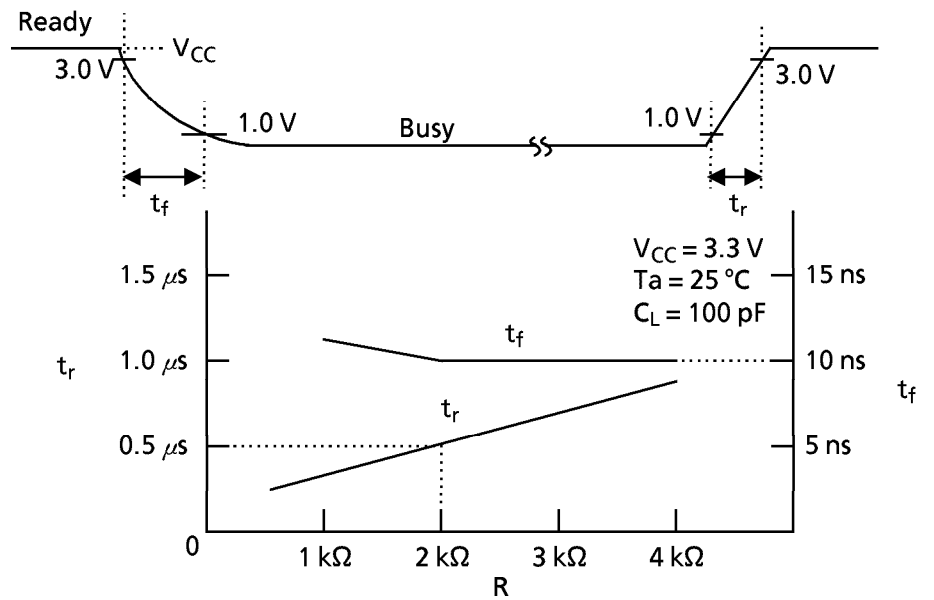


Figure 19.

This data may vary from device to device. We recommend that you use this data as a reference when selecting a resistor value.



(8) Status after power-on

The following sequence is necessary because some input signals may not be stable at power-on.

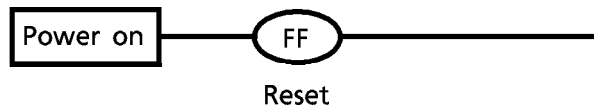


Figure 20.

(9) Power-on/off sequence:

The \bar{WP} signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary:

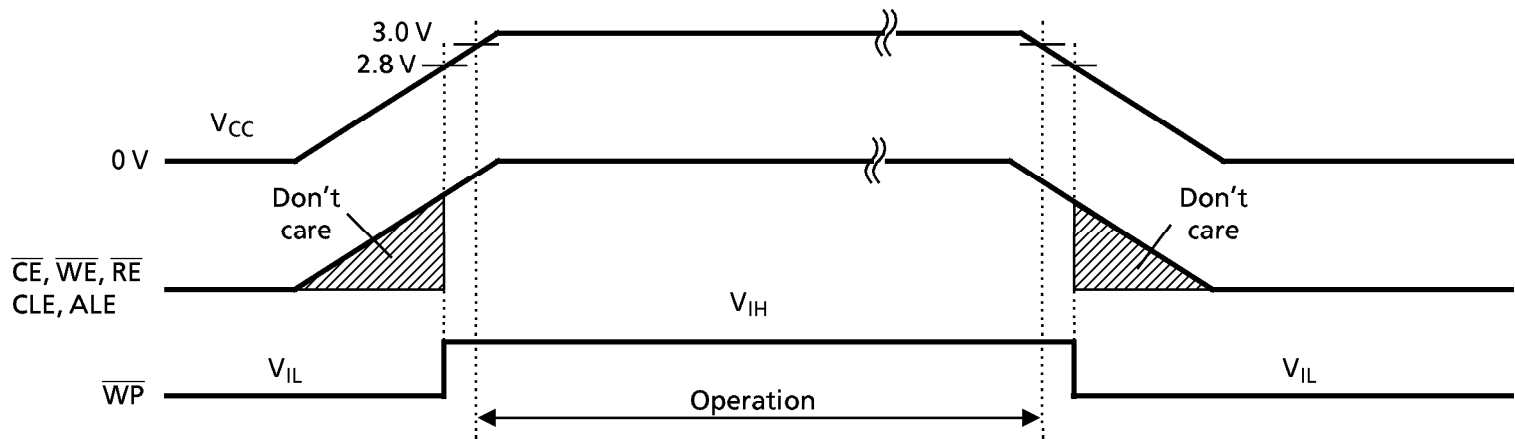
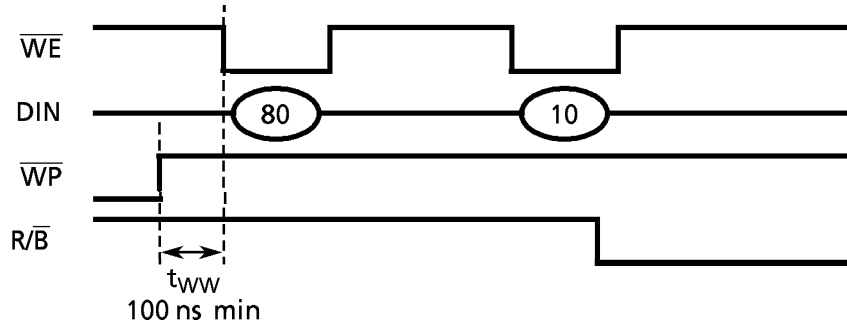
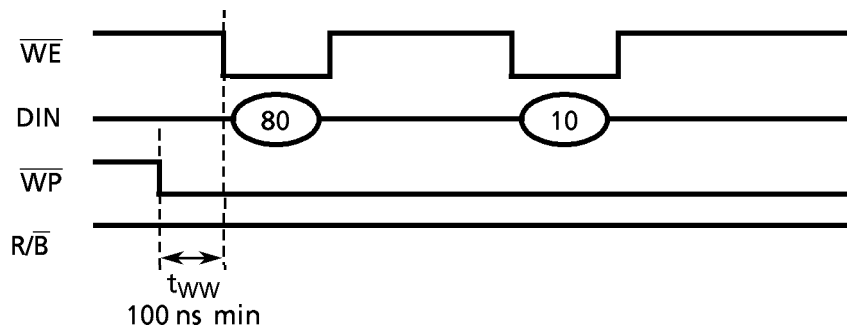
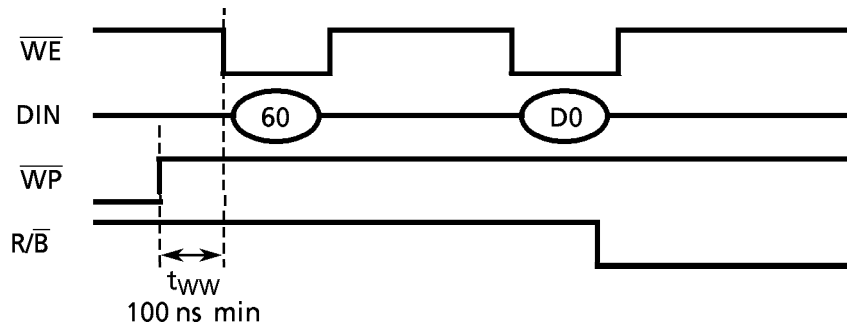
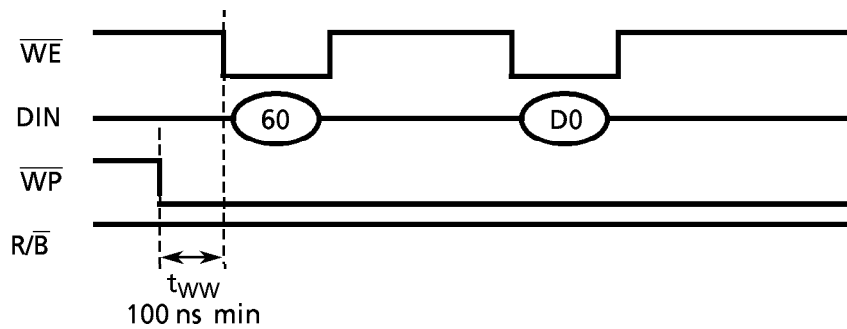


Figure 21. Power-on/off Sequence

(10) Note regarding the \overline{WP} signal

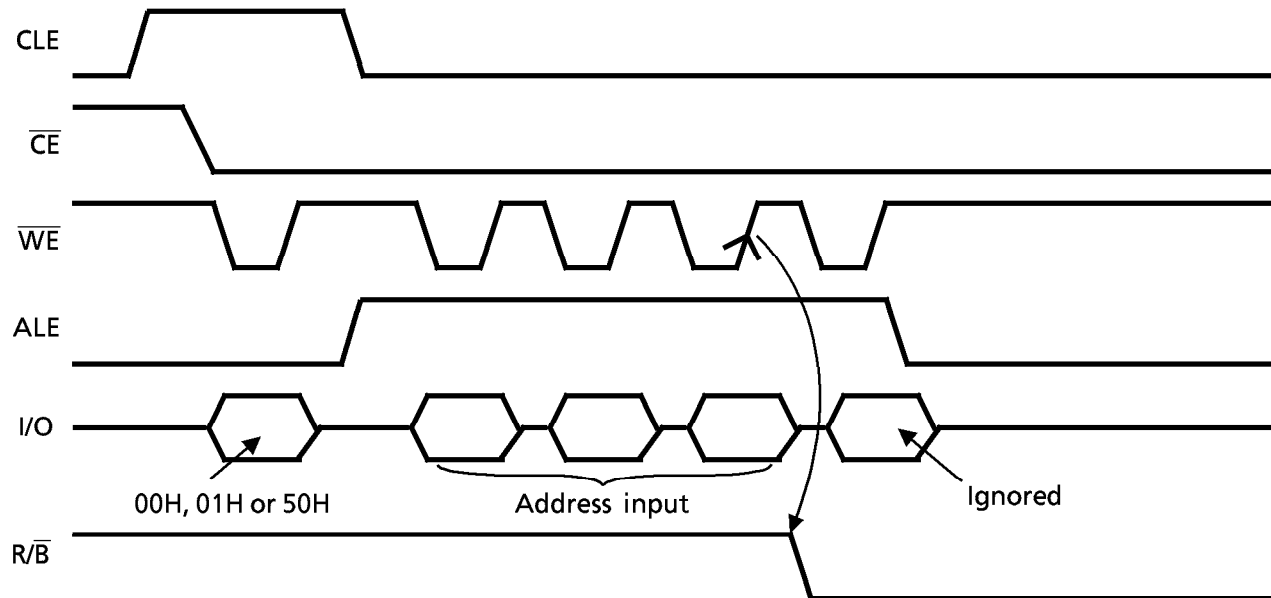
The Erase and Program operations are automatically reset when \overline{WP} goes Low. The operations are enabled and disabled as follows:

Enable ProgrammingDisable ProgrammingEnable ErasingDisable Erasing

(11) When four address cycles are input

Although the device may read in a fourth address, it is ignored inside the chip.

Read operation



Internal read operation starts when \overline{WE} goes High in the third cycle.

Figure 22.

Program operation

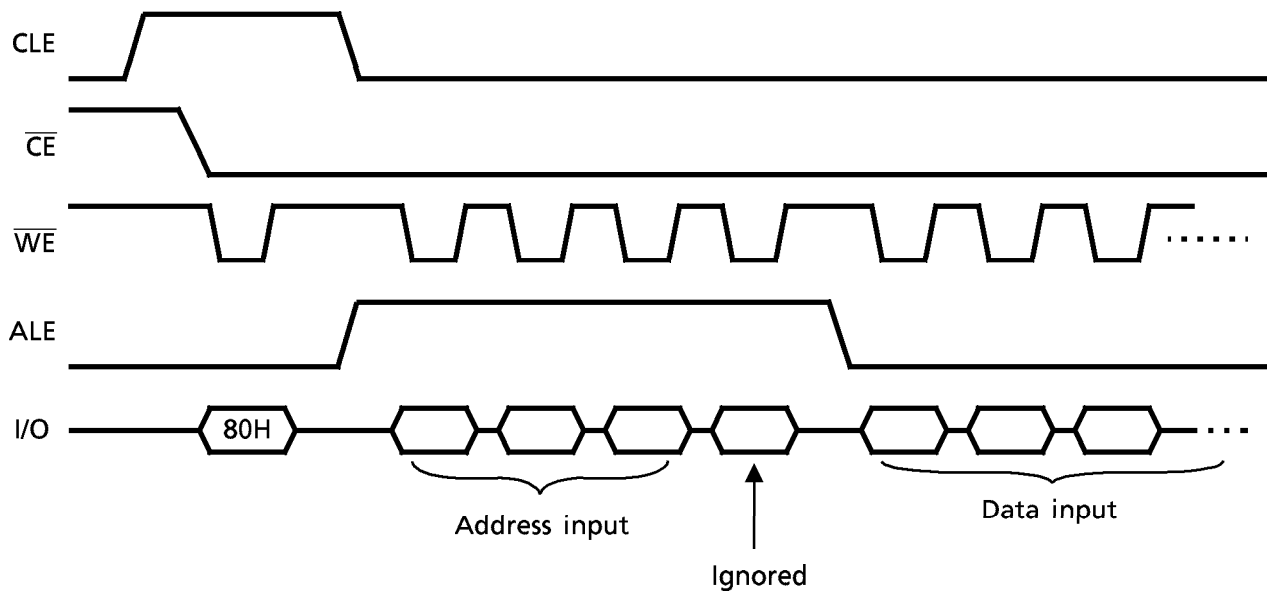


Figure 23.

(12) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 10 segments. Each segment can be programmed individually as follows:

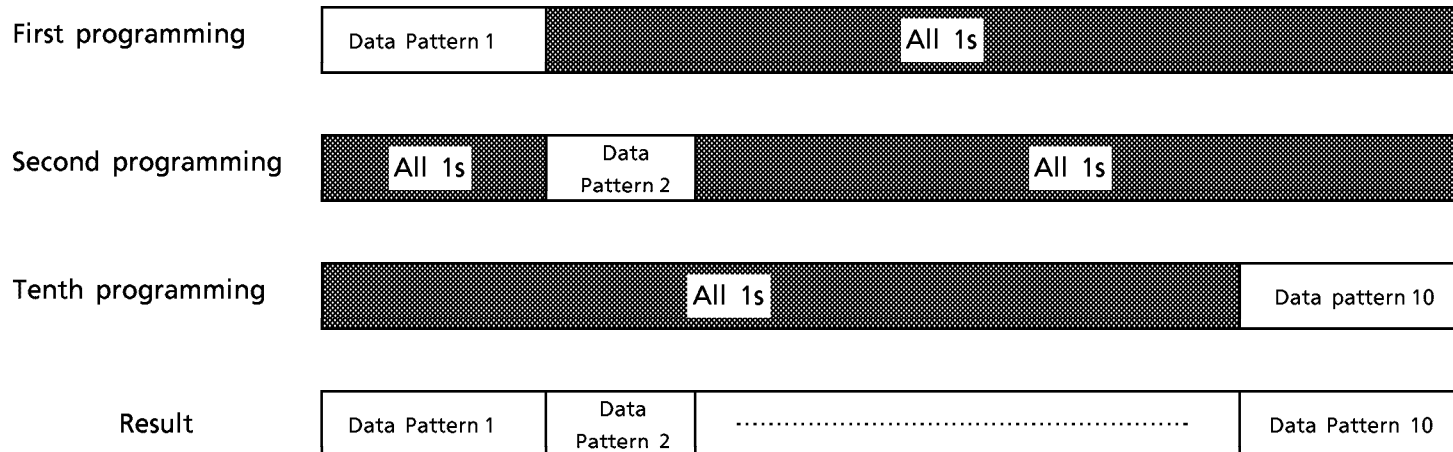


Figure 24.

Note: The input data for unprogrammed or previously programmed page segments must be "1" (i.e. the inputs for all page bytes outside the segment which is to be programmed should be set to all "1").

(13) Note regarding the \overline{RE} signal

The internal column address counter is incremented synchronously with the \overline{RE} clock in Read mode. Therefore, once the device has been set to Read mode by a "00H", "01H" or "50H" command, the internal column address counter is incremented by the \overline{RE} clock independently of the address input timing. If the \overline{RE} clock input pulses start before the address input, and the pointer reaches the last column address, an internal read operation (array \rightarrow register) will occur and the device will enter Busy state. (Refer to Figure 25.)

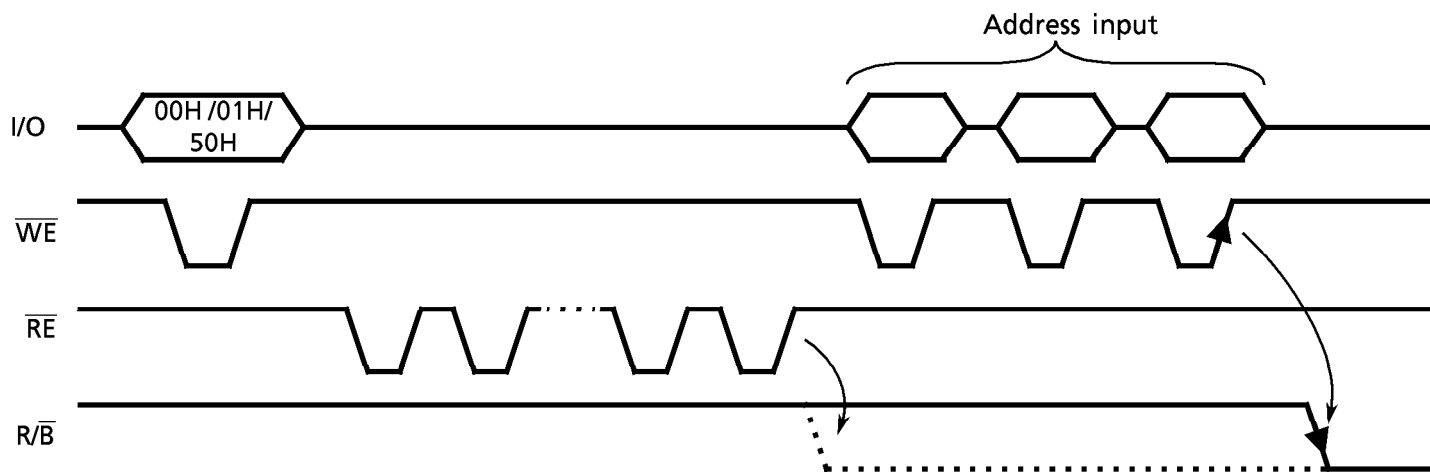


Figure 25.

Hence the \overline{RE} clock input must start after the address input.

(14) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:

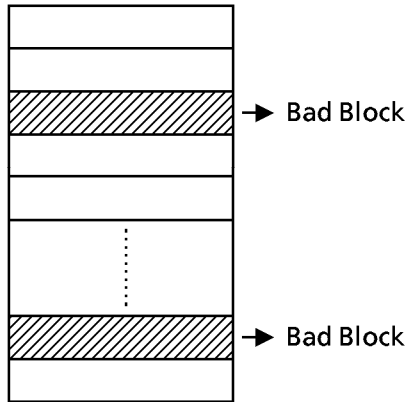


Figure 26.

Check if the device has any bad blocks after device installation into the system. Do not try to access bad blocks. A bad block does not affect the performance of good blocks because it is isolated from the Bit line by the Select gate.

The number of valid blocks is as follows:

| | MIN | TYP. | MAX | UNIT |
|---------------------|------|------|------|-------|
| Valid (Good) Blocks | 1004 | - | 1024 | Block |

Figure 28 shows the flow for bad block testing

(15) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.

The following possible failure modes should be considered when implementing a highly reliable system

| FAILURE MODE | | DETECTION AND COUNTERMEASURE SEQUENCE |
|--------------|--------------------------------|---|
| Block | Erase Failure | Status Read after Erase → Block Replacement |
| Page | Programming Failure | Status Read after Program → Block Replacement |
| Single Bit* | Programming Failure "1 → 0" | (1) Block Verify after Program → Retry |
| | | (2) ECC |

- ECC : Error Correction Code → Hamming Code etc.
Example: 1-bit correction & 2-bit detection
- Block Replacement

Program

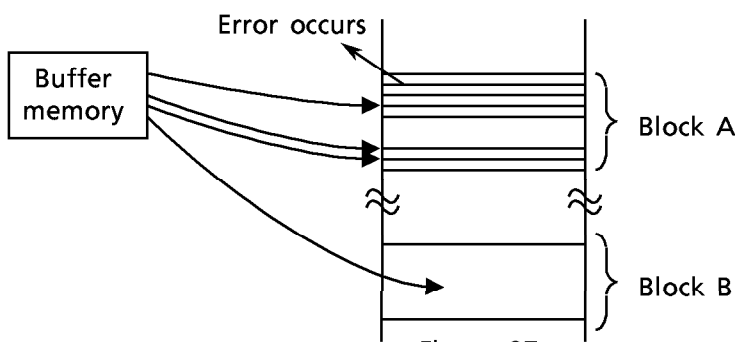


Figure 27.

When an error happens in Block A, try to reprogram the data into another (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs in an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

BAD BLOCK TEST FLOW

C : Checkerboard pattern
 C̄ : Inverted checkerboard pattern
 Blank check : 1 Block Read (FFH)

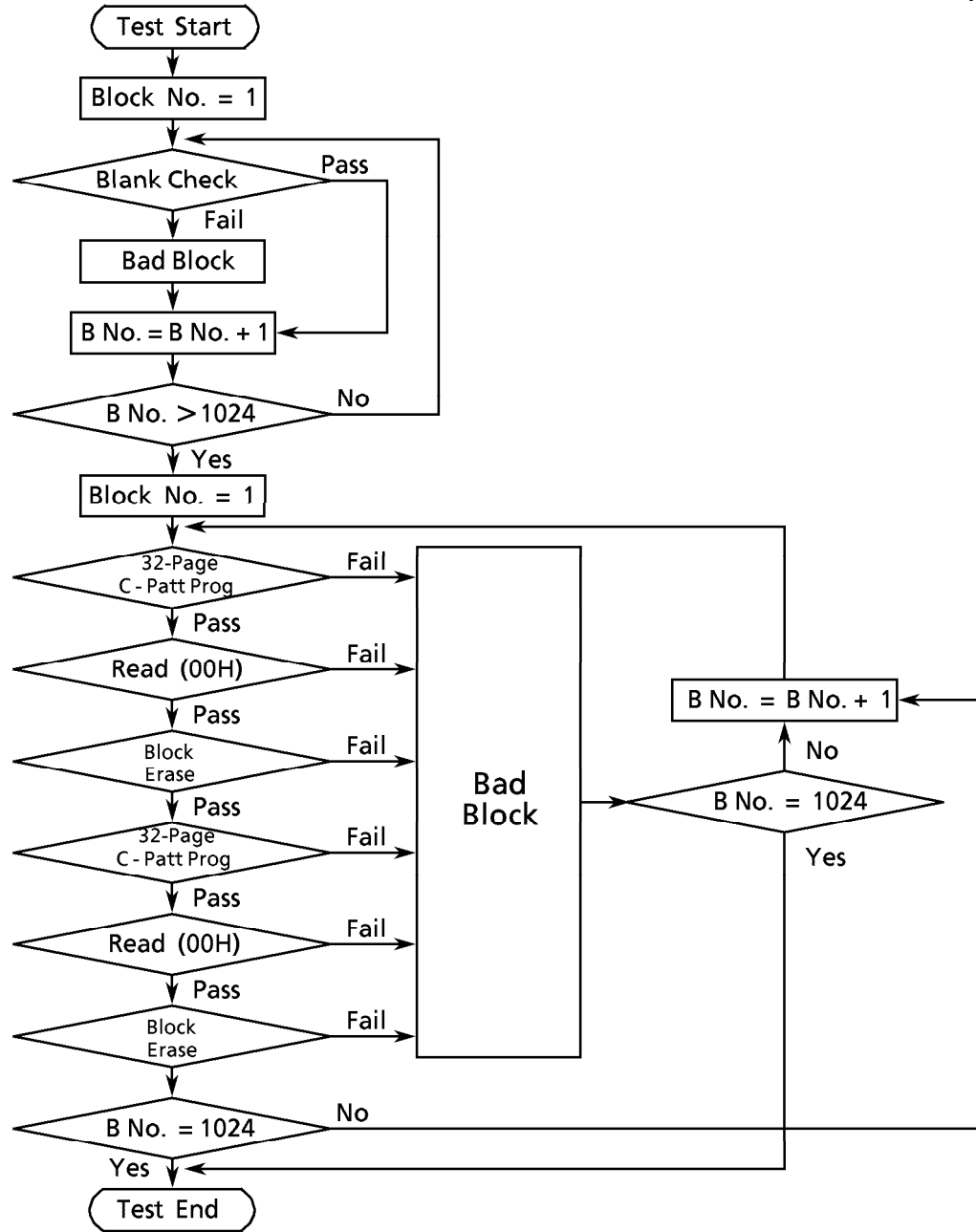


Figure 28.

PACKAGE DIMENSIONS

- Plastic TSOP

TSOP I 48-P-1220-0.50

Unit: mm

