16-Bit, 100 kSPS PulSAR Differential ADC in MSOP

AD7684

FEATURES

16-bit resolution with no missing codes
Throughput: 100 kSPS
INL: ±1 LSB typ, ±3 LSB max
True differential analog input range: ±V_{REF}
0 V to V_{REF} with V_{REF} up to VDD on both inputs
Single-supply operation: 2.7 V to 5.5 V
Serial interface SPI-®/QSPI-™/MICROWIRE-™/DSP-compatible
Power Dissipation : 4 mW @ 5 V, 1.5 mW @ 2.7 V, 150 µW @ 2.7 V/10 kSPS
Standby current: 1 nA
8-lead MSOP package

APPLICATION DIAGRAM

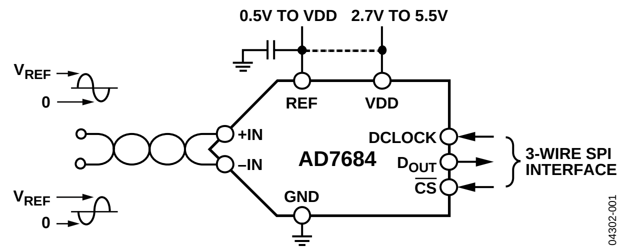

Figure 1.

APPLICATIONS

Battery-powered equipment
Data acquisition
Instrumentation
Medical instruments
Process control

Table 1. MSOP, QFN (LFCSP)/SOT-23, 16-Bit PulSAR ADCs

Type	100 kSPS	250 kSPS	500 kSPS
True Differential	AD7684	AD7687	AD7688
Pseudo Differential/Unipolar	AD7683	AD7685 AD7694	AD7686
Unipolar	AD7680		

GENERAL DESCRIPTION

The AD7684 is a 16-bit, charge redistribution, successive approximation, PulSAR™ analog-to-digital converter (ADC) that operates from a single power supply, VDD, between 2.7 V to 5.5 V. It contains a low power, high speed, 16-bit sampling ADC with no missing codes, an internal conversion clock, and a serial, SPI-compatible interface port. The part also contains a low noise, wide bandwidth, short aperture delay, track-and-hold circuit. On the $\overline{CS}$ falling edge, it samples the voltage difference between +IN and –IN pins. The reference voltage, REF, is applied externally and can be set up to the supply voltage. Its power scales linearly with throughput.

The AD7684 is housed in an 8-lead MSOP package, with an operating temperature specified from −40°C to +85°C.

Rev. 0

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REVISION HISTORY

10/04—Initial Version: Revision 0

SPECIFICATIONS

VDD = 2.7 V to 5.5 V; V_{REF} = VDD; T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	+IN – (−IN)	$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage	+IN, −IN	−0.1		VDD + 0.1	V
Analog Input CMRR	f_{IN} = 100 kHz		65		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance		See the Analog Input section.			
THROUGHPUT SPEED					
Complete Cycle				10	µS
Throughput Rate		0		100	kSPS
DCLOCK Frequency		0		2.9	MHz
REFERENCE					
Voltage Range		0.5		VDD + 0.3	V
Load Current	100 kSPS, $V_{+IN} = V_{-IN} = V_{REF}/2$ = 2.5 V		50		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		0.3 × VDD	V
V_{IH}		0.7 × VDD		VDD + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
Input Capacitance			5		pF
DIGITAL OUTPUTS					
Data Format		Serial 16 Bits Twos Complement.			
V_{OH}	I_{SOURCE} = −500 µA	VDD − 0.3			V
V_{OL}	I_{SINK} = +500 µA			0.4	V
POWER SUPPLIES					
VDD	Specified performance	2.7		5.5	V
VDD Range[1]		2.0		5.5	V
Operating Current	100 kSPS throughput				
	VDD = 5 V		800		µA
	VDD = 2.7 V		560		µA
Standby Current[2, 3]	VDD = 5 V, 25°C		1	50	nA
Power Dissipation	VDD = 5 V		4	6	mW
	VDD = 2.7 V		1.5		mW
	VDD = 2.7 V, 10 kSPS throughput		150		µW
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] See the Typical Performance Characteristics section for more information.
[2] With all digital inputs forced to VDD or GND, as required.
[3] During acquisition phase.

VDD = 5 V; V_{REF} = VDD; T_A = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error		−3	±1	+3	LSB
Transition Noise			0.5		LSB
Gain Error[1], T_{MIN} to T_{MAX}			±2	±15	LSB
Gain Error Temperature Drift			±0.3		ppm/°C
Zero Error, T_{MIN} to T_{MAX}			±0.4	±1.6	mV
Zero Temperature Drift			±0.3		ppm/°C
Power Supply Sensitivity	VDD = 5 V ±5%		±0.05		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 1 kHz	88	91		dB[2]
Spurious-Free Dynamic Range	f_{IN} = 1 kHz		−108		dB
Total Harmonic Distortion	f_{IN} = 1 kHz		−106		dB
Signal-to-(Noise + Distortion)	f_{IN} = 1 kHz	88	91		dB
Effective Number of Bits	f_{IN} = 1 kHz		14.8		Bits

[1] See the Terminology section. These specifications include full temperature range variation, but do not include the error contribution from the external reference.
[2] All specifications in dB are referred to a full-scale input, FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

VDD = 2.7 V; V_{REF} = 2.5 V; T_A = −40°C to +85°C, unless otherwise noted.

Table 4.

Parameter	Conditions	Min	Typ	Max	Unit
ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error		−3	±1	+3	LSB
Transition Noise			0.85		LSB
Gain Error[1], T_{MIN} to T_{MAX}			±2	±15	LSB
Gain Error Temperature Drift			±0.3		ppm/°C
Zero Error, T_{MIN} to T_{MAX}			±0.7	±3.5	mV
Zero Temperature Drift			±0.3		ppm/°C
Power Supply Sensitivity	VDD = 2.7 V ±5%		±0.05		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 1 kHz		86		dB[2]
Spurious-Free Dynamic Range	f_{IN} = 1 kHz		−100		dB
Total Harmonic Distortion	f_{IN} = 1 kHz		−98		dB
Signal-to-(Noise + Distortion)	f_{IN} = 1 kHz		86		dB
Effective Number of Bits	f_{IN} = 1 kHz		14		Bits

[1] See the Terminology section. These specifications do include full temperature range variation, but do not include the error contribution from the external reference.
[2] All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

TIMING SPECIFICATIONS

VDD = 2.7 V to 5.5 V; T_A = −40°C to +85°C, unless otherwise noted.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
Throughput Rate	t_{CYC}			100	kHz
$\overline{CS}$ Falling to DCLOCK Low	t_{CSD}			0	μs
$\overline{CS}$ Falling to DCLOCK Rising	t_{SUCS}	20			ns
DCLOCK Falling to Data Remains Valid	t_{HDO}	5	16		ns
$\overline{CS}$ Rising Edge to D_{OUT} High Impedance	t_{DIS}		14	100	ns
DCLOCK Falling to Data Valid	t_{EN}		16	50	ns
Acquisition Time	t_{ACQ}	400			ns
D_{OUT} Fall Time	t_F		11	25	ns
D_{OUT} Rise Time	t_R		11	25	ns

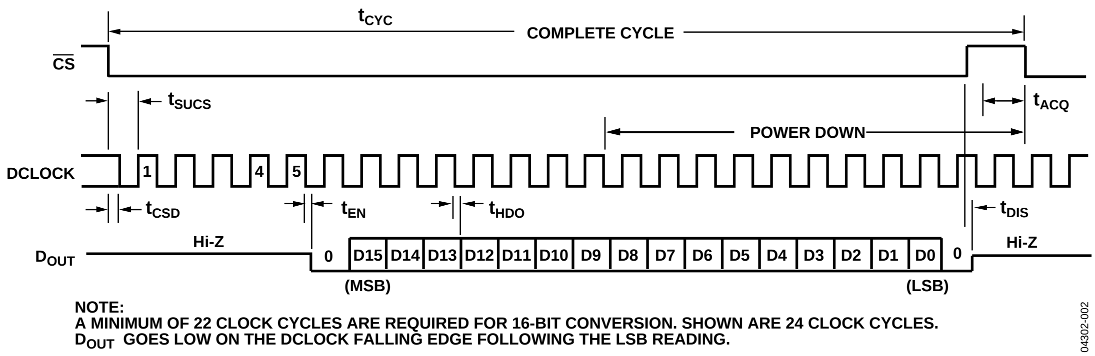

Figure 2. Serial Interface Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs	
+IN[1], –IN[1]	GND – 0.3 V to VDD + 0.3 V or ±130 mA
REF	GND – 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD to GND	−0.3 V to +6 V
Digital Inputs to GND	−0.3 V to VDD + 0.3 V
Digital Outputs to GND	−0.3 V to VDD + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	200°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Temperature Range	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] See the Analog Input section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

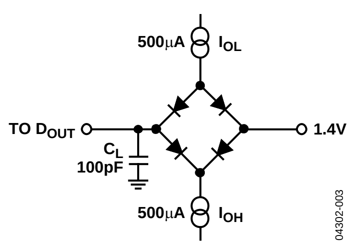

Figure 3. Load Circuit for Digital Interface Timing

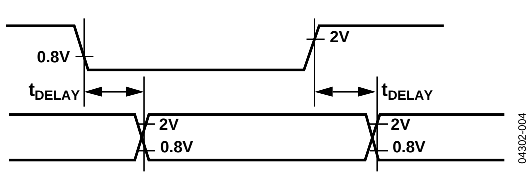

Figure 4. Voltage Reference Levels for Timing

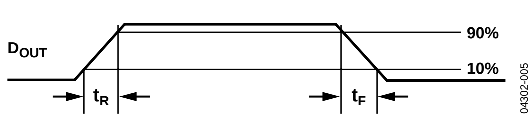

Figure 5. D_{OUT} Rise and Fall Timing

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

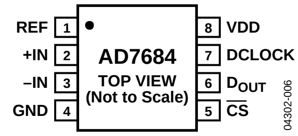

Figure 6. 8-Lead MSOP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Function
1	REF	AI	Reference Input Voltage. The REF range is from 0.5 V to VDD. It is referred to the GND pin. This pin should be decoupled closely to the pin with a ceramic capacitor of a few µF.
2	+IN	AI	Differential Positive Analog Input.
3	–IN	AI	Differential Negative Analog Input.
4	GND	P	Power Supply Ground.
5	$\overline{CS}$	DI	Chip Select Input. On its falling edge, it initiates the conversions. The part returns in shutdown mode as soon as the conversion is done. It also enables D_{OUT}. When high, D_{OUT} is high impedance.
6	D_{OUT}	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
7	DCLOCK	DI	Serial Data Clock Input.
8	VDD	P	Power Supply.

[1] AI = Analog Input; DI = Digital Input; DO = Digital Output; and P = Power.

TERMINOLOGY

Integral Nonlinearity Error (INL)

Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 21).

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error

Zero error is the difference between the ideal midscale voltage, i.e., 0 V, and the actual voltage producing the midscale output code, i.e., 0 LSB.

Gain Error

The first transition (from 100 . . . 00 to 100 . . . 01) should occur at a level ½ LSB above the nominal negative full scale (−4.999924 V for the ±5 V range). The last transition (from 011…10 to 011…11) should occur for an analog voltage 1½ LSB below the nominal full scale (4.999771 V for the ±5 V range.) The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the idea levels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula

$$ENOB = \left(S/[N+D]_{dB} - 1.76\right)/6.02$$

and is expressed in bits.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

Signal-to-(Noise + Distortion) Ratio (S/[N+D])

S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in dB.

Aperture Delay

Aperture delay is a measure of the acquisition performance and is the time between the falling edge of the $\overline{CS}$ input and when the input signal is held for a conversion.

Transient Response

Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function was applied.

TYPICAL PERFORMANCE CHARACTERISTICS

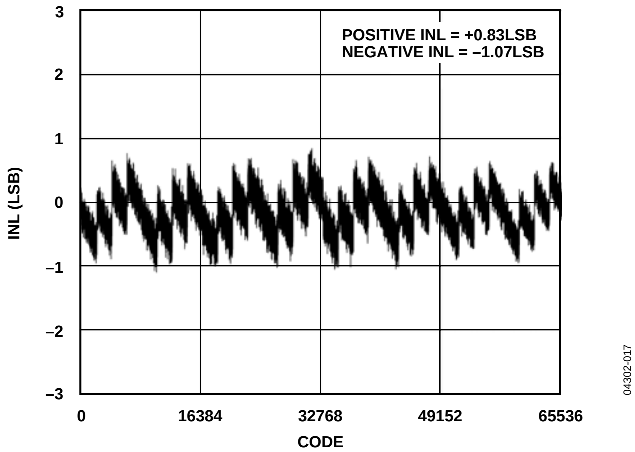

Figure 7. Integral Nonlinearity vs. Code

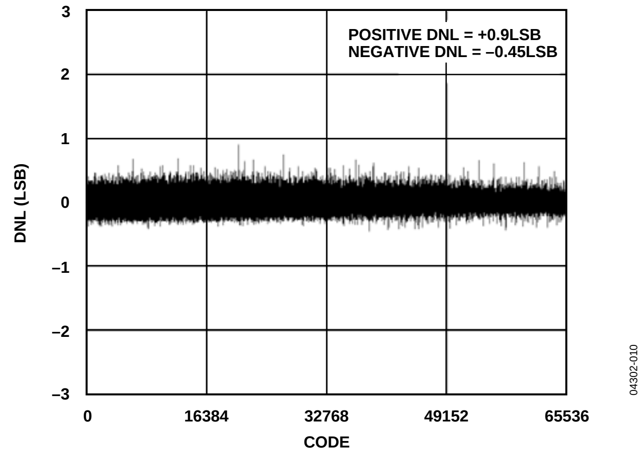

Figure 10. Differential Nonlinearity vs. Code

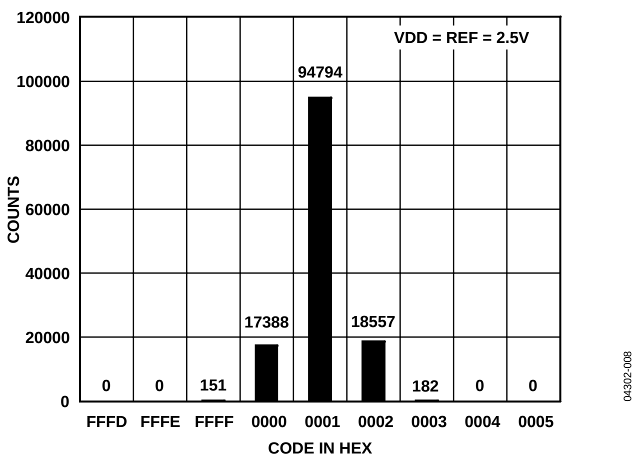

Figure 8. Histogram of a DC Input at the Code Center

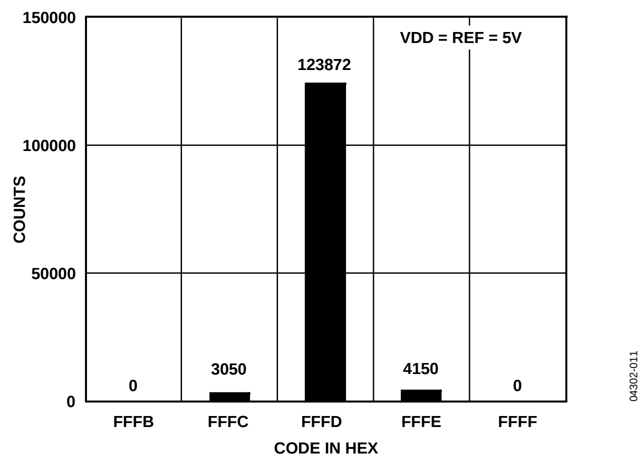

Figure 11. Histogram of a DC Input at the Code Center

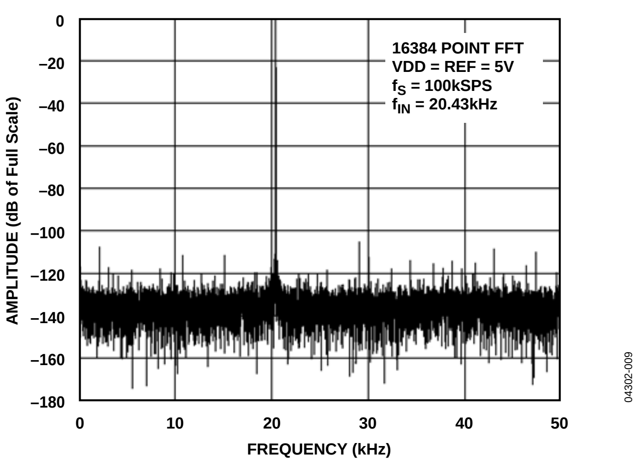

Figure 9. FFT Plot

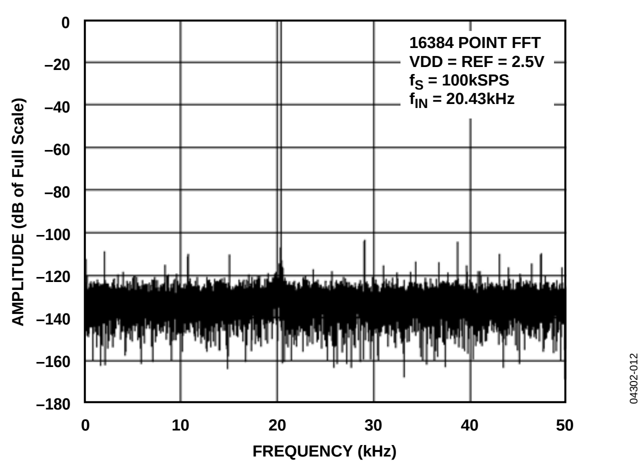

Figure 12. FFT Plot

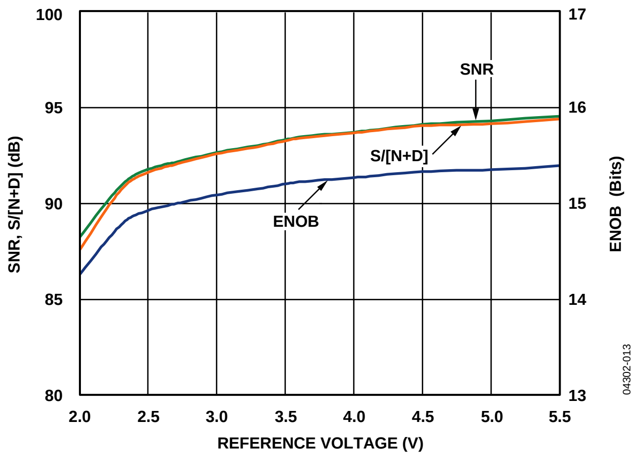

Figure 13. SNR, S/(N + D), and ENOB vs. Reference Voltage

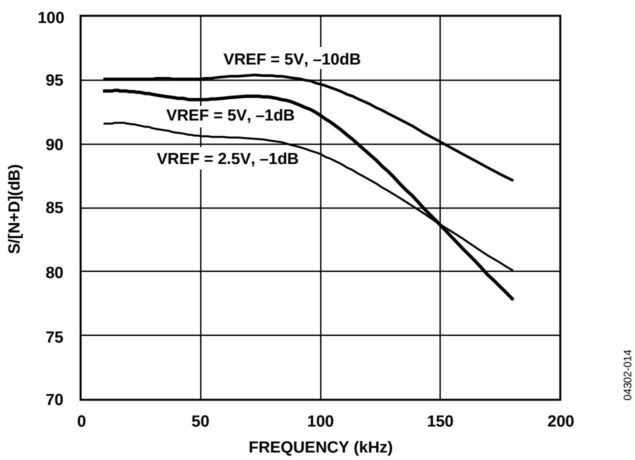

Figure 14. S/[N + D] vs. Frequency

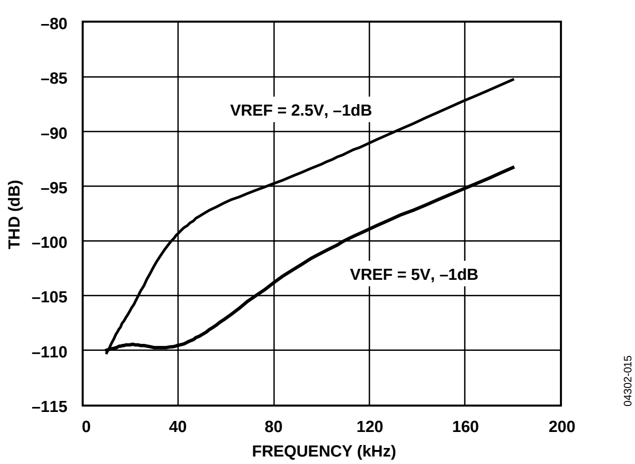

Figure 15. THD, ENOB vs. Frequency

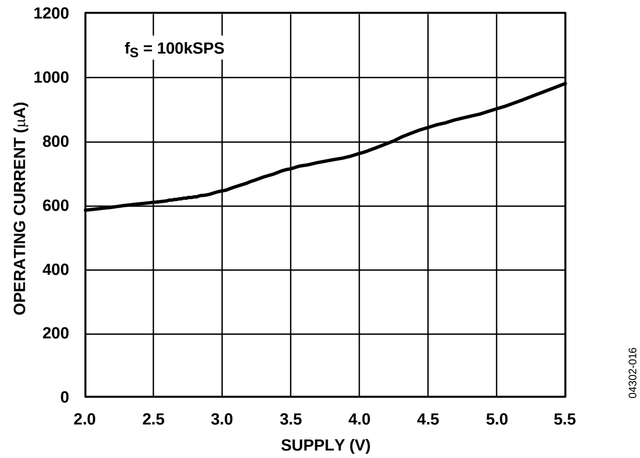

Figure 16. Operating Current vs. Supply

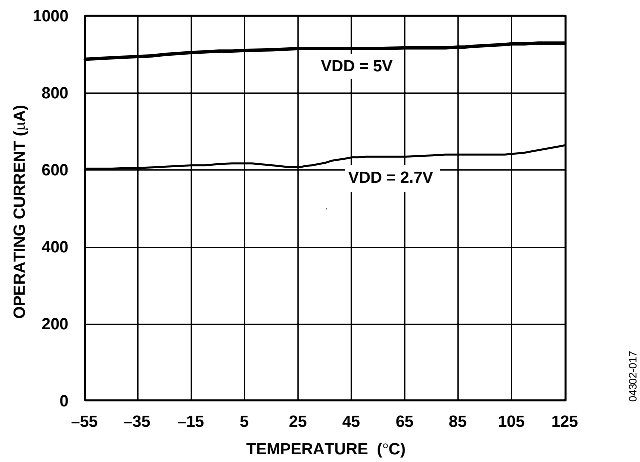

Figure 17. Operating Current vs. Temperature

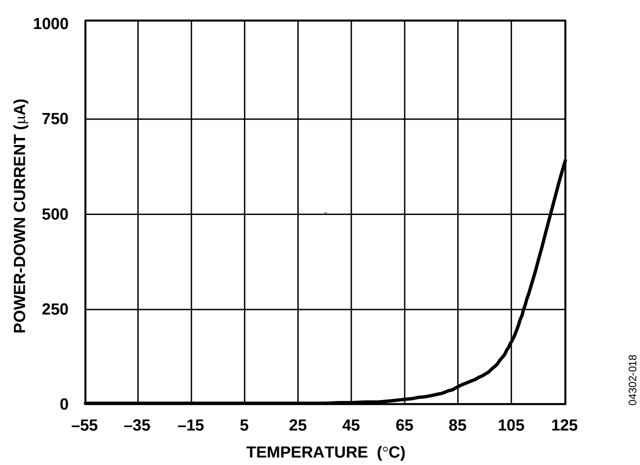

Figure 18. Power-Down Current vs. Temperature

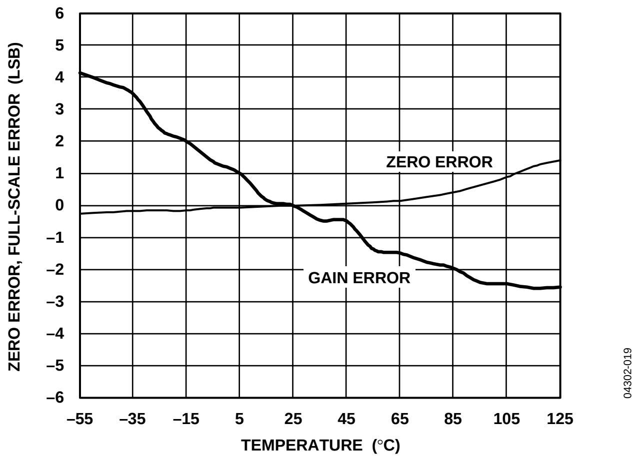

Figure 19. Offset and Gain Error vs. Temperature

APPLICATION INFORMATION

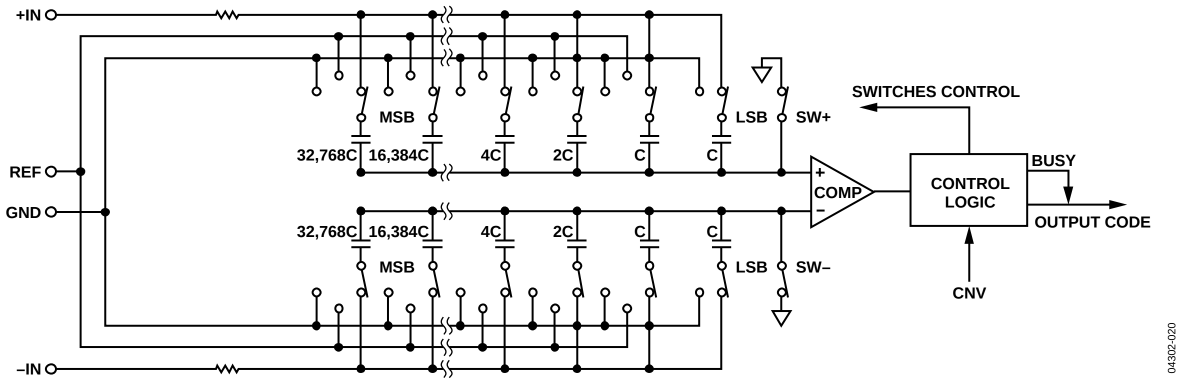

Figure 20. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7684 is a low power, single-supply, 16-bit ADC using a successive approximation architecture. It is capable of converting 100,000 samples per second (100 kSPS) and powers down between conversions. When operating at 10 kSPS, for example, it consumes typically 150 µW with a 2.7 V supply, ideal for battery-powered applications.

The AD7684 provides the user with an on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple, multiplexed channel applications.

The AD7684 is specified from 2.7 V to 5.5 V. It is housed in a 8-lead MSOP package.

CONVERTER OPERATION

The AD7684 is a successive approximation ADC based on a charge redistribution DAC. Figure 20 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary-weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the +IN and −IN inputs. When the acquisition phase is complete and the $\overline{CS}$ input goes low, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs, +IN and −IN, captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary-weighted voltage steps ($V_{REF}/2$, $V_{REF}/4 \ldots V_{REF}/65536$). The control logic toggles these switches, starting with the MSB, in order to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase and the control logic generates the ADC output code.

TRANSFER FUNCTIONS

The ideal transfer function for the AD7684 is shown in Figure 21 and Table 8.

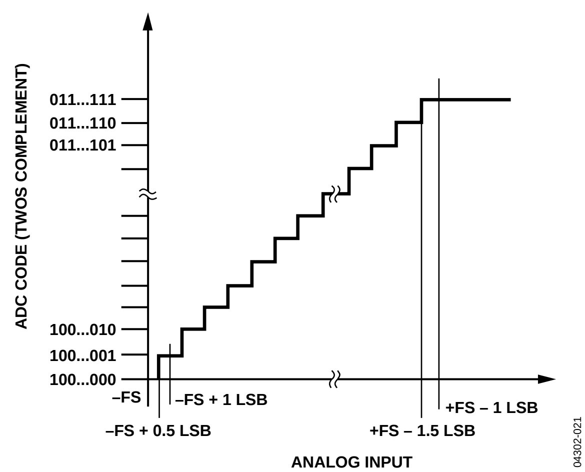

Figure 21. ADC Ideal Transfer Function

Table 8. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output Code Hexa
FSR – 1 LSB	4.999847 V	7FFF[1]
Midscale + 1 LSB	152.6 µV	0001
Midscale	0 V	0000
Midscale – 1 LSB	−152.6 µV	FFFF
–FSR + 1 LSB	−4.999847 V	8001
–FSR	−5 V	8000[2]

[1] This is also the code for an overranged analog input ($V_{+IN} – V_{–IN}$ above $V_{REF} – V_{GND}$).
[2] This is also the code for an underranged analog input ($V_{+IN} – V_{–IN}$ below $–V_{REF} + V_{GND}$).

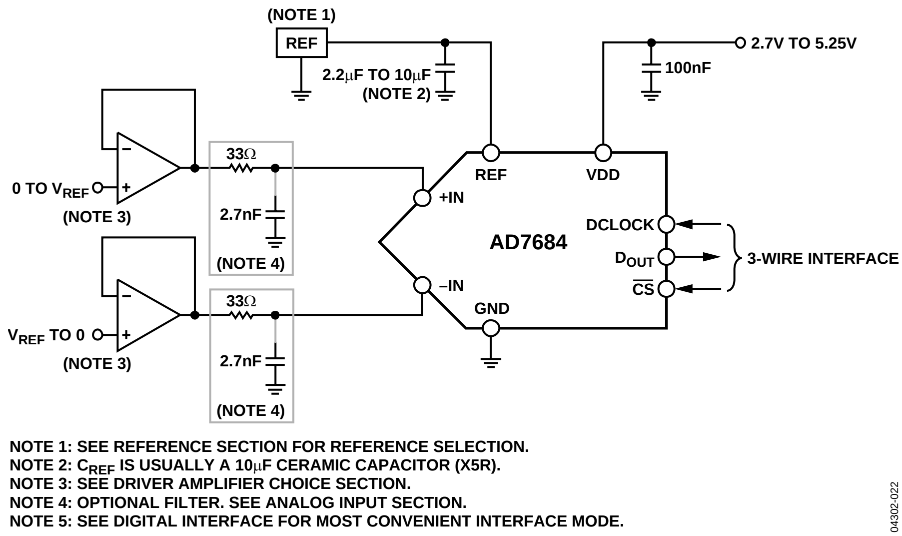

Figure 22. Typical Application Diagram

TYPICAL CONNECTION DIAGRAM

Figure 22 shows an example of the recommended application diagram for the AD7684.

ANALOG INPUT

Figure 23 shows an equivalent circuit of the input structure of the AD7684. The two diodes, D1 and D2, provide ESD protection for the analog inputs, +IN and −IN. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V, because this will cause these diodes to become forward-biased and start conducting current. However, these diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from VDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

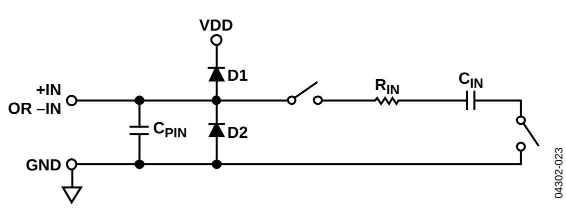

Figure 23. Equivalent Analog Input Circuit

This analog input structure allows the sampling of the differential signal between +IN and −IN. By using this differential input, small signals common to both inputs are rejected. For instance, by using −IN to sense a remote signal ground, ground potential differences between the sensor and the local ADC ground are eliminated. During the acquisition phase, the impedance of the analog input +IN can be modeled as a parallel combination of the capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 600 Ω and is a lumped component made up of some serial resistors and the on-resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, when the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the AD7684 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance.

DRIVER AMPLIFIER CHOICE

Although the AD7684 is easy to drive, the driver amplifier needs to meet the following requirements:

- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7684. Note that the AD7684 has a noise much lower than most other 16-bit ADCs and, therefore, can be driven by a noisier op amp while preserving the same or better system performance. The noise coming from the driver is filtered by the AD7684 analog input circuit 1-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used.
- For ac applications, the driver needs to have a THD performance suitable to that of the AD7684. Figure 15 shows the THD vs. frequency that the driver should exceed.
- For multichannel multiplexed applications, the driver amplifier and the AD7684 analog input circuit must be able to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection.

Table 9. Recommended Driver Amplifiers

Amplifier	Typical Application
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
OP184	Low power, low noise, and low frequency
AD8605, AD8615	5 V single-supply, low power
AD8519	Small, low power, and low frequency
AD8031	High frequency and low power

VOLTAGE REFERENCE INPUT

The AD7684 voltage reference input, REF, has a dynamic input impedance. It should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source (e.g., an unbuffered reference voltage like the low temperature drift ADR43x reference or a reference buffer using the AD8031 or the AD8605), a 10 μF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If desired, smaller reference decoupling capacitor values down to 2.2 μF can be used with a minimal impact on performance, especially DNL.

POWER SUPPLY

The AD7684 powers down automatically at the end of each conversion phase and therefore the power scales linearly with the sampling rate, as shown in Figure 24. This makes the part ideal for low sampling rates (even of a few Hz) and low battery-powered applications.

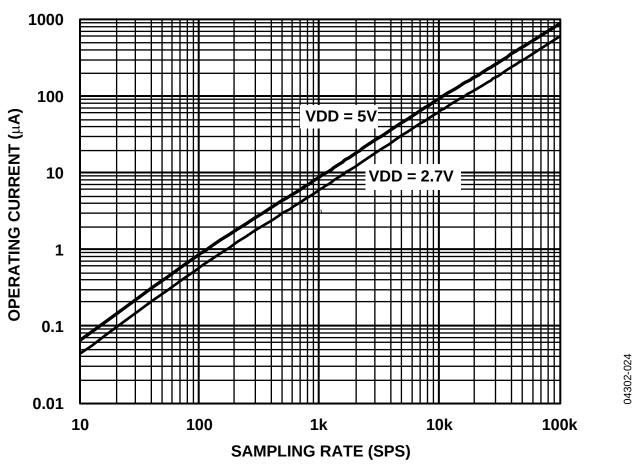

Figure 24. Operating Current vs. Sampling Rate

DIGITAL INTERFACE

The AD7684 is compatible with SPI, QSPI, digital hosts, and DSPs (e.g., Blackfin® ADSP-BF53x or ADSP-219x). The connection diagram is shown in Figure 25 and the corresponding timing is given in Figure 2.

A falling edge on $\overline{CS}$ initiates a conversion and the data transfer. After the fifth DCLOCK falling edge, D_{OUT} is enabled and forced low. The data bits are then clocked MSB first by subsequent DCLOCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host also using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time.

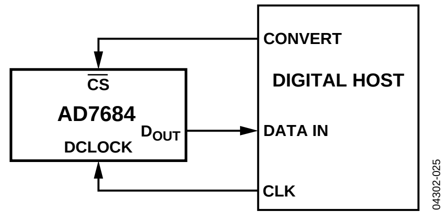

Figure 25. Connection Diagram

LAYOUT

The printed circuit board housing the AD7684 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7684 with all its analog signals on the left side and all its digital signals on the right side eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7684 is used as a shield. Fast switching signals, such as $\overline{CS}$ or clocks, should never run near analog signal paths. Crossover of digital and analog signals should be avoided.

At least one ground plane should be used. It could be common or split between the digital and analog section. In such a case, it should be joined underneath the AD7684.

The AD7684 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, and ideally right up against, the REF and GND pins and by connecting these pins with wide, low impedance traces.

Finally, the power supply, VDD, of the AD7684 should be decoupled with a ceramic capacitor, typically 100 nF, and placed close to the AD7684. It should be connected using short and large traces to provide low impedance paths and reduce the effect of glitches on the power supply lines.

EVALUATING THE AD7684'S PERFORMANCE

Other recommended layouts for the AD7684 are outlined in the evaluation board for the AD7684 (EVAL-AD7684). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-CONTROL BRD2.

OUTLINE DIMENSIONS

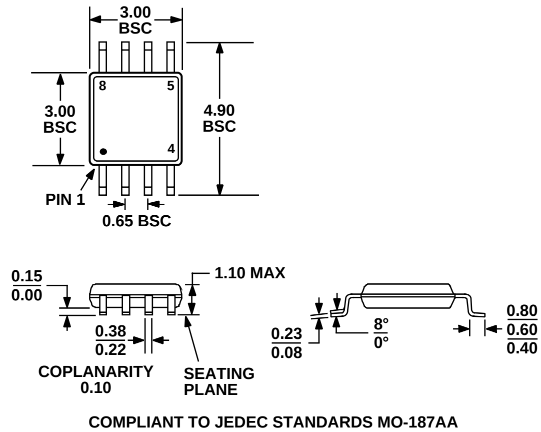

Figure 26. 8-Lead Micro Small Outline Package [MSOP]
(RM-8)
Dimensions Shown in Millimeters

ORDERING GUIDE

Models	Integral Nonlinearity	Temperature Range	Package (Option)	Transport Media, Quantity	Branding
AD7684BRM	±3 LSB max	−40°C to +85°C	MSOP (RM-8)	Tube, 50	C1D
AD7684BRMRL7	±3 LSB max	−40°C to +85°C	MSOP (RM-8)	Reel, 1,000	C1D
EVAL-AD7684CB[1]			Evaluation Board		
EVAL-CONTROL BRD2[2]			Controller Board		
EVAL-CONTROL BRD3[2]			Controller Board		

[1] This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRDx for evaluation/demonstration purposes.
[2] These boards allow a PC to control and communicate with all Analog Devices' evaluation boards ending in the CB designators.

NOTES