18-Bit, 2 MSPS SAR ADC

Preliminary Technical Data

AD7641

FEATURES

18-bit resolution with no missing codes
2.5V internal low drift refernce
Throughput:
2 MSPS (Warp mode)
1.5 MSPS (Normal mode)
INL: ±2 LSB typical
S/(N+D): 93 dB typical @ 100 kHz (V_{REF} = 2.5 V)
THD: −100 dB typical @ 100 kHz
Differential input range: ±V_{REF} (V_{REF} up to 2.5 V)
No pipeline delay (SAR architecture)
Parallel (18-, 16-, or 8-bit bus)
Serial 5 V/3.3 V/2.5 V interface
SPI®/QSPI™/MICROWIRE™/DSP compatible
On-board low drift reference with buffer and temperature sensor
Single 2.5 V supply operation
Power dissipation: 100 mW typical @ 2 MSPS
Power-down mode
48-LQFP and LFCSP packages
Speed upgrade of the AD7674
Pin-to-pin compatible with the AD7621

APPLICATIONS

Medical instruments
High dynamic data acquisition
Instrumentation
Spectrum analysis
ATE

GENERAL DESCRIPTION

The AD7641 is a 18-bit, 2 MSPS, charge redistribution SAR, fully differential analog-to-digital converter that operates from a single 2.5 V power supply. The part contains a high-speed 18-bit sampling ADC, an internal conversion clock, an internal reference buffer, error correction circuits, and both serial and parallel system interface ports. It features a very high sampling rate mode (Warp) and a fast mode (Normal) for asynchronous conversion rate applications. The AD7641 is hardware factory calibrated and comprehensively tested to ensure ac parameters such as signal-to-noise ratio (SNR) and total harmonic distortion (THD) in addition to the more traditional dc parameters of gain, offset and linearity. Operation is specified from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

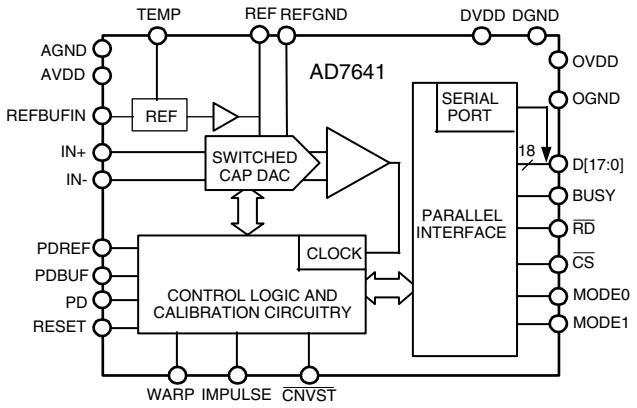

Figure 1.

Table 1. PulSAR Selection

	kSPS			
Type	**100 to 250**	**500 to 570**	**800 to 1000**	**>1000**
Pseudo Differential	AD7651 AD7660/61	AD7650/52 AD7664/66	AD7653 AD7667	
True Bipolar	AD7663	AD7665	AD7671	
True Differential	AD7675	AD7676	AD7677	AD7621
18 Bit	AD7678	AD7679	AD7674	AD7641
Multichannel/ Simultaneous		AD7654	AD7655	

PRODUCT HIGHLIGHTS

1. High resolution and Fast Throughput.
   The AD7641 is a 2 MSPS, charge redistribution, 18-bit SAR ADC (no latency).
2. Superior INL.
   The AD7641 has a maximum integral nonlinearity of 2 LSB with no missing 18-bit codes.
3. Single-Supply Operation.
   Operates from a single 2.5 V supply. Also features a power-down mode.
4. Serial or Parallel Interface.
   Versatile parallel (18-, 16-, or 8-bit bus) or 2-wire serial interface arrangement compatible with either 2.5 V, 3.3 V, or 5 V logic.

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SPECIFICATIONS

Table 2. −40°C to +85°C, V_{REF} = AVDD, AVDD = DVDD = OVDD = 2.5 V, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		18			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN} to AGND	-0.1		AVDD	V
Analog Input CMRR	f_{IN} = 100 kHz		60		dB
Input Current	2 MSPS Throughput		TBD		µA
Input Impedance[1]			See Analog Inputs Section		
THROUGHPUT SPEED					
Complete Cycle	In Warp Mode			500	ns
Throughput Rate	In Warp Mode	0.001		2	MSPS
Time Between Conversions	In Warp Mode			1	ms
Complete Cycle	In Normal Mode			667	ns
Throughput Rate	In Normal Mode	0		1.5	MSPS
DC ACCURACY					
Integral Linearity Error		−3	± 2	+3	LSB[2]
Differential Linearity Error		−1			LSB
No Missing Codes		18			Bits
Transition Noise	V_{REF}= AVDD		56		µV
Gain Error, T_{MIN} to T_{MAX} [3]				±TBD	% of FSR
Gain Error Temperature Drift			±0.5		ppm/°C
Zero Error, T_{MIN} to T_{MAX} [3]			±TBD	±TBD	LSB
Zero Error Temperature Drift			±1.6		ppm/°C
Power Supply Sensitivity	AVDD = 2.5V ± 5%		±5		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 100 kHz,				
	V_{REF}=AVDD		93		dB[4]
	V_{REF}=2.048V		91.3		dB
Spurious Free Dynamic Range	f_{IN}= 100 kHz		100		dB
Total Harmonic Distortion	f_{IN}= 100 kHz		−100		dB
Signal-to-(Noise+Distortion)	f_{IN}= 100 kHz,		93		dB
	f_{IN}= 100 kHz, -60 dB Input		33		dB
-3 dB Input Bandwidth			50		MHz
SAMPLING DYNAMICS					
Aperture Delay			1		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			160	ns
Overvoltage recovery				160	ns
REFERENCE					
External Reference Voltage Range	REF	TBD	2.048	AVDD	V
REF Current Drain	2 MSPS Throughput		TBD		µA
REF Voltage with reference buffer	REFBUFIN=1.2V	2	2.048	2.1	V
Reference Buffer Input Voltage	REFBUFIN	TBD	1.2	TBD	V
REFBUFIN Input Current		−1		+ 1	µA
INTERNAL REFERENCE					
Internal Reference Voltage	@ 25°C	1.197	1.2	1.203	V
Internal Reference Temp Drift	– 40°C to +85°C		3		ppm/°C
REFBUFIN Line Regulation	AVDD = 2.5V ± 5%		±15		ppm/V
REFBUFIN Output Resistance					kΩ
Turn-on Settling Time			5		ms
Long-term Stability	1,000 Hours		100		ppm/1000hours

Parameter	Conditions	Min	Typ	Max	Unit
Hysterisis			50		ppm
Temperature Pin Voltage Output	@ 25°C		300		mV
Temperature Sensitivity			1		mV/°C
TEMP pin Output Resistance			4		kΩ
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.6	V
V_{IH}		+1.7		5.25	V
I_{IL}		–1		+1	µA
I_{IH}		–1		+1	µA
DIGITAL OUTPUTS					
Data Format[5]					
Pipeline Delay[6]					
V_{OL}	I_{SINK}= 500 µA			0.4	V
V_{OH}	I_{SOURCE}= -500 µA	OVDD – 0.3			V
POWER SUPPLIES					
Specified Performance					
AVDD		2.37	2.5	2.63	V
DVDD		2.37	2.5	2.63	V
OVDD		2.3		3.6	V
Operating Current[7]	2 MSPS Throughput				
AVDD			15		mA
DVDD[8]			4.5		mA
OVDD			130		µA
Power Dissipation[7]	PDBUF = HIGH @ 2 MSPS		100		mW
	PDBUF = LOW @ 2 MSPS		108		mW
In Power-down mode	PD = HIGH		TBD		µW
TEMPERATURE RANGE[9]					
Specified Performance	T_{MIN} to T_{MAX}	-40		+85	°C

[1]See analog Input section
[2] LSB means Least Significant Bit. With the ±2.5 V input range, one LSB is 19.07 µV.
[3] See Definition of Specifications section. These specifications do not include the error contribution from the external reference.
[4] All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale unless otherwise specified.
[5] Parallel or serial 18 bit..
[6] Conversion results are available immediately after completed conversion.
[7] In Warp mode.
[8] Tested in parallel reading mode.
[9] Contact factory for extended temperature range.

TIMING SPECIFICATIONS

Table 3. –40°C to +85°C, AVDD = DVDD = 2.5 V, OVDD = 2.3 V to 3.6 V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
Refer to Figure 13 and Figure 14					
Convert Pulse Width	t_1	5			ns
Time Between Conversions (Warp Mode/Normal Mode)[1]	t_2	500/667		Note 1	ns
$\overline{CNVST}$ LOW to BUSY HIGH Delay	t_3			30	ns
BUSY HIGH All Modes Except in Master Serial Read After Convert (Warp Mode/Normal Mode)	t_4			340/465	ns
Aperture Delay	t_5		1		ns
End of Conversion to BUSY LOW Delay	t_6	10			ns
Conversion Time (Warp Mode/Normal Mode)	t_7			340/465	ns
Acquisition Time (Warp Mode/Normal Mode)	t_8	70/100			ns
RESET Pulsewidth	t_9	10			ns
Refer to Figure 15, Figure 16, and Figure 17 (Parallel Interface Modes)					
$\overline{CNVST}$ LOW to Data Valid Delay (Warp Mode/Normal Mode)	t_{10}			340/465	ns
Data Valid to BUSY LOW Delay	t_{11}	20			ns
Bus Access Request to Data Valid	t_{12}			40	ns
Bus Relinquish Time	t_{13}	2		15	ns
Refer to Figure 19 and Figure 20 (Master Serial Interface Modes) [2]					
$\overline{CS}$ LOW to SYNC Valid Delay	t_{14}			TBD	ns
$\overline{CS}$ LOW to Internal SCLK Valid Delay	t_{15}			TBD	ns
$\overline{CS}$ LOW to SDOUT Delay	t_{16}			TBD	ns
$\overline{CNVST}$ LOW to SYNC Delay (Warp Mode/Normal Mode)	t_{17}		TBD		
SYNC Asserted to SCLK First Edge Delay [3]	t_{18}	TBD			ns
Internal SCLK Period [3]	t_{19}	TBD		TBD	ns
Internal SCLK HIGH [3]	t_{20}	TBD			ns
Internal SCLK LOW [3]	t_{21}	TBD			ns
SDOUT Valid Setup Time	t_{22}	TBD			ns
SDOUT Valid Hold Time	t_{23}	TBD			ns
SCLK Last Edge to SYNC Delay [3]	t_{24}	TBD			ns
$\overline{CS}$ HIGH to SYNC HI-Z	t_{25}			TBD	ns
$\overline{CS}$ HIGH to Internal SCLK HI-Z	t_{26}			TBD	ns
$\overline{CS}$ HIGH to SDOUT HI-Z	t_{27}			TBD	ns
BUSY HIGH in Master Serial Read after Convert[3]	t_{28}		TBD		ns
$\overline{CNVST}$ LOW to SYNC Asserted Delay (Warp Mode/Normal Mode)	t_{29}		TBD		ns
SYNC Deasserted to BUSY LOW Delay	t_{30}		TBD		ns
Refer to Figure 21 and Figure 22 (Slave Serial Interface Modes)					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	2		7	ns
SDIN Setup Time	t_{33}	TBD			ns
SDIN Hold Time	t_{34}	TBD			ns
External SCLK Period	t_{35}	12.5			ns
External SCLK HIGH	t_{36}	5			ns
External SCLK LOW	t_{37}	5			ns

[1] In warp mode only, the maximum time between conversions is 1ms; otherwise, there is no required maximum time.
[2] In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.
[3] In serial master read during convert mode.

ABSOLUTE MAXIMUM RATINGS

Table 4. AD7641 Stress Ratings[1]

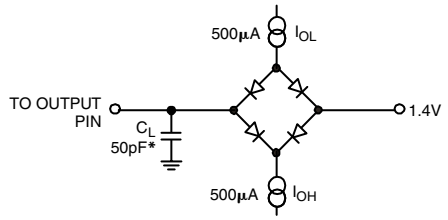
Parameter	Rating
Analog Inputs	
IN+[2], IN-[2], REF, REFBUFIN, REFGND to AGND	AVDD + 0.3 V to AGND – 0.3 V
Ground Voltage Differences	
AGND, DGND, OGND	±0.3 V
Supply Voltages	
AVDD, DVDD	–0.3 V to +2.7 V
OVDD	–0.3 V to +3.8 V
Digital Inputs	–0.3 V to 5.5V
Internal Power Dissipation[3]	700 mW
Internal Power Dissipation[4]	2.5 W
Junction Temperature	150°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

[2] See Analog Inputs section.

[3] Specification is for device in free air: 48-Lead LQFP: θ_{JA} = 91°C/W, θ_{JC} = 30°C/W.

[4] Specification is for device in free air: 48-Lead LFCSP: θ_{JA} = 26°C/W.



*IN SERIAL INTERFACE MODES, THE SYNC, SCLK, AND SDOUT TIMINGS ARE DEFINED WITH A MAXIMUM LOAD C_L OF 10pF; OTHERWISE, THE LOAD IS 50pF MAXIMUM.

Figure 2. Load Circuit for Digital Interface Timing SDOUT, SYNC, SCLK Outputs, C_L=10 pF

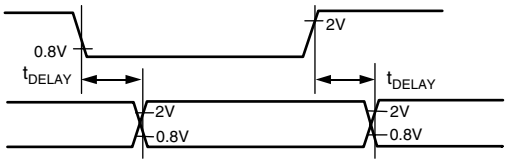


Figure 3. Voltage Reference Levels for Timing

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

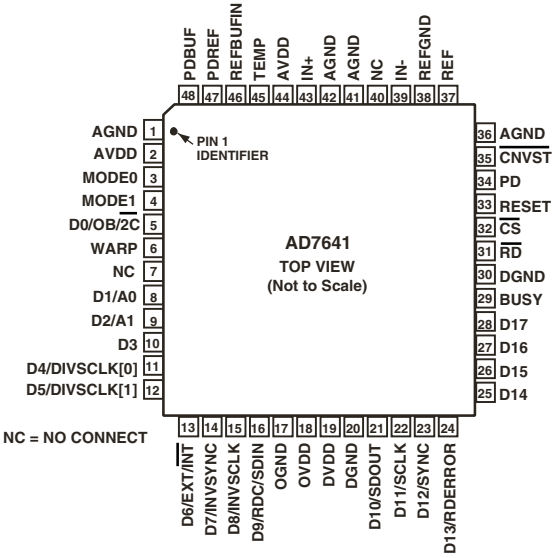


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 36, 41, 42	AGND	P	Analog power ground pin.
2, 44	AVDD	P	Input analog power pins. Nominally 2.5 V
7, 40	NC		No Connect
3	MODE0	DI	Data Output Interface mode Selection.
4	MODE1	DI	Data Output Interface mode Selection:

Interface MODE #	MODE0	MODE1	Description
0	0	0	18-bit Interface
1	0	1	16-bit Interface
2	1	0	Byte Interface
3	1	1	Serial Interface

5	D0/OB/$\overline{2C}$	DI/O	When MODE=0 (18-bit interface mode), this pin is Bit 0 of the parallel port data output bus and the data coding is straight binary. In all other modes, this pin allows choice of Straight Binary/Binary Two's Complement. When OB/$\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted resulting in a two's complement output from its internal shift register.
6	WARP	DI	Conversion mode selection. When HIGH, this input selects the fastest mode, the maximum throughput is achievable, and a minimum conversion rate must be applied in order to guarantee full specified accuracy. When LOW, full accuracy is maintained independent of the minimum conversion rate.
8	D1/A0	DI/O	When MODE=0 (18-bit interface mode), this pin is Bit 1 of the parallel port data output bus. In all other modes, this input pin controls the form in which data is output as shown in Table 6.
9	D2/A1	DI/O	When MODE=0 or MODE=1 (18-bit or 16-bit interface mode), this pin is Bit 2 of the parallel port data output bus. In all other modes, this input pin controls the form in which data is output as shown in Table 6.
10	D3	DO	In all modes except MODE=3, this output is used as Bit 3 of the Parallel Port Data Output Bus. This pin is always an output regardless of the interface mode.
11, 12	D[4:5] or DIVSCLK[0:1]	DI/O	In all modes except MODE=3, these pins are Bit 4 and Bit 5 of the Parallel Port Data Output Bus. In MODE=3 (serial mode), when EXT/$\overline{INT}$ is LOW, and RDC/SDIN is LOW, which serial master read after convert, these inputs, part of the serial port, are used to slow down if desired the internal serial clock clocks the data output. In other serial modes, these pins are not used.

Pin No.	Mnemonic	Type[1]	Description
13	D6 or EXT/$\overline{INT}$	DI/O	In all modes except MODE=3, this output is used as Bit 6 of the Parallel Port Data Ouput Bus. When MODE=3 (serial mode), this input, part of the serial port, is used as a digital select input for choosing the internal or an external data clock. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input.
14	D7or INVSYNC	DI/O	In all modes except MODE=3, this output is used as Bit 7 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this input, part of the serial port, is used to select the active state of the SYNC signal. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
15	D8 or INVSCLK	DI/O	In all modes except MODE=3, this output is used as Bit 8 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this input, part of the serial port, is used to invert the SCLK signal. It is active in both master and slave mode.
16	D9 or RDC/SDIN	DI/O	In all modes except MODE=3, this output is used as Bit 9 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this input, part of the serial port, is used as either an external data input or a read mode selection input depending on the state of EXT/$\overline{INT}$. When EXT/$\overline{INT}$ is HIGH, RDC/SDIN could be used as a data input to daisy chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 18 SCLK periods after the initiation of the read sequence. When EXT/$\overline{INT}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output SDOUT only when the conversion is complete.
17	OGND	P	Input/Output Interface Digital Power Ground.
18	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply than the supply of the host interface (2.5 V or 3 V).
19	DVDD	P	Digital Power. Nominally at 2.5 V.
20	DGND	P	Digital Power Ground.
21	D10 or SDOUT	DO	In all modes except MODE=3, this output is used as Bit 10 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this output, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip shift register. The AD7641 provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logical level of OB/$\overline{2C}$. In serial mode, when EXT/$\overline{INT}$ is LOW, SDOUT is valid on both edges of SCLK. In serial mode, when EXT/$\overline{INT}$ is HIGH: If INVSCLK is LOW, SDOUT is updated SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
22	D11 or SCLK	DI/O	In all modes except MODE=3, this putput is used as the Bit 11 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this pin, part of the serial port, is used as a serial data clock input or output, dependent upon the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
23	D12 or SYNC	DO	In all modes except MODE=3, this output is used as the Bit 12 of the Parallel Port Data Output Bus. When MODE=3 (serial mode), this output, part of the serial port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{INT}$ = Logic LOW). When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and remains HIGH while SDOUT output is valid. When a read sequence is initiated and INVSYNC is HIGH, SYNC is driven LOW and remains LOW while SDOUT output is valid.
24	D13 or RDERROR	DO	In all modes except MODE=3, this output is used as the Bit 12 of the Parallel Port Data Output Bus. In MODE=3 (serial mode) and when EXT/$\overline{INT}$ is HIGH, this output, part of the serial port, is used as a incomplete read error flag. In slave mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed high.
25-28	D[14:17]	DO	Bit 14 to Bit 17 of the Parallel Port Data output bus. These pins are always outputs regardless of the interface mode.
29	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started, and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data ready clock signal.
30	DGND	P	Must be tied to digital ground.
31	$\overline{RD}$	DI	Read Data. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled.
32	$\overline{CS}$	DI	Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external clock.

Pin No.	Mnemonic	Type[1]	Description
33	RESET	DI	Reset Input. When set to a logic HIGH, reset the AD7641. Current conversion if any is absorbed. If not used, this pin could be tied to the DGND.
34	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
35	$\overline{\text{CNVST}}$	DI	Start Conversion. A falling edge on CNVST puts the internal sample/hold into the hold state and initiates a conversion.
37	REF	AI	Reference Input Voltage and Internal Reference Buffer Output. Apply an external reference on this pin if the internal reference buffer is not used. Should be decoupled effectively with or without the internal buffer.
38	REFGND	AI	Reference Input Analog Ground.
39	IN-	AI	Differential Negative Analog Input.
43	IN+	AI	Differential Negative Analog Input.
45	TEMP	AO	Temperature sensor analog output.
46	REFBUFIN	AI	Internal Reference Output and Reference Buffer Input Voltage. The internal reference buffer has a fixed gain. It outputs 2.048V typically when 1.2V is applied on this pin.
47	PDREF	DI	This pin allows the choice of internal or external voltage references. When LOW, the on-chip reference is turned on. When HIGH, the internal reference is switched off and an external reference must be used.
48	PDBUF	DI	This pin allows the choice of buffering an internal or external reference with the internal buffer. When LOW, the buffer is selected. When HIGH, the buffer is switched off.

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital Input; DI/O = bidirectional digital; DO = digital output; P = Power.

Table 6. Data Bus Interface Definition

MODE	MODE0	MODE1	D0/OB/$\overline{\text{2C}}$	D1/A0	D2/A1	D[3]	D[4:9]	D[10:11]	D[12:15]	D[16:17]	DESCRIPTION
0	0	0	R[0]	R[1]	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	18-Bit Parallel
1	0	1	OB/$\overline{\text{2C}}$	A0:0	R[2]	R[3]	R[4:9]	R[10:11]	R[12:15]	R[16:17]	16-Bit High Word
1	0	1	OB/$\overline{\text{2C}}$	A0:1	R[0]	R[1]	All Zeros				16-Bit Low Word
2	1	0	OB/$\overline{\text{2C}}$	A0:0	A1:0	All Hi-Z		R[10:11]	R[12:15]	R[16:17]	8-Bit HIGH Byte
2	1	0	OB/$\overline{\text{2C}}$	A0:0	A1:1	All Hi-Z		R[2:3]	R[4:7]	R[8:9]	8-Bit MID Byte
2	1	0	OB/$\overline{\text{2C}}$	A0:1	A1:0	All Hi-Z		R[0:1]	All Zeros		8-Bit LOW Byte
2	1	0	OB/$\overline{\text{2C}}$	A0:1	A1:1	All Hi-Z		All Zeros		R[0:1]	8-Bit LOW Byte
3	1	1	OB/$\overline{\text{2C}}$	All Hi-Z		Serial Interface					Serial Interface

R[0:17] is the 8-bit ADC value stored in its output register.

TERMINOLOGY

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Gain Error
The first transition (from 000 . . . 00 to 000 . . . 01) should occur for an analog voltage 1/2 LSB above the nominal – full scale (–2.047992 V for the ±2.048V range). The last transition (from 111 . . . 10 to 111 . . . 11) should occur for an analog voltage 1 ½ LSB below the nominal full scale (2.047977 V for the ±2.048V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Zero Error
The zero error is the difference between the ideal mid-scale input voltage (0 V) and the actual voltage producing the mid-scale output code.

Spurious Free Dynamic Range (SFDR)/
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula:

$$ENOB = \left(S/[N+D]_{dB} - 1.76\right)/6.02)$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal to (Noise + Distortion) Ratio (S/[N+D])
S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

Aperture Delay
Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signal is held for a conversion.

Transient Response
The time required for the AD7641 to achieve its rated accuracy after a full-scale step function is applied to its input.

Reference Voltage Temperature Coefficient
The change of the internal reference output voltage V over the operating temperature range and normalized by the output voltage at 25°C, expressed in ppm/°C. The equation follows:

$$TCV\left(ppm/°C\right) = \frac{V(T_2) - V(T_1)}{V(25°C) \times (T_2 - T_1)} \times 10^6$$

where:
V(25°C) = V at 25°C
$V(T_2)$ = V at Temperature 2
$V(T_1)$ = V at Temperature 1

Reference Voltage Long-Term Stability
Typical shift of output voltage at 25°C on a sample of parts subjected to operation life test of 1000 hours at 125°C:

$$\Delta V(ppm) = \frac{V(t_1) - V(t_0)}{V(t_0)} \times 10^6$$

where:
$V(t_0)$ = V at 25°C at Time 0
$V(t_1)$ = V at 25°C after 1,000 hours operation at 125°C

Reference Voltage Thermal Hysteresis
Thermal hysteresis is defined as the change of output voltage after the device is cycled through temperature from +25°C to -40°C to +125°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle

$$V_{HYS}(ppm) = \frac{V_{TC} - V(25°C)}{V(25°C)} \times 10^6$$

where:
V(25°C) = V at 25°C
V_{TC} = V at 25°C after temperature cycle at +25°C to -40°C to +125°C and back to +25°C

CIRCUIT INFORMATION

The AD7641 is a very fast, low-power, single-supply, precise 18-bit analog-to-digital converter (ADC) using successive approximation architecture.

The AD7641 features different modes to optimize performances according to the applications. In Warp mode, the AD7641 is capable of converting 2,000,000 samples per second (2 MSPS). The AD7641 provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

The AD7641 can be operated from a single 2.5 V supply and be interfaced to either 5 V or 3.3 V or 2.5 V digital logic. It is housed in a 48-lead LQFP or a tiny LFCSP packages that combines space savings and allows flexible configurations as either serial or parallel interface. The AD7641 is a pin-to-pin-compatible upgrade of the AD7674.

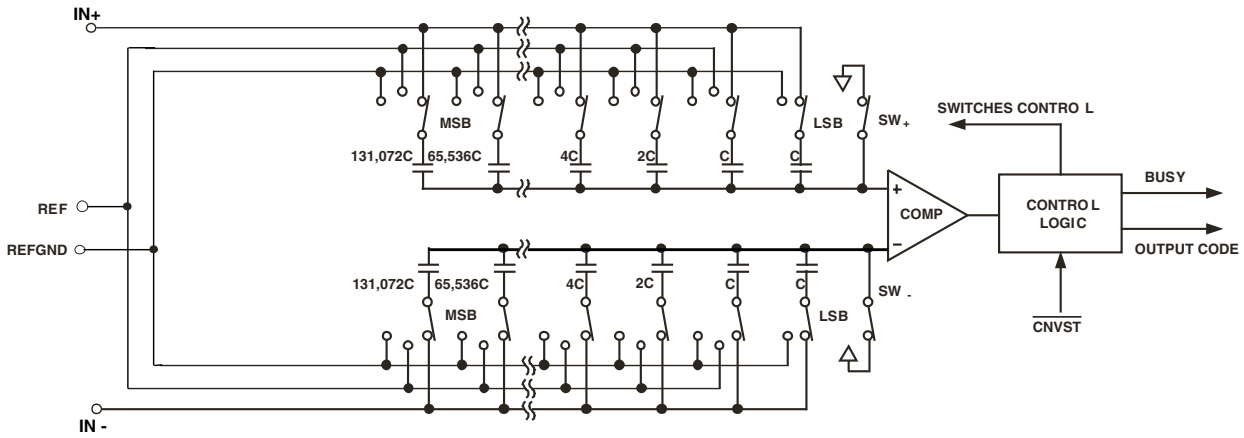


Figure 5. ADC Simplified Schematic

CONVERTER OPERATION

The AD7641 is a successive approximation analog-to-digital converter based on a charge redistribution DAC. Figure 5 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 18 binary weighted capacitors which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to AGND via SW+ and SW-. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on IN+ and IN- inputs. When the acquisition phase is complete and the CNVST input goes low, a conversion phase is initiated. When the conversion phase begins, SW+ and SW- are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the inputs IN+ and IN- captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between REFGND or REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4 \ldots V_{REF}/262144$). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output low.

MODES OF OPERATION

The AD7641 features two modes of operations; Warp and Normal. Each of these modes is more suitable for specific applications.

The Warp mode allows the fastest conversion rate up to 2 MSPS. However, in this mode, and this mode only, the full specified accuracy is guaranteed only when the time between conversion does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms, for instance, after power-up, the first conversion result should be ignored. This mode makes the AD7641 ideal for applications where fast sample rate are required.

The normal mode is the fastest mode (1.5 MSPS) without any limitation about the time between conversions. This mode makes the AD7641 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

TRANSFER FUNCTIONS

Except in 18 Bit interface mode, using the OB/$\overline{2C}$ digital input, the AD7641 offers two output codings: straight binary and two's complement. The ideal transfer characteristic for the AD7641 is shown in Figure 6 and Table 7.

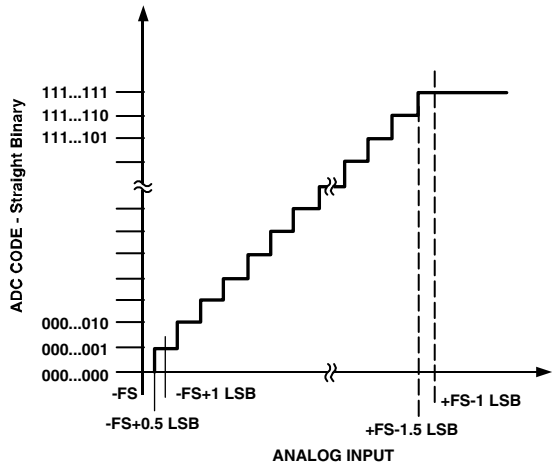
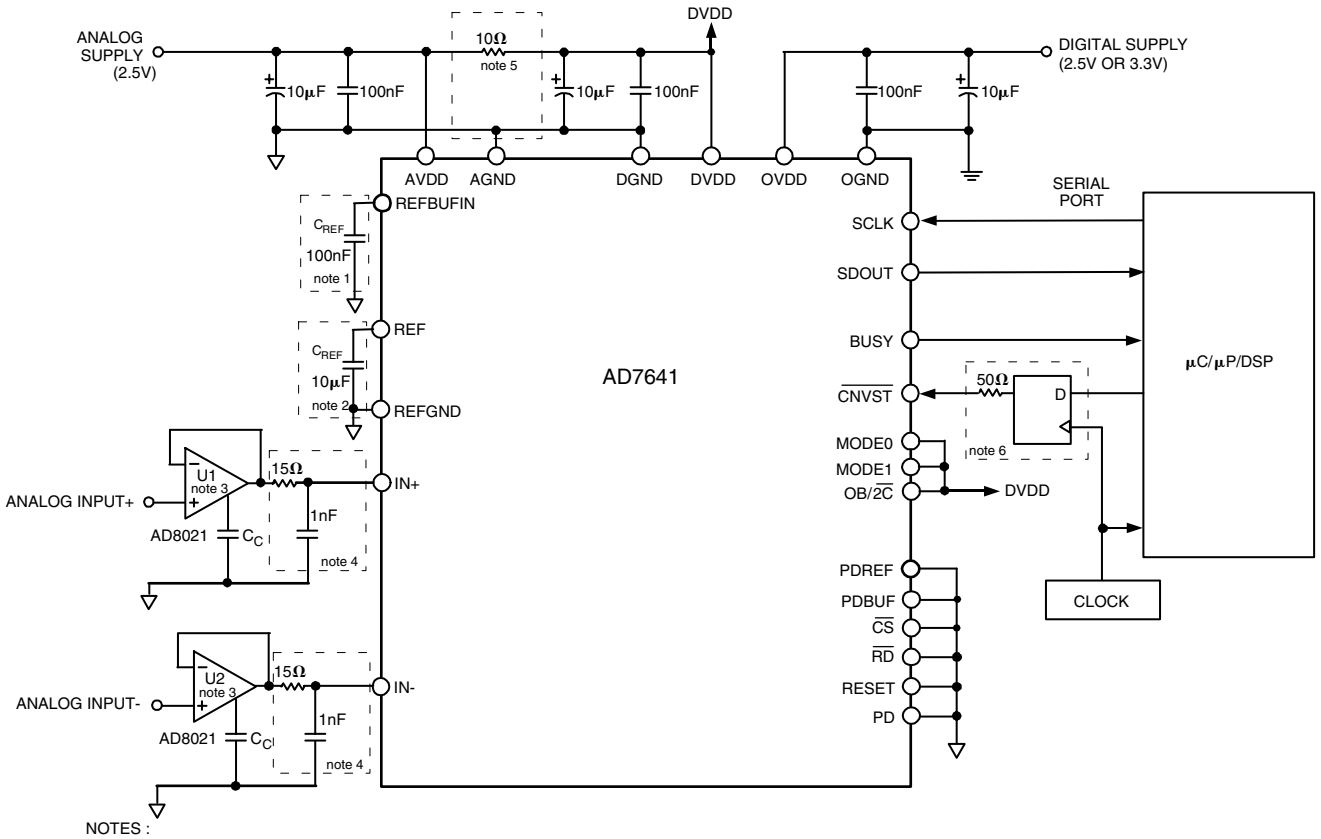


Figure 6. ADC Ideal Transfer Function

Table 7. Output Codes and Ideal Input Voltages

	Digital Output Code (Hex)		
Description	**Analog Input V_{REF}= 2.048V**	**Straight Binary**	**Twos Complement**
FSR –1 LSB	2.047984 V	3FFFF[1]	1FFFF[1]
FSR – 2 LSB	2.047969 V	3FFFE	1FFE
Midscale + 1 LSB	15.625µV	20001	00001
Midscale	0 V	20000	00000
Midscale – 1 LSB	-15.625µV	1FFFF	3FFFF
-FSR + 1 LSB	-2.047984 V	00001	20001
-FSR	-2.048 V	00000[2]	20000[2]

[1] This is also the code for overrange analog input ($V_{IN+} – V_{IN-}$ above $V_{REF} – V_{REFGND}$).
[2] This is also the code for underrange analog input ($V_{IN+} – VI_{N-}$ below $-V_{REF} + V_{REFGND}$).



NOTES :
Note 1 : See Voltage Reference Input Section.
Note 2 : C_{REF} is 10µF ceramic capacitor or low esr tantalum. Ceramic size 1206 Panasonic ECJ-3xB0J106 is recommended. See Voltage Reference Input Section.
Note 3 : The AD8021 is recommended. See Driver Amplifier Choice Section.
Note 4 : See Analog Inputs Section.
Note 5 : Option. See Power Supply Section.
Note 6 : Optional Low jitter CNVST. See Conversion Control Section.

Figure 7. Typical Connection Diagram (Internal reference buffer, serial interface)

TYPICAL CONNECTION DIAGRAM

Figure 7 shows a typical connection diagram for the AD7641. Different circuitry shown on this diagram are optional and are discussed below.

ANALOG INPUTS

Figure 8 shows a simplified analog input section of the AD7641.

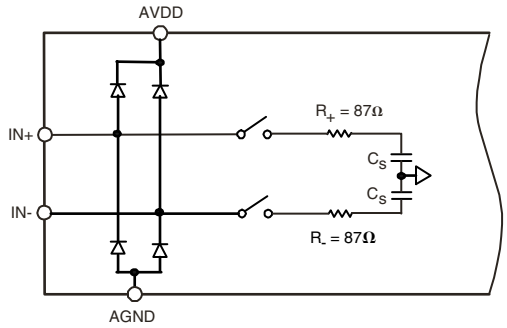


Figure 8. AD7641 simplified Analog input

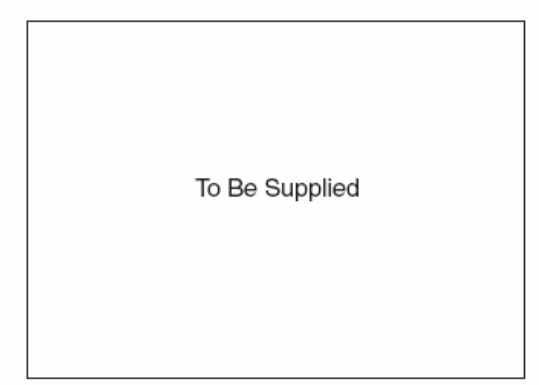


Figure 9. Analog Input CMRR vs. Frequency

During the acquisition phase, for AC signals, the AD7641 behaves like a one pole RC filter consisted of the equivalent resistance R+ , R- and C_S. The resistors R_+ and R_- are typically TBD Ω and are lumped component made up of some serial resistor and the on resistance of the switches. The capacitor C_S is typically TBD pF and is mainly the ADC sampling capacitor. This one pole filter with a typical -3dB cutoff frequency of 50 MHz reduces undesirable aliasing effect and limits the noise coming from the inputs.

Because the input impedance of the AD7641 is very high, the AD7641 can be driven directly by a low impedance source without gain error. This allows, as shown in Figure 7, an external one-pole RC filter between the output of the amplifier and the ADC analog inputs to even further improve the noise filtering done by the AD7641 analog input circuit. However, the source impedance has to be kept low because it affects the ac performances, especially the total harmonic distortion. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7641 is easy to drive, the driver amplifier needs to meet at least the following requirements:

- The driver amplifier and the AD7641 analog input circuit have to be able together to settle for a full-scale step the capacitor array at a 18-bit level (0.0004%). In the amplifier's datasheet, the settling at 0.1% or 0.01% is more commonly specified. It could significantly differ from the settling time at 18 bit level and, therefore, it should be verified prior to the driver selection. The tiny op-amp AD8021 which combines ultra low noise and a high gain bandwidth meets this settling time requirement.

- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the AD7641. The noise coming from the driver is filtered by the AD7641 analog input circuit one-pole low-pass filter made by R_+, R_- and C_S. The SNR degradation due to the amplifier is :

$$SNR_{LOSS} = 20LOG\left(\frac{56}{\sqrt{3136 + \pi f_{-3dB}\left(Ne_N\right)^2}}\right)$$

where :

f_{-3dB} is the -3dB input bandwidth in MHz of the AD7641 (50 MHz) or the cutoff frequency of the input filter if any used
N is the noise factor of the amplifiers (1 if in buffer configuration)
e_N is the equivalent input noise voltage of each op-amp in $nV/(Hz)^{1/2}$

For instance, a driver with an equivalent input noise of 2nV/√Hz like the AD8021 and configured as a buffer, thus with a noise gain of +1, the SNR degrades by only 0.17 dB with the filter in Figure 7, and 0.8 dB without.

- The driver needs to have a THD performance suitable to that of the AD7641.

The AD8021 meets these requirements and is usually appropriate for almost all applications. The AD8021 needs an external compensation capacitor of 10 pF. This capacitor should have good linearity as an NPO ceramic or mica type.

The AD8022 could also be used where dual version is needed and gain of 1 is used.

The AD8027 is another option where lower supply and dissipation are desired.

SINGLE TO DIFFERENTIAL DRIVER

For applications using unipolar analog signals, a single ended to differential driver will allow for a differential input into the part. The schematic is shown in Figure 10. This configuration, when provided an input signal of 0 to V_{REF} , will produce a differential $\pm V_{REF}$ with midscale at $V_{REF}/2$.

If the application can tolerate more noise, the AD8138 – a differential driver, can be used.

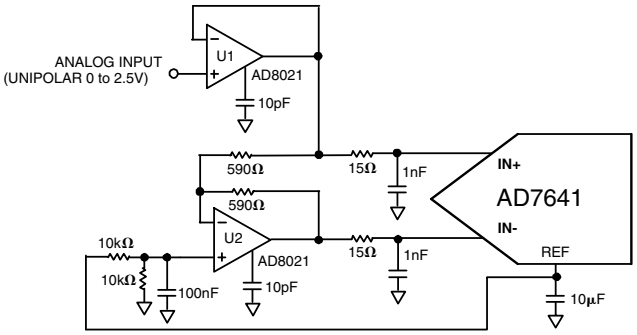


Figure 10. Single Ended to Differential Driver Circuit (Internal Reference Buffer Used)

VOLTAGE REFERENCE

The AD7641 allows the choice of either a very low temperature drift internal voltage reference or an external reference.

Unlike many ADC with internal reference, the internal reference of the AD7641 provides excellent performances and can be used in almost all applications. It is temperature compensated to 1.2V ± TBD mV with a typical drift of TBD ppm/°C, a typical long-term stability of TBD ppm and a typical hysterisis of TBD ppm.

However, the advantages to use the external reference voltage directly are :

- The power saving of about 8mW typical when the internal reference and its buffer are powered down (PDREF and PDBUF High)
- The SNR and dynamic range improvement of about 1.7 dB resulting of the use of a reference voltage very close to the supply (2.5V) instead of a typical 2.048V reference when the internal buffer is used.

To use the internal reference along with the internal buffer, PDREF and PDBUF should both be LOW. This will produce a voltage on REFBUFIN of 1.2 V and the buffer will amplify it resulting in a 2.048 V reference on REF pin.

It is useful to decouple the REFBUFIN pin with a 100 nF ceramic capacitor. The output impedance of the REFBUFIN pin is 16 kΩ. Thus, the 100 nF capacitor provides an RC filter for noise reduction.

To use an external reference along with the internal buffer, PDREF should be HIGH and PDBUF should be low. This powers down the internal reference and allows for the 1.2 V reference to be applied to REFBUFIN.

To use an external reference directly on REF pin, PDREF and PDBUF should both be HIGH.

It should be noted that the internal reference and internal buffer are independent of the power down (PD) pin of the part. Furthermore, powering up the internal reference and internal buffer requires time due to the charge of the REF decoupling.

In both cases, the voltage reference input REF has a dynamic input impedance and requires, therefore, an efficient decoupling between REF and REFGND inputs. When the internal reference buffer is used, this decoupling consists of a 10 µF ceramic capacitor (e.g. : Panasonic ECJ-3xB0J106 1206 size).

When external reference is used, the decoupling consists of a low ESR 47 µF tantalum capacitor connected to the REF and REFGND inputs with minimum parasitic inductance.

TEMPERATURE SENSOR

The TEMP pin, which measures the temperature of the AD7641, can be used as shown in Figure 11. The output of the TEMP pin is applied to one of the inputs of the analog switch (e.g. : ADG779) and the ADC itself is used to measure its own temperature. This configuration could be very useful to improve the calibration accuracy over the temperature range.

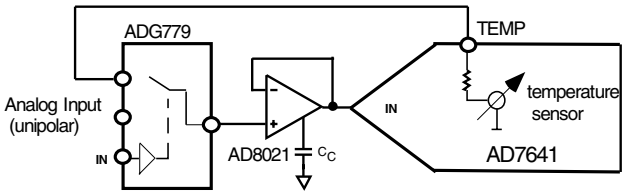


Figure 11. Use of the Temperature Sensor

POWER SUPPLY

The AD7641 uses three sets of power supply pins: an analog 2.5 V supply AVDD, a digital 2.5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.3 V and 5.25 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply as shown in Figure 7. The AD7641 is independent of power supply sequencing and thus free from supply voltage induced latchup. Additionally, it is very insensitive to power supply variations over a wide frequency range as shown in Figure 12.

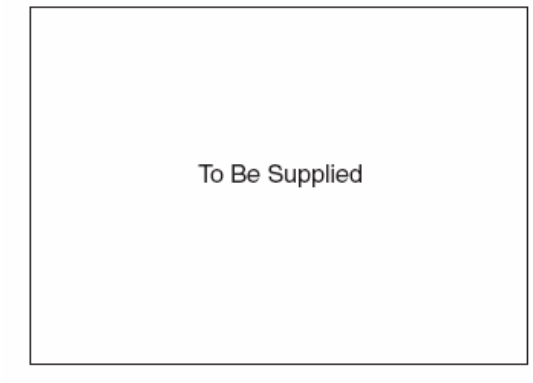


Figure 12. PSRR vs. Frequency

CONVERSION CONTROL

Figure 13 shows the detailed timing diagrams of the conversion process. The AD7641 is controlled by the signal $\overline{\text{CNVST}}$ which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals.

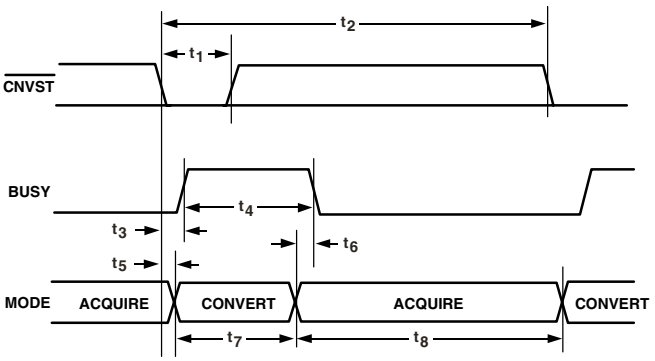


Figure 13. Basic Conversion Timing

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with special care with fast, clean edges and levels, with minimum overshoot and undershoot or ringing.

For applications where the SNR is critical, the $\overline{\text{CNVST}}$ signal should have a very low jitter. Some solutions to achieve that are to use a dedicated oscillator for $\overline{\text{CNVST}}$ generation or, at least, to clock it with a high frequency low jitter clock as shown in Figure 7.

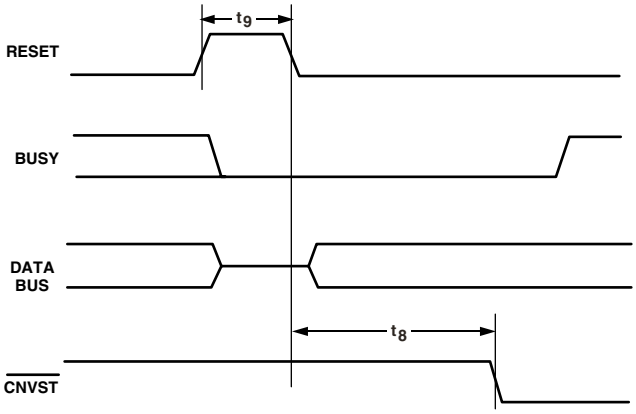


Figure 14. RESET Timing

INTERFACES

DIGITAL INTERFACE

The AD7641 has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel data bus. The AD7641 digital interface also accommodates both 2.5V, 3.3V or 5V logic with OVDD either at 2.5V or 3.3V. OVDD defines the logic high output voltage. In most applications, the OVDD supply pin of the AD7641 is connected to the host system interface 2.5V or 3.3V digital supply. Finally, except in 18 bit interface mode, by using the OB/$\overline{2C}$ input pin, both two's complement or straight binary coding can be used.

The two signals $\overline{CS}$ and $\overline{RD}$ control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{CS}$ allows the selection of each AD7641 in multi-circuits applications and is held low in a single AD7641 design. $\overline{RD}$ is generally used to enable the conversion result on the data bus.

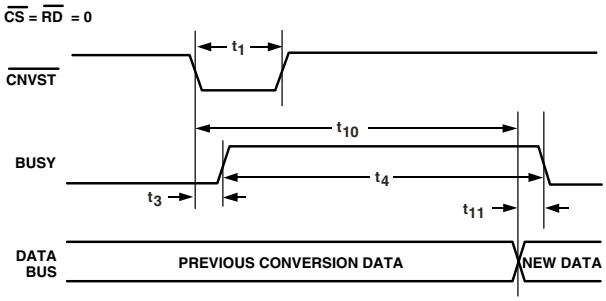


Figure 15. Master Parallel Data Timing for Reading (Continuous Read)

PARALLEL INTERFACE

The AD7641 is configured to use the parallel interface with either a 18-bit, 16-bit or 8-bit bus width according to the Table 6. The data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion as shown, respectively, in Figure 16 and Figure 17. When the data is read during the conversion, however, it is recommended that it is read only during the first half of the conversion phase. That avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry. Please refer to Table 6 for a detailed description of the different options available.

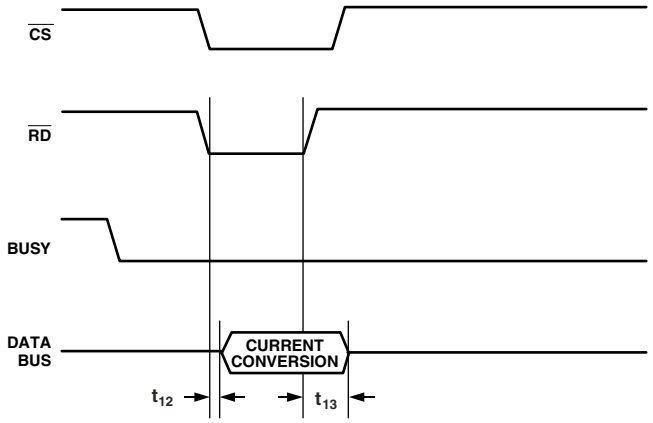


Figure 16. Slave Parallel Data Timing for Read (Read After Convert)

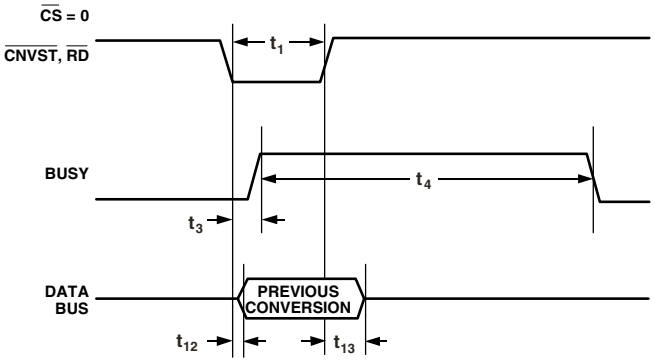


Figure 17. Slave Parallel Data Timing for Reading (Read During Convert)

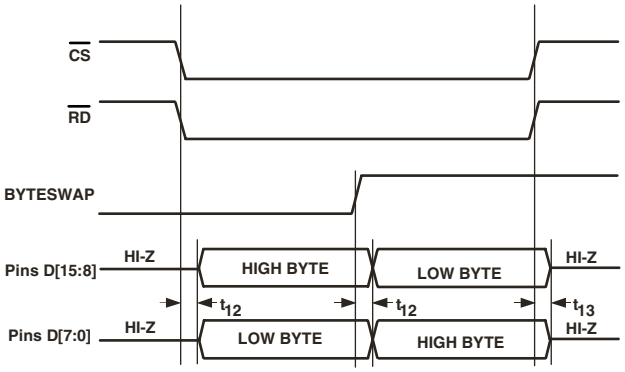


Figure 18. 8-Bit and 16-Bit Parallel Interface

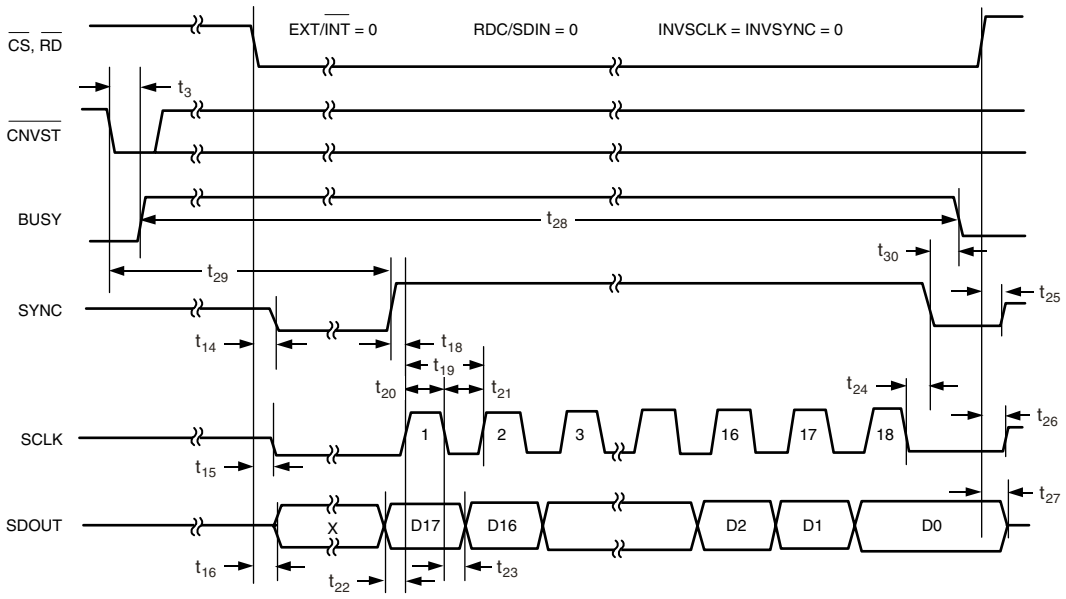


Figure 19. Master Serial Data Timing for Reading (Read After Convert)

SERIAL INTERFACE

The AD7641 is configured to use the serial interface when MODE0 and MODE1 are held high. The AD7641 outputs 18 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 18 clock pulses provided on SCLK pin. The output data is valid on both the rising and falling edge of the data clock. That allows a fast serial interface speed by using the same clock edge to output the data from the ADC and to sample the previous bit by the digital host.

MASTER SERIAL INTERFACE

Internal Clock

The AD7641 is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{\text{INT}}$ pin is held low. The AD7641 also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted if desired. Depending on RDC/SDIN input, the data can be read after each conversion or during the following conversion. Figure 19 and Figure 20 show the detailed timing diagrams of these two modes.

Usually, because the AD7641 is used with a fast throughput, the mode master read during conversion is the most recommended serial mode when it can be used.

In read-during-conversion mode, the serial clock and data toggle at appropriate instants which minimize potential feedthrough between digital activity and the critical conversion decisions.

In read-after-conversion mode, it should be noted that, unlike in other modes, the signal BUSY returns low after the 18 data bits are pulsed out and not at the end of the conversion phase which results in a longer BUSY width.

To accommodate slow digital hosts, the serial clock can be slowed down by using DIVSCLK.

SLAVE SERIAL INTERFACE

External Clock

The AD7641 is configured to accept an externally supplied serial data clock on the SCLK pin when the EXT/$\overline{\text{INT}}$ pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{\text{CS}}$ When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 21 and Figure 22 show the detailed timing diagrams of these methods.

While the AD7641 is performing a bit decision, it is important that voltage transients not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the AD7641 provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it be a discontinuous clock that is toggling only when BUSY is low or, more importantly, that it does not transition during the latter half of BUSY high.

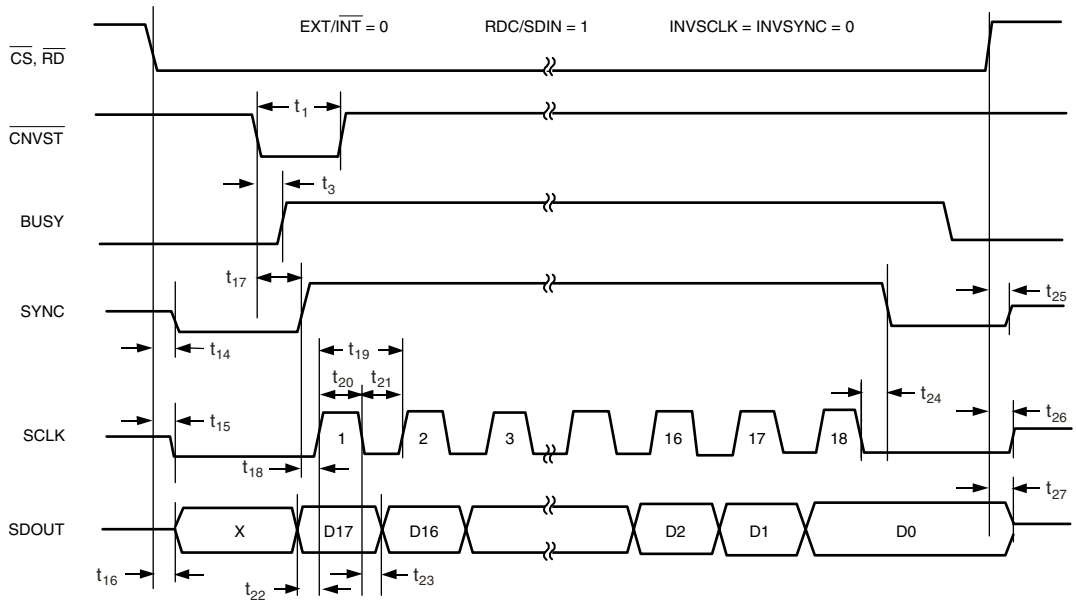


Figure 20. Master Serial Data Timing for Reading (Read Previous Conversion During Convert)

External Discontinuous Clock Data Read After Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 21 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning low, the result of this conversion can be read while both $\overline{CS}$ and $\overline{RD}$ are low. The data is shifted out, MSB first, with 18 clock pulses and is valid on both rising and falling edge of the clock.

Among the advantages of this method, the conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process.

Another advantage is to be able to read the data at any speed up to 80 MHz which accommodates both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the AD7641 provides a "daisy-chain" feature using the RDC/SDIN input pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired as, for instance, in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 23. Simultaneous sampling is possible by using a common $\overline{CNVST}$ signal. It should be noted that the RDC/SDIN input is latched on the edge of SCLK opposite to the one used to shift out the data on SDOUT.Hence, the MSB of the "upstream" converter just follows the LSB of the "downstream" converter on the next SCLK cycle.

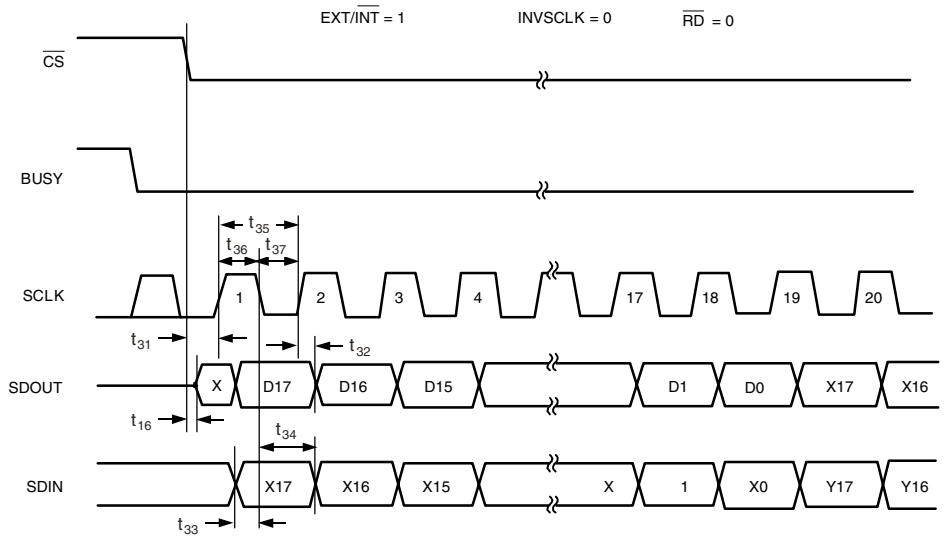


Figure 21. Slave Serial Data Timing for Reading (Read After Convert)

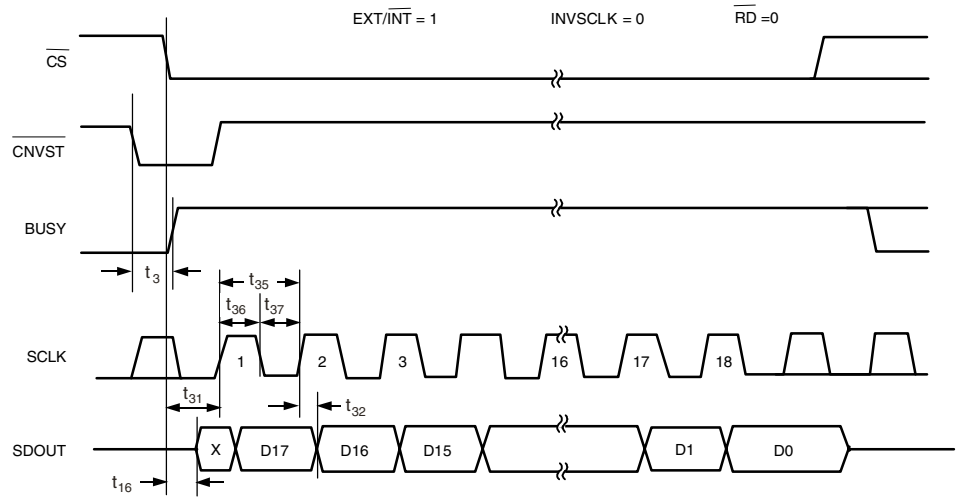


Figure 22. Slave Serial Data Timing for Reading (Read Previous Conversion During Convert)

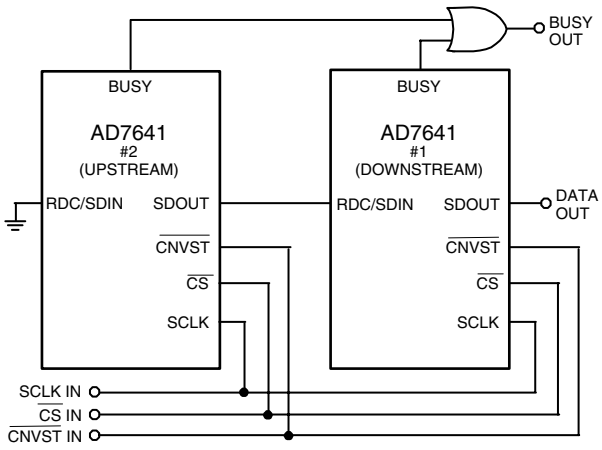


Figure 23. Two AD7641 in a "Daisy-Chain" Configuration

External Clock Data Read During Conversion

Figure 22 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{CS}$ and $\overline{RD}$ are both low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 18 clock pulses and is valid on both rising and falling edge of the clock. The 18 bits have to be read before the current conversion is complete. If that is not done, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no "daisy chain" feature in this mode and RDC/SDIN input should always be tied either high or low. To reduce performance degradation due to digital activity, a fast discontinuous clock of TBD is recommended to ensure that all the bits are read during the first half of the conversion phase. It is also possible to begin to read the data after conversion and continue to read the last bits even after a new conversion has been initiated.

MICROPROCESSOR INTERFACING

The AD7641 is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The AD7641 is designed to interface either with a parallel 8-bit or 16-bit wide interface or with a general purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the AD7641 to prevent digital noise from coupling into the ADC. The following section illustrates the use of the AD7641 with an SPI equipped DSP, the ADSP-219x.

SPI Interface (ADSP-219x)

Figure 22 shows an interface diagram between the AD7641 and an SPI-equipped DSP, ADSP219x. To accommodate the slower speed of the DSP, the AD7641 acts as a slave device and data must be read after conversion. This mode also allows the "daisy chain" feature. The convert command could be initiated in response to an internal timer interrupt. The 18-bit output data are read with 3 SPI byte access. The reading process could be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the DSP. The Serial Peripheral Interface (SPI) on the ADSP-219x is configured for master mode (MSTR) = 1, Clock Polarity Bit (CPOL) = 0, Clock Phase Bit (CPHA) = 1 and SPI interrupt enable (TIMOD) =00 by writing to the SPI Control Register (SPICLTx). It should be noted that to meet all timing requirements, the SPI clock should be limited to 17Mbits/s which allow to read an ADC result in about 1.1 µs. When higher sampling rate is desired, it is recommended to use one of the parallel interface mode with the ADSP-219x.

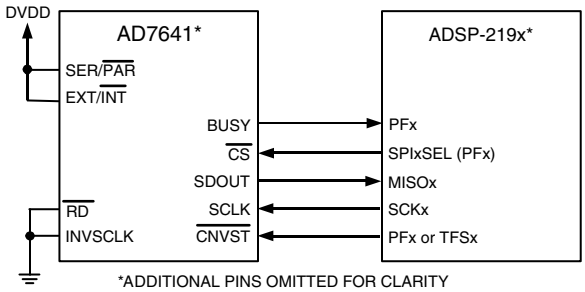


Figure 24. Interfacing the AD7641 to SPI Interface

APPLICATION HINTS

LAYOUT

The AD7641 has very good immunity to noise on the power supplies. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD7641 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7641, or, at least, as close as possible to the AD7641. If the AD7641 is in a system where multiple devices require analog to digital ground connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7641.

It is recommended to avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7641 to avoid noise coupling. Fast switching signals like $\overline{\text{CNVST}}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board. The power supply lines to the AD7641 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supplies impedance presented to the AD7641 and reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supplies pins AVDD, DVDD and OVDD close to, and ideally right up against these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD7641 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended if no separate supply is available, to connect the DVDD digital supply to the analog supply AVDD through an RC filter as shown in Figure 7, and connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high-frequency spikes.

The AD7641 has four different ground pins; REFGND, AGND, DGND, and OGND. REFGND senses the reference voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. The decoupling capacitor should be close to the ADC and connected with short and large traces to minimize parasitic inductances.

EVALUATING THE AD7641 PERFORMANCE

A recommended layout for the AD7641 is outlined in the documentation of the EVAL-AD7641-CB, evaluation board for the AD7641. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the Eval-Control BRD3.

OUTLINE DIMENSIONS

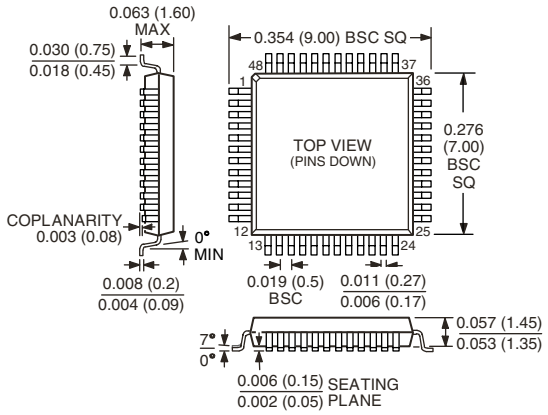


Figure 25. 48-Lead Quad Flatpack (LQFP)
(ST-48)
Dimensions shown in inches and (millimeters)

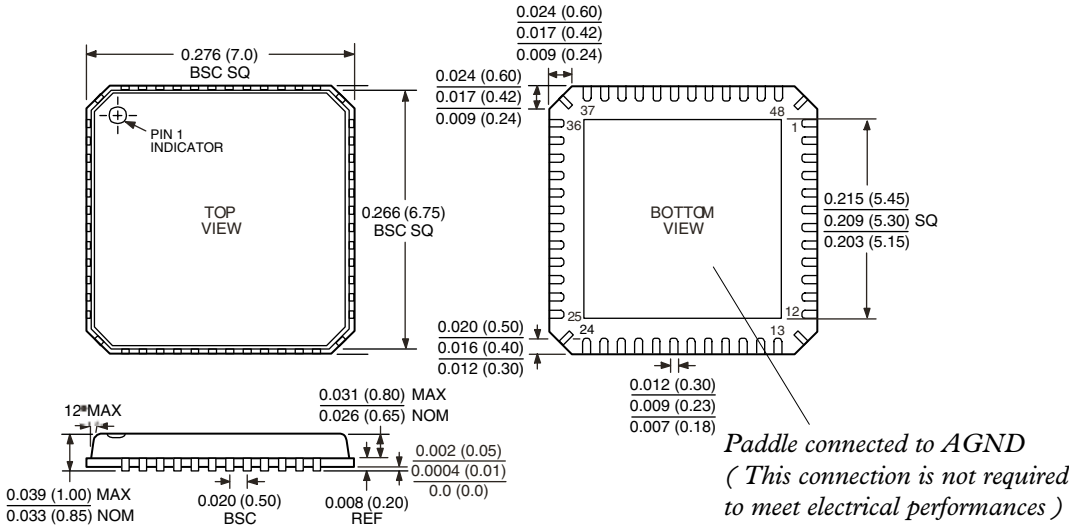


Figure 26. 48-Lead Frame Chip Scale Package (LFCSP)
(CP-48)
(Dimensions shown in millimeters and (inchs)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7641AST	-40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7641ASTRL	-40°C to +85°C	Quad Flatpack (LQFP)	ST-48
AD7641ACP	-40°C to +85°C	Chip Scale (LFCSP)	CP-48
AD7641ACPRL	-40°C to +85°C	Chip Scale (LFCSP)	CP-48
EVAL-AD7641CB[1]		Evaluation Board	
EVAL-CONTROL BRD2[2]		Controller Board	
EVAL-CONTROL BRD3[2]		Controller Board	

[1] This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD2 or the EVAL-CONTROL BRD3 for evaluation/demonstration purposes.
[2] This board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.