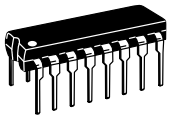
MC141541

Enhanced Monitor On-Screen Display
CMOS

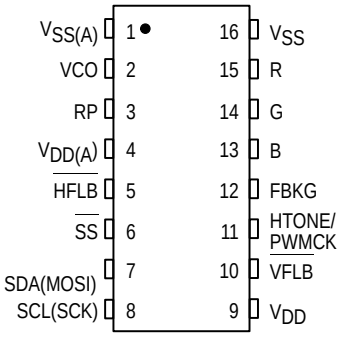


P SUFFIX
PLASTIC DIP
CASE 648

ORDERING INFORMATION

MC141541P	Plastic DIP

PIN ASSIGNMENT



The MC141541 is a high performance HCMOS device designed to interface with a microcontroller unit to allow colored symbols or characters to be displayed on a color monitor. The on–chip PLL allows both multi–system operation and self–generation of system timing. It also minimizes the MCU's burden through its built–in 273 bytes display/control RAM. By storing a full screen of data and control information, this device has the capability to carry out 'screen–refresh' without MCU supervision.

Since there is no spacing between characters, special graphics–oriented characters can be generated by combining two or more character blocks. There are two different resolutions that users can choose. By changing the number of dots per horizontal line to 320 (CGA) or 480 (EGA), smaller characters with higher resolution can be easily achieved.

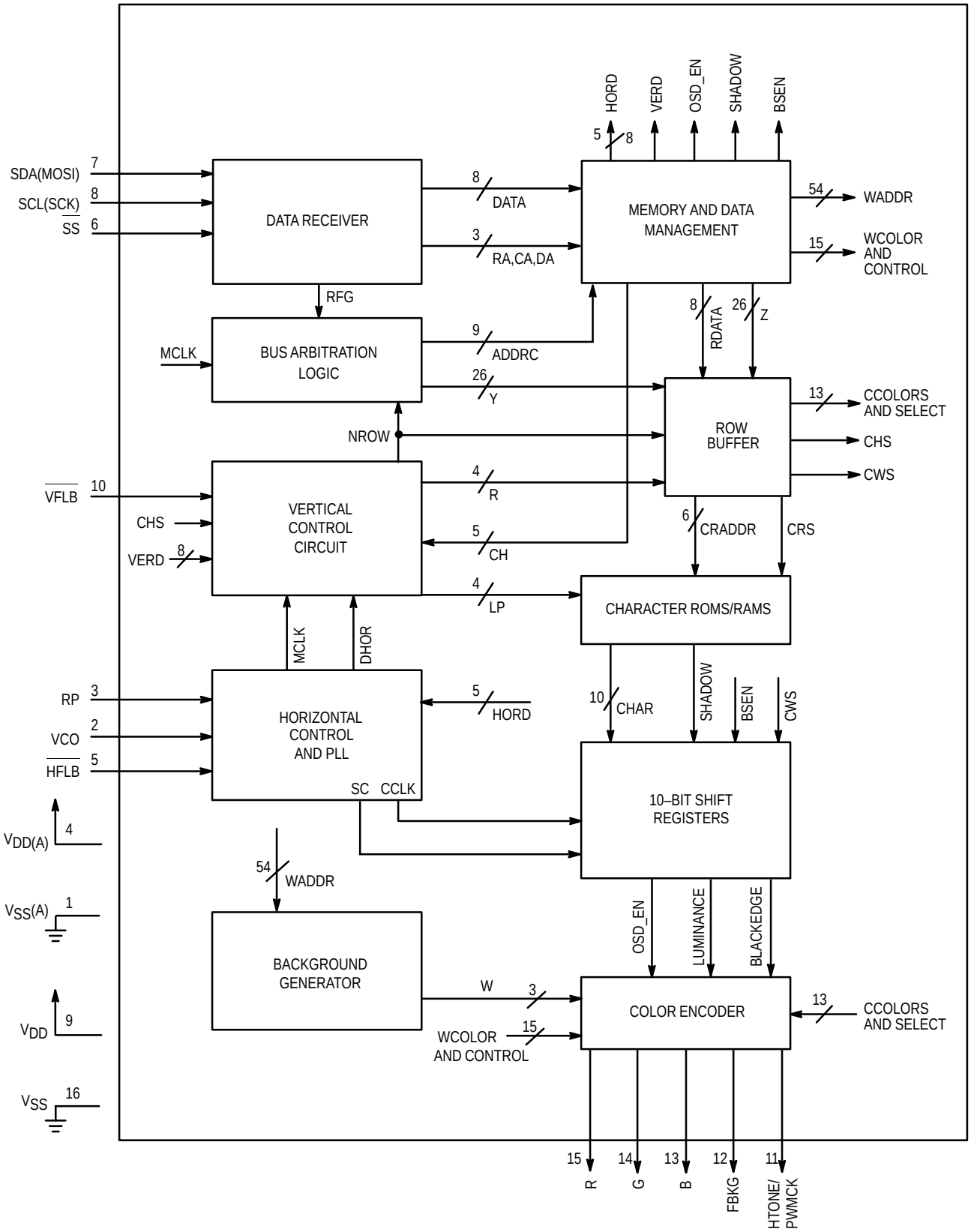
Special functions such as character bordering or shadowing, multi–level windows, double height and double width, and programmable vertical length of character can also be incorporated. Furthermore, neither massive information update nor extremely high data transmission rate are expected for normal on–screen display operation, and serial protocols are implemented in lieu of any parallel formats to achieve minimum pin count.

A special feature, character RAM fonts, is implemented in this MOSD enhanced version (EMOSD). Users can download their own fonts and display them at any time once the chip is powered on. There are two ways for users to build and store fonts. One is a conventional approach to have masked ROM fonts. A newer approach is to store the fonts in the EPROM accessed by the MCU and then download them into the EMOSD character RAM. With this new technique, users have more flexibility in preparing their fonts and the effective number of fonts is greatly increased.

- Two Selectable Resolutions: 320 (CGA) and 480 (EGA) Dots per Line
- Fully Programmable Character Array of 10 Rows by 24 Columns
- 273 Bytes Direct Mapping Display RAM Architecture
- Internal PLL Generates a Wide–Ranged System Clock
- For High–End Monitor Application, Maximum Horizontal Frequency is 110 kHz (52.8 MHz Dot Clock at 480 Mode)
- Programmable Vertical Height of Character to Meet Multi–Sync Requirement
- Programmable Vertical and Horizontal Positioning for Display Center
- 120 Characters and Graphic Symbols ROM and Eight Programmable Character RAM
- 10 x 16 Dot Matrix Character
- Character–by–Character Color Selection
- A Maximum of Four Selectable Colors per Row
- Double Character Height and Double Character Width
- Character Bordering or Shadowing
- Three Fully Programmable Background Windows with Overlapping Capability
- Provides a Clock Output Synchronous to the Incoming H Sync for External PWM
- M_BUS (IIC) Interface with Address $7A
- Single Positive 5 V Supply

REV 1
2/97 TN97031200

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	25	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

AC ELECTRICAL CHARACTERISTICS ($V_{DD} = V_{DD(A)} = 5.0$ V, $V_{SS} = V_{SS(A)} = 0$ V, $T_A = 25°C$, Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and HTONE/PWMCK) C_{load} = 30 pF, see Figure 1				
t_r	Rise Time	—	—	6	ns
t_f	Fall Time	—	—	6	ns
F_{HFLB}	HFLB Input Frequency	—	—	110	kHz

DC CHARACTERISTICS $V_{DD} = V_{DD(A)} = 5.0$ V ± 10%, $V_{SS} = V_{SS(A)} = 0$ V, $T_A = 25°C$, Voltage Referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
	Digital Input Voltage (Not Including SDA and SCL)				
V_{IL}	Logic Low	—	—	0.3 V_{DD}	V
V_{IH}	Logic High	0.7 V_{DD}	—	—	V
	Input Voltage of Pin SDA and SCL in SPI Mode				
V_{IL}	Logic Low	—	—	0.3 V_{DD}	V
V_{IH}	Logic High	0.7 V_{DD}	—	—	V
	Input Voltage of Pin SDA and SCL in M_BUS Mode				
V_{IL}	Logic Low	—	—	0.3 V_{DD}	V
V_{IH}	Logic High	0.7 V_{DD}	—	—	V
I_{II}	High–Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	µA
I_{II}	Input Current (Not Including RP, VCO, R, G, B, FBKG and HTONE/PWMCK)	– 10	—	+ 10	µA
I_{DD}	Supply Current (No Load on Any Output)	—	—	+ 15	mA

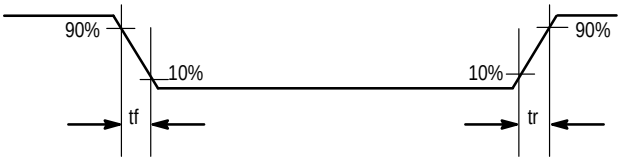


Figure 1. Switching Characteristics

PIN DESCRIPTIONS

$V_{SS(A)}$ (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL operation is separated from digital ground for optimal performance.

VCO (Pin 2)

Pin 2 is a control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)

An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The maximum voltage at Pin 3 should not exceed 3.5 V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)

Pin 4 is a positive 5 V supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)

This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock an internal system clock generated by the on–chip VCO circuit.

$\overline{\text{SS}}$ (Pin 6)

This input pin is part of the SPI serial interface. An active low signal generated by the master device enables this slave device to accept data. This pin should be pulled high to terminate the SPI communication. If M_BUS is employed as the serial interface, this pin should be tied to either V_{DD} or V_{SS}.

SDA (MOSI) (Pin 7)

Data and control messages are being transmitted to this chip from a host MCU via one of the two serial bus systems. With either protocol, this wire is configured as a uni–directional data line. (Detailed description of these two protocols will be discussed in the M_BUS and SPI sections).

SCL (SCK) (Pin 8)

A separate synchronizing clock input from the transmitter is required for either protocol. Data is read at the rising edge of each clock signal.

V_{DD} (Pin 9)

This is the power pin for the digital logic of the chip.

$\overline{\text{VFLB}}$ (Pin 10)

Similar to Pin 5, this pin inputs a negative polarity vertical synchronize signal pulse.

HTONE/PWMCK (Pin 11)

This is a multiplexed pin. When the PWMCK_EN bit is cleared after power–on or by the MCU, this pin is HTONE and outputs a logic high during windowing except when graphics or characters are being displayed. It is used to lower the external R, G, and B amplifiers' gain to achieve a transparent windowing effect. If the PWMCK_EN bit is set to 1 via M_BUS or SPI, this pin is changed to a mode–dependent clock output with 50/50 duty cycle and is synchronous with the input horizontal synchronization signal at Pin 5. The frequency is dependent on the mode in which the EMOSD is currently running. The exact frequencies in the different resolution modes are described in Table 1.

Table 1. PWM CLK Frequency

Resolution	Frequency	Duty Cycle
320 dots/line	32 x H_f	50/50
480 dots/line	48 x H_f	50/50

NOTE: H_f is the frequency of the input H sync on Pin 5.

Typically, this clock is fed into an external pulse width modulation module as its clock source. Because of the synchronization between PWM clock and H sync, a better performance on the PWM controlled functions can be achieved.

FBKG (Pin 12)

This pin outputs a logic high while displaying characters or windows when the FBKGC bit in the frame control register is 0, and output a logic high only while displaying characters when the FBKGC bit is 1. It is defaulted to high–impedance state after power–on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pins 13,14,15)

EMOSD color output is TTL level RGB to the host monitor. These three signals are active high output pins that are in a high–impedance state when EMOSD is disabled.

V_{SS} (Pin 16)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141541 is a full–screen memory architecture. Refresh is performed by the built–in circuitry after a screenful of display data has been loaded through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are transmitted via one of the two serial buses: M_BUS or SPI (mask option). These two sets of buses are multiplexed onto a single set of wires. Standard parts offer M_BUS transmission. Parts which offer SPI transmission mode must be specially manufactured as custom parts.

Data is received from the serial port and stored by the memory management circuit. Line data is stored in a row buffer for display and refreshing. During this storing and retrieving cycle, bus arbitration logic patrols the internal traffic to make sure that no crashes occur between the slower serial bus receiver and the fast 'screen–refresh' circuitry. After the full–screen display data is received through one of the serial communication interfaces, the link can be terminated if a change of the display is not required.

The bottom half of the Block Diagram contains the hardware functions for the entire system. It performs all the EMOSD functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the incoming horizontal sync signal at Pin 5 HFLB), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

M_BUS Serial Communication

This is a two–wire serial communication link that is fully compatible with the IIC bus system. It consists of an SDA bi-directional data line and an SCL clock input line. Data is sent from a transmitter (master) to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 100 kbps and the default chip address is $7A, but is hardware changeable by mask set.

Operating Procedure

Figure 2 shows the M_BUS transmission format. The master initiates a transmission routine by generating a start condition followed by a slave address byte. Once the address is properly identified, the slave will respond with an acknowledge signal by pulling the SDA line low during the ninth SCL clock. Each data byte that follows must be eight bits long, plus the acknowledge bit, for a total of nine bits. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in the **Data Transmission Formats** section. In the cases of no acknowlege or completion of data transfer, the master will generate a stop condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent, in order to activate the EMOSD circuitry of MC141541 so that the received information can be displayed.

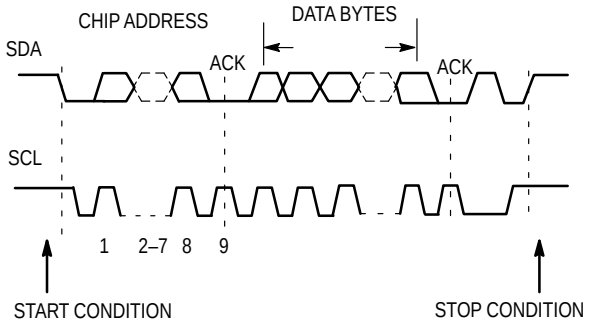


Figure 2. M_BUS Format

DATA TRANSMISSION FORMATS

In this enhanced version MOSD, both display RAM, control registers, and character RAM fonts need to be programmed after power–on. The arrangement of the display RAM and control registers is on the row–column basis, while the character RAM is on the segment–line basis. Although the address basis is different, the data downloading protocols are very similar and will be described in the following sections.

Display RAM and Control Registers

After the proper identification by the receiving device, a data train of arbitrary length is transmitted from the master. There are three transmission formats from (a) to (c) as stated below. The data train in each sequence consists of row address (R), column address (C), and display information (I), as shown in Figure 3. In format (a), display information data must be preceded with the corresponding row address and column address. This format is particularly suitable for updating small amounts of data between different rows. However, if the current information byte has the same row address as the one before, format (b) is recommended.

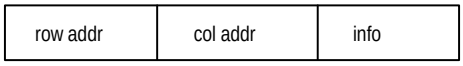


Figure 3. Data Packet

For a full–screen pattern change that requires a massive information update, or during power–up, most of the row and column addresses of either (a) or (b) formats will be consecutive. Therefore, a more efficient data transmission format (c) should be applied. This sends the RAM starting row and column addresses once only, and then treats all subsequent data as display information. The row and column addresses will be automatically incremented internally for each display information data from the starting location.

The data transmission formats are:

(a) R – > C – > I – > R – > C – > I – > . . . . . .

(b) R – > C – > I – > C – > I – > C – > I. . . . . .

(c) R – > C – > I – > I – > I – > . . . . . .

To differentiate the row and column addresses when transferring data from master, the MSB (most significant bit) is set, as in Figure 4: ‘1’ to represent row, and ‘0’ for column address. Furthermore, to distinguish the column address between formats (a), (b), and (c), the sixth bit of the column address is set to ‘1’ which represents format (c), and ‘0’ for format (a) or (b). However, there is some limitation on using mixed formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	X	X	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don’t care D: valid data

Figure 4. Row & Column Address Bit Patterns

Character RAM

The structure of eight character RAM fonts is shown in Figure 5. They occupy the font number from 0 to 7. Because of the 10 x 16 dot matrix font, each font is broken down into two segments in the horizontal direction and 16 lines in the vertical direction. Therefore, there are five dots that need to be defined for each specified segment–line location. This 5–bit data forms the lower five bits of the information data byte and the higher three bits are ignored. Because there are 16 segments (two segments per font) and 16 lines, both the segment and line addresses are four bits wide.

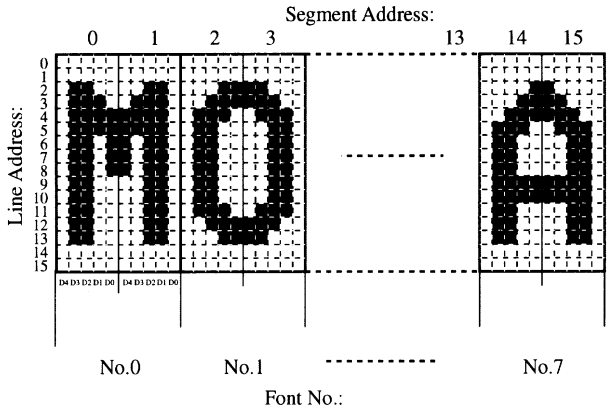
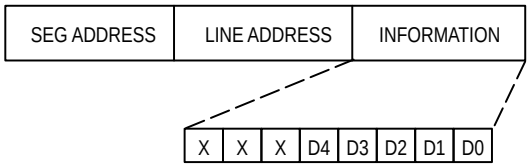


Figure 5. Segment Address Structure

Basically, the transmission format is very similar to that for display RAM or control registers. The major difference is to replace the row and column address with segment address and line address, respectively. After the proper identification by the receiving device, a data train of arbitrary length is transmitted from the master.

There are three transmission formats, from (a) to (c) as stated below. The data train in each sequence consists of segment adress (S), line address (L), and font information (I), as shown in Figure 6. In format (a), each font information data has to be preceded with the corresponding segment address and line address. This format is particularly suitable for updating small portions of font patterns. However, if the current information byte has the same segment address as the one before, format (b) is recommended.



NOTE: X means don't care bit and D means valid data bit.

Figure 6. Data Packet

For a new font pattern change which requires a massive information update, or during power–up, most of the segment and column address on either format (a) or (b) will appear to be redundant. A more efficient data transmission format (c) should be applied. It sends the character RAM starting segment and line addresses only once, and then treats all subsequent data as font information. The segment and line addresses will be automatically incremented internally for each RAM font data from the starting location.

The data transmission formats are:

(a) S – > L– > I – > S – > L – > I – > . . . . . .

(b) S – > L – > I – > L – > I – > L – > I. . . . . .

(c) S – > L – > I – > I – > I – > . . . . . .

To differentiate the segment address from row and line addresses when transferring data, Bit 7 (MSB) and Bit 6 are set, as in Figure 7, to '11' to represent segment address, or '00' to represent line address in format (a) or (b), or '01' to represent line address in format (c). However, there is some limitation on using mixed formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
SEG	1	1	X	X	D	D	D	D	a, b, c
LINE	0	0	X	X	D	D	D	D	a, b
LINE	0	1	X	X	D	D	D	D	c

X: don't care D: valid data

Figure 7. Segment and Line Address Bit Patterns

MEMORY MANAGEMENT

Inside this chip there are three kinds of RAM: display RAM, control registers, and character RAM. Display RAM and control registers are addressed with row and column (coln) number in sequence, while the character RAM is addressed with segment and line number. The transmission format is described in the **Data Transmission Formats** section. In addition to the eight RAM fonts numbered from $00 to $07, 120 masked ROM fonts numbered from $08 to $7F are also built in to this chip.

Display RAM and Control Registers

The spaces between Row 0 and Coln 0 to Row 9 and Coln 23 are called display registers, and each contains a character RAM/ROM number corresponding to a display location on the monitor screen. Every data row is associated with two control registers, located at Coln 30 and 31 of their respective rows, that control the character display format for that row. In addition, three window control registers for each of three windows, together with three frame control registers, occupy the first 13 columns of Row 10.

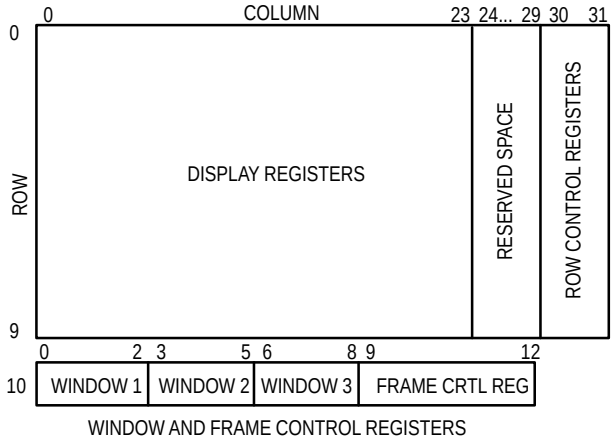


Figure 8. Memory Map

The user should handle the internal RAM address location with care, especially those rows with double length alphanumeric symbols. For example, if Row n is destined to be double height on the memory map, the data displayed on screen Rows n and n+1 will be represented by the data contained in the memory address of Row n only. The data of the next Row n+1 on the memory map will appear on the screen as n+2 and n+3 row space, and so on. Hence, it is not necessary to load a row of blank data to compensate for the double row. The user should minimize excessive rows of data in

memory in order to avoid overrunning the limited amount of row space on the screen.

For rows with double width alphanumeric symbols, only the data contained in the even numbered columns of the memory map are shown. Odd numbered columns are treated in the same manner as double height rows.

Character RAM/ROM

The RAM fonts occupy the font numbers $00 to $07, and their patterns can be changed at any time via the SPI or M_BUS protocol. The masked ROM fonts are fixed and located from number $08 to $7F. See Figure 9 for details.

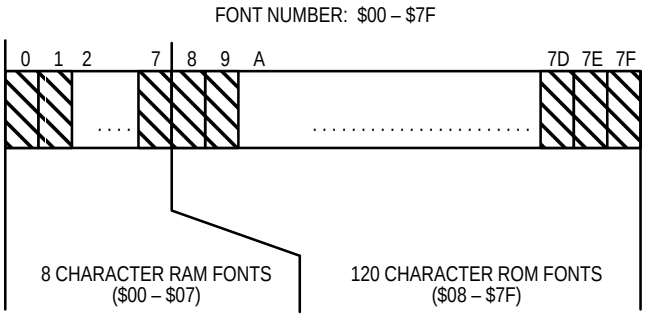
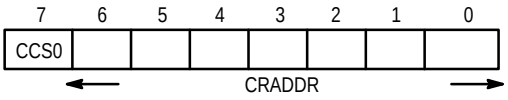


Figure 9. Arrangement of Character RAM/ROM Fonts

REGISTERS

Display Register

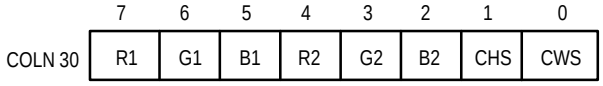


Bit 7 CCS0 — This bit defines a specific character color out of the two preset colors. Color 1 is selected if this bit is cleared, and Color 2 otherwise.

Bit 6–0 CRADDR — These seven bits address the 128 characters or symbols residing in the character ROM.

Row Control Registers

Coln 30

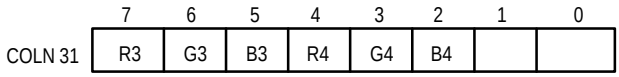


Bits 7–2 — Color 1 is determined by R1, G1, and B1; Color 2 by R2, G2, and B2.

Bit 1 CHS — This bit determines the height of a display symbol. When it is set, the symbol is displayed in double height.

Bit 0 CWS — Bit 0 is similar to Bit 1; when this bit is set, the character is displayed in double width.

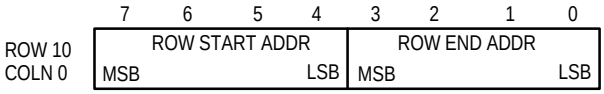
Coln 31



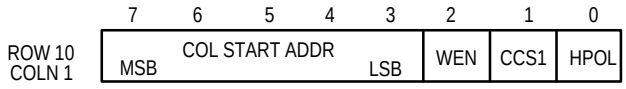
Bits 7–2 — Color 3 is determined by R3, G3, and B3; Color 4 by R4, G4, and B4.

Window 1 Registers

Row 10 Coln 0



Row 10 Coln 1

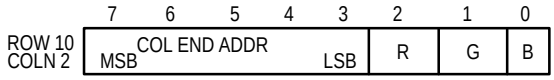


Bit 2 WEN — This bit enables the background Window 1 generation when it is set.

Bit 1 CCS1 — This additional color select bit provides the characters residing within Window 1 with two extra color selections, making a total of four selections for that row.

Bit 0 HPOL — This bit selects the polarity of the incoming horizontal sync signal (HFLB) on Pin 5. If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power–on, this bit is cleared.

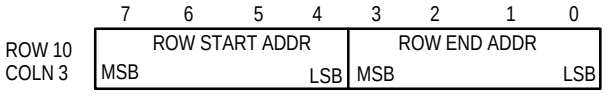
Row 10 Coln 2



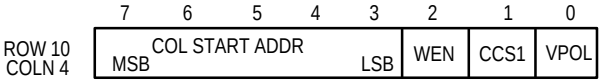
Bits 2–0 R, G and B — These bits control the color of Window 1. Window 1 occupies Columns 0–2 of Row 10; Window 2 occupies Columns 3–5; and Window 3 occupies Columns 6–8. Window 1 has the highest priority, and Window 3 the least. If window overlapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 10 Coln 3



Row 10 Coln 4

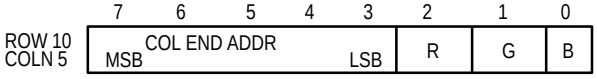


Bit 2 WEN — This bit enables the background Window 2 generation when it is set.

Bit 1 CCS1 — This additional color select bit provides the characters residing within Window 2 with two extra color selections, making a total of four selections for that row.

Bit 0 VPOL — This bit selects the polarity of the incoming vertical sync signal (VFLB) on Pin 5. If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power–on, this bit is cleared.

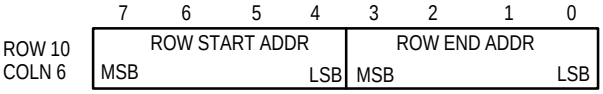
Row 10 Coln 5



Bit 2–0 R, G and B — These bits control the color of Window 2. Window 1 occupies Columns 0–2 of Row 10; Window 2 occupies Columns 3–5; and Window 3 occupies Columns 6–8. Window 1 has the highest priority, and Window 3 the least. If window overlapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 10 Coln 6



Row 10 Coln 7

	7	6	5	4	3	2	1	0
ROW 10 COLN 7	COL START ADDR MSB				LSB	WEN	CCS1	PWMCK_EN

Bit 2 WEN — This bit enables the background Window 3 generation when it is set.

Bit 1 CCS1 — This additional color select bit provides the characters residing within Window 3 with two extra color selections, making a total of four selections for that row.

Bit 0 PWMCK_EN — When this bit is set to 1, the HTONE/PWMCK pin will be switched to a clock output which is synchronous to the H sync and used as an external PWM (pulse width modulation) clock source. Refer to the pin description of HTONE/PWMCK for more information. After power–on, the default value is 0.

Row 10 Coln 8

	7	6	5	4	3	2	1	0
ROW 10 COLN 8	COL END ADDR MSB				LSB	R	G	B

Bit 2–0 R, G and B — These bits control the color of Window 3. Window 1 occupies Columns 0–2 of Row 10; Window 2 occupies Columns 3–5; and Window 3 occupies 6–8. Window 1 has the highest priority, and Window 3 the least. If window overlapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Frame Control Registers

Frame Control Register Row 10 Coln 9

	7	6	5	4	3	2	1	0
COLN 9	VERTD MSB							LSB

Bit 7–0 VERTD — These eight bits define the vertical starting position. There are a total of 256 steps, with an increment of four horizontal lines per step for each field. The value cannot be zero anytime, and the default value is 4.

Frame Control Register Row 10 Coln 10

	7	6	5	4	3	2	1	0
COLN 10	TB	HORD MSB						LSB

Bit 7 TB — Reserved test bit.

Bit 6–0 HORD — These bits define the horizontal starting position for character display. Seven bits give a total of 96 steps and each increment represents a five–dot shift to the right on the monitor screen. The value cannot be zero anytime, and the default value is 10.

Frame Control Register Row 10 Coln 11

	7	6	5	4	3	2	1	0
COLN 11	TB	TB	CH5	CH4	CH3	CH2	CH1	CH0

Bit 7 TB — Reserved test bit.

Bit 6 TB — Reserved test bit.

Bit 5–0 CH5–CH0 — These six bits determine the displayed character height. It is possible to have a proper character height by setting a value greater than or equal to 16 on a different horizontal frequency monitor. Setting a value below 16 will not have a predictable result. Figure 10 illustrates how this chip expands the built–in character font to the desired height.

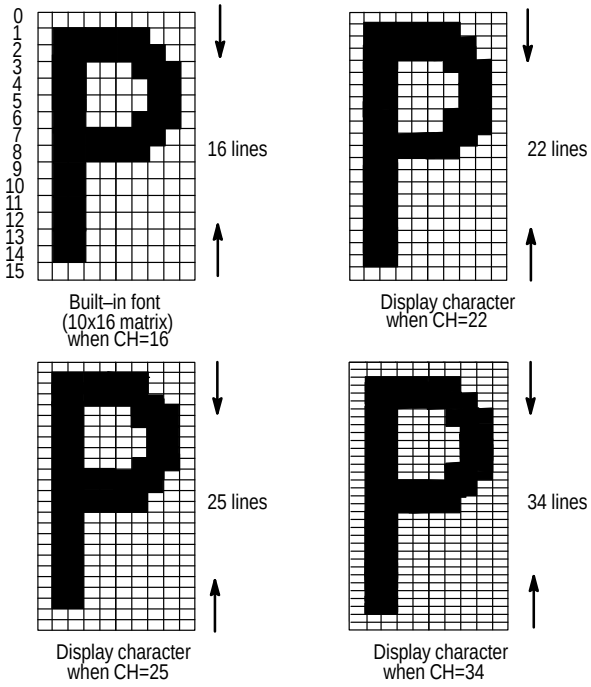


Figure 10. Variable Character Height

Frame Control Register Row 10 Coln 12

	7	6	5	4	3	2	1	0
COLN 12	OSD_EN	BSEN	SHADOW	TB	X32B	TB		FBKGC

Bit 7 OSD_EN — The OSD circuit is activated when this bit is set.

Bit 6 BSEN — This bit enables the character bordering or shadowing function when it is set.

Bit 5 SHADOW — Characters with black–edge shadowing are selected if this bit is set; otherwise bordering prevails.

Bit 4 TB — Reserved test bit.

Bit 3 X32B — This bit determines the number of dots per horizontal line. There are 320 dots per horizontal line if Bit X32B is clear, which is also the default power–on state. Otherwise, 480 dots per horizontal sync line is chosen when Bit X32B is set to 1. Refer to Table 2 for details.

Bit 2 TB — Reserved test bit.

Bit 1 TB — Reserved test bit.

Bit 0 FBKGC — Bit 0 determines the configuration of the FBKG output pin. When it is clear, the FBKG pin outputs high while displaying characters or windows; otherwise, the FBKG pin outputs high only while displaying characters.

Table 2. Resolution Setting

Register Setting (32B)	0	1
Dot Number per H Sync Line	320	480

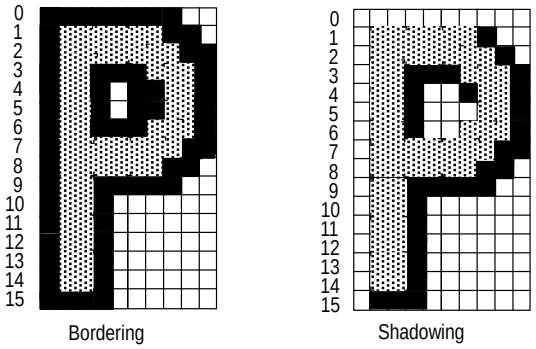


Figure 11. Character Bordering and Shadowing

Frame Format and Timing

Figure 12 illustrates the positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area outside the “safe viewing area” for the display characters. Notice that there are two components in the equations stated in Figure 12 for horizontal and vertical delays: fixed delays from the leading edge of HFLB and VFLB signals, regardless of the values of HORD and VERTD (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; and variable delays determined by the values of HORD and VERTD. Refer to **Frame Control Registers Coln 9 and 10** for the definitions of VERTD and HORD.

Phase detection pulse width is a function of the external charge–up resistor, which is the 330 kΩ resistor in a series with 2 kΩ to VCO pin in the Application Diagram. Dot frequency is determined by the equation *H freq x 320* if Bit X32B is clear, and *H freq x 480* if Bit X32B is set to 1 and Bit X64 is 0. For example, dot frequency is 10.24 MHz if H freq is 32 kHz while Bit X32B is 0. If Bit X32B is 1 and Bit X64 is 0, the dot frequency will be 15.36 MHz (one and a half of the original one).

When double character width is selected for a row, only the even–numbered characters will be displayed, as shown in Row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configuring each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of VFLB of the next frame, to avoid wrapping display characters of the last few rows in the current frame into the next frame. The number of display dots in a horizontal scan line is always fixed at 240, regardless of row character width and the setting of Bit X32B.

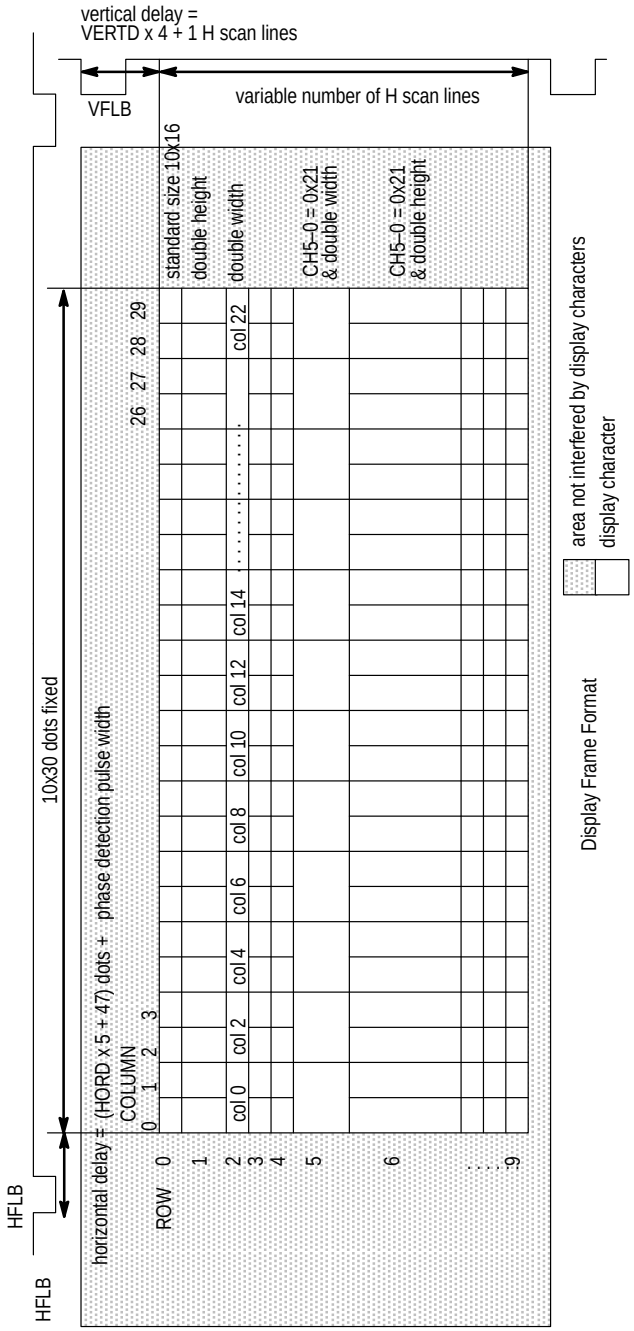


Figure 12. Display Frame Format

Although there are 24 character display registers that can be programmed for each row, not every programmed character can be shown on the screen in 320–dot resolution. Usually only 24 characters can be shown in this resolution at most. This is induced by the time that is required to retrace the H scan line. At 480–dot resolution, a total of 24 characters can be displayed on the screen if the horizontal delay register is set properly.

Figure 13 illustrates the timing of all output signals as a function of window and fast–blanking features. Line 3 of all three characters is used to illustrate the timing signals. The shaded area depicts the window area. The characters on the left and right appear identical except for the FBKGC bit. The middle character does not have a window as its background. Notice that signal HTONE/PWMCK is active only in the window area. Timing of the signal FBKG depends on the configuration of the FBKGC bit. The configuration of the FBKGC bit affects only the FBKG signal timing; it has no effect on the timing of HTONE/PWMCK. Waveform ‘R, G, or B’, which is the actual waveform at R, G, or B pin, is the logical OR of waveform ‘character R, G, or B’ and waveform ‘window R, G, or B’. ‘Character R, G, or B’ and ‘window R, G, or B’ are internal signals for illustration purpose only. Also notice that HTONE/PWMCK has exactly the same waveform as ‘window R, G, or B’.

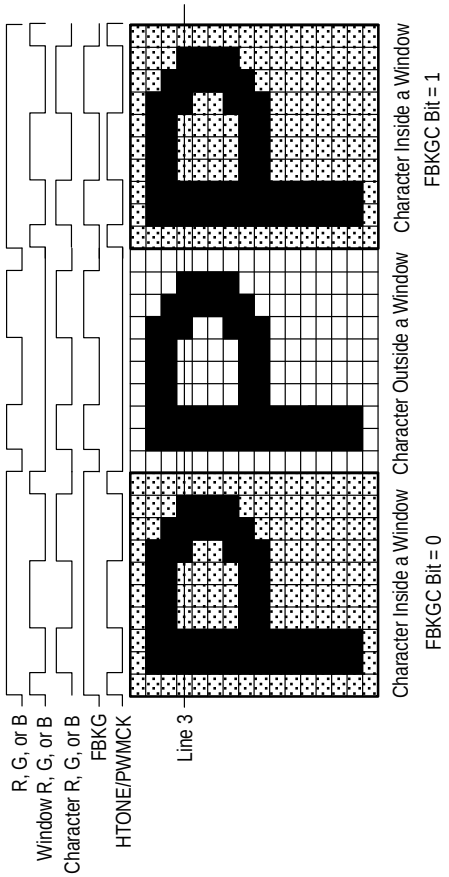


Figure 13. Timing of Output Signals as a Function of Window and FBKGC Bit Features

FONT

Icon Combination

MC141541 contains 120–character ROM and eight RAM. The user can create an on–screen menu based on those characters and programmable RAM. Refer to Table 3 for icon combinations.

Table 3. Combination Map

ICON	ROM ADDRESS (HEX)
Volume Bar I	48, 49, 57
Volume Bar II	47
Size	4F, 50
Position	51, 52
Geometry	53, 54, 55, 56
Contrast	58,59
Brightness	5A, 5B
Horizontal Position	5C, 5D
Horizontal Sizing	5E, 5F
Vertical Position	60, 61
Vertical Sizing	62, 63
Pin Cushion	64, 65
Deguassing	66, 67
Trapezoid	6C, 6D, 6E, 6F
Parallelogram	68, 69, 6A, 6B
Color Select	70, 71
Video Level	72, 73
Input Select	74, 75
Recall	76,77
Save	78, 79
Left/Right Arrows	7A, 7B
INC/DEC sign	7C, 7D
Speaker	7E, 7F

ROM CONTENT

Figures 14 – 17 show the ROM content of MC141541.

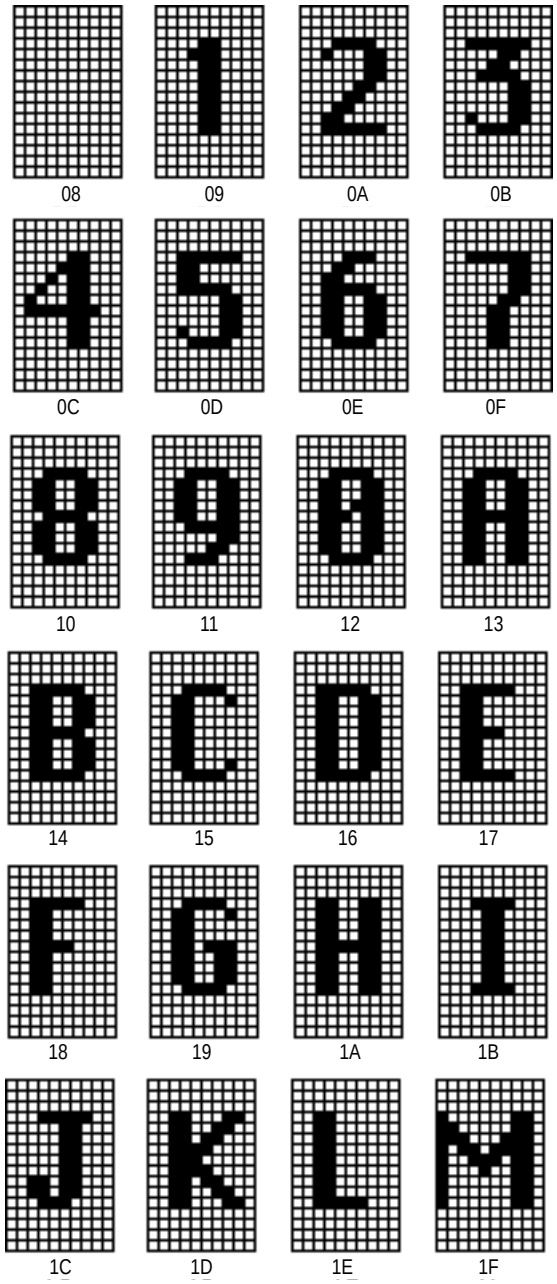


Figure 14. ROM Address ($08 – $1F)

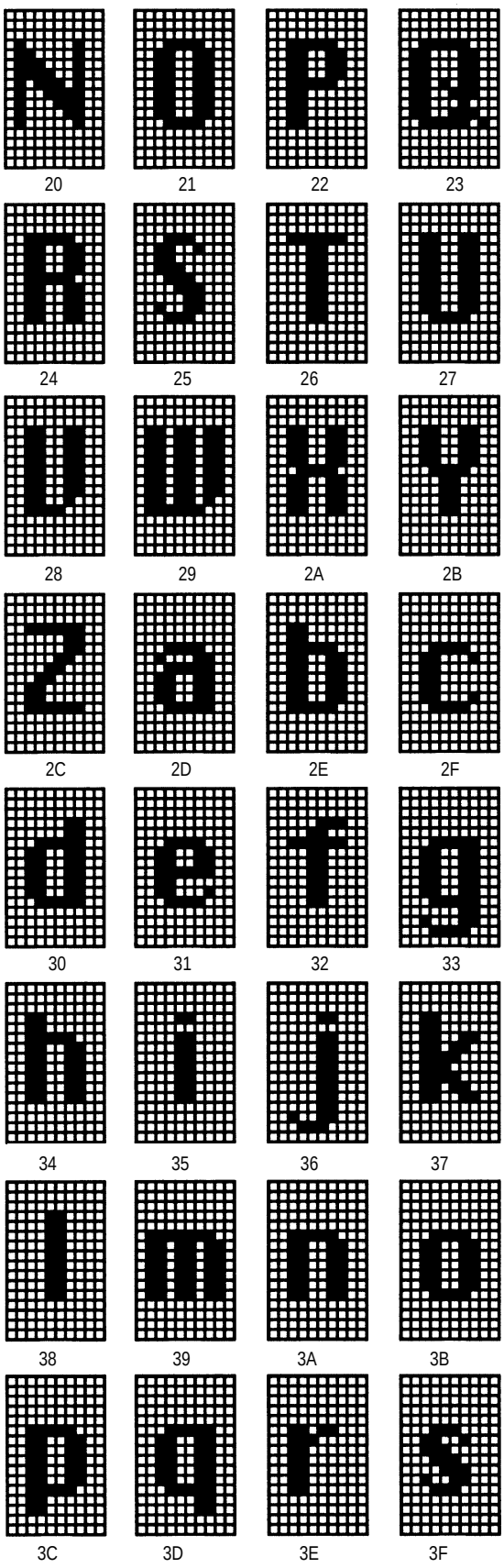


Figure 15. ROM Address ($20 – $3F)

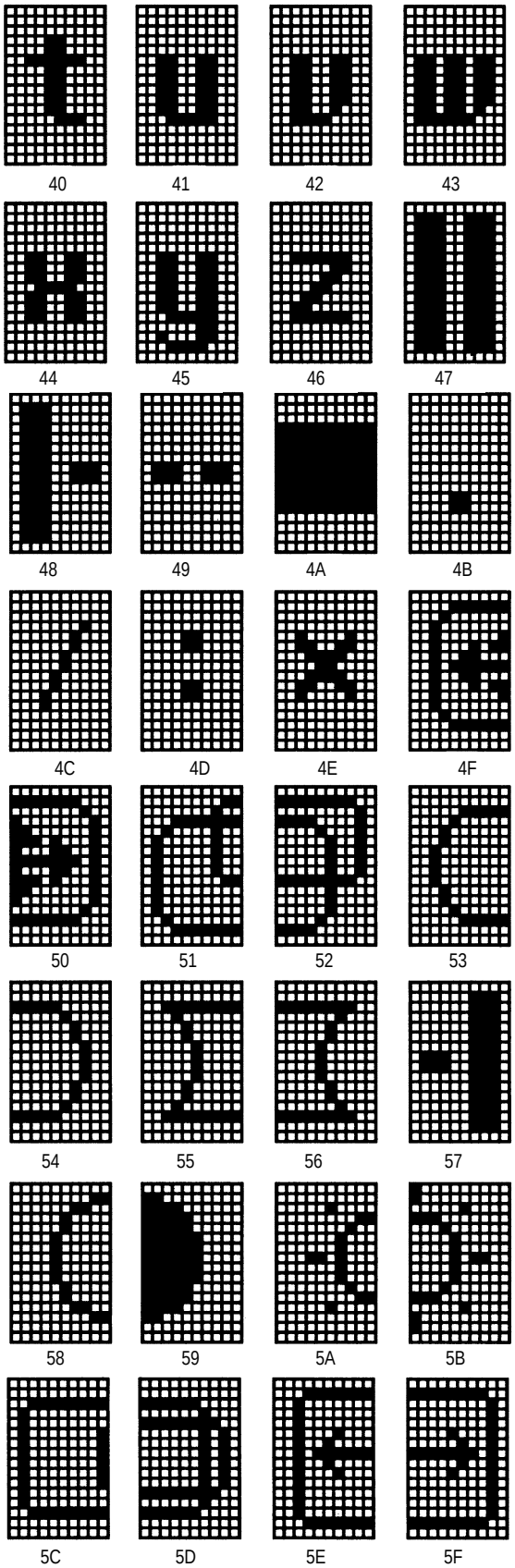


Figure 16. ROM Address ($40 – $5F)

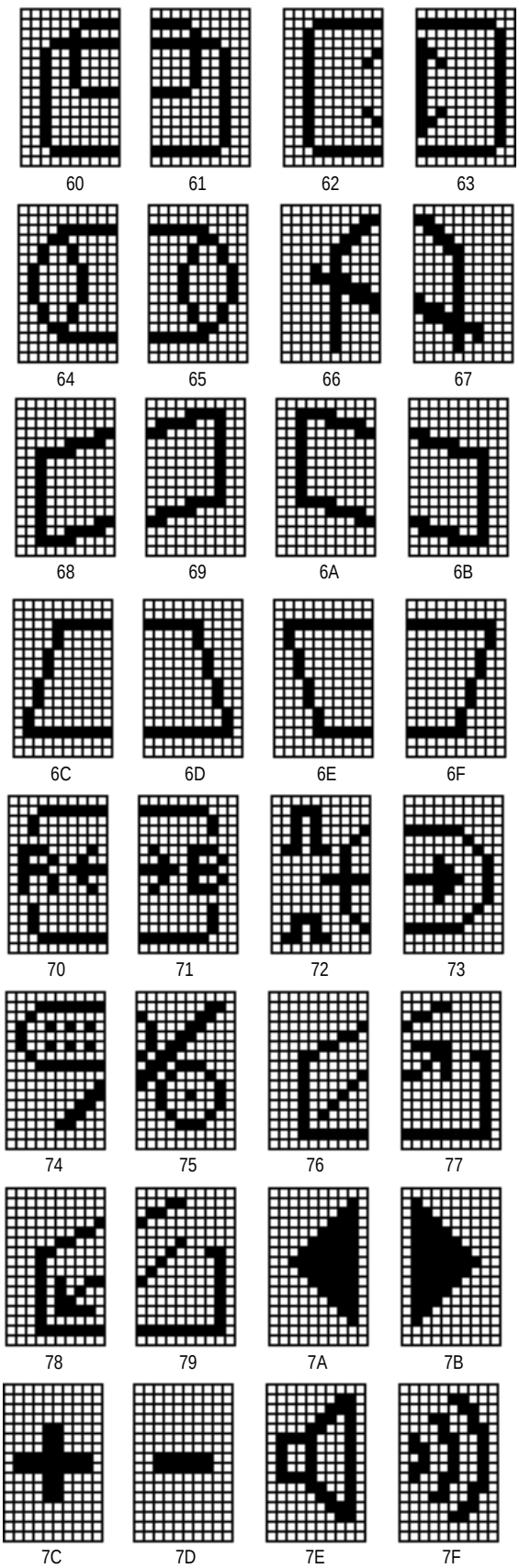


Figure 17. ROM Address ($60 – $7F)

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141541P has a built–in PLL for multi–system application. Pin 2 voltage is dc–based for the internal VCO in the PLL. When the input frequency (HFLB) to Pin 5 increases, the VCO frequency will increase accordingly. This forces the PLL to a higher locked frequency output. The frequency should be equal to 320/480 x HFLB (depending on resolution).This is the pixel dot clock.

Display distortion is caused by noise on Pin 2. Positive noise increases the VCO frequency above normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side of the display window.

In order to have distortion–free display, the following recommendations should be considered:

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should be connected to PCB common ground. The $V_{SS(A)}$ and V_{SS} grounds should be totally separated (i.e. $V_{SS(A)}$ is floating). Refer to the Application Diagram for the ground connections.
- The dc supply path for Pin 9 (V_{DD}) should be separated from other switching devices.
- The LC filter should be connected between Pin 9 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.
- Two small capacitors can be connected between Pins 2 and 3, and between Pins 3 and 4.

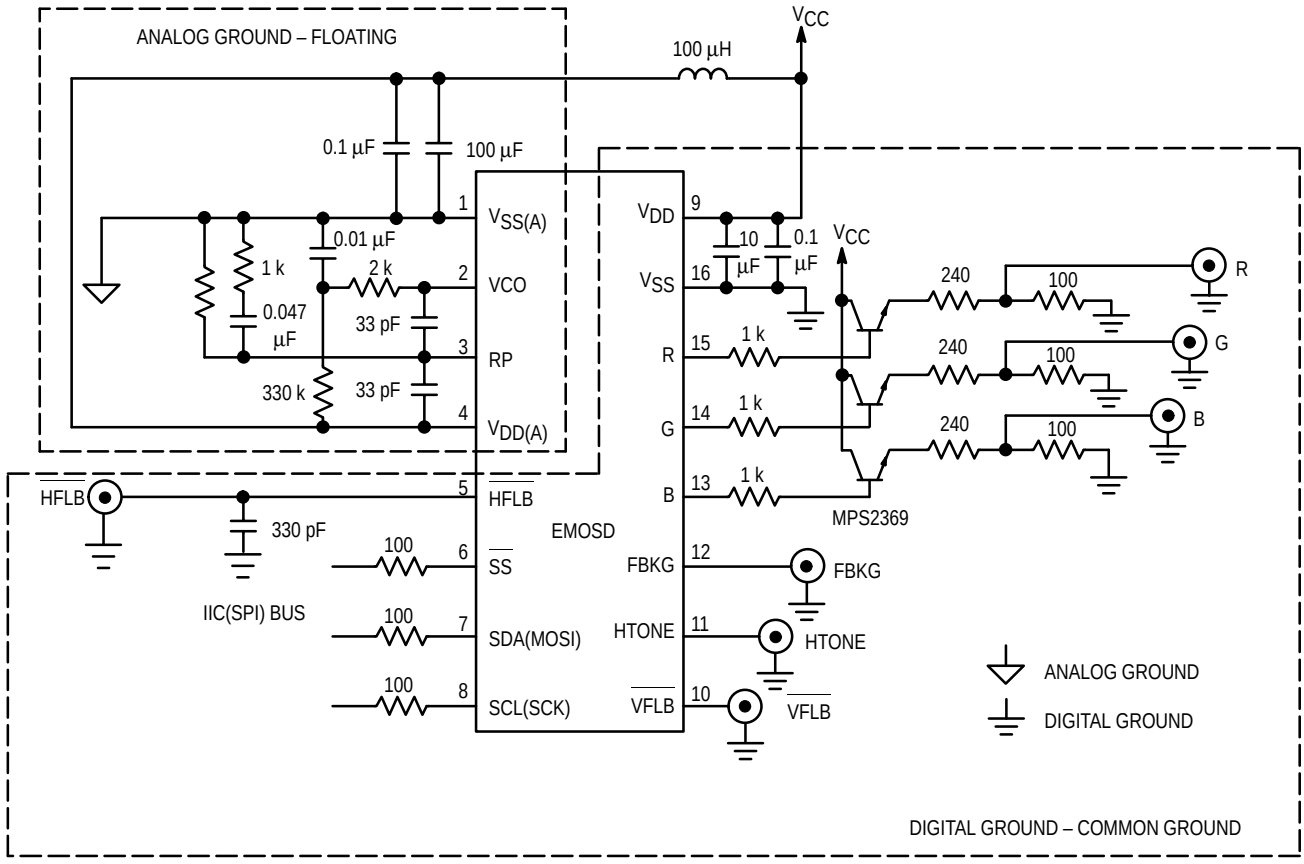
Jittering

Most display jittering is caused by HFLB jittering on Pin 5. Care must be taken if the HFLB signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. A small capacitor can be added between Pin 5 and Pin 16 to smooth the signal. Refer to the value used in the Application Diagram.

Display Dancing

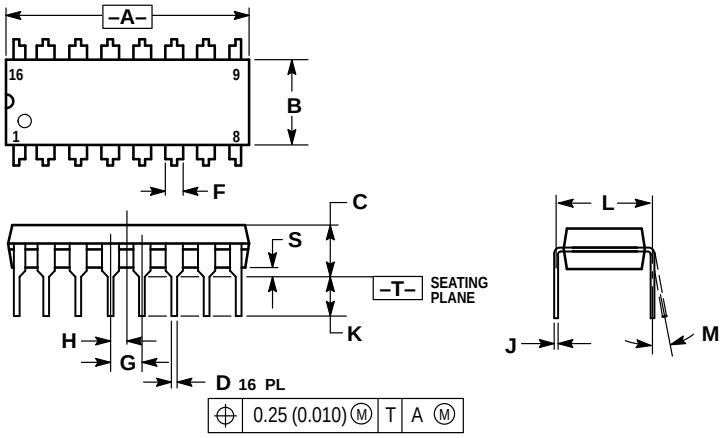
Most display dancing is caused by interference of the serial bus. It can be avoided by adding series resistors to the serial bus.

APPLICATION DIAGRAM



PACKAGE DIMENSIONS

P SUFFIX
PLASTIC DIP
CASE 648–08



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

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