

## 16-SEGMENT X 14-Digit VFD CONTROLLER / DRIVER

### ■ GENERAL DESCRIPTION

The NJU3426 is a VFD (Vacuum Fluorescent Display) controller/driver to dynamically drive up to 16 segments x 14 digits. It consists of display data RAM, an address counter, command registers, a serial interface and high voltage drivers. The NJU3426 features the direct connection to MPU and the high voltage drivers of 45V well-suited for various VFD displays.

### ■ PACKAGE OUTLINE

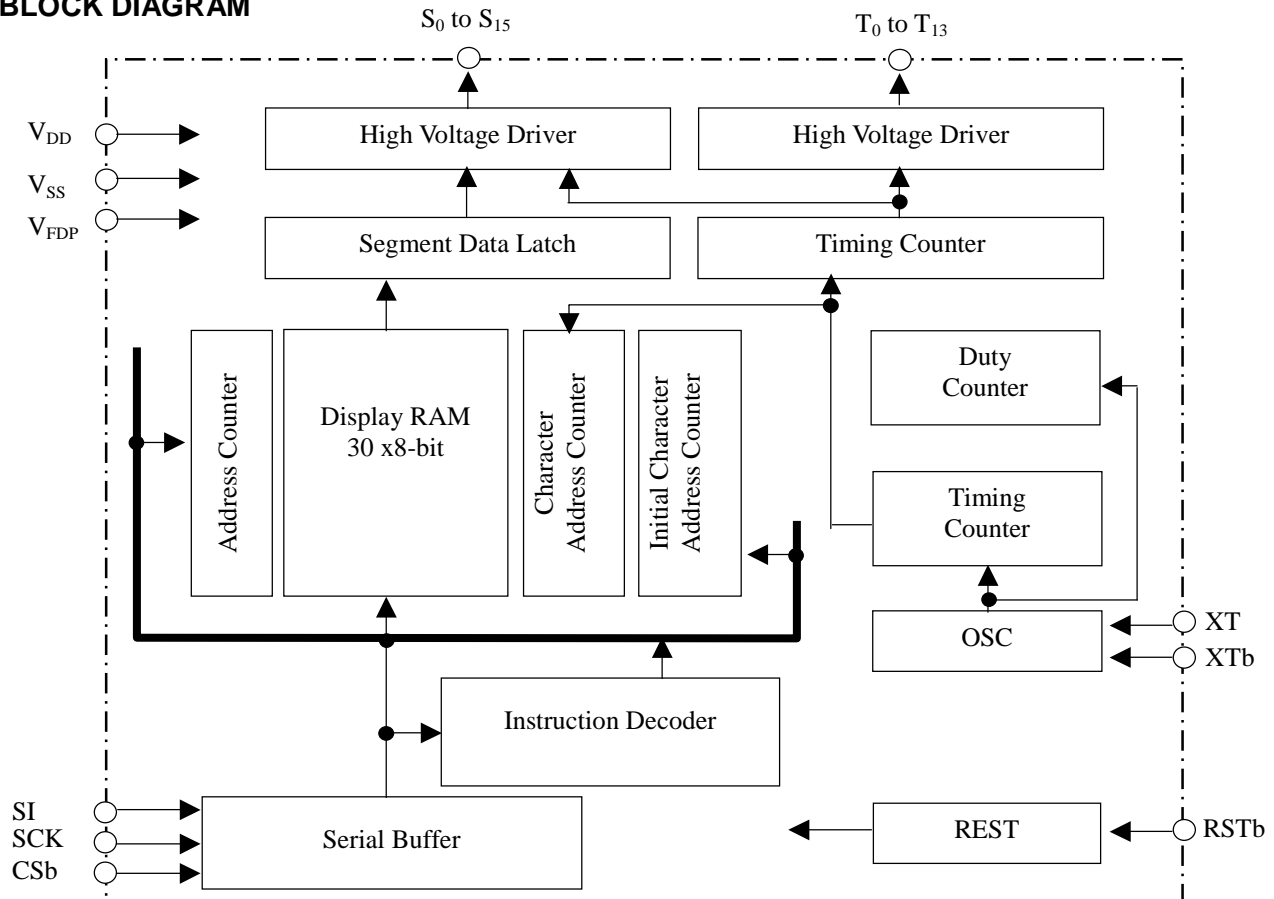


**NJU3426FP1**

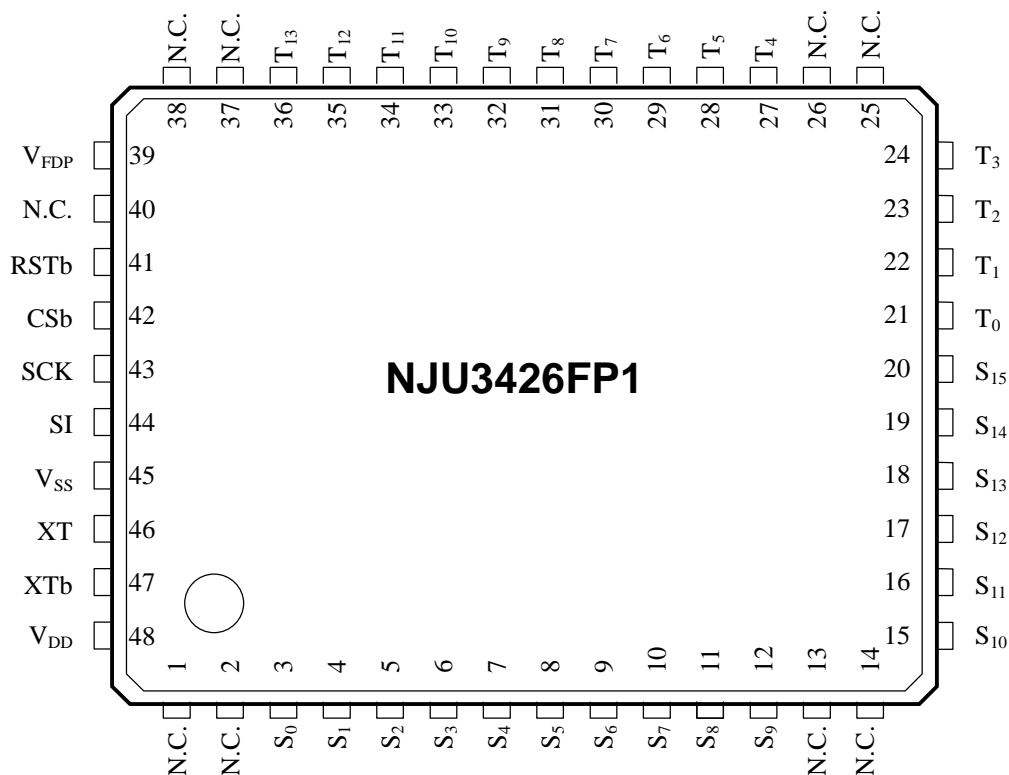
### ■ FEATURES

- Directly Drives 16-segment x 14-digit
- High VFD Driving Voltage :  $|V_{DD}-V_{FDP}| \leq 45V$
- Display Shift Function
- Programmable Duty Ratio for Timing Signal  
: 2/16, 4/16, 6/16, 8/16, 10/16, 12/16, 14/16, 15/16 duty
- Display ON/OFF Control Function
- Display Data RAM : 30 x 8-bit
- Built-in Oscillator (External Ceramic Resonator or External Resistor or External Clock)
- 8-bit Serial Interface
- Power-ON Reset Function
- Operating Voltage : 3.3V / 5.0V
- C-MOS Technology
- Package Outline : QFP48-P1

### ■ BLOCK DIAGRAM



## ■ PIN CONFIGURATION



## ■ TERMINAL DISCRPTION

| PAD No.                                | SYMBOL                            | FUNCTION   |
|--|-----------------------------------|--|
| 48                                     | V <sub>DD</sub>                   | Power Supply For Logic Voltage<br>3.3V / 5.0V  |
| 45                                     | V <sub>SS</sub>                   | Ground<br>V <sub>SS</sub> =0V  |
| 39                                     | V <sub>FDP</sub>                  | Power Supply For VFD Driving Voltage   |
| 46<br>47                               | XT<br>XTb                         | Ceramic Resonator Connection, Resistor Connection, or External Clock Input<br>The internal oscillator is formed by connecting an external ceramic resonator to these pins. When an external oscillator is used instead of the internal oscillator, the external clock is input to the XT and the XTb must be open. |
| 3 to 12,<br>15 to 20                   | S <sub>0</sub> to S <sub>15</sub> | Segment output terminals (Pulled down)   |
| 21 to 24,<br>27 to 36                  | T <sub>0</sub> to T <sub>13</sub> | Timing output terminals (Pulled down)  |
| 41                                     | RSTb                              | Reset terminal (Pulled up)<br>Active "L": Reset is executed when this pin is "L".<br>Reset does not change the contents of display data RAM.   |
| 42                                     | CSb                               | Chip Select<br>Active "L": Data transmission is enable when this pin is "L".   |
| 43                                     | SCK                               | Serial Clock Input   |
| 44                                     | SI                                | Serial Data Input (8 bits = 1 word)  |
| 1, 2, 13,<br>14, 25, 26,<br>37, 38, 40 | N.C.                              | Non connections<br>These pins must be open.  |

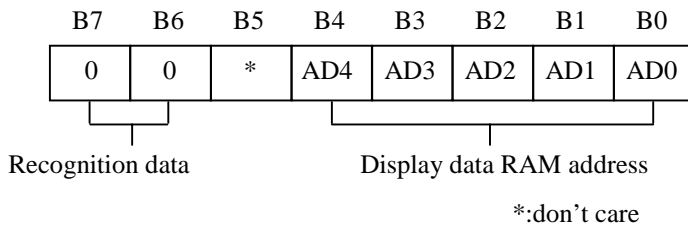
## ■ FUNCTION DESCRIPTION

### (1) ADDRESS COUNTER

The address counter specifies the “Display data RAM address”, and the display data is transferred to or from this address. For the data transmission, once an initial RAM address is determined, the display data can be continuously transmitted without setting the RAM address. When the upper 2 bits (B7 and B6) of the 1st word are “0,0”, the lower 5 bits (B4 to B0) are interpreted as RAM address data. And the 2nd word is interpreted as display data which is stored in the RAM address specified by the 1st word, and simultaneously the RAM address is counted up.

Although the “Display data RAM address” can be set only in the range of “0,0,0,0,0” (00<sub>H</sub>) and “1,1,1,0,1” (1D<sub>H</sub>), the auto-increment keeps counting up to “1,1,1,1,1” (1F<sub>H</sub>), and the RAM address finally wraps to “0,0,0,0,0” (00<sub>H</sub>) then begins counting up. Note that the display data, specified to the RAM address of “1,1,1,1,0” (1E<sub>H</sub>) or “1,1,1,1,1” (1F<sub>H</sub>), is ignored in this sequence.

### DISPLAY DATA RAM ADDRESS



| Character address | B7 B6 B5 B4 B3 B2 B1 B0 |  |  |  |  |  |  |  | RAM Address | B7 B6 B5 B4 B3 B2 B1 B0 |                 |                 |                 |                 |                 |                 |                | RAM Address    |                 |
|-------------------|-------------------------|--|--|--|--|--|--|--|-------------|-------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|-----------------|
|                   |                         |  |  |  |  |  |  |  |             |                         |                 |                 |                 |                 |                 |                 |                |                |                 |
|                   | C <sub>0</sub>          |  |  |  |  |  |  |  |             | 01 <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 00 <sub>H</sub> |
| T <sub>0</sub>    | C <sub>1</sub>          |  |  |  |  |  |  |  |             | 03 <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 02 <sub>H</sub> |
| T <sub>1</sub>    | C <sub>2</sub>          |  |  |  |  |  |  |  |             | 05 <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 04 <sub>H</sub> |
| T <sub>2</sub>    | C <sub>3</sub>          |  |  |  |  |  |  |  |             | 07 <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 06 <sub>H</sub> |
| T <sub>3</sub>    | C <sub>4</sub>          |  |  |  |  |  |  |  |             | 09 <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 08 <sub>H</sub> |
| T <sub>4</sub>    | C <sub>5</sub>          |  |  |  |  |  |  |  |             | 0B <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 0A <sub>H</sub> |
| T <sub>5</sub>    | C <sub>6</sub>          |  |  |  |  |  |  |  |             | 0D <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 0C <sub>H</sub> |
| T <sub>6</sub>    | C <sub>7</sub>          |  |  |  |  |  |  |  |             | 0F <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 0E <sub>H</sub> |
| T <sub>7</sub>    | C <sub>8</sub>          |  |  |  |  |  |  |  |             | 11 <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 10 <sub>H</sub> |
| T <sub>8</sub>    | C <sub>9</sub>          |  |  |  |  |  |  |  |             | 13 <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 12 <sub>H</sub> |
| T <sub>9</sub>    | C <sub>10</sub>         |  |  |  |  |  |  |  |             | 15 <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 14 <sub>H</sub> |
| T <sub>10</sub>   | C <sub>11</sub>         |  |  |  |  |  |  |  |             | 17 <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 16 <sub>H</sub> |
| T <sub>11</sub>   | C <sub>12</sub>         |  |  |  |  |  |  |  |             | 19 <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 18 <sub>H</sub> |
| T <sub>12</sub>   | C <sub>13</sub>         |  |  |  |  |  |  |  |             | 1B <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 1A <sub>H</sub> |
| T <sub>13</sub>   | C <sub>14</sub>         |  |  |  |  |  |  |  |             | 1D <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 1C <sub>H</sub> |
|                   |                         |  |  |  |  |  |  |  |             | 1F <sub>H</sub>         |                 |                 |                 |                 |                 |                 |                |                | 1E <sub>H</sub> |
|                   |                         |  |  |  |  |  |  |  |             |                         | S <sub>15</sub> | S <sub>14</sub> | S <sub>13</sub> | S <sub>12</sub> | S <sub>11</sub> | S <sub>10</sub> | S <sub>9</sub> | S <sub>8</sub> |                 |
|                   |                         |  |  |  |  |  |  |  |             |                         |                 |                 |                 |                 |                 |                 |                |                |                 |

☒ : Non-existent Address

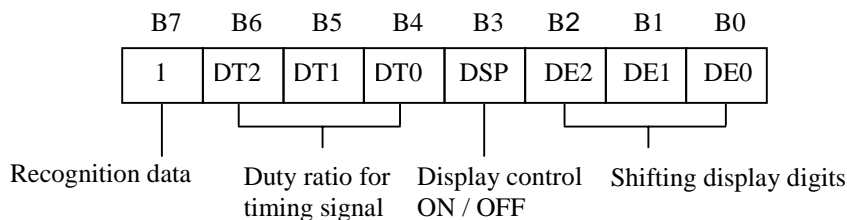
### DISPLAY DATA RAM MAP

## (2) COMMAND REGISTER 1

The “Command register 1” is used for setting “Duty ratio for timing signal”, “Display control ON/OFF” and “Shifting display digits”. When the upper 1 bit (B7) of the 1<sup>st</sup> word is “1”, the lower 7 bits (B6 to B0) are interpreted as command data, and stored in the “Command register 1”. The contents of the “Command register 1” are initialized to the default values by the power-ON reset or the reset signal, as shown below.

### DEFAULT VALUES OF COMMAND REGISTER 1

- Duty ratio for timing signal : 2/16
- Display control ON/OFF : OFF
- Shifting display digits : 7



| DT2 | DT1 | DT0 | Duty ratio for timing signal |
|-----|-----|-----|------------------------------|
| 0   | 0   | 0   | 2/16                         |
| 0   | 0   | 1   | 4/16                         |
| 0   | 1   | 0   | 6/16                         |
| 0   | 1   | 1   | 8/16                         |
| 1   | 0   | 0   | 10/16                        |
| 1   | 0   | 1   | 12/16                        |
| 1   | 1   | 0   | 14/16                        |
| 1   | 1   | 1   | 15/16                        |

Note.) The output waveforms of timing signal are shown in “**■ TIMING SIGNAL / DUTY-CHANGE WAVEFORM**”.

| DSP | Display control |
|-----|-----------------|
| 0   | OFF             |
| 1   | ON              |

Note.) When the “Display control OFF” is set, segment drivers output waveforms but all timing signal outputs are halted

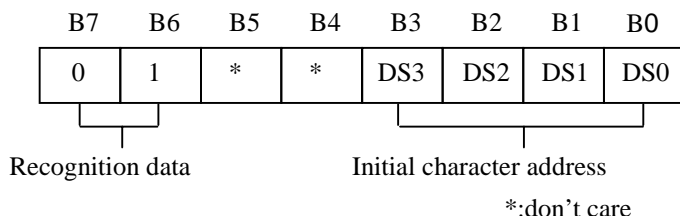
| DE2 | DE1 | DE0 | Shifting display digits |
|-----|-----|-----|-------------------------|
| 0   | 0   | 0   | 7                       |
| 0   | 0   | 1   | 8                       |
| 0   | 1   | 0   | 9                       |
| 0   | 1   | 1   | 10                      |
| 1   | 0   | 0   | 11                      |
| 1   | 0   | 1   | 12                      |
| 1   | 1   | 0   | 13                      |
| 1   | 1   | 1   | 14                      |

### (3) COMMAND REGISTER 2

The “Command register 2” is used for setting the “Initial character address”, which corresponds to the T<sub>0</sub> pin. When the upper 2 bits (B7 and B6) of the 1<sup>st</sup> word is “0,1”, the lower 4 bits (B3 to B0) are interpreted as command data and stored in the “Command register 2”. The contents of the “Command register 2” are initialized to the default values by the power-ON reset or the reset signal, as shown below.

#### DEFAULT VALUES OF COMMAND REGISTER 2

- Initial character address : C1 (0,0,0,1)



| DS3 | DS2 | DS1 | DS0 | Initial character address |
|-----|-----|-----|-----|---------------------------|
| 0   | 0   | 0   | 0   | C <sub>0</sub>            |
| 0   | 0   | 0   | 1   | C <sub>1</sub>            |
| 0   | 0   | 1   | 0   | C <sub>2</sub>            |
| 0   | 0   | 1   | 1   | C <sub>3</sub>            |
| 0   | 1   | 0   | 0   | C <sub>4</sub>            |
| 0   | 1   | 0   | 1   | C <sub>5</sub>            |
| 0   | 1   | 1   | 0   | C <sub>6</sub>            |
| 0   | 1   | 1   | 1   | C <sub>7</sub>            |
| 1   | 0   | 0   | 0   | C <sub>8</sub>            |
| 1   | 0   | 0   | 1   | C <sub>9</sub>            |
| 1   | 0   | 1   | 0   | C <sub>10</sub>           |
| 1   | 0   | 1   | 1   | C <sub>11</sub>           |
| 1   | 1   | 0   | 0   | C <sub>12</sub>           |
| 1   | 1   | 0   | 1   | C <sub>13</sub>           |
| 1   | 1   | 1   | 0   | C <sub>14</sub>           |
| 1   | 1   | 1   | 1   | Prohibited                |

## (4) DISPLAY SHIFT OPERATION

The display shift operation is performed by changing the “Initial character address” of the “Command register 2”. And the number of digits for the display shift in the loop is determined by the “Shifting display digits” of the “Command register 1”. In other words, shifting display area ranges from the “Initial character address” specified by the “Command register 2” to the last address specified by the “Command register 1”.

The default value of the “Initial character address” is  $C_1$  (0,0,0,1), as shown in the table of “Display data RAM”. In addition, supposing that the value of the “Shifting display digits” is “N”, the “Initial character address” should be set in the range of  $C_0$  and  $C_N$  in order not to exceed the digit “N”. Because the display shift operation is not applied to the addresses beyond the digit “N”, the display images, which were initially set up, appear on these addresses. Just for reference, one character of display image is composed of 16 segments.

### HOW TO SET LEFT DISPLAY SHIFT

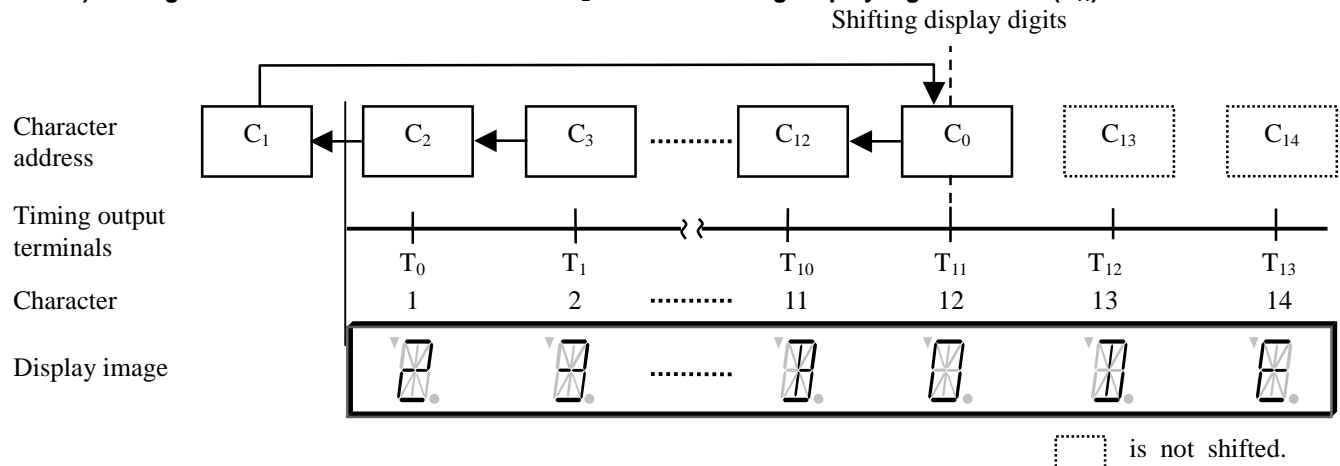
The left display shift is carried out by incrementing the “Initial character address” gradually like  $C_2, C_3, C_4, \dots, C_N$ . To the contrary, decrementing the address performs right display shift. The following description shows the example on how to set the left display shift, using alphanumeric display images such as “0”, “1”, “2”, ..., “9”, “A”, “B”, ..., and “E”.

#### STEP1) Setting display images in the display data RAM

- Display RAM data

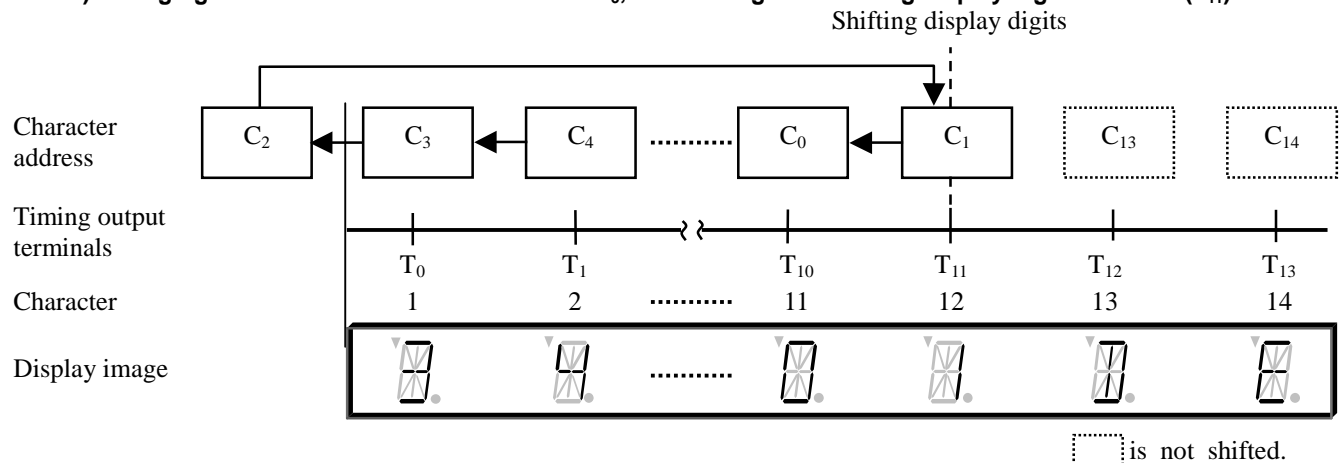
| Character address | $C_0$ | $C_1$ | $C_2$ | $C_3$ | $C_4$ | $C_5$ | $C_6$ | $C_7$ | $C_8$ | $C_9$ | $C_{10}$ | $C_{11}$ | $C_{12}$ | $C_{13}$ | $C_{14}$ |
|-------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|----------|----------|----------|----------|----------|
| Display image     | 0     | 1     | 2     | 3     | 4     | 5     | 6     | 7     | 8     | 9     | A        | B        | C        | D        | E        |

#### STEP2) Setting the “Initial character address” to $C_2$ and the “Shifting display digits N” to 12 ( $T_{11}$ ).

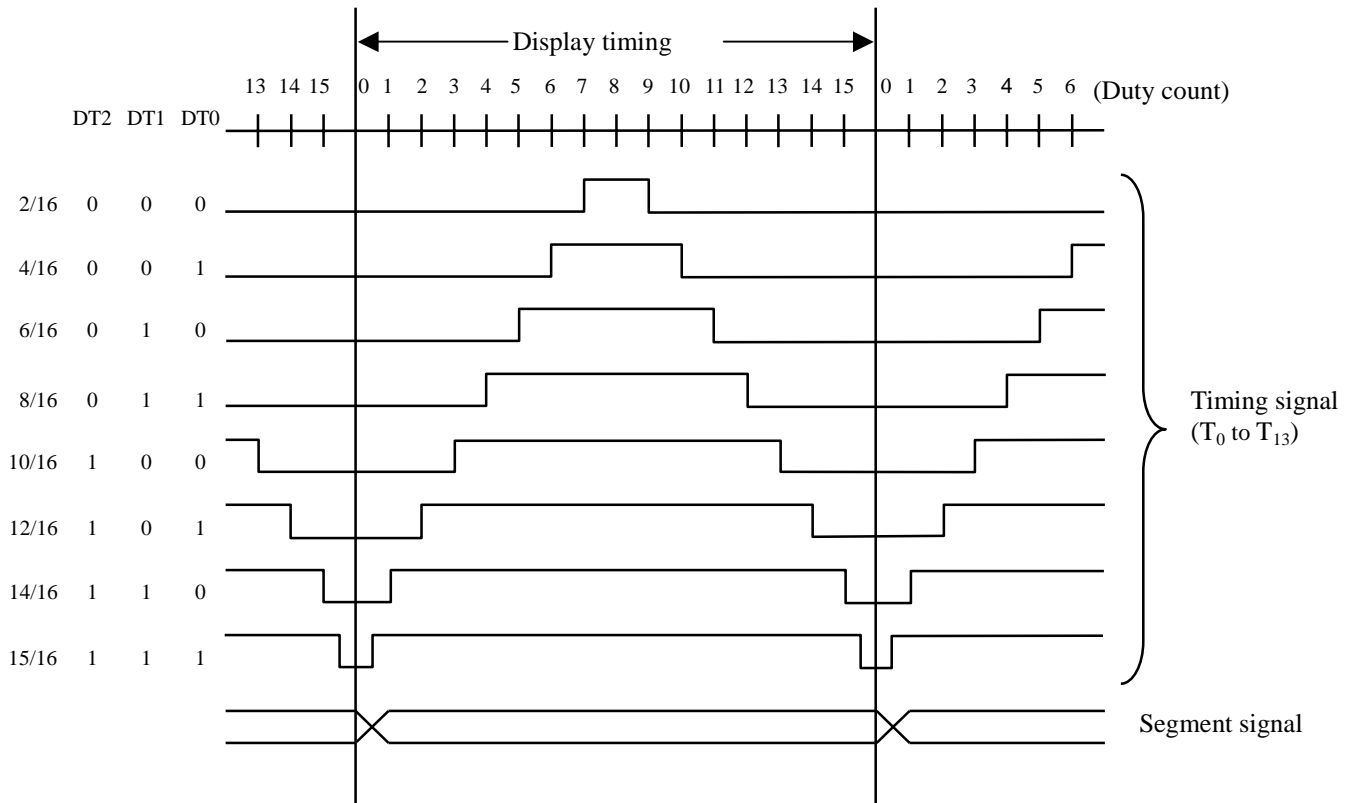


In this setting, the display images of “2”, “3”, ... appear on the  $T_0, T_1, T_2, \dots, T_{10}$  pins respectively, and the image “0” is on the  $T_{11}$  pin, which is assigned to the 12<sup>th</sup> character address. The display images “D” and “E” don’t shift but remain on the  $T_{12}$  and  $T_{13}$  pins, assigned to the 13<sup>th</sup> and 14<sup>th</sup> characters respectively, because their character addresses are outside the digit “N”.

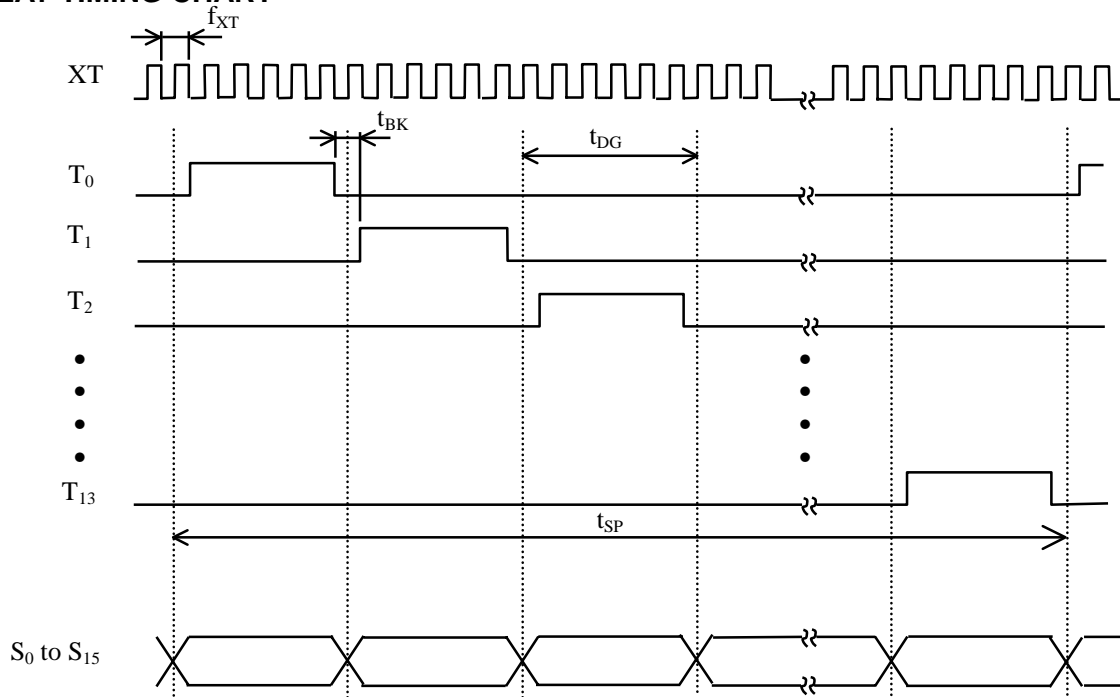
#### STEP3) Changing the “Initial character address” to $C_3$ , and leaving the “Shifting display digits N” as 12 ( $T_{11}$ ).



## ■ TIMING SIGNAL / DUTY-CHANGE WAVEFORM



## ■ DISPLAY TIMING CHART

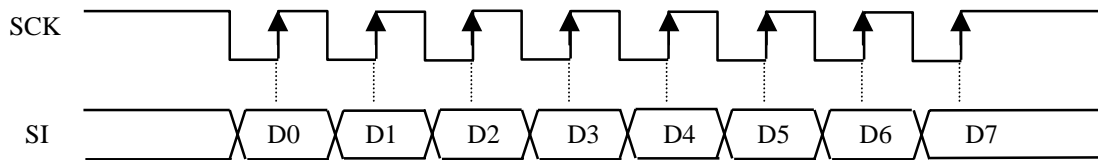


|                                       |  |                                 |
|---------------------------------------|--|---------------------------------|
| Oscillation frequency                 | : $f_{XT}$                                 | : 800kHz to 3.5MHz              |
| Minimum blanking time<br>(duty 15/16) | : $t_{BK} = (1/f_{XT}) \times 16 \times 2$ | : 40 $\mu$ s to 9.14 $\mu$ s    |
| 1-character display time              | : $t_{DG} = t_{BK} \times 16$              | : 640 $\mu$ s to 146.28 $\mu$ s |
| 1-cycle display time                  | : $t_{SP} = t_{DG} \times 14$              | : 8.96ms to 2.05ms              |

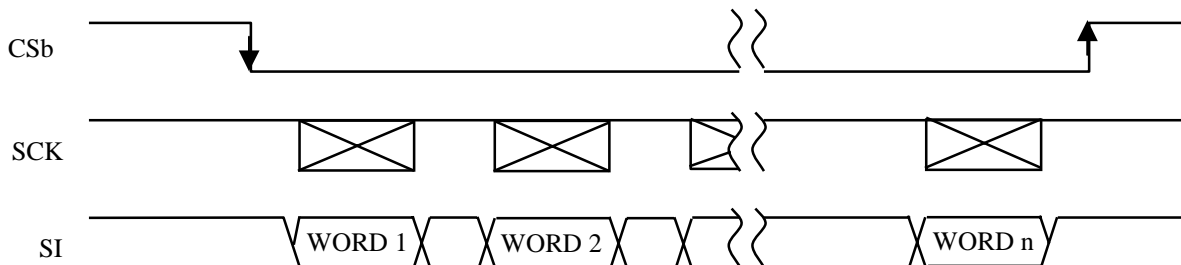
## (5) SERIAL DATA TRANSMISSION

Communication between the **NJU3426** and MPU uses the serial data transmission with synchronous clock, and 8 bits serial data constitutes 1 word. Each bit on the SI pin is latched at the rising edge of the serial clock (SCK), and the entire 8 bits are loaded as 1 word at the rising edge of the chip select (CSb).

During a data transmission, multiple words are transferred continuously. The 1<sup>st</sup> word is either "Display data RAM address", "Command register 1" or "Command register 2". When the 1<sup>st</sup> word is RAM address data, the 2<sup>nd</sup> and ascending words are interpreted as display data. When it's the "Command register 1 or 2", the 2<sup>nd</sup> and ascending words are ignored.



**SERIAL DATA TIMING**



**SERIAL DATA TRANSMISSION FORMAT**

- Serial input data

### DATA FORMAT FOR THE 1<sup>ST</sup> WORD

#### DISPLAY DATA RAM ADDRESS

| B7 | B6 | B5 | B4  | B3  | B2  | B1  | B0  |
|----|----|----|-----|-----|-----|-----|-----|
| 0  | 0  | *  | AD4 | AD3 | AD2 | AD1 | AD0 |

\*:don't care

#### COMMAND DATA 1

| B7 | B6  | B5  | B4  | B3  | B2  | B1  | B0  |
|----|-----|-----|-----|-----|-----|-----|-----|
| 1  | DT2 | DT1 | DT0 | DSP | DE2 | DE1 | DE0 |

\*:don't care

#### COMMAND DATA 2

| B7 | B6 | B5 | B4 | B3  | B2  | B1  | B0  |
|----|----|----|----|-----|-----|-----|-----|
| 0  | 1  | *  | *  | DS3 | DS2 | DS1 | DS0 |

\*:don't care

### SERIAL DATA FOR THE 2<sup>ND</sup> AND ASCENDING WORDS

When the 1<sup>st</sup> word is the "Display data RAM address", the 2<sup>nd</sup> and ascending words are interpreted as display data. When the 1<sup>st</sup> word is the "Command register 1 or 2", the 2<sup>nd</sup> and ascending words are ignored.



## ■ ABSOLUTE MAXIMAM RATINGS

( $V_{SS}=0V$ ,  $T_a=25^{\circ}C$ )

| PARAMETER                  | SYMBOL    | RATINGS                     | UNIT        | CONDITIONS                                |
|----------------------------|-----------|-----------------------------|-------------|---|
| Supply voltage             | $V_{DD}$  | -0.3 to +7.0                | V           |   |
| Input voltage              | $V_{IN}$  | -0.3 to $V_{DD}+0.3$        | V           |   |
| VFD driving voltage        | $V_{FDP}$ | $V_{DD}-45$ to $V_{DD}+0.3$ | V           | Relative to $V_{DD}$ .                    |
| “H” level output current 1 | $I_{OH1}$ | -15                         | mA          | 1 pin out of $S_0$ to $S_{15}$ pins       |
| “H” level output current 2 | $I_{OH2}$ | -35                         | mA          | 1 pin out of $T_0$ to $T_{13}$ pins       |
| “L” level output current   | $I_{OL}$  | 20                          | mA          |   |
| Operating temperature      | $T_{opr}$ | -40 to 85                   | $^{\circ}C$ |   |
| Storage temperature        | $T_{stg}$ | -55 to 125                  | $^{\circ}C$ |   |
| Power dissipation          | PD        | 1500                        | mW          | On two-layer board of based on the JEDEC. |

Note 1): The LSI must be used inside the “Absolute maximum ratings”. Otherwise, an electrical or physical stress may cause a permanent damage to the LSI.

Note 2): De-coupling capacitors should be placed on  $V_{DD}$  and  $V_{SS}$  and  $V_{FDP}$  and  $V_{SS}$  for stable operation.

Note 3): The following voltage relation must be maintained;  $V_{DD} > V_{SS} \geq V_{FDP}$ ,  $V_{SS}=0$ .

## ■ ELECTRICAL CHARACTERISTICS

• DC characteristics 1

( $V_{DD}=5.0V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $85^{\circ}C$ )

| PARAMETER                 | SYMBOL    | CONDITIONS   | MIN                                     | TYP   | MAX          | UNIT       |    |
|---------------------------|-----------|--|---|-------|--------------|------------|----|
| Operating voltage         | $V_{DD}$  | $V_{DD}$ terminal  | 4.5                                     |       | 5.5          | V          |    |
| “H” level input voltage   | $V_{IH}$  | XT, RSTb, CSb, SCK, SI terminals   | 0.8 $V_{DD}$                            |       | 0.2 $V_{DD}$ | V          |    |
| “L” level input voltage   | $V_{IL}$  |  |   |       |              |            |    |
| Input off leak current    | $I_{IZ}$  | CSb, SCK, SI terminals<br>$V_{DD}=5.5V$ , $V_I=0$ or $5.5V$  |   |       | $\pm 1$      | $\mu A$    |    |
| Display output current    | $I_{OH}$  | $S_0$ to $S_{15}$ terminals  | $V_{DD}=4.5V$ ,<br>$V_{FDP}=V_{DD}-40V$ | -4.5  | -9           |            | mA |
|                           |           | $T_0$ to $T_{13}$ terminals  | $V_{OH}=V_{DD}-2.5V$                    | -10.5 | -21          |            | mA |
| Pull-up resistance        | $R_{UR}$  | RSTb terminal, $T_a=25^{\circ}C$ , $V_I=V_{SS}$  | 100                                     |       | 280          | k $\Omega$ |    |
| Pull-down resistance      | $R_{DST}$ | $S_0$ to $S_{15}$ , $T_0$ to $T_{13}$ terminals, $T_a=25^{\circ}C$<br>$V_I=V_{DD}$ , $V_{FDP}=V_{DD}-40V$  | 60                                      |       | 160          | k $\Omega$ |    |
| Logic operating current   | $I_{SS}$  | $V_{SS}$ terminal,<br>All Segment/Timing output terminals open, RSTb terminal open,<br>Ceramic resonator:1MHz,<br>All Segment output OFF and All Timing output OFF |   | 1     | 2            | mA         |    |
| Display operating current | $I_{FDP}$ | $V_{FDP}$ terminal, $V_{FDP}=V_{DD}-40V$ ,<br>Ceramic resonator:1MHz,<br>All Segment/Timing output ON  |   | 10    | 15           | mA         |    |

• AC characteristics 1

( $V_{DD}=5.0V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $85^{\circ}C$ )

| PARAMETER                                    | SYMBOL                | CONDITIONS                           | MIN  | TYP | MAX    | UNIT    |
|--|-----------------------|--------------------------------------|------|-----|--------|---------|
| Operating oscillation frequency              | $f_{XT}$              | Fig. 1                               | 0.8  |     | 3.5    | MHz     |
| CR oscillation frequency *                   | $f_{CR}$              | $T_a=25^{\circ}C$<br>$R_f=27k\Omega$ | 0.85 | 1   | 1.15   | MHz     |
| External clock Input<br>Rise time, Fall time | $t_{CLH}$ , $t_{CLL}$ | Fig. 2                               |      |     | 250 *) | ns      |
| Serial input data setup time                 | $t_{SIS}$             | Fig. 2                               | 35   |     |        | ns      |
| Serial input data hold time                  | $t_{SIH}$             | Fig. 2                               | 35   |     |        | ns      |
| Serial clock frequency                       | $f_{SCK}$             | Fig. 3                               |      |     | 1.5    | MHz     |
| Serial clock interval time                   | $t_{SCI}$             | Fig. 3                               | 10   |     |        | $\mu s$ |
| Reset pulse width                            | $t_{RSTb}$            | Fig. 4                               | 10   |     |        | $\mu s$ |
| Power rise time                              | $t_R$                 | Fig. 5                               | 0.05 |     | 10     | ms      |

\*) Noises on SCK during rise time or fall time may cause malfunctions. Testing samples in the application is recommended.

• DC characteristics 2

( $V_{DD}=3.3V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $85^{\circ}C$ )

| PARAMETER                 | SYMBOL    | CONDITIONS  | MIN   | TYP | MAX         | UNIT      |
|---------------------------|-----------|---|---|-----|-------------|-----------|
| Operating voltage         | $V_{DD}$  | $V_{DD}$ terminal   | 3.0   |     | 3.6         | V         |
| “H” level input voltage   | $V_{IH}$  | XT, RSTb, CSb, SCK, SI terminals  | $0.8V_{DD}$   |     | $0.2V_{DD}$ | V         |
| “L” level input voltage   | $V_{IL}$  |   |   |     |             |           |
| Input off leak current    | $I_{IZ}$  | CSb, SCK, SI terminals<br>$V_{DD}=3.6V$ , $V_I=0$ or $3.6V$   |   |     | $\pm 1$     | $\mu A$   |
| Display output current    | $I_{OH}$  | $S_0$ to $S_{15}$ terminals   | $V_{DD}=3.0V$ ,<br>$V_{FDP}=V_{DD}-40V$ ,<br>$V_{OH}=V_{DD}-1.5V$ |     |             | mA        |
|                           |           | $T_0$ to $T_{13}$ terminals   |   |     |             |           |
| Pull-up resistance        | $R_{UR}$  | RSTb terminal, $T_a=25^{\circ}C$ , $V_I=V_{SS}$   | 100   |     | 280         | $k\Omega$ |
| Pull-down resistance      | $R_{DST}$ | $S_0$ to $S_{15}$ , $T_0$ to $T_{13}$ terminals, $T_a=25^{\circ}C$<br>$V_I=V_{DD}$ , $V_{FDP}=V_{DD}-40V$   | 60  |     | 160         | $k\Omega$ |
| Logic operating current   | $I_{SS}$  | $V_{SS}$ terminal,<br>All Segment/Timing output terminals open, RSTb terminal open,<br>Ceramic resonator: 1MHz,<br>All Segment output OFF and All Timing output OFF |   | 0.8 | 1.5         | mA        |
| Display operating current | $I_{FDP}$ | $V_{FDP}$ terminal, $V_{FDP}=V_{DD}-40V$ ,<br>Ceramic resonator: 1MHz,<br>All Segment/Timing output ON  |   | 10  | 15          | mA        |

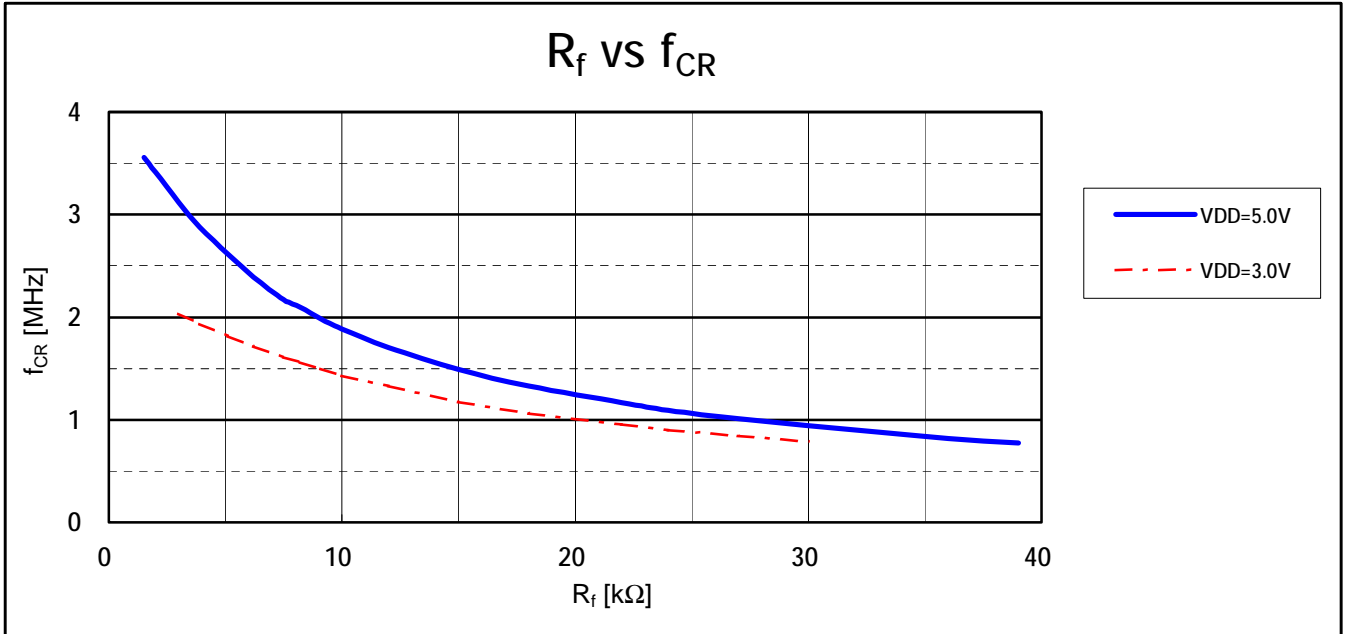
• AC characteristics 2

( $V_{DD}=3.3V$ ,  $V_{SS}=0V$ ,  $T_a=-40$  to  $85^{\circ}C$ )

| PARAMETER                                    | SYMBOL                | CONDITIONS                           | MIN  | TYP | MAX    | UNIT    |
|--|-----------------------|--------------------------------------|------|-----|--------|---------|
| Operating oscillation frequency              | $f_{XT}$              | Fig. 1                               | 0.8  |     | 2      | MHz     |
| CR oscillation frequency *                   | $f_{CR}$              | $T_a=25^{\circ}C$<br>$R_f=18k\Omega$ | 0.85 | 1   | 1.15   | MHz     |
| External clock Input<br>Rise time, Fall time | $t_{CLH}$ , $t_{CLL}$ | Fig. 2                               |      |     | 250 *) | ns      |
| Serial input data setup time                 | $t_{SIS}$             | Fig. 2                               | 70   |     |        | ns      |
| Serial input data hold time                  | $t_{SIH}$             | Fig. 2                               | 70   |     |        | ns      |
| Serial clock frequency                       | $f_{SCK}$             | Fig. 3                               |      |     | 0.8    | MHz     |
| Serial clock interval time                   | $t_{SCI}$             | Fig. 3                               | 10   |     |        | $\mu s$ |
| Reset pulse width                            | $t_{RSTb}$            | Fig. 4                               | 20   |     |        | $\mu s$ |
| Power rise time                              | $t_R$                 | Fig. 5                               | 0.05 |     | 5      | ms      |

\*) Noises on SCK during rise time or fall time may cause malfunctions. Testing samples in the application is recommended.

\* Relation between external resistor ( $R_f$ ) and oscillation frequency ( $f_{CR}$ ).  
The frequency can be adjusted by the selection of external resistor  $R_f$ , as shown in “ $R_f$  vs  $f_{CR}$ ”.  
Refer to circuit example of “**APPLICATION CIRCUIT (b) CR oscillation**”.



This graph shows a reference characteristic, and this performance is not guaranteed.

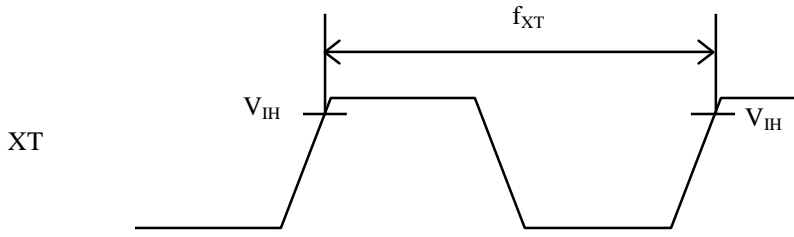


Fig. 1

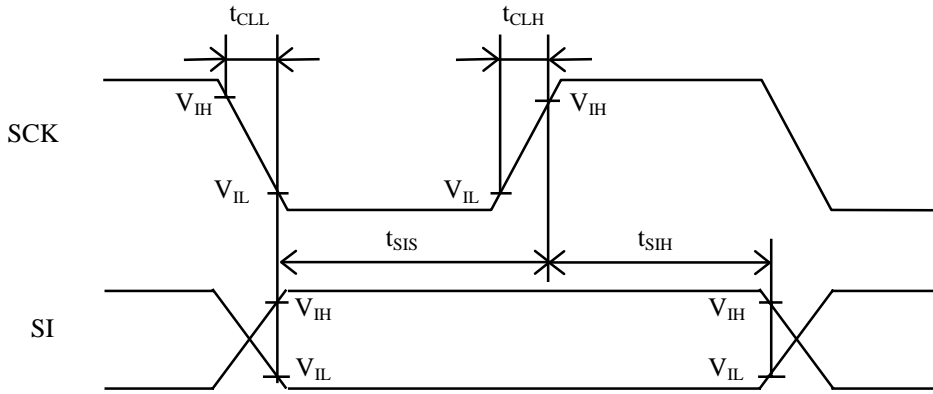


Fig. 2

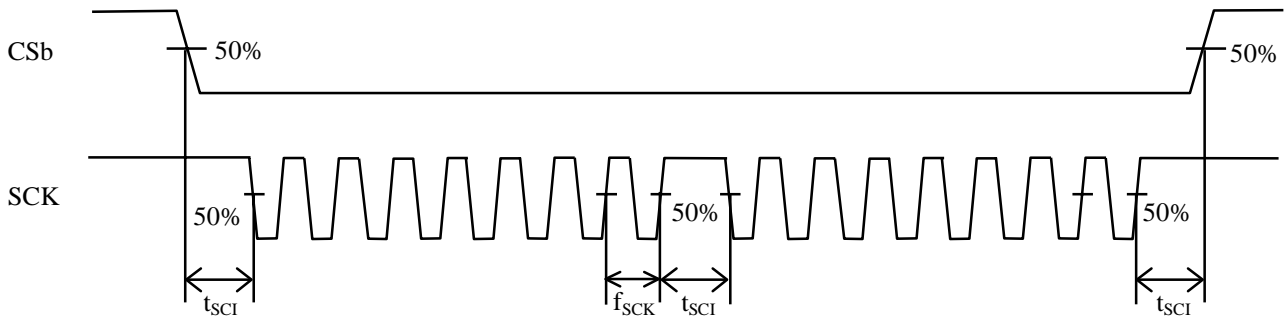


Fig. 3

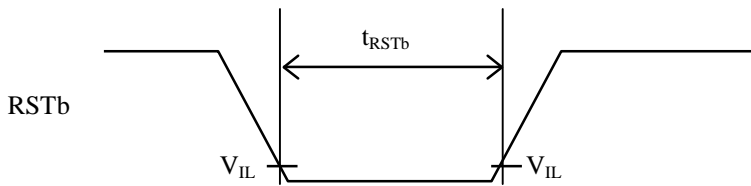


Fig. 4

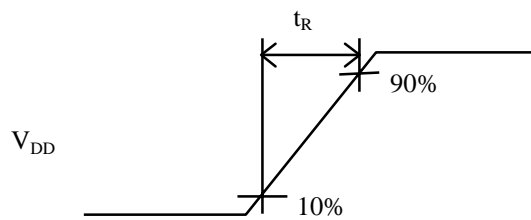
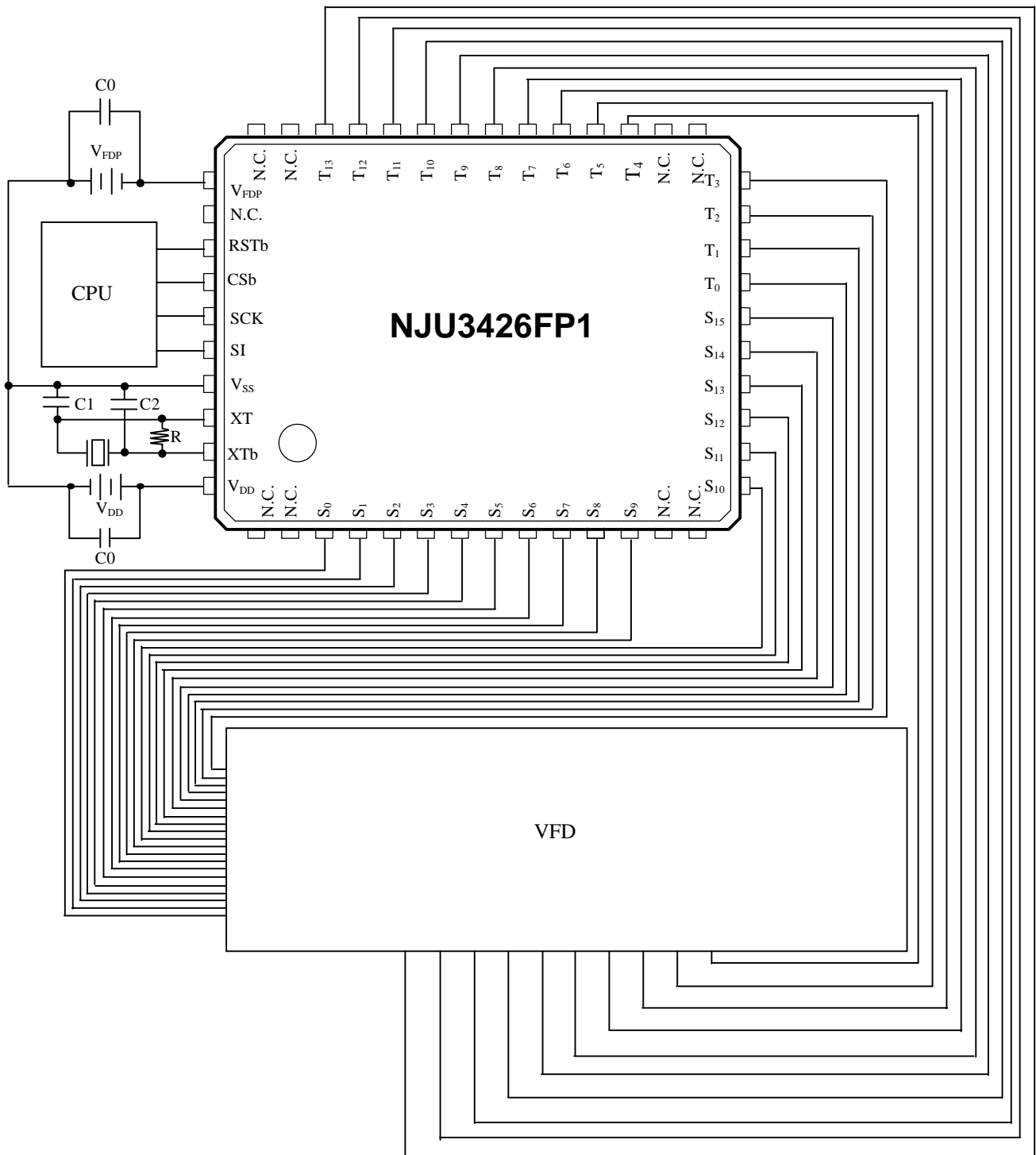


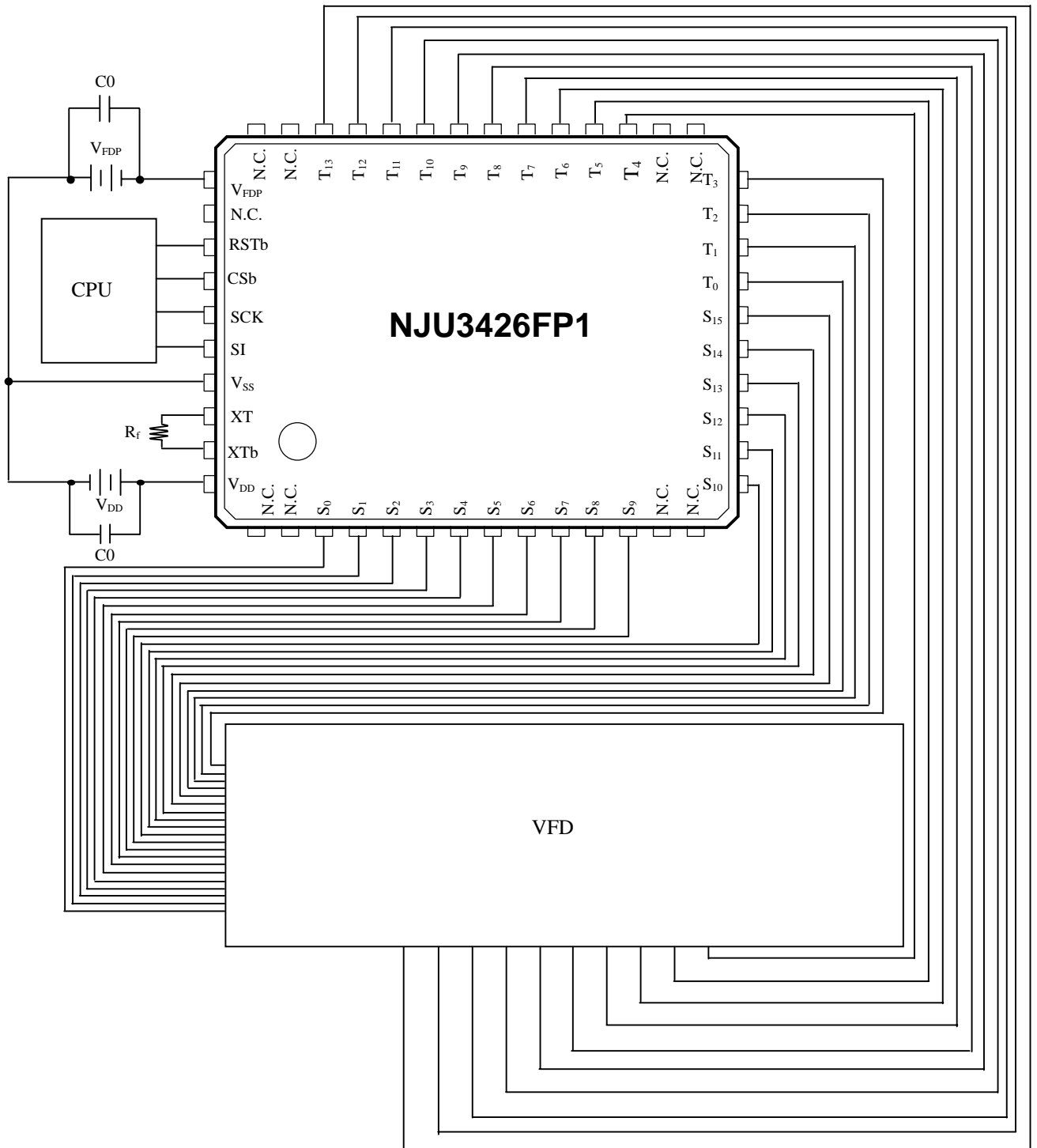
Fig. 5

## APPLICATION CIRCUIT

(a) Ceramic Resonator Oscillation



(b) Ceramic Resonator Oscillation



**[CAUTION]**  
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