PM4328

TECT3

HIGH DENSITY T1/E1 FRAMER WITH INTEGRATED M13 MULTIPLEXER

DATASHEET

PROPRIETARY AND CONFIDENTIAL

ISSUE 1: AUGUST 2001

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 FEATURES

- Integrates 28 T1 framers, 21 E1 framers and a full featured M13 multiplexer with DS3 framer in a single monolithic device for terminating DS3 multiplexed T1 or E1 streams.
- Four fundamental modes of operation:
  - Up to 28 T1 streams M13 multiplexed into a serial DS3.
  - Up to 21 E1 streams multiplexed into a DS3 following the ITU-T G.747 recommendation. This E1 mode of operation is restricted to using the serial clock and data or H-MVIP system interfaces.
  - DS3 M13 Multiplexer with ingress or egress per link monitoring.
  - Unchannelized DS3 framer mode for access to the entire DS3 payload.
- Supports transfer of PCM data to/from 1.544MHz and 2.048MHz serial interface system-side devices. Also supports a fractional T1 or E1 system interface with independent ingress/egress Nx64Kb/s rates. Supports a 2.048 MHz system-side interface for T1 mode without external clock gapping.
- Supports 8Mb/s H-MVIP on the system interface for all T1 or E1 links, a separate 8Mb/s H-MVIP system interface for all T1 or E1 CAS channels and a separate 8Mb/s H-MVIP system interface for all T1 or E1 CCS and V5.1/V5.2 channels.
- Supports a byte serial Scaleable Bandwidth Interconnect (SBI) bus interface for high density system side device interconnection of up to 84 T1 streams or 3 DS3 streams.
- Provides jitter attenuation in the T1 or E1 receive and transmit directions.
- Provides two independent de-jittered T1 or E1 recovered clocks for system timing and redundancy.
- Provides per-DS0 line loopback and per link diagnostic and line loopbacks.
- Provides an on-board programmable binary sequence generator and detector for error testing at DS3 rates. Includes support for patterns recommended in ITU-T O.151.

- Also provides PRBS generators and detectors on each tributary for error testing at DS1, E1 and NxDS0 rates as recommended in ITU-T O.151 and O.152.
- Provides robbed bit signaling extraction and insertion on a per-DS0 basis.
- Provides programmable idle code substitution, data and sign inversion, and digital milliwatt code insertion on a per-DS0 basis.
- Supports the M23 and C-bit parity DS3 formats.
- Standalone unchannelized DS3 framer mode for access to the entire DS3 payload.
- When configured to operate as a DS3 Framer, gapped transmit and receive clocks can be optionally generated for interface to link layer devices which only need access to payload data bits.
- DS3 Transmit clock source can be selected from either an external oscillator or from the receive side clock (loop-timed).
- Register level compatibility with the PM4388 TOCTL Octal T1 Framer, the PM6388 EOCTL Octal E1 Framer, the PM4351 COMET E1/T1 transceiver and the PM8313 D3MX M13 Multiplexer/Demultiplexer.
- Provides a generic 8-bit microprocessor bus interface for configuration, control and status monitoring.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power 2.5V/3.3V CMOS technology. All pins are 5V tolerant.
- 324-pin fine pitch PBGA package (23mm x 23mm). Supports industrial temperature range (-40^{o}C to 85^{o}C) operation.

Each one of 28 T1 receiver sections:

- Frames to DS-1 signals in SF and ESF formats.
- Frames to TTC JT-G.704 multiframe formatted J1 signals. Supports the alternate CRC-6 calculation for Japanese applications.
- Accepts gapped data streams to support higher rate demultiplexing.

- Provides Red, Yellow, and AIS alarm integration.
- Provides ESF bit-oriented code detection and an HDLC/LAPD interface for terminating the ESF facility data link.
- Indicates signaling state change, and two superframes of signaling debounce on a per-DS0 basis.
- Provides an HDLC interface with 128 bytes of buffering for terminating the facility data link.
- Provides performance monitoring counters sufficiently large as to allow performance monitor counter polling at a minimum rate of once per second. Optionally, updates the performance monitoring counters and interrupts the microprocessor once per second, timed to the receive line.
- Provides an optional elastic store which may be used to time the ingress streams to a common clock and frame alignment, or to facilitate per-DS0 loopbacks.
- Provides DS-1 robbed bit signaling extraction, with optional data inversion, programmable idle code substitution, digital milliwatt code substitution, bit fixing, and two superframes of signaling debounce on a per-channel basis.
- A pseudo-random sequence user selectable from $2^{11} - 1$, $2^{15} - 1$ or$2^{20} - 1$, may be detected in the T1 stream in either the ingress or egress directions. The detector counts pattern errors using a 24-bit non-saturating PRBS error counter. The pseudo-random sequence can be the entire T1 or any combination of DS0s within a framed T1.
- Line side interface is the DS3 interface via the M13 multiplex.
- System side interface is either serial clock and data, H-MVIP or SBI bus.
- Frames in the presence of and detects the “Japanese Yellow” alarm.
- Provides external access for up to two de-jittered recovered T1 clocks.

Each one of 21 E1 receiver sections:

- Frames to ITU-T G.704 basic and CRC-4 multiframe formatted E1 signals. The framing procedures are consistent ITU-T G.706 specifications.
- Provides an HDLC interface with 128 bytes of buffering for terminating the national use bit data link.

- Extracts 4-bit codewords from the E1 national use bits as specified in ETS 300 233.
- V5.2 link indication signal detection.
- Provides performance monitoring counters sufficiently large as to allow performance monitor counter polling at a minimum rate of once per second. Optionally, updates the performance monitoring counters and interrupts the microprocessor once per second, timed to the receive line.
- Provides a two-frame elastic store buffer for backplane rate adaptation that performs controlled slips and indicates slip occurrence and direction.
- Frames to the E1 signaling multiframe alignment when enabled and extracts channel associated signaling. Alternatively, a common channel signaling data link may be extracted from timeslot 16.
- Can be programmed to generate an interrupt on change of signaling state.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- A pseudo-random sequence user selectable from 2^{11} –1, 2^{15} –1 or2^{20} –1, may be detected in the E1 stream in either the ingress or egress directions. The detector counts pattern errors using a 24-bit non-saturating PRBS error counter. The pseudo-random sequence can be the entire E1 or any combination of timeslots within the framed E1.
- Line side interface is the DS3 interface mutiplexed as per the G.747 recommendation.
- System side interface is either serial clock and data or H-MVIP.
- Provides external access for up to two de-jittered recovered E1 clocks.

Each one of 28 T1 transmitter sections:

- May be timed to its associated receive clock (loop timing) or may derive its timing from a common egress clock or a common transmit clock; the transmit line clock may be synthesized from an N*8kHz reference.
- Provides minimum ones density through Bell (bit 7), GTE or “jammed bit 8” zero code suppression on a per-DS0 basis.

- Provides a 128 byte buffer to allow insertion of the facility data link using the host interface.
- Supports transmission of the alarm indication signal (AIS) or the Yellow alarm signal in both SF and ESF formats.
- Provides a digital phase locked loop for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmitter.
- Automatically generates and transmits DS-1 performance report messages to ANSI T1.231and ANSI T1.408 specifications.
- Supports the alternate ESF CRC-6 calculation for Japanese applications.
- A pseudo-random sequence user selectable from 2^{11} –1, 2^{15} –1 or 2^{20} –1, may be inserted into the T1 stream in either the ingress or egress directions. The pseudo-random sequence can be inserted into the entire T1 or any combination of DS0s within the framed T1.
- Line side interface is through the DS3 Interface via the M13 multiplex.
- System side interface is either serial clock and data, H-MVIP or SBI bus.

Each one of 21 E1 transmitter sections:

- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmit path.
- Transmits G.704 basic and CRC-4 multiframe formatted E1.
- Supports unframed mode and framing bit, CRC, or data link by-pass.
- Provides signaling insertion, programmable idle code substitution, digital milliwatt code substitution, and data inversion on a per channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- Provides a digital phase locked loop for generation of a low jitter transmit clock.

- A pseudo-random sequence user selectable from 2^{11} –1, 2^{15} –1 or 2^{20} –1, may be inserted into the E1 stream in either the ingress or egress directions. The pseudo-random sequence can be inserted into the entire E1 or any combination of timeslots within the framed E1.

- Optionally inserts a datalink in the E1 national use bits.

- Supports 4-bit codeword insertion in the E1 national use bits as specified in ETS 300 233

- Supports transmission of the alarm indication signal (AIS) and the Yellow alarm signal.

- Line side interface is the DS3 interface mutiplexed as per the G.747 recommendation.

- System side interface is either serial clock and data or H-MVIP

DS3 Receiver Section:

- Frames to a DS3 signal with a maximum average reframe time of less than 1.5 ms (as required by TR-TSY-000009 Section 4.1.2 and TR-TSY-000191 Section 5.2).

- Decodes a B3ZS-encoded signal and indicates line code violations. The definition of line code violation is software selectable.

- Provides indication of M-frame boundaries from which M-subframe boundaries and overhead bit positions in the DS3 stream can be determined by external processing.

- Detects the DS3 alarm indication signal (AIS) and idle signal. Detection algorithms operate correctly in the presence of a 10^{-3} bit error rate.

- Extracts valid X-bits and indicates far end receive failure (FERF).

- Accumulates up to 65,535 line code violation (LCV) events per second, 65,535 P-bit parity error events per second, 1023 F-bit or M-bit (framing bit) events per second, 65,535 excessive zero (EXZ) events per second, and when enabled for C-bit parity mode operation, up to 16,383 C-bit parity error events per second, and 16,383 far end block error (FEBE) events per second.

- Detects and validates bit-oriented codes in the C-bit parity far end alarm and control channel.

- Terminates the C-bit parity path maintenance data link with an integral HDLC receiver having a 128-byte deep FIFO buffer with programmable interrupt threshold. Supports polled or interrupt-driven operation. Selectable none, one or two address match detection on first byte of received packet.

- Programmable pseudo-random test-sequence detection–(up to 2^{32} -1 bit length patterns conforming to ITU-T O.151 standards) and analysis features.

DS3 Transmit Section:

- Provides the overhead bit insertion for a DS3 stream.

- Provides a bit serial clock and data interface, and allows the M-frame boundary and/or the overhead bit positions to be located via an external interface

- Provides B3ZS encoding.

- Generates an B3Zs encoded 100… repeating pattern to aid in pulse mask testing.

- Inserts far end receive failure (FERF), the DS3 alarm indication signal (AIS) and the idle signal when enabled by internal register bits.

- Provides optional automatic insertion of far end receive failure (FERF) on detection of loss of signal (LOS), out of frame (OOF), alarm indication signal (AIS) or red alarm condition.

- Provides diagnostic features to allow the generation of line code violation error events, parity error events, framing bit error events, and when enabled for the C-bit parity application, C-bit parity error events, and far end block error (FEBE) events.

- Supports insertion of bit-oriented codes in the C-bit parity far end alarm and control channel.

- Optionally inserts the C-bit parity path maintenance data link with an integral HDLC transmitter. Supports polled and interrupt-driven operation.

- Provides programmable pseudo-random test sequence generation (up to 2^{32}-1 bit length sequences conforming to ITU-T O.151 standards) or any

repeating pattern up to 32 bits. The test pattern can be framed or unframed. Diagnostic abilities include single bit error insertion or error insertion at bit error rates ranging from 10^{-1} to 10^{-7}.

M23 Multiplexer Section:

- Multiplexes 7 DS2 bit streams into a single M23 format DS3 bit stream.
- Performs required bit stuffing/destuffing including generation and interpretation of C-bits.
- Includes required FIFO buffers for rate adaptation in the multiplex path.
- Allows insertion and detection of per DS2 payload loopback requests encoded in the C-bits to be activated under microprocessor control.
- Internally generates DS2 clock for use in integrated M13 or C-bit parity multiplex applications. Alternatively accepts external DS2 clock reference.
- Allows per DS2 alarm indication signal (AIS) to be activated or cleared for either direction under microprocessor control.
- Allows DS2 alarm indication signal (AIS) to be activated or cleared in the demultiplex direction automatically upon loss of DS3 frame alignment or signal.
- Supports C-bit parity DS3 format.

DS2 Framer Section:

- Frames to a DS2 (ANSI T1.107 section 8) signal with a maximum average reframe time of less than 7 ms (as required by TR-TSY-000009 Section 4.1.2 and TR-TSY-000191 Section 5.2).
- Detects the DS2 alarm indication signal (AIS) in 9.9 ms in the presence of a 10^{-3} bit error rate.
- Extracts the DS2 X-bit remote alarm indication (RAI) bit and indicates far end receive failure (FERF).
- Accumulates up to 255 DS2 M-bit or F-bit error events per second.

DS2 Transmitter Section:

- Generates the required X, F, and M bits into the transmitted DS2 bit stream. Allows inversion of inserted F or M bits for diagnostic purposes.
- Provides for transmission of far end receive failure (FERF) and alarm indication signal (AIS) under microprocessor control.
- Provides optional automatic insertion of far end receive failure (FERF) on detection of out of frame (OOF), alarm indication signal (AIS) or red alarm condition.

M12 Multiplexer Section:

- Multiplexes four DS1 bit streams into a single M12 format DS2 bit stream.
- Performs required bit stuffing including generation and interpretation of C-bits.
- Includes required FIFO buffers for rate adaptation in the multiplex path.
- Performs required inversion of second and fourth multiplexed DS1 streams as required by ANSI T1.107 Section 7.2.
- Allows insertion and detection of per DS1 payload loopback requests encoded in the C-bits to be activated under microprocessor control.
- Allows per tributary alarm indication signal (AIS) to be activated or cleared for either direction under microprocessor control.
- Allows automatic tributary AIS to be activated upon DS2 out of frame.

Synchronous System Interfaces:

- Provides seven 8Mb/s H-MVIP data interfaces for synchronous access to all the DS0s of all 28 T1 links or all timeslots of all 21 E1s. T1 DS0s are bundled from four T1 links in sequential order (i.e. 1-4, 5-8, 9-12, 13-16, 17-20, 21-24, 25-28). In normal mode, E1 timeslots are bundled from 4 E1 links in sequential order (i.e. 1-4, 5-8, 9-12, 13-16, 17-20 and 21 by itself). In G.747 mode, E1 timeslots are bundled from 3 E1 links in sequential order, spaced by a reserved timeslot on every 4th frame (i.e. 1-3/X, 4-6/X, 7-9/X, 10-12/X, 13-15/X, 16-18/X, 19-21/X).

- Provides seven 8Mb/s H-MVIP interfaces for synchronous access to all channel associated signaling (CAS) bits for all T1 DS0s or E1 timeslots. The CAS bits occupy one nibble of every byte on the H-MVIP interfaces and are repeated over the entire T1 or E1 multi-frame.

- Provides a single 8Mb/s H-MVIP interface for common channel signaling (CCS) channels as well as V5.1 and V5.2 channels. In T1 mode DS0 24 is available through this interface. In E1 mode timeslots 15, 16 and 31 are available through this interface.

- All links accessed via the H-MVIP interface will be synchronously timed to the common H-MVIP clock and frame alignment signals, CMV8MCLK, CMVFP, CMVFPC.

- H-MVIP access for Channel Associated Signaling is available with the Scaleable Bandwidth Interconnect bus as an optional replacement for CAS access over the SBI bus as well as with the H-MVIP data interface. Common Channel Signaling H-MVIP access is available with the SBI bus, serial PCM and H-MVIP data interfaces.

- Compatible with H-MVIP PCM backplanes supporting 8.192 Mbit/s.

Scaleable Bandwidth Interconnect (SBI) Bus:

- Provides a high density byte serial interconnect for all framed and unframed TECT3 links. Utilizes an Add/Drop configuration to asynchronously mutliplex up to 84 T1s or 3 DS3s, equivalent to three TECT3s, with multiple payload or link layer processors.

- External devices can access unframed DS3, framed unchannelized DS3, unframed (clear channel) T1s or framed T1s over this interface.

- Framed and unframed T1 access can be selected on a per T1 basis.

- Synchronous access for T1 DS0 channels is supported in a locked format mode.

- Channel associated signaling bits for channelized T1 are explicitly identified across bus.

- Transmit timing is mastered either by the TECT3 or a layer 2 device connecting to the SBI bus. Timing mastership is selectable on a per tributary basis, where a tributary is either an individual T1 or a DS3.

2 APPLICATIONS

- High density T1 interfaces for multiplexers, multi-service switches, routers and digital modems.
- High density E1 interfaces for multiplexers, multi-service switches, routers and digital modems.
- Frame Relay switches and access devices (FRADS)
- M23 Based M13 Multiplexer
- C-Bit Parity Based M13 Multiplexer
- Channelized and Unchannelized DS3 Frame Relay Interfaces

3 REFERENCES

- American National Standard for Telecommunications - Digital Hierarchy - Synchronous DS3 Format Specifications, ANSI T1.103-1993
- American National Standard for Telecommunications - Digital Hierarchy - Formats Specification, ANSI T1.107-1995
- American National Standard for Telecommunications - Digital Hierarchy - Layer 1 In-Service Digital Transmission Performance Monitoring, ANSI T1.231-1997
- American National Standard for Telecommunications - Carrier to Customer Installation - DS-1 Metallic Interface Specification, ANSI T1.403-1995
- American National Standard for Telecommunications - Customer Installation–to-Network - DS3 Metallic Interface Specification, ANSI T1.404-1994
- American National Standard for Telecom–unications - Integrated Services Digital Network (ISDN) Primary Rate- Customer Installation Metallic Interfaces Layer 1 Specification, ANSI T1.408-1990
- Bell Communications Research, TR–TSY-000009 - Asynchronous Digital Multiplexes Requirements and Objectives, Issue 1, May 1986
- Bell Communications Research - DS-1 Rate Digital Service Monitoring Unit Functional Specification, TA-TSY-000147, Issue 1, October, 1987
- Bell Communications Research - Alarm Indication Signal Requirements and Objectives, TR-TSY-000191 Issue 1, May 1986
- Bell Communications Research - Wideband and Broadband Digital Cross-Connect Systems Generic Criteria, TR-NWT-000233, Issue 3, November 1993
- Bell Communications Research - Integrated Digital Loop Carrier Generic Requirements, Objectives, and Interface, TR-NWT-000303, Issue 2, December, 1992
- Bell Communications Research - Transport Systems Generic Requirements (TSGR): Common Requirement, TR-TSY-000499, Issue 5, December, 1993
- Bell Communications Research - OTGR: Network Maintenance Transport Surveillance - Generic Digital Transmission Surveillance, TR-TSY-000820, Section 5.1, Issue 1, June 1990

- AT&T - Requirements For Interfacing Digital Terminal Equipment To Services Employing The Extended Superframe Format, TR 54016, September, 1989.
- AT&T - Accunet T1.5 - Service Description and Interface Specification, TR 62411, December, 1990
- ITU Study Group XVIII – Report R 105, Geneva, 9-19 June 1992
- ETSI - ETS 300 011 - ISDN Primary Rate User-Network Interface Specification and Test Principles, 1992.
- ETSI - ETS 300 233 - Access Digital Section for ISDN Primary Rates, May 1994
- ETSI - ETS 300 324-1 - Signaling Protocols and Switching (SPS); V interfaces at the Digital Local Exchange (LE) V5.1 Interface for the Support of Access Network (AN) Part 1: V5.1 Interface Specification, February, 1994.
- ETSI - ETS 300 347-1 - Signaling Protocols and Switching (SPS); V Interfaces at the Digital Local Exchange (LE) V5.2 Interface for the Support of Access Network (AN) Part 1: V5.2 Interface Specification, September 1994.
- ITU-T - Recommendation G.704 - Synchronous Frame Structures Used at Primary Hierarchical Levels, July 1995.
- ITU-T - Recommendation G.706 - Frame Alignment and CRC Procedures Relating to G.704 Frame Structures, 1991.
- ITU-T - Recommendation G.732 – Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s, 1993.
- ITU-T Recommendation G.747 – Second Order Digital Multiplex Equipment Operating at 6312kbit/s and Multiplexing Three Tributaries at 2048 kbit/s, 1988
- ITU-T Recommendation G.775, - Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria, 11/94
- ITU-T Recommendation G.823, - The Control of Jitter and Wander within Digital Networks which are Based on the 2048 kbit/s Hierarchy, 03/94
- ITU-T Recommendation G.964, - V-Interfaces at the Digital Local Ex–hange (LE) - V5.1 Interface (Based on 2048 kbit/s) for the Support of Access Network (AN), June 1994.

- ITU-T Recommendation G.965, - V-Interfaces at the Digital Local Ex–hange (LE) - V5.2 Interface (Based on 2048 kbit/s) for the Support of Access Network (AN), March –995.
- ITU-T - Recommend–tion I.431 - Primary Rate User-Network Interface – Layer 1 Specification, 1993.
- ITU-T Recommendation O.151 – Error Performance Measuring Equipment Operating at the Primary Rate and Above, October 1992
- ITU-T Recommendation O.152 – Error Performance Measuring Equipment for Bit Rates of 64 kbit/s and N x 64 kbit/s, October 1992
- ITU-T Recommendation O.153 - Basic Parameters for the Measurement of Error Performance at Bit Rates below the Primary Rate, October 1992.
- ITU-T Recommendation Q.921 - ISDN User-Network Interface Data Link Layer Specification, March 1993
- International Organization for Standardization, ISO 3309:1984 - High-Level Data Link Control procedures - Frame Structure
- PMC-Sierra Inc., PMC-1980577 – Saturn Compatible Scaleable Bandwidth Interface (SBI) Specification, Issue 3, 1998
- TTC Standard JT-G704 - Frame Structures on Primary and Secondary Hierarchical Digital Interfaces, 1995.
- TTC Standard JT-G706 - Frame Synchronization and CRC Procedure
- TTC Standard JT-I431 - ISDN Primary Rate User-Network Interface Layer 1 - Specification, 1995.
- Nippon Telegraph and Telephone Corporation - Technical Reference for High-Speed Digital Leased Circuit Services, Third Edition, 1990.
- GO-MVIP, Multi-Vendor Integration Protocol, MVIP-90, Release 1.1, 1994
- GO-MVIP, H-MVIP Standard, Release1.1a, 1997

4 APPLICATION EXAMPLES

Figure 1: Channelized DS3 Circuit Emulation Application

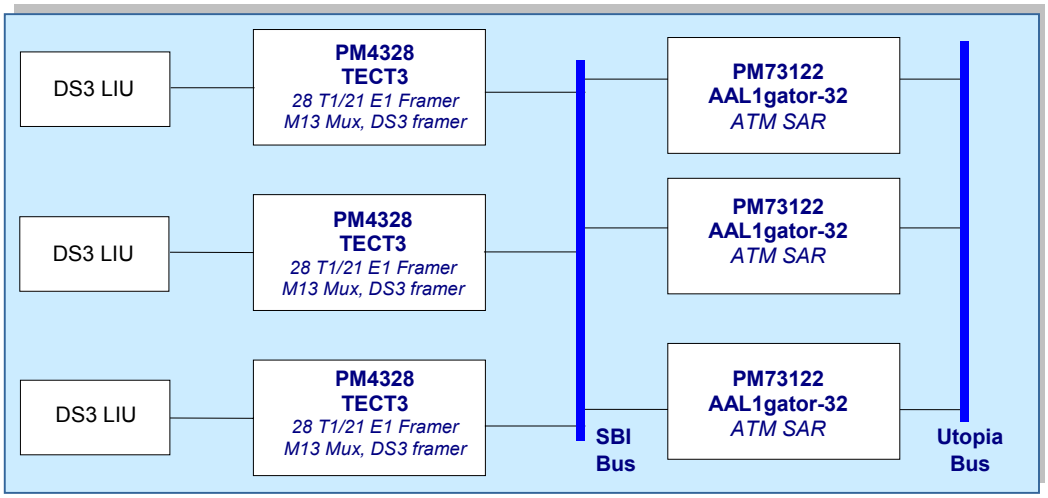
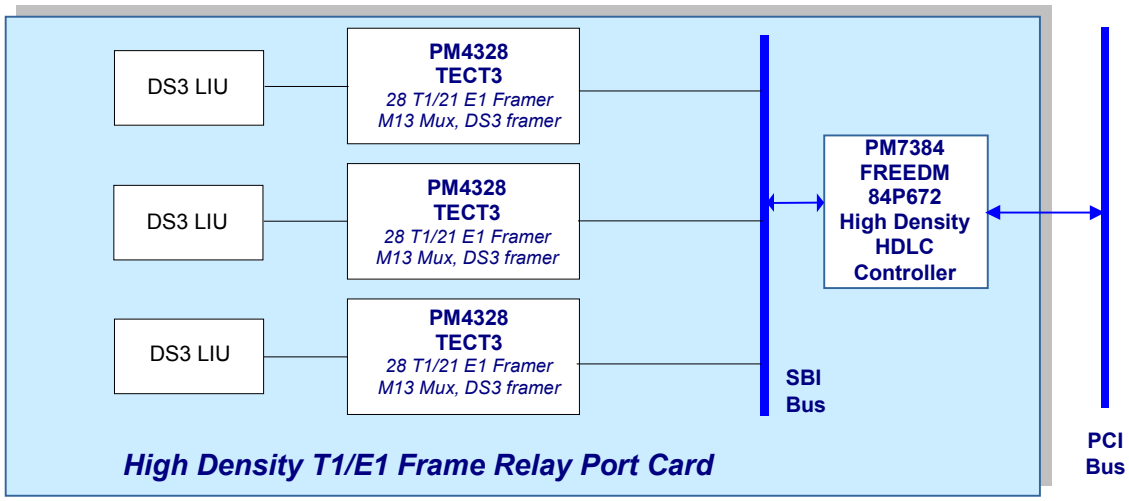


Figure 2: High Density Frame Relay Application

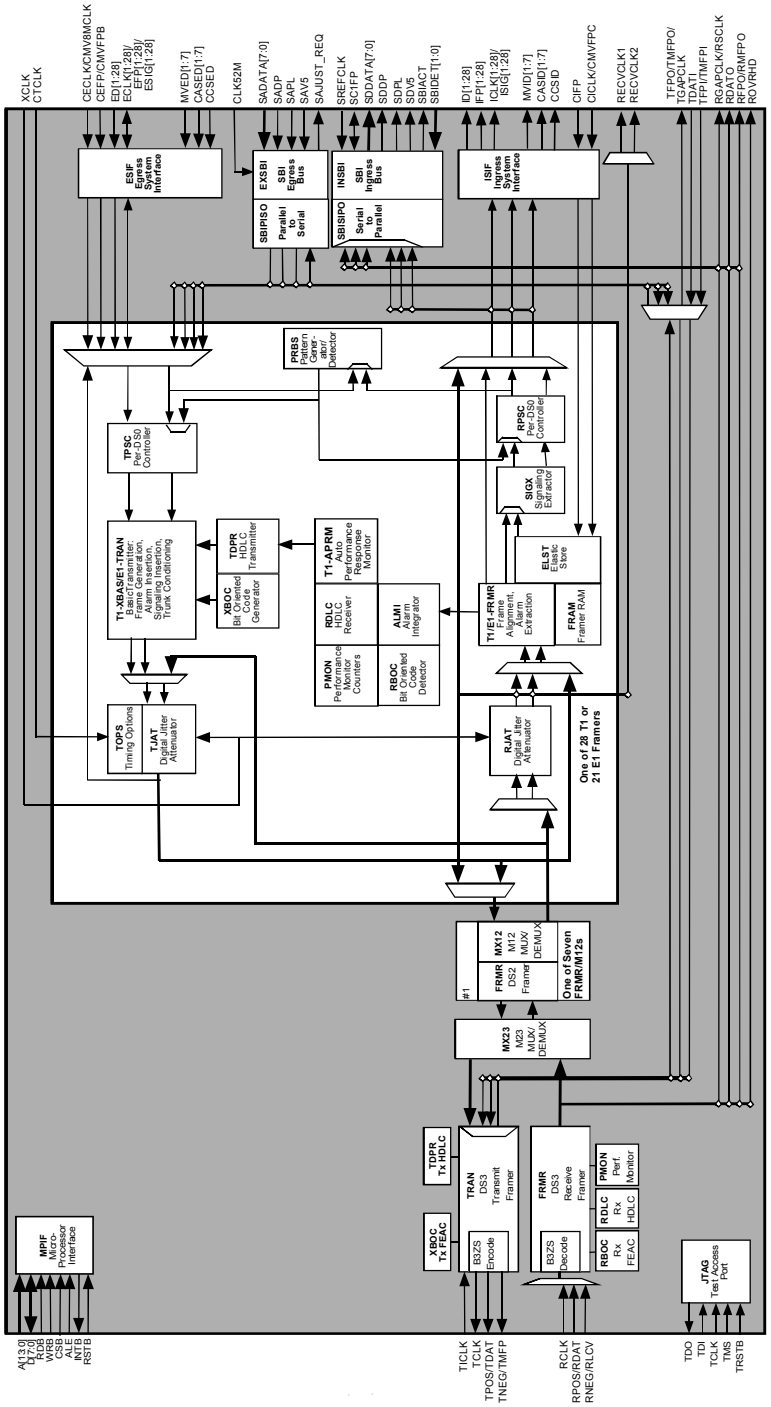


5 BLOCK DIAGRAM

5.1 Top Level Block Diagram

The diagram below shows the complete TECT3. T1 or E1 links can be multiplexed into a DS3 (E1s following the ITU-T G.747 recommendation). System side access to the T1s is available via the serial clock and data, H-MVIP or SBI bus interfaces. System side access to the E1s is available via the serial clock and data or H-MVIP interfaces. DS3 line side access is via the clock and data interface for line interface units. Unchannelized DS3 system side access is available through a serial clock and data interface or the SBI bus, both shown at the top of the diagram.

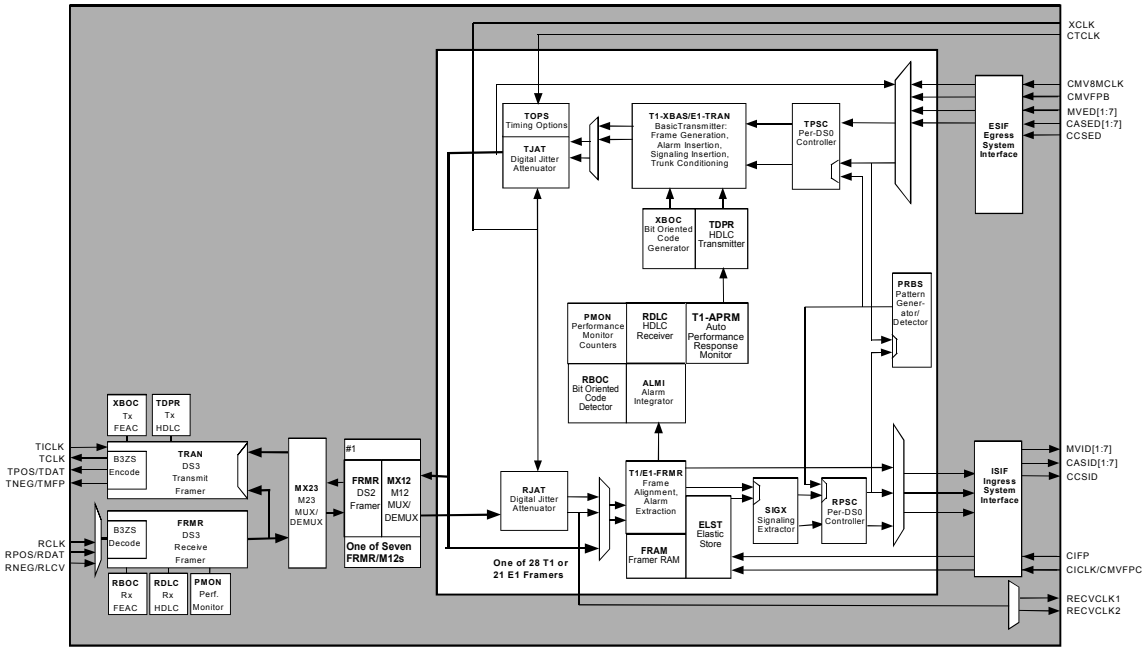
Figure 3: TECT3 Block Diagram



5.2 M13 Multiplexer Mode Block Diagram

Figure 4 shows the TECT3, configured as a M13 multiplexer, connected to a synchronous H-MVIP system side bus. In this example the TECT3 provides synchronous access to the fully channelized T1s (access to all DS0s) multiplexed into the DS3. There is also synchronous H-MVIP access to all channel associated signaling channels (CAS). An additional H-MVIP interface can be used to provide synchronous access to the common channel signaling channels (CCS), although this same information is available within the data H-MVIP signals.

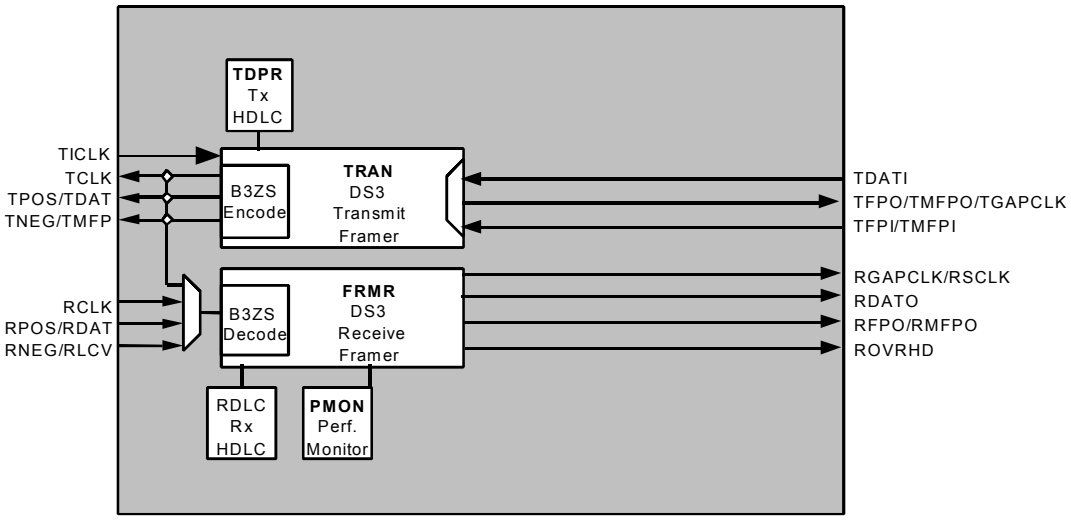
Figure 4: M13 Multiplexer Block Diagram



5.3 DS3 Framer Only Block Diagram

Figure 5 shows the TECT3 configured as a DS3 framer. In this mode the TECT3 provides access to the full DS3 unchannelized payload. The payload access (right side of diagram) has two clock and data interfacing modes, one utilizing a gapped clock to mask out the DS3 overhead bits and the second utilizing an ungapped clock with overhead indications on a separate overhead signal. The SBI bus can also be used to provide access to the unchannelized DS3.

Figure 5: DS3 Framer Only Mode Block Diagram



6 DESCRIPTION

The PM4328 High Density T1/E1 Framer with Integrated M13 Multiplexer (TECT3) is a feature-rich device for use in any applications requiring high density link termination over T1 or E1 channelized DS3.

The TECT3 supports asynchronous multiplexing and demultiplexing of 28 DS1s into a DS3 signal as specified by ANSI T1.107 and Bell Communications Research TR-TSY-000009.

This device can also be configured as a DS3 framer, providing external access to the full DS3 payload.

The TECT3 can be used as an M13 multiplexer with performance monitoring in either the ingress or egress direction for up to 28 T1s or 21 E1s. In this configuration the T1 and E1 transmit framers are disabled and either the ingress or egress T1 or E1 signals are routed to the T1 or E1 framers for performance monitoring purposes.

Each of the T1 and E1 framers and transmitters is independently software configurable, allowing timing master and feature selection without changes to external wiring. This device is able to operate in T1 mode or E1 mode but not a mix of T1 and E1 modes.

In the ingress direction, each of the 28 T1 framers is demultiplexed from a channelized DS3 . Each T1 framer can be configured to frame to either of the common DS1 signal formats: (SF, ESF) or to be bypassed (unframed mode). Each T1 framer detects and indicates the presence of Yellow and AIS patterns and also integrates Yellow, Red, and AIS alarms.

T1 performance monitoring with accumulation of CRC-6 errors, framing bit errors, out-of-frame events, and changes of frame alignment is provided. The TECT3 also detects the presence of ESF bit oriented codes, and detects and terminates HDLC messages on the ESF data link. The HDLC messages are terminated in a 128 byte FIFO. An elastic store that optionally supports slip buffering and adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing and interrupt on signaling state change on a per-DS0 basis. The TECT3 also supports idle code substitution, digital milliwatt code insertion, data extraction, trunk conditioning, data sign and magnitude inversion, and pattern generation or detection on a per-DS0 basis.

In the egress direction, framing is generated for 28 T1s into the DS3. Each T1 transmitter frames to SF or ESF DS1 formats, or framing can be optionally

disabled. The TECT3 supports signaling insertion, idle code substitution, data insertion, line loopback, data inversion and zero-code suppression on a per-DS0 basis. PRBS generation or detection is supported on a framed and unframed T1 basis.

In the ingress direction, each of the 21 E1 framers is extracted from the DS3 following the ITU-T G.747 recommendation. Each E1 framer detects and indicates the presence of remote alarm and AIS patterns and also integrates Red and AIS alarms.

The E1 framers support detection of various alarm conditions such as loss of frame, loss of signaling multiframe and loss of CRC multiframe. The E1 framers also support reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and time slot 16 alarm indication signal.

E1 performance monitoring with accumulation of CRC-4 errors, far end block errors and framing bit errors is provided. The TECT3 provides a receive HDLC controller for the detection and termination of messages on the national use bits. Detection of the 4-bit Sa-bit codewords defined in ITU-T G.704 and ETSI 300-233 is supported. V5.2 link ID signal detection is also supported. An interrupt may be generated on any change of state of the Sa codewords. An elastic store for slip buffering and rate adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-channel basis. Receive side data and signaling trunk conditioning is also provided.

In the egress direction, framing is generated for 21 E1s into the DS3 following the ITU-T G.747 recommendation.Each E1 transmitter generates framing for a basic G.704 E1 signal. The signaling multiframe alignment structure and the CRC multiframe structure may be optionally inserted. Framing can be optionally disabled. Transmission of the 4-bit Sa codewords defined in ITU-T G.704 and ETSI 300-233 is supported. PRBS generation or detection is supported on a framed and unframed E1 basis.

The TECT3 can generate a low jitter transmit clock from a variety of clock references, and also provides jitter attenuation in the receive path. Two low jitter recovered T1 clocks can be routed outside the TECT3 for network timing applications.

Serial PCM interfaces to each T1 framer allow 1.544 Mbit/s ingress/egress system interfaces to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic.

In synchronous backplane systems 8Mb/s H-MVIP interfaces are provided for access to 672 DS0 channels, channel associated signaling (CAS) for all 672 DS0 channels and common channel signaling (CCS) for all 28 T1s. The DS0 data channel H-MVIP and CAS H-MVIP access is multiplexed with the serial PCM interface pins. The CCS signaling H-MVIP interface is independent of the DS0 channel and CAS H-MVIP access. The use of any of the H-MVIP interfaces requires that common clocks and frame pulse be used along with T1 slip buffers.

A Scaleable Bandwidth Interconnect (SBI) high density byte serial system interface provides higher levels of integration and dense interconnect. The SBI bus interconnects up to 84 T1s both synchronously or asynchronously. The SBI allows transmit timing to be mastered by either the TECT3 or link layer device connected to the SBI bus. This interconnect allows up to 3 TECT3s to be connected in parallel to provide the full complement of 84 T1s of traffic. In addition to framed T1s, the TECT3 can transport unframed T1 links and framed or unframed DS3 links over the SBI bus.

When configured as a DS3 multiplexer/demultiplexer or DS3 framer, the TECT3 accepts and outputs either or both digital B3ZS-encoded bipolar and unipolar signals compatible with M23 and C-bit parity applications.

In the DS3 receive direction, the TECT3 frames to DS3 signals with a maximum average reframe time of 1.5 ms in the presence of 10^{-3} bit error rate and detects line code violations, loss of signal, framing bit errors, parity errors, C-bit parity errors, far end block errors, AIS, far end receive failure and idle code. The DS3 framer is an off-line framer, indicating both out of frame (OOF) and change of frame alignment (COFA) events. The error events (C-BIT, FEBE, etc.) are still indicated while the framer is OOF, based on the previous frame alignment. When in C-bit parity mode, the Path Maintenance Data Link and the Far End Alarm and Control (FEAC) channels are extracted. HDLC receivers are provided for Path Maintenance Data Link support. In addition, valid bit-oriented codes in the FEAC channels are detected and are available through the microprocessor port.

Error event accumulation is also provided by the TECT3. Framing bit errors, line code violations, excessive zeros occurrences, parity errors, C-bit parity errors, and far end block errors are accumulated. Error accumulation continues even while the off-line framers are indicating OOF. The counters are intended to be polled once per second, and are sized so as not to saturate at a 10^{-3} bit error rate. Transfer of count values to holding registers is initiated through the microprocessor interface.

In the DS3 transmit direction, the TECT3 inserts DS3 framing, X and P bits. When enabled for C-bit parity operation, bit-oriented code transmitters and HDLC transmitters are provided for insertion of the FEAC channels and the Path Maintenance Data Links into the appropriate overhead bits. Alarm Indication

Signals, Far End Receive Failure and idle signal can be inserted using either internal registers or can be configured for automatic insertion upon received errors. When M23 operation is selected, the C-bit Parity ID bit (the first C-bit of the first M sub-frame) is forced to toggle so that downstream equipment will not confuse an M23-formatted stream with stuck-at-1 C-bits for C-bit Parity application. Transmit timing is from an external reference or from the receive direction clock.

The TECT3 also supports diagnostic options which allow it to insert, when appropriate for the transmit framing format, parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, all-zeros, AIS, Remote Alarm Indications, and Remote End Alarms. A Pseudo Random Binary Sequence (PRBS) can be inserted into a DS3 payload and checked in the receive DS3 payload for bit errors. A fixed 100100… pattern is available for insertion directly into the B3ZS encoder for proper pulse mask shape verification.

When configured in DS3 multiplexer mode, seven 6312 kbit/s data streams are demultiplexed and multiplexed into and out of the DS3 signal. Bit stuffing and rate adaptation is performed. The C-bits are set appropriately, with the option of inserting DS2 loopback requests. Interrupts can be generated upon detection of loopback requests in the received DS3. AIS may be inserted in the any of the 6312 kbit/s tributaries in both the multiplex and demultiplex directions. C-bit parity is supported by sourcing a 6.3062723 MHz clock, which corresponds to a stuffing ratio of 100%.

Framing to the demultiplexed 6312 kbit/s data streams supports DS2 (ANSI TI.107) frame formats. The maximum average reframe time is 7ms for DS2. Far end receive failure is detected and M-bit and F-bit errors are accumulated. The DS2 framer is an off-line framer, indicating both OOF and COFA events. Error events (FERF, MERR, FERR, PERR, RAI, framing word errors) are still indicated while the DS2 framer is indicating OOF, based on the previous alignment.

Each of the seven 6312 kbit/s multiplexers may be independently configured to multiplex and demultiplex four 1544 kbit/s DS1s into and out of a DS2 formatted signal. Tributary frequency deviations are accommodated using internal FIFOs and bit stuffing. The C-bits are set appropriately, with the option of inserting DS1 loopback requests. Interrupts can be generated upon detection of loopback requests in the received DS2. AIS may be inserted in any of the low speed tributaries in both multiplex and demultiplex directions.

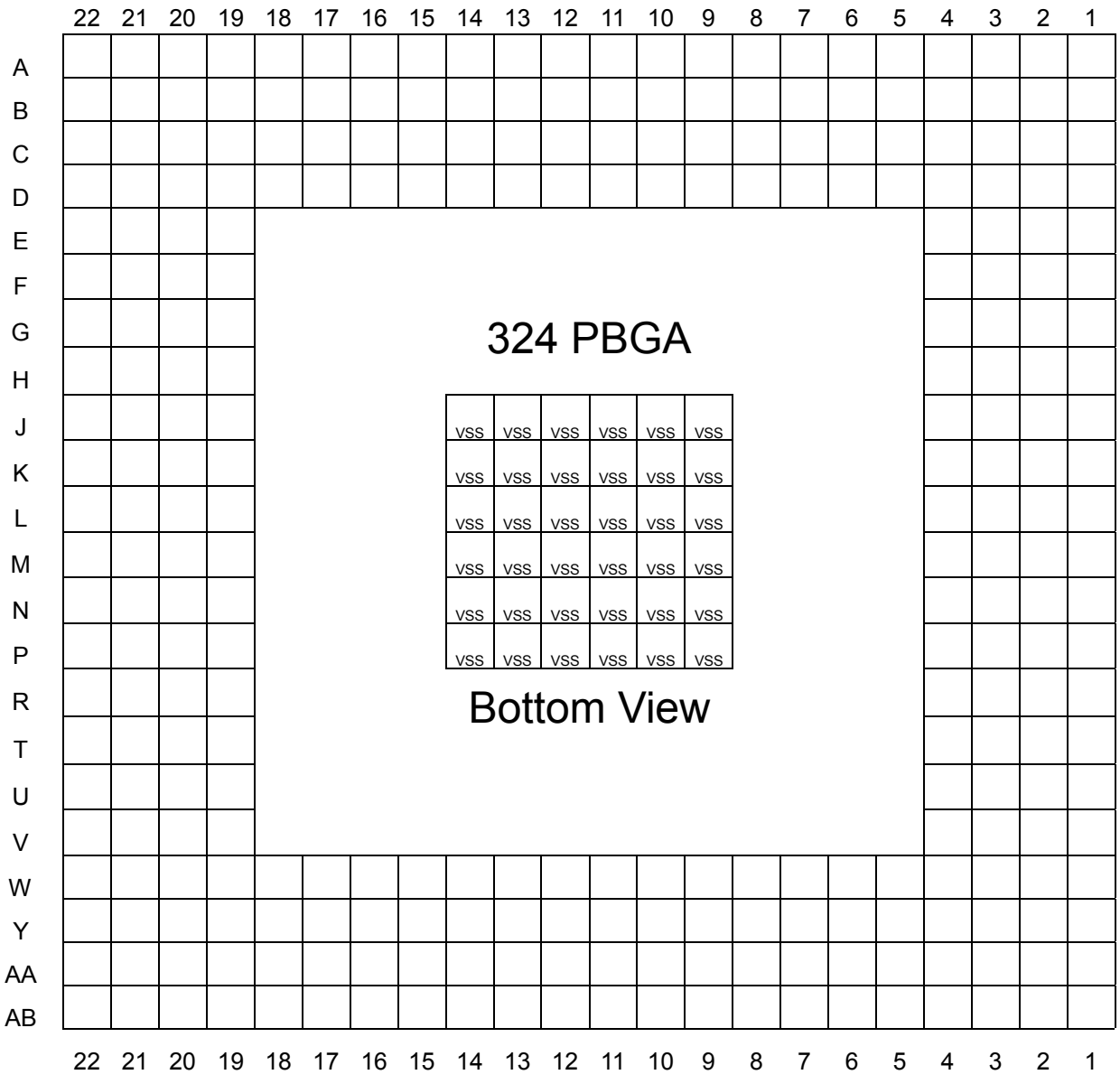
When configured as a DS3 framer the unchannelized payload of the DS3 link is available to an external device.

The TECT3 is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be masked and acknowledged through the microprocessor interface.

7 PIN DIAGRAM

The TECT3 is currently planned to be packaged in a 324-pin PBGA package having a body size of 23mm by 23mm and a ball pitch of 1.0 mm. The center 36 balls are not used as signal I/Os and are thermal balls. Pin names and locations are defined in the Pin Description Table in section 8. Mechanical information for this package is in the section 19.

Figure 6: Pin Diagram



8 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
DS3 Line Side Interface			
RCLK	Input	W5	**Receive Input Clock (RCLK).** RCLK provides the receive direction timing. RCLK is a DS3, nominally a 44.736 MHz, 50% duty cycle clock input.
RPOS/RDAT	Input	Y7	**Positive Input Pulse (RPOS).** RPOS represents the positive pulses received on the B3ZS-encoded DS3 when dual rail input format is selected. **Receive Data Input (RDAT).** RDAT represents the NRZ (unipolar) DS3 input data stream when single rail input format is selected. RPOS and RDAT are sampled on the rising edge of RCLK by default and may be enabled to be sampled on the falling edge of RCLK by setting the RFALL bit in the DS3 Master Receive Line Options register.
RNEG/RLCV	Input	AB6	**Negative Input Pulse (RNEG).** RNEG represents the negative pulses received on the B3ZS-encoded DS3 when dual rail input format is selected. **Line code violation (RLCV).** RLCV represents receive line code violations when single rail input format is selected. RNEG and RLCV are sampled on the rising edge of RCLK by default and may be enabled to be sampled on the falling edge of RCLK by setting the RFALL bit in the DS3 Master Receive Line Options register.
TCLK	Output	AA7	**Transmit Clock (TCLK).** TCLK provides timing for circuitry downstream of the DS3 transmitter of the TECT3. TCLK is nominally a 44.736 MHz, 50% duty cycle clock.

Pin Name	Type	Pin No.	Function
TPOS/TDAT	Output	AB7	**Transmit Positive Pulse (TPOS).** TPOS represents the positive pulses transmitted on the B3ZS-encoded DS3 line when dual-rail output format is selected. **Transmit Data Output (TDAT).** TDAT represents the NRZ (unipolar) DS3 output data stream when single rail output format is selected. TPOS and TDAT are updated on the falling edge of TCLK by default but may be enabled to be updated on the rising edge of TCLK by setting the TRISE bit in the DS3 Master Transmit Line Options register. TPOS and TDAT are updated on TICLK rather than TCLK when the TICLK bit in the DS3 Master Transmit Line Options register is set.
TNEG/TMFP	Output	W6	**Transmit Negative Pulse (TNEG).** TNEG represents the negative pulses transmitted on the B3ZS-encoded DS3 line when dual-rail output format is selected. **Transmit Multiframe Pulse (TMFP).** This signal marks the transmit M-frame alignment when configured for single rail operation. TMFP indicates the position of overhead bits in the transmit transmission system stream, TDAT. TMFP is high during the first bit (X1) of the multiframe. TNEG and TMFP are updated on the falling edge of TCLK by default but may be enabled to be updated on the rising edge of TCLK by setting the TRISE bit in the DS3 Master Transmit Line Options register. TNEG and TMFP are updated on TICLK rather than TCLK when the TICLK bit in the DS3 Master Transmit Line Options register is set.
TICLK	Input	AA6	**Transmit input clock (TICLK).** TICLK provides the transmit direction timing. TICLK is nominally a 44.736 MHz, 50% duty cycle clock. This clock is only required when using the DS3 transmitter with the DS3 line side interface. When not used this clock input should be connected to ground.

Pin Name	Type	Pin No.	Function
XCLK/VCLK	Input	E20	**Crystal Clock Input (XCLK).** This 24 times T1 or E1 clock provides timing for many of the T1 and E1 portions of TECT3. XCLK is nominally a 37.056 MHz ± 32ppm, 50% duty cycle clock when configured for T1 modes and is nominally a 49.152 MHz ± 32ppm, 50% duty cycle clock when configured for E1 modes. This clock is required for all operating modes of the TECT3. **Test Vector Clock (VCLK).** This signal is used during production testing.
DS3 System Side Interface			
RGAPCLK/RSCLK	Output	Y3	**Framer Recovered Gapped Clock (RGAPCLK).** RGAPCLK is valid when the TECT3 is configured as a DS3 framer by setting the OPMODE[1:0] bits in the Global Configuration register and the RXGAPEN bit in the DS3 Master Unchannelized Interface Options register. RGAPCLK is the recovered clock and timing reference for RDATO. RGAPCLK is held either high or low during bit positions which correspond to overhead. **Framer Recovered Clock (RSCLK).** RSCLK is valid when the TECT3 is configured as a DS3 framer by setting the OPMODE[1:0] bits in the Global Configuration register. RSCLK is the recovered clock and timing reference for RDATO, RFPO/RMFPO, and ROVRHD. This signal shares a signal pin with ICLK[1]. When enabled for unchannelized DS3 operation this signal will be RGAPCLK/RSCLK, otherwise it will be ICLK[1].
RDATO	Output	AA5	**Framer Receive Data (RDATO).** RDATO is valid when the TECT3 is configured as a DS3 framer by setting the OPMODE[1:0] bits in the Global Configuration register. RDATO is the received data aligned to RFPO/RMFPO and ROVRHD. RDATO is updated on either the falling or rising edge of RGAPCLK or RSCLK, depending on the value of

Pin Name	Type	Pin No.	Function
			the RSCLKR bit in the DS3 Master Unchannelized Interface Options register. By default RDATO will be updated on the falling edge of RGAPCLK or RSCLK. This signal shares a signal pin with ID[1] and MVID[1]. This signal will be RDATO only when enabled for unchannelized DS3 operation.
RFPO/RMFPO	Output	AB5	**Framer Receive Frame Pulse/Multi-frame Pulse (RFPO/RMFPO).** RFPO/RMFPO is valid when the TECT3 is configured to be in framer only mode by setting the OPMODE[1:0] bits in the Global Configuration register. RFPO is aligned to RDATO and indicates the position of the first bit in each DS3 M-subframe. RMFPO is aligned to RDATO and indicates the position of the first bit in each DS3 M-frame. This is selected by setting the RXMFPO bit in the Master Framer Configuration Registers. RFPO/RMFPO is updated on either the falling or rising edge of RSCLK depending on the setting of the RSCLKR bit in the DS3 Master Unchannelized Interface Options register. This signal shares a signal pin with IFP[1]. When enabled for unchannelized DS3 operation this signal will be RFPO/RMFPO, otherwise it will be IFP[1].
ROVRHD	Output	Y6	**Framer Receive Overhead (ROVRHD).** ROVRHD is valid when the TECT3 is configured as a DS3 framer by setting the OPMODE[1:0] bits in the Global Configuration register. ROVRHD will be high whenever the data on RDATO corresponds to an overhead bit position. ROVRHD is updated on the either the falling or rising edge of RSCLK depending on the setting of the RSCLKR bit in the DS3 Master Unchannelized Interface Options register. This signal shares a signal pin with ID[2] and CASID[1]. This signal will be ROVRHD only when enabled for unchannelized DS3 operation.

Pin Name	Type	Pin No.	Function
TFPO/TMFPO/ TGAPCLK	Output	AB3	**Framer Transmit Frame Pulse/Multi-frame Pulse Reference (TFPO/TMFPO).** TFPO/TMFPO is valid when the TECT3 is configured as a DS3 framer by setting the OPMODE[1:0] bits in the Global Configuration register and setting the TXGAPEN bit to 0 in the DS3 Master Unchannelized Interface Options register. TFPO pulses high for 1 out of every 85 clock cycles, giving a reference M-subframe indication. TMFPO pulses high for 1 out of every 4760 clock cycles, giving a reference M-frame indication. TFPO/TMFPO is updated on the falling edge of TICLK. TFPO/TMFPO can be configured to be updated on the rising edge of TICLK by setting the TDATIFALL bit to 1in the DS3 Master Unchannelized Interface Options register.. **Framer Gapped Transmit Clock (TGAPCLK).** TGAPCLK is valid when the TECT3 is configured as a DS3 framer by setting the OPMODE[1:0] bits in the Global Configuration register and setting the TXGAPEN bit to 1 in the DS3 Master Unchannelized Interface Options register. TGAPCLK is derived from the transmit reference clock TICLK or from the receive clock if loop-timed. The overhead bit (gapped) positions are generated internal to the device. TGAPCLK is held high during the overhead bit positions. This clock is useful for interfacing to devices which source payload data only. TGAPCLK is used to sample TDATI and TFPI/TMFPI when TXGAPEN is set to 1. This signal shares a signal pin with ECLK[1]. When enabled for unchannelized DS3 operation this signal will be TFPO/TMFPO/TGAPCLK, otherwise it will be ECLK[1].
TDATI	Input	AB4	**Framer Transmit Data (TDATI).** TDATI contains the serial data to be transmitted when the TECT3 is configured as a DS3 framer by setting the

Pin Name	Type	Pin No.	Function
			OPMODE[1:0] bits in the Global Configuration register. TDATI is sampled on the rising edge of TICLK if the TXGAPEN bit in the DS3 Master Unchannelized Interface Options register is logic 0. If TXGAPEN is logic 1, then TDATI is sampled on the rising edge of TGAPCLK. TDATI can be configured to be sampled on the falling edge of TICLK or TGAPCLK by setting the TDATIFALL bit in the DS3 Master Unchannelized Interface Options register. This signal shares a signal pin with ED[1] and MVED[1]. This signal will be TDATI only when enabled for unchannelized DS3 operation.
TFPI/TMFPI	Input	AA3	**Framer Transmit Frame Pulse/Multiframe Pulse (TFPI/TMFPI).** TFPI/TMFPI is valid when the TECT3 is configured as a DS3 framer by setting the OPMODE[1:0] bits in the Global Configuration register. TFPI indicates the position of all overhead bits in each DS3 M-subframe. TFPI is not required to pulse at every frame boundary. TMFPI indicates the position of the first bit in each DS3 M-frame. TMFPI is not required to pulse at every multiframe boundary. TFPI/TMFPI is sampled on the rising edge of TICLK if the TXGAPEN bit in the DS3 Master Unchannelized Interface Options register is logic 0. If TXGAPEN is logic 1, then TFPI/TMFPI is sampled on the rising edge of TGAPCLK. TFPI/TMFPI can be configured to be sampled on the falling edge of TICLK or TGAPCLK by setting the TDATIFALL bit to 1in the DS3 Master Unchannelized Interface Options register. This signal shares a signal pin with ED[2] and CASED[1]. This signal will be TFPI/TMFPI only when enabled for unchannelized DS3 operation.

Pin Name	Type	Pin No.	Function
T1 and E1 System Side Serial Clock and Data Interface			
ICLK[1]/ISIG[1] ICLK[2]/ISIG[2] ICLK[3]/ISIG[3] ICLK[4]/ISIG[4] ICLK[5]/ISIG[5] ICLK[6]/ISIG[6] ICLK[7]/ISIG[7] ICLK[8]/ISIG[8] ICLK[9]/ISIG[9] ICLK[10]/ISIG[10] ICLK[11]/ISIG[11] ICLK[12]/ISIG[12] ICLK[13]/ISIG[13] ICLK[14]/ISIG[14] ICLK[15]/ISIG[15] ICLK[16]/ISIG[16] ICLK[17]/ISIG[17] ICLK[18]/ISIG[18] ICLK[19]/ISIG[19] ICLK[20]/ISIG[20] ICLK[21]/ISIG[21] ICLK[22]/ISIG[22] ICLK[23]/ISIG[23] ICLK[24]/ISIG[24] ICLK[25]/ISIG[25] ICLK[26]/ISIG[26] ICLK[27]/ISIG[27] ICLK[28]/ISIG[28]	Output	Y3 AB2 AB20 AB21 W22 Y20 H22 F19 W3 AA1 H3 H1 L22 K19 F22 G20 T3 U1 D1 C1 H19 G19 E19 F21 K3 J4 E3 D2	**Ingress Clocks (ICLK[1:28]).** The Ingress Clocks are active when the external signaling interface is disabled. Each ingress clock is optionally a smoothed (jitter attenuated) version of the associated receive clock from the DS3 multiplexer. When the Clock Master: NxChannel mode is active, ICLK[x] is a gapped version of the smoothed receive clock. When Clock Master: Full T1/E1 mode is active, IFP[x] and ID[x] are updated on the active edge of ICLK[x]. When the Clock Master: NxDS0 mode is active, ID[x] is updated on the active edge of ICLK[x]. **Ingress Signaling (ISIG[1:28]).** When the Clock Slave: External Signaling mode is enabled, each ISIG[x] contains the extracted signaling bits for each channel in the frame, repeated for the entire superframe. Each channel's signaling bits are valid in bit locations 5,6,7,8 of the channel and are channel-aligned with the ID[x] data stream. ISIG[x] is updated on the active edge of the common ingress clock, CICLK. In E1 mode only ICLK[1:21] and ISIG[1:21] are used. ICLK[1]/ISIG[1] shares a pin with the DS3 system interface signal RGAPCLK/RSCLK.
IFP[1] IFP[2] IFP[3] IFP[4] IFP[5] IFP[6] IFP[7] IFP[8] IFP[9] IFP[10] IFP[11]	Output	AB5 V3 W20 AA22 Y21 W21 K22 K21 Y1 W1 F4	**Ingress Frame Pulse (IFP[1:28]).** The IFP[x] outputs are intended as timing references. IFP[x] indicates the frame alignment or the superframe alignment of the ingress stream, ID[x]. When Clock Master: Full T1/E1 mode is active, IFP[x] is updated on the active edge of the associated ICLK[x]. When Clock Master: NxDS0 mode is active, ICLK[x] is gapped during the pulse on IFP[x]. When the Clock Slave ingress modes are active, IFP[x] is updated on the active edge of CICLK. I the Clear

Pin Name	Type	Pin No.	Function
IFP[12] IFP[13] IFP[14] IFP[15] IFP[16] IFP[17] IFP[18] IFP[19] IFP[20] IFP[21] IFP[22] IFP[23] IFP[24] IFP[25] IFP[26] IFP[27] IFP[28]		G1 V20 Y22 K20 J19 W4 V1 E1 D9 U19 R22 J22 J20 K1 K2 D8 A9	Channel modes IFP[x] is not used. In E1 mode only IFP[1:21] is used. IFP[1] shares a pin with the DS3 system interface signal RFPO/RMFPO. IFP[20,27,28] shares pins with the SBI interface signals SDDP, SDPL, SDV5.
ID[1] ID[2] ID[3] ID[4] ID[5] ID[6] ID[7] ID[8] ID[9] ID[10] ID[11] ID[12] ID[13] ID[14] ID[15] ID[16] ID[17] ID[18] ID[19] ID[20] ID[21] ID[22] ID[23] ID[24]	Output	AA5 Y6 AA20 T19 R19 P20 G22 G21 Y2 W2 G4 H2 P21 P22 A12 D12 U2 V4 D11 A11 M19 L19 D10 A10	**Ingress Data (ID[1:28]).** Each ID[x] signal contains the recovered data stream which may have been passed through the elastic store. When the Clock Slave ingress modes are active, the ID[x] stream has passed through the elastic store and is aligned to the common ingress timing. In this mode ID[x] is updated on the active edge of CICLK. When the Clock Master ingress modes are active, ID[x] is aligned to the receive line timing and is updated on the active edge of the associated ICLK[x]. In E1 mode only ID[1:21] are used. ID[1,5,9,13,17,21,25] share pins with the H-MVIP data signals MVID[1:7]. ID[2,6,10,14,18,22,26] share pins with the H-MVIP CAS signals CASID[1:7]. ID[1] shares a pin with the DS3 system interface signal RDATO. ID[2] shares a pin with the DS3 system interface signal ROVRHD. ID[15,16,19,20,23,24,27,28] shares pins with the SBI interface bus SDDATA[7:0].

Pin Name	Type	Pin No.	Function
ID[25] ID[26] ID[27] ID[28]		J1 H4 B10 C10	
CICLK	Input	N1	**Common Ingress Clock (CICLK).** CICLK is either a 1.544MHz clock in T1 mode or a 2.048MHz clock in T1 or E1 modes, with optional gapping for adaptation to non-uniform backplane data streams. CICLK is common to all 28 T1 or 21 E1 framers. CIFP is sampled on the active edge of CICLK. When the Clock Slave ingress modes are active, ID[x], ISIG[x], and IFP[x] are updated on the active edge of CICLK. CICLK is a nominal 1.544 or 2.048 MHz clock +/- 50ppm with a 50% duty cycle. This signal shares a pin with the H-MVIP signal CMVFPC. By default this input is CICLK.
CIFP	Input	P4	**Common Ingress Frame Pulse (CIFP).** When the elastic store is enabled (Clock Slave mode is active on the ingress side), CIFP is used to frame align the ingress data to the system frame alignment. CIFP is common to all 28 T1 or 21 E1 framers. When frame alignment is required, a pulse at least 1 CICLK cycle wide must be provided on CIFP a maximum of once every frame (nominally 193 or 256 bit times). CIFP is sampled on the active edge of CICLK as selected by the CIFE bit in the Master Common Ingress Serial and H-MVIP Interface Configuration register.
CTCLK	Input	M3	**Common Transmit Clock (CTCLK).** This input signal is used as a reference transmit tributary clock which can be used in egress Clock Master modes. Depending on the configuration of the TECT3, CTCLK may be a line rate clock (so the transmit clock is generated directly from CTCLK, or from CTCLK after jitter attenuation), or a multiple of 8kHz (Nx8khz, where $1 \leq N \leq 256$) so long as CTCLK is jitter-free when divided down to 8kHz (in which case the transmit clock is

Pin Name	Type	Pin No.	Function
			derived by the DJAT PLL using CTCLK as a reference). The TECT3 may be configured to ignore the CTCLK input and utilize CECLK or one of the recovered Ingress clocks instead, RECVCLK1 and RECVCLK2. Receive tributary clock[x] is automatically substituted for CTCLK if line loopback is enabled.
CECLK	Input	N4	**Common Egress Clock (CECLK).** The common egress clock is used to time the egress interface when Clock Slave mode is enabled in the egress side. CECLK may be a 1.544MHz or 2.048MHz clock with optional gapping for adaptation from non-uniform system clocks. When the Clock Slave: EFP Enabled mode is active, CEFP and ED[x] are sampled on the active edge of CECLK, and EFP[x] is updated on the active edge of CECLK. When the Clock Slave: External Signaling mode is active, CEFP, ESIG[x] and ED[x] are sampled on the active edge of CECLK. CECLK is a nominal 1.544 or 2.048 MHz clock +/- 50ppm with a 50% duty cycle. This signal shares a pin with the H-MVIP signal CMV8MCLK. By default this input is CECLK.
CEFP	Input	M2	**Common Egress Frame Pulse (CEFP).** CEFP may be used to frame align the framers to the system backplane. If frame alignment only is required, a pulse at least 1 CECLK cycle wide must be provided on CEFP every 193 bit times for T1 mode or every 256 bit times for T1 and E1 modes (T1 mode using 2.048MHz clock). If superframe alignment is required, transmit superframe alignment must be enabled, and a pulse at least 1 CECLK cycle wide must be provided on CEFP every 12 or 24 frame times for T1 mode, on the first F-bit of the multiframe. CEFP is sampled on the active edge of CECLK as selected by the CEFE bit in the Master Common Egress Serial and H-MVIP Interface Configuration register. CEFP has no effect in the Clock Master egress modes.

Pin Name	Type	Pin No.	Function
			This signal shares a pin with the H-MVIP signal CMVFPB. By default this input is CEFP.
ED[1] ED[2] ED[3] ED[4] ED[5] ED[6] ED[7] ED[8] ED[9] ED[10] ED[11] ED[12] ED[13] ED[14] ED[15] ED[16] ED[17] ED[18] ED[19] ED[20] ED[21] ED[22] ED[23] ED[24] ED[25] ED[26] ED[27] ED[28]	Input	AB4 AA3 P19 N20 N21 N22 A7 A2 T2 R4 A3 B4 N19 M22 D6 C7 P2 M1 D4 B6 C20 E22 A5 B5 L1 L2 A4 C5	**Egress Data (ED[1:28]).** The egress data streams to be transmitted are input on these pins. When the Clock Master modes are active, ED[x] is sampled on the active edge of ECLK[x], except for Clock Master: Serial Data and H-MVIP CCS, when ED[x] is sampled on the active edge of ICLK[x]. When the Clock Slave egress modes are active, ED[x] is sampled on the active edge of CECLK, except for Clock Slave: Clear channel mode when ED[x] is sampled on the active edge of ECLK[x]. In E1 mode only ED[1:21] are used. ED[1,5,9,13,17,21,25] share pins with the H-MVIP data signals MVED[1:7]. ED[2,6,10,14,18,22,26] share pins with the H-MVIP CAS signals CASED[1:7]. ED[1] shares a pin with the DS3 system interface signal TDATI. ED[2] shares a pin with the DS3 system interface signal TFPI/TMFPI. ED[7,8,11,12,15,16,19,20,23,24,27,28] shares pins with the SBI interface add bus signals.

Pin Name	Type	Pin No.	Function
ECLK[1]/EFP[1]/ESIG[1] ECLK[2]/EFP[2]/ESIG[2] ECLK[3]/EFP[3]/ESIG[3] ECLK[4]/EFP[4]/ESIG[4] ECLK[5]/EFP[5]/ESIG[5] ECLK[6]/EFP[6]/ESIG[6] ECLK[7]/EFP[7]/ESIG[7] ECLK[8]/EFP[8]/ESIG[8] ECLK[9]/EFP[9]/ESIG[9] ECLK[10]/EFP[10]/ESIG[10] ECLK[11]/EFP[11]/ESIG[11] ECLK[12]/EFP[12]/ESIG[12] ECLK[13]/EFP[13]/ESIG[13] ECLK[14]/EFP[14]/ESIG[14] ECLK[15]/EFP[15]/ESIG[15] ECLK[16]/EFP[16]/ESIG[16] ECLK[17]/EFP[17]/ESIG[17] ECLK[18]/EFP[18]/ESIG[18] ECLK[19]/EFP[19]/ESIG[19] ECLK[20]/EFP[20]/ESIG[20] ECLK[21]/EFP[21]/ESIG[21] ECLK[22]/EFP[22]/ESIG[22] ECLK[23]/EFP[23]/ESIG[23] ECLK[24]/EFP[24]/ESIG[24] ECLK[25]/EFP[25]/ESIG[25] ECLK[26]/EFP[26]/ESIG[26] ECLK[27]/EFP[27]/ESIG[27] ECLK[28]/EFP[28]/ESIG[28]	I/O	AB3 Y4 Y19 AA21 AB22 V22 T21 T22 AB1 T1 G2 G3 U21 V19 D21 C21 U4 R1 D3 F1 T20 U22 B22 D20 L3 K4 E4 F2	**Egress Clock (ECLK[1:28]).** When the Clock Master mode is active, ECLK[x] is an output and is used to sample the associated egress data, ED[x]. ECLK[x] is a version of the transmit clock[x] which is generated from the receive clock or the common transmit clock, CTCLK. When in Clock Master: NxChannel mode, ECLK[x] is gapped during the framing bit position and optionally for between 1 and 23 DS0 channels or 1 and 32 channel timeslots in the associated ED[x] stream. When Clock Master: Clear Channel is active ECLK[x] is not gapped. When in Clock Slave: Clear Channel mode this input is an input and is used to sampled ED[x]. ED[x] is sampled on the active edge of the associated ECLK[x]. **Egress Frame Pulse (EFP[1:28]).** When the Clock Slave: EFP Enabled mode is active, the EFP[1:28] outputs indicate the frame alignment or the superframe alignment of each of the 28 framers. EFP[x] is updated on the active edge of CECLK. **Egress Signaling (ESIG[1:28]).** When the Clock Slave: External Signaling mode is active, the ESIG[1:28] input carries the signaling bits for each channel in the transmit data frame, repeated for the entire superfram'. Each channel's signaling bits are in bit locations 5,6,7,8 of the channel and are frame-aligned by the common egress frame pulse, CEFP. ESIG[x] is sampled on the active edge of CECLK.

Pin Name	Type	Pin No.	Function
			ECLK[1]/EFP[1]/ESIG[1] shares a pin with the DS3 system interface output signal TFPO/TMFPO/TGAPCLK.
H-MVIP System Side Interfaces			
CMV8MCLK	Input	N4	**Common 8M H-MVIP Clock (CMV8MCLK).** The common 8.192 Mbps H-MVIP data provides the data clock for receive and transmit links configured for operation in 8.192 Mbps H-MVIP mode. CMV8MCLK is used to sample data on MVID[1:7], MVED[1:7], CASID[1:7], CASED[1:7], CCSID and CCSED. CMV8MCLK is nominally a 50% duty cycle clock with a frequency of 16.384MHz. The H-MVIP interfaces are enabled via the SYSOPT[2:0] bits in the Global Configuration register. This signal shares a pin with CECLK. By default this input is CECLK.
CMVFPC	Input	N1	**Common H-MVIP Frame Pulse Clock (CMVFPC).** The common 8.192 Mbps H-MVIP frame pulse clock provides the frame pulse clock for receive and transmit links configured for operation in 8.192 Mbps H-MVIP mode. CMVFPC is used to sample CMVFPB. CMVFPC is nominally a 50% duty cycle clock with a frequency of 4.096 MHz. The falling edge of CMVFPC must be aligned with the falling edge of CMV8MCLK with no more than ±10ns skew. The H-MVIP interfaces are enabled via the SYSOPT[2:0] bits in the Global Configuration register. This signal shares a pin with CICLK. By default this input is CICLK.
CMVFPB	Input	M2	**Common H-MVIP Frame Pulse (CMVFPB).** The active low common frame pulse for 8.192 Mbps H-MVIP signals references the beginning of each frame for links operating in 8.192Mbps H-MVIP mode. The H-MVIP interfaces are enabled via the

Pin Name	Type	Pin No.	Function
			SYSOPT[2:0] bits in the Global Configuration register. The CMVFPB frame pulse occurs every 125us for a and is sampled on the falling edge of CMVFPC. This signal shares a pin with CEFP. By default this input is CEFP.
MVID[1] MVID[2] MVID[3] MVID[4] MVID[5] MVID[6] MVID[7]	Output	AA5 R19 Y2 P21 U2 M19 J1	**H-MVIP Ingress Data (MVID[1:7]).** MVID[x] carries the recovered T1 or E1 channels which have passed through the elastic store. Each MVID[x] signal carries the channels of four complete T1s or E1s. MVID[x] carries the T1 or E1 data equivalent to ID[(4x-3):(4x)]. MVID[x] is aligned to the common H-MVIP 16.384Mb/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. MVID[x] is updated on every second rising or falling edge of the common H-MVIP 16.384Mb /s clock, CMV8MCLK, as fixed by the common H-MVIP frame pulse clock, CMVFPC. The updating edge of CMV8MCLK is selected via the CMVIDE bit in the Master Common Ingress Serial and H-MVIP Interface Configuration register. In E1 mode only MVID[1:6] are used. MVID[1:7] shares the same pins as ID[1,5,9,13,17,21,25].
CASID[1] CASID[2] CASID[3] CASID[4] CASID[5] CASID[6] CASID[7]	Output	Y6 P20 W2 P22 V4 L19 H4	**Channel Associated Signaling Ingress Data (CASID[1:7]).** CASID[x] carries the channel associated signaling stream extracted from all the T1 or E1 channels. Each CASID[x] signal carries CAS for four complete T1s or E1s. CASID[x] carries the corresponding CAS values of the channel carried in MVID[x]. CASID[x] is aligned to the common H-MVIP 16.384Mb/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CASID[x] is updated on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The updating edge of CMV8MCLK is selected via the CMVIDE bit in the Master Common Ingress Serial and H-MVIP Interface

Pin Name	Type	Pin No.	Function
			Configuration register. CASID[1:7] shares the same pins as ID[2,6,10,14,18,22,26].
CCSID	Output	T4	**Common Channel Signaling Ingress Data (CCSID).** In T1 mode CCSID carries the 28 common channel signaling channels extracted from each of the 28 T1s. In E1 mode CCSID carries up to 3 timeslots (15,16, 31) from each of the 21 E1s. CCSID is formatted according to the H-MVIP standard. CCSID is aligned to the common H-MVIP 16.384Mb/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CCSID is updated on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The updating edge of CMV8MCLK is selected via the CMVIDE bit in the Master Common Ingress Serial and H-MVIP Interface Configuration register.
MVED[1] MVED[2] MVED[3] MVED[4] MVED[5] MVED[6] MVED[7]	Input	AB4 N21 T2 N19 P2 C20 L1	**MVIP Egress Data (MVED[1:7]).** The egress data streams to be transmitted are input on these pins. Each MVED[x] signal carries the channels of four complete T1s formatted according to the H-MVIP standard. MVED[x] carries the egress data equivalent to ED[(4x-3):(4x)]. MVID[x] is aligned to the common H-MVIP 16.384Mb/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. MVID[x] is sampled on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The sampling edge of CMV8MCLK is selected via the CMVEDE bit in the Master Common Ingress Serial and H-MVIP Interface Configuration register. In E1 mode only MVED[1:6] are used. MVED[1:7] shares the same pins as ED[1,5,9,13,17,21,25].
CASED[1] CASED[2] CASED[3]	Input	AA3 N22 R4	**Channel Associated Signaling Egress Data (CASED[1:7]).** CASED[x] carries the channel associated signaling stream to be transmitted in the T1

Pin Name	Type	Pin No.	Function
CASED[4] CASED[5] CASED[6] CASED[7]		M22 M1 E22 L2	DS0s or E1 timeslots. Each CASED[x] signal carries CAS for four complete T1s or E1s formatted according to the H-MVIP standard. CASED[x] carries the corresponding CAS values of the channel data carried in MVED[x]. CASED[x] is aligned to the common H-MVIP 16.384Mb/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CASED[x] is sampled on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The sampling edge of CMV8MCLK is selected via the CMVEDE bit in the Master Common Ingress Serial and H-MVIP Interface Configuration register. CASED[1:7] shares the same pins as ED[2,6,10,14,18,22,26].
CCSED	Input	P1	**Common Channel Signaling Egress Data (CCSED).** In T1 mode CCSED carries the 28 common channel signaling channels to be transmitted in each of the 28 T1s. In E1 mode CCSED carries up to 3 timeslots (15,16, 31) to be transmitted in each of the 21 E1s. CCSED is formatted according to the H-MVIP standard. CCSED is aligned to the common H-MVIP 16.384Mb/s clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CCSED is sampled on every second rising or falling edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. The sampling edge of CMV8MCLK is selected via the CMVEDE bit in the Master Common Ingress Serial and H-MVIP Interface Configuration register.

Pin Name	Type	Pin No.	Function
Recovered T1 and E1 Clocks			
RECVCLK1	Output	D22	**Recovered Clock 1 (RECVCLK1).** This clock output is a recovered and de-jittered clock from any one of the 28 T1 framers or 21 E1 framers.
RECVCLK2	Output	C22	**Recovered Clock 2 (RECVCLK2).** This clock output is a recovered and de-jittered clock from any one of the 28 T1 framers or 21 E1 framers.
Scaleable Bandwidth Interconnect Interface			
SREFCLK	Input	B7	**System Reference Clock (SREFCLK).** This system reference clock is a nominal 19.44MHz +/-50ppm 50% duty cycle clock. This clock is common to both the add and drop sides of the SBI bus.
SC1FP	I/O	A6	**System C1 Frame Pulse (SC1FP).** The System C1 Frame Pulse is used to synchronize devices interfacing to the SBI bus. This signal is common to both the add and drop sides of the system SBI bus. By default, SC1FP is an input. The TECT3 can alternatively be configured to generate this frame pulse - as an output on SC1FP - for use by all other devices connected to the same SBI bus. Note that all devices interconnected via an SBI interface must be synchronized to an SC1FP signal from a single common source. As an input, SC1FP is sampled on the rising edge of SREFCLK. It normally indicates SBI mutiframe alignment, and thus should be asserted for a single SREFCLK cycle every 9720 SREFCLK cycles or some multiple thereof (i.e. every 9720*N SREFCLK cycles, where N is a positive integer). In synchronous SBI mode, however, SC1FP is used to indicate T1 signaling multiframe alignment, and thus should be asserted for a single SREFCLK cycle once every 12 SBI mutiframes (48 T1 frames or 116640 SREFCLK cycles). As an output, SC1FP is generated on the rising edge

Pin Name	Type	Pin No.	Function
			of SREFCLK. It normally indicates SBI mutiframe alignment by pulsing high once every 9720 SREFCLK cycles. In synchronous SBI mode, however, SC1FP is used to indicate T1 signaling multiframe alignment by pulsing once every 12 SBI mutiframes (48 T1 frames or 116640 SREFCLK cycles).
SADATA[0] SADATA[1] SADATA[2] SADATA[3] SADATA[4] SADATA[5] SADATA[6] SADATA[7]	Input	D6 C7 D4 B6 A5 B5 A4 C5	**System Add Bus Data (SADATA[7:0]).** The System add data bus is a time division multiplexed bus which carries the T1 and DS3 tributary data is byte serial format over the SBI bus structure. This device only monitors the add data bus during the timeslots assigned to this device. SADATA[7:0] is sampled on the rising edge of SREFCLK. This bus shares pins with ED[15,16,19,20,23,24,27,28].
SADP	Input	A2	**System Add Bus Data Parity (SADP).** The system add bus signal carries the even or odd parity for the add bus signals SADATA[7:0], SAPL and SAV5. The TECT3 monitors parity across all links on the add bus. SADP is sampled on the rising edge of SREFCLK. This signal shares a pin with signal ED[8].
SAPL	Input	B4	**System Add Bus Payload Active (SAPL).** The add bus payload active signal indicates valid data within the SBI bus structure. This signal must be high during all octets making up a tributary. This signal goes high during the V3 or H3 octet of a tributary to indicate negative timing adjustments between the tributary rate and the fixed SBI bus structure. This signal goes low during the octet after the V3 or H3 octet of a tributary to indicate positive timing adjustments between the tributary rate and the fixed SBI bus structure. The TECT3 only monitors the add bus payload active signal during the tributary timeslots assigned to this device. SAPL is sampled on the rising edge of SREFCLK.

Pin Name	Type	Pin No.	Function
			This signal shares a pin with signal ED[12].
SAV5	Input	A3	**System Add Bus Payload Indicator (SAV5).** The add bus payload indicator locates the position of the floating payloads for each tributary within the SBI bus structure. Timing differences between the tributary timing and the synchronous SBI bus are indicated by adjustments of this payload indicator relative to the fixed SBI bus structure. All timing adjustments indicated by this signal must be accompanied by appropriate adjustments in the SAPL signal. The TECT3 only monitors the add bus payload Indicator signal during the tributary timeslots assigned to this device. SAV5 is sampled on the rising edge of SREFCLK. This signal shares a pin with signal ED[11].
SAJUST_REQ	Output Tristate	D7	**System Add Bus Justification Request (SAJUST_REQ).** The justification request signals the Link Layer device to speed up, slow down or maintain the rate which it is sending data to the TECT3. This is only used when the TECT3 is the timing master for the tributary transmit direction. This active high signal indicates negative timing adjustments when asserted high during the V3 or H3 octet of the tributary. In response to this the Link Layer device sends an extra byte in the V3 or H3 octet of the next SBI bus multi-frame. Positive timing adjustments are requested by asserting justification request high during the octet following the V3 or H3 octet. The Link Layer device responds to this request by not sending an octet during the V3 or H3 octet of the next multi-frame. The TECT3 only drives the justification request signal during the tributary timeslots assigned to this device. SAJUST_REQ is updated on the rising edge of SREFCLK.

Pin Name	Type	Pin No.	Function
SDDATA[0] SDDATA[1] SDDATA[2] SDDATA[3] SDDATA[4] SDDATA[5] SDDATA[6] SDDATA[7]	Output Tristate	A12 D12 D11 A11 D10 A10 B10 C10	**System Drop Bus Data (SDDATA[7:0]).** The System drop data bus is a time division multiplexed bus which carries the T1 and DS3 tributary data is byte serial format over the SBI bus structure. This device only drives the data bus during the timeslots assigned to this device. SDDATA[7:0] is updated on the rising edge of SREFCLK. This bus shares pins with ID[15,16,19,20,23,24,27,28].
SDDP	Output Tristate	D9	**System Drop Bus Data Parity (SDDP).** The system drop bus signal carries the even or odd parity for the drop bus signals SDDATA[7:0], SDPL and SDV5. The TECT3 only drives the data bus parity during the timeslots assigned to this device unless configured for bus master mode. In this case, all undriven links should be driven externally with correctly generated parity. SDDP is updated on the rising edge of SREFCLK. This signal shares a pin with IFP[20].
SDPL	Output Tristate	D8	**System Drop Bus Payload Active (SDPB).** The payload active signal indicates valid data within the SBI bus structure. This signal is asserted during all octets making up a tributary. This signal goes high during the V3 or H3 octet of a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI bus structure. This signal goes low during the octet after the V3 or H3 octet of a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI bus structure. The TECT3 only drives the payload active signal during the tributary timeslots assigned to this device. SDPL is updated on the rising edge of SREFCLK. This signal shares a pin with IFP[27].
SDV5	Output Tristate	A9	**System Drop Bus Payload Indicator (SDV5).** The payload indicator locates the position of the floating payloads for each tributary within the SBI bus

Pin Name	Type	Pin No.	Function
			structure. Timing differences between the tributary timing and the synchronous SBI bus are indicated by adjustments of this payload indicator relative to the fixed SBI bus structure. All timing adjustments indicated by this signal are accompanied by appropriate adjustments in the SDPL signal. The TECT3 only drives the payload Indicator signal during the tributary timeslots assigned to this device. SDV5 is updated on the rising edge of SREFCLK. This signal shares a pin with IFP[28].
SBIACT	Output	A8	**SBI Output Active (SBIACT).** The SBI Output Active indicator is high whenever the TECT3 is driving the SBI drop bus signals. This signal is used by other TECT3s or other SBI devices to detect SBI configuration problems by detecting other devices driving the SBI bus during the same tributary as the device listening to this signal. This output is updated on the rising edge or SREFCLK.
CLK52M	Input	P3	**52MHz Clock Reference (CLK52M).** The 52Mhz clock reference is used to generate a gapped DS3 clock when receiving a DS3 from the SBI bus interface. This clock has two nominal values. The first is a nominal 51.84MHz 50% duty cycle clock. The second is a nominal 44.928MHz 50% duty cycle clock. When this clock is not used this input must be connected to ground.
SBIDET[0] SBIDET[1]	Input	C8 A7	**SBI Bus Activity Detection (SBIDET[1:0]).** The SBI bus activity detect input detects tributary collisions between devices sharing the same SBI bus. Each SBI device driving the bus also drives an SBI active signal (SBIACT). This pair of activity detection inputs monitors the active signals from two other SBI devices. When unused this signal should be connected to ground.

Pin Name	Type	Pin No.	Function
			A collision is detected when either of SBIDET[1:0] signals are active concurrently with this device driving SBIACT. When collisions occur the SBI drivers are disabled and an interrupt is generated to signal the collision. These signals are sampled on the rising edge of SREFCLK. SBIDET[1] is shared with serial interface signal ED[7].
Microprocessor Interface			
INTB	Output OD	A16	**Active low Open-Drain Interrupt (INTB).** This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source.
CSB	Input	D16	**Active Low Chip Select (CSB).** This signal is low during TECT3 register accesses. CSB has an integral pull up resistor.
RDB	Input	B16	**Active Low Read Enable (RDB).** This signal is low during TECT3 register read accesses. The TECT3 drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	C15	**Active Low Write Strobe (WRB).** This signal is low during a TECT3 register write access. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.

Pin Name	Type	Pin No.	Function
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	C14 B14 A14 D14 C13 B13 A13 D13	**Bidirectional Data Bus (D[7:0]).** This bus provides TECT3 register read and write accesses.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10] A[11] A[12] A[13]	Input	A17 C16 D18 D19 B17 A18 A19 A20 C18 B19 B20 A21 C19 B21	**Address Bus (A[13:0]).** This bus selects specific registers during TECT3 register accesses. Signal A[13] selects between normal mode and test mode register access. A[13] has an integral pull down resistor.
RSTB	Input	A22	**Active Low Reset (RSTB).** This signal provides an asynchronous TECT3 reset. RSTB is a Schmitt triggered input with an integral pull up resistor.
ALE	Input	D17	**Address Latch Enable (ALE).** This signal is active high and latches the address bus A[13:0] when low. When ALE is high, the internal address latches are transparent. It allows the TECT3 to interface to a multiplexed address/data bus. The ALE input has an integral pull up resistor.
JTAG Interface			
TCK	Input	C3	**Test Clock (TCK).** This signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.

Pin Name	Type	Pin No.	Function
TMS	Input	C2	**Test Mode Select (TMS).** This signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	C4	**Test Data Input (TDI).** This signal carries test data into the TECT3 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Output	B3	**Test Data Output (TDO).** This signal carries test data out of the TECT3 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	B1	**Active low Test Reset (TRSTB).** This signal provides an asynchronous TECT3 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull up resistor. TRSTB must be asserted during the power up sequence. Note that if not used, TRSTB must be connected to the RSTB input.
Miscellaneous Pins			
NO CONNECT		A1 B2 A11 AB11 AB8 W7 W8 AB9 W9 Y10 AA10 AB10 W10 Y11	**No Connect.** These pins are not connected to any internal logic.

Pin Name	Type	Pin No.	Function
Power and Ground Pins			
VDD3.3[17] VDD3.3[16] VDD3.3[15] VDD3.3[14] VDD3.3[13] VDD3.3[12] VDD3.3[11] VDD3.3[10] VDD3.3[9] VDD3.3[8] VDD3.3[7] VDD3.3[6] VDD3.3[5] VDD3.3[4] VDD3.3[3] VDD3.3[2] VDD3.3[1]	Power	N2 AA12 L21 C12 F3 M4 U3 Y5 AA9 AA14 Y18 U20 M21 F20 C17 B11 D5	**Power (VDD3.3[17:1]).** The VDD3.3[17:1] pins should be connected to a well decoupled +3.3V DC power supply.
VDD2.5[8] VDD2.5[7] VDD2.5[6] VDD2.5[5] VDD2.5[4] VDD2.5[3] VDD2.5[2] VDD2.5[1]	Power	J2 R2 AA8 AA15 R21 H21 A15 C9	**Power (VDD2.5[8:1]).** The VDD2.5[8:1] pins should be connected to a well-decoupled +2.5V DC power supply.
VSS3.3[45] VSS3.3[44] VSS3.3[43] VSS3.3[42] VSS3.3[41] VSS3.3[40] VSS3.3[39] VSS3.3[38] VSS3.3[37] VSS3.3[36] VSS3.3[35] VSS3.3[34] VSS3.3[33] VSS3.3[32]	Ground	N3 Y12 L20 B12 E2 L4 V2 AA4 Y9 W11 Y14 Y17 AA19 V21	**Ground (VSS3.3[45:1]).** The VSS3.3[45:1] pins should be connected to GND.

Pin Name	Type	Pin No.	Function
VSS3.3[31] VSS3.3[30] VSS3.3[29] VSS3.3[28] VSS3.3[27] VSS3.3[26] VSS3.3[25] VSS3.3[24] VSS3.3[23] VSS3.3[22] VSS3.3[21] VSS3.3[20] VSS3.3[19] VSS3.3[18] VSS3.3[17] VSS3.3[16] VSS3.3[15] VSS3.3[14] VSS3.3[13] VSS3.3[12] VSS3.3[11] VSS3.3[10] VSS3.3[9] VSS3.3[8] VSS3.3[7] VSS3.3[6] VSS3.3[5] VSS3.3[4] VSS3.3[3] VSS3.3[2] VSS3.3[1]		M20 J21 E21 B18 D15 C11 B8 C6 W12 W13 AA13 Y13 W14 AB14 W15 W16 AB15 W17 AB16 Y16 AA16 AB17 AB13 AB12 AA17 AB18 W18 AA18 AB19 W19 AA2	
VSSQ[4] VSSQ[3] VSSQ[2] VSSQ[1]	Ground	N3 Y12 L20 B12	**Ground (VSSQ[4:1]).** The VSSQ[4:1] pins should be connected to GND.

Pin Name	Type	Pin No.	Function
VSS2.5[8] VSS2.5[7] VSS2.5[6] VSS2.5[5] VSS2.5[4] VSS2.5[3] VSS2.5[2] VSS2.5[1]		J3 R3 Y8 Y15 R20 H20 B15 B9	**Ground (VSS2.5[8:1]).** The VSS2.5[8:1] pins should be connected to GND.
VSS[36] VSS[35] VSS[34] VSS[33] VSS[32] VSS[31] VSS[30] VSS[29] VSS[28] VSS[27] VSS[26] VSS[25] VSS[24] VSS[23] VSS[22] VSS[21] VSS[20] VSS[19] VSS[18] VSS[17] VSS[16] VSS[15] VSS[14] VSS[13] VSS[12] VSS[11] VSS[10] VSS[9] VSS[8] VSS[7] VSS[6] VSS[5] VSS[4]		J14 J13 J12 J11 J10 J9 K14 K13 K12 K11 K10 K9 L14 L13 L12 L11 L10 L9 M14 M13 M12 M11 M10 M9 N14 N13 N12 N11 N10 N9 P14 P13 P12	**Thermal Ground (VSS).** The VSS[36:1] pins should be connected to a ground plane for enhanced thermal conductivity.

Pin Name	Type	Pin No.	Function
VSS[3] VSS[2] VSS[1]		P11 P10 P9	

NOTES ON PIN DESCRIPTIONS:

1. All TECT3 inputs and bi-directionals present minimum capacitive loading and operate at TTL logic levels.

2. All TECT3 outputs and bi-directionals have at least 2 mA drive capability. The bidirectional data bus outputs, D[7:0], have 4 mA drive capability. The outputs TCLK, TPOS/TDAT, TNEG/TMFP, RGAPCLK/RSCLK, RDATAO, RFPO/RMFPO, ROVRHD, TFPO/TMFPO/TGAPCLK, SBIACT, RECVCLK1, RECVCLK2, MVID[7:0], CASID[7:0], CCSID and INTB have 4 mA drive capability. The SBI outputs , SDDATA[7:0], SDDP, SDPL, SDV5, and SAJUST_REQ, have 8 mA drive capability. The bidirectional SBI signal SC1FP has 8 mA drive capability.

3. IOL = -2mA for others.

4. Inputs RSTB, ALE, TMS, TDI, TRSTB and CSB have internal pull-up resistors.

5. Input A[13] has an internal pull-down resistor.

6. All unused inputs should be connected to GROUND.

7. All TECT3 outputs can be tristated under control of the IEEE P1149.1 test access port, even those which do not tristate under normal operation. All outputs and bi-directionals are 5 V tolerant when tristated.

8. Power to the VDD3.3 and VDDQ pins should be applied *before* power to the VDD2.5 pins is applied. Similarly, power to the VDD2.5 pins should be removed *before* power to the VDD3.3 and VDDQ pins are removed.

9. All TECT3 inputs are 5V tolerant.

9 FUNCTIONAL DESCRIPTION

9.1 T1 Framer (T1-FRMR)

The T1 framing function is provided by the T1-FRMR block. This block searches for the framing bit position in the ingress stream. It works in conjunction with the FRAM block to search for the framing bit pattern in the standard superframe (SF), or extended superframe (ESF) framing formats. When searching for frame, the FRMR simultaneously examines each of the 193 (SF) or each of the 772 (ESF) framing bit candidates. The FRAM block is addressed and controlled by the FRMR while frame synchronization is acquired.

The time required to acquire frame alignment to an error-free ingress stream, containing randomly distributed channel data (i.e. each bit in the channel data has a 50% probability of being 1 or 0), is dependent upon the framing format. For SF format, the T1-FRMR block will determine frame alignment within 4.4ms 99 times out of 100. For ESF format, the T1-FRMR will determine frame alignment within 15 ms 99 times out of 100.

Once the T1-FRMR has found frame, the ingress data is continuously monitored for framing bit errors, bit error events (a framing bit error in SF or a CRC-6 error in ESF), and severely errored framing events. The T1-FRMR also detects out-of-frame, based on a selectable ratio of framing bit errors.

The T1-FRMR can also be disabled to allow reception of unframed data.

9.2 E1 Framer (E1-FRMR)

The E1 framing function is provided by the E1-FRMR block. The E1-FRMR block searches for basic frame alignment, CRC multiframe alignment, and channel associated signaling (CAS) multiframe alignment in the incoming recovered PCM stream.

Once the E1-FRMR has found basic (or FAS) frame alignment, the incoming PCM data stream is continuously monitored for FAS/NFAS framing bit errors. Framing bit errors are accumulated in the framing bit error counter contained in the PMON block. Once the E1-FRMR has found CRC multiframe alignment, the PCM data stream is continuously monitored for CRC multiframe alignment pattern errors, and CRC-4 errors. CRC-4 errors are accumulated in the CRC error counter of the PMON block. Once the E1-FRMR has found CAS multiframe alignment, the PCM data is continuously monitored for CAS multiframe alignment pattern errors. The E1-FRMR also detects and indicates loss of basic frame, loss of CRC multiframe, and loss of CAS multiframe, based

on user-selectable criteria. The reframe operation can be initiated by software (via the E1-FRMR Frame Alignment Options Register), by excessive CRC errors, or when CRC multiframe alignment is not found within 400 ms. The E1-FRMR also identifies the position of the frame, the CAS multiframe, and the CRC multiframe.

The E1-FRMR extracts the contents of the International bits (from both the FAS frames and the NFAS frames), the National bits, and the Extra bits (from timeslot 16 of frame 0 of the CAS multiframe), and stores them in the E1-FRMR International/National Bits register and the E1-FRMR Extra Bits register. Moreover, the FRMR also extracts submultiframe-aligned 4-bit codewords from each of the National bit positions Sa4 to Sa8, and stores them in microprocessor-accessible registers that are updated every CRC submultiframe.

The E1-FRMR identifies the raw bit values for the Remote (or distant frame) Alarm (bit 3 in timeslot 0 of NFAS frames) and the Remote Signaling Multiframe (or distant multiframe) Alarm (bit 6 of timeslot 16 of frame 0 of the CAS multiframe) via the E1-FRMR International/National Bits Register, and the E1-FRMR Extra Bits Register respectively. Access is also provided to the "debounced" remote alarm and remote signaling multiframe alarm bits which are set when the corresponding signals have been a logic 1 for 2 or 3 consecutive occurrences, as per Recommendation O.162. Detection of AIS and timeslot 16 AIS are provided. AIS is also integrated, and an AIS Alarm is indicated if the AIS condition has persisted for at least 100 ms. The out of frame (OOF=1) condition is also integrated, indicating a Red Alarm if the OOF condition has persisted for at least 100 ms.

An interrupt may be generated to signal a change in the state of any status bits (OOF, OOSMF, OOCMF, AIS or RED), and to signal when any event (RAI, RMAI, AISD, TS16AISD, COFA, FER, SMFER, CMFER, CRCE or FEBE) has occurred. Additionally, interrupts may be generated every frame, CRC submultiframe, CRC multiframe or signaling multiframe.

Basic Frame Alignment Procedure

The E1-FRMR searches for basic frame alignment using the algorithm defined in ITU-T Recommendation G.706 sections 4.1.2 and 4.2.

The algorithm finds frame alignment by using the following sequence:

1. Search for the presence of the correct 7-bit FAS (‘0011011’);

2. Check that the FAS is absent in the following frame by verifying that bit 2 of the assumed non-frame alignment sequence (NFAS) TS 0 byte is a logic 1;

3. Check that the correct 7-bit FAS is present in the assumed TS 0 byte of the next frame.

If either of the conditions in steps 2 or 3 are not met, a new search for frame alignment is initiated in the bit immediately following the second 7-bit FAS sequence check. This "hold-off" is done to ensure that new frame alignment searches are done in the next bit position, modulo 512. This facilitates the discovery of the correct frame alignment, even in the presence of fixed timeslot data imitating the FAS.

Once frame alignment is found, the block sets the OOF indication low, indicates a change of frame alignment (if it occurred), and monitors the frame alignment signal, indicating errors occurring in the 7-bit FAS pattern and in bit 2 of NFAS frames, and indicating the debounced value of the Remote Alarm bit (bit 3 of NFAS frames). Using debounce, the Remote Alarm bit has <0.00001% probability of being falsely indicated in the presence of a 10^{-3} bit error rate. The block declares loss of frame alignment if 3 consecutive FASs have been received in error or, additionally, if bit 2 of NFAS frames has been in error for 3 consecutive occasions. In the presence of a random 10^{-3} bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of >12 minutes.

The E1-FRMR can be forced to initiate a basic frame search at any time when any of the following conditions are met:

- the software re-frame bit in the E1-FRMR Frame Alignment Options register goes to logic 1;
- the CRC Frame Find Block is unable to find CRC multiframe alignment; or
- the CRC Frame Find Block accumulates excessive CRC evaluation errors ($\geq$ 915 CRC errors in 1 second) and is enabled to force a re-frame under that condition.

CRC Multiframe Alignment Procedure

The E1-FRMR searches for CRC multiframe alignment by observing whether the International bits (bit 1 of TS 0) of NFAS frames follow the CRC multiframe alignment pattern. Multiframe alignment is declared if at least two valid CRC

multiframe alignment signals are observed within 8 ms, with the time separating two alignment signals being a multiple of 2 ms

Once CRC multiframe alignment is found, the OOCMFV register bit is set to logic 0, and the E1-FRMR monitors the multiframe alignment signal, indicating errors occurring in the 6-bit MFAS pattern, errors occurring in the received CRC and the value of the FEBE bits (bit 1 of frames 13 and 15 of the multiframe). The E1-FRMR declares loss of CRC multiframe alignment if basic frame alignment is lost. However, once CRC multiframe alignment is found, it cannot be lost due to errors in the 6-bit MFAS pattern.

Under the CRC-to-non-CRC interworking algorithm, if the E1-FRMR can achieve basic frame alignment with respect to the incoming PCM data stream, but is unable to achieve CRC-4 multiframe alignment within the subsequent 400 ms, the distant end is assumed to be a non CRC-4 interface. The details of this algorithm are illustrated in the state diagram in Figure 7.

Figure 7: CRC Multiframe Alignment Algorithm

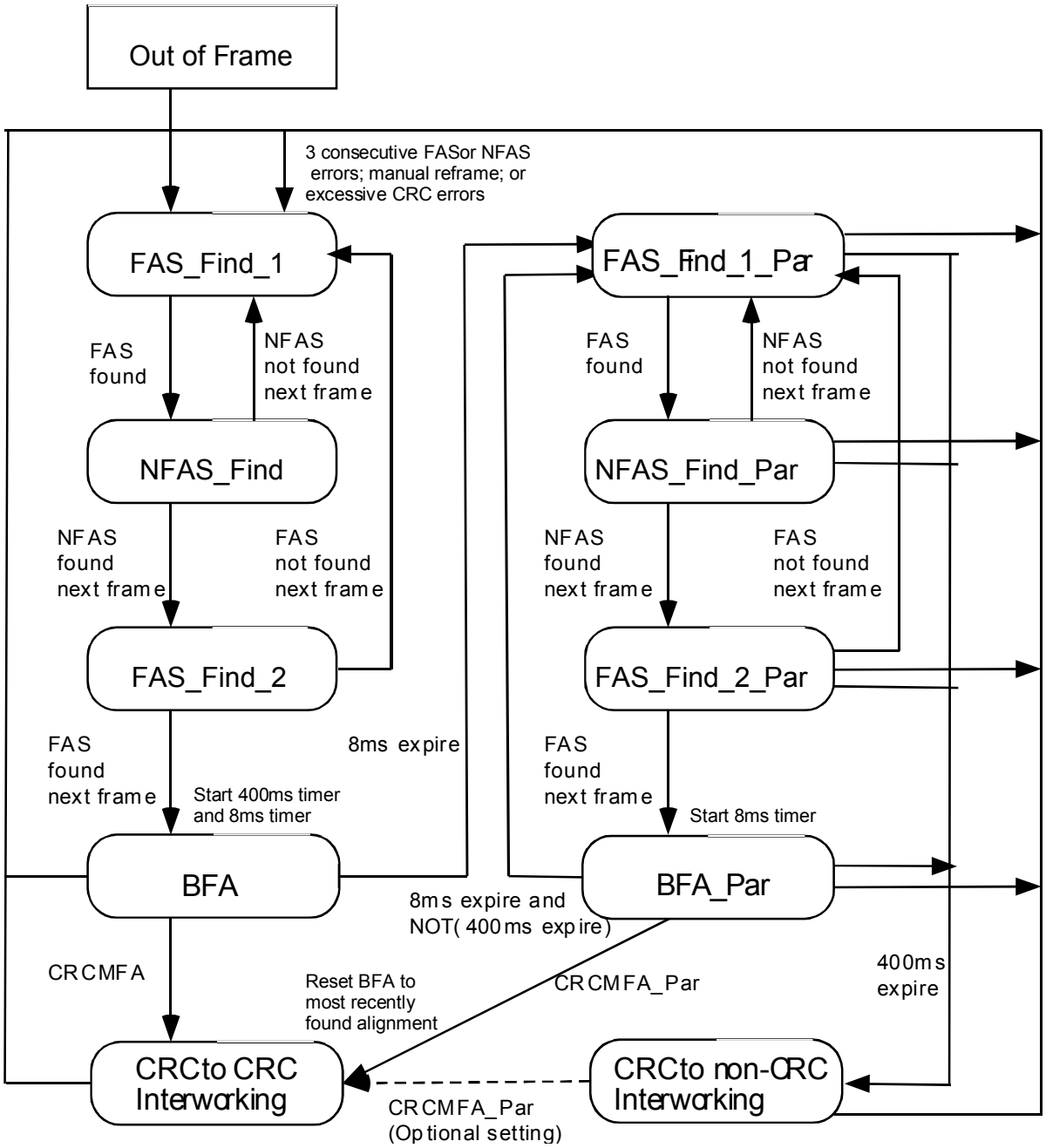


Table 1: E1-FRMR Framing States

State	Out of Frame	Out of Offline Frame
FAS_Find_1	Yes	No
NFAS_Find	Yes	No
FAS_Find_2	Yes	No
BFA	No	No
CRC to CRC Interworking	No	No
FAS_Find_1_Par	No	Yes
NFAS_Find_Par	No	Yes
FAS_Find_2_Par	No	Yes
BFA_Par	No	No
CRC to non-CRC Interworking	No	No

The states of the primary basic framer and the parallel/offline framer in the E1-FRMR block at each stage of the CRC multiframe alignment algorithm are shown in Table 1.

From an out of frame state, the E1-FRMR attempts to find basic frame alignment in accordance with the FAS/NFAS/FAS G.706 Basic Frame Alignment procedure outlined above. Upon achieving basic frame alignment, a 400 ms timer is started, as well as an 8 ms timer. If two CRC multiframe alignment signals separated by a multiple of 2 ms are observed before the 8 ms timer has expired, CRC multiframe alignment is declared.

If the 8 ms timer expires without achieving multiframe alignment, a new offline search for basic frame alignment is initiated. This search is performed in accordance with the Basic Frame Alignment procedure outlined above. However, this search does not immediately change the actual basic frame alignment of the system (i.e., PCM data continues to be processed in accordance with the first basic frame alignment found after an out of frame state while this frame alignment search occurs as a parallel operation).

When a new basic frame alignment is found by this offline search, the 8 ms timer is restarted. If two CRC multiframe alignment signals separated by a multiple of 2 ms are observed before the 8 ms timer has expired, CRC multiframe alignment is declared and the basic frame alignment is set accordingly (i.e., the basic frame alignment is set to correspond to the frame alignment found by the parallel offline search, which is also the basic frame alignment corresponding to the newly found CRC multiframe alignment).

Subsequent expirations of the 8 ms timer will likewise reinitiate a new search for basic frame alignment. If, however, the 400 ms timer expires at any time during this procedure, the E1-FRMR stops searching for CRC multiframe alignment and declares CRC-to-non-CRC interworking. In this mode, the E1-FRMR may be

optionally set to either halt searching for CRC multiframe altogether, or may continue searching for CRC multiframe alignment using the established basic frame alignment. In either case, no further adjustments are made to the basic frame alignment, and no offline searches for basic frame alignment occur once CRC-to-non-CRC interworking is declared: it is assumed that the established basic frame alignment at this point is correct.

AIS Detection

When an unframed all-ones receive data stream is received, an AIS defect is indicated by setting the AISD bit to logic 1 when fewer than three zero bits are received in 512 consecutive bits or, optionally, in each of two consecutive periods of 512 bits. The AISD bit is reset to logic 0 when three or more zeros in 512 consecutive bits or in each of two consecutive periods of 512 bits. Finding frame alignment will also cause the AISD bit to be set to logic 0.

Signaling Frame Alignment

Once the basic frame alignment has been found, the E1-FRMR searches for Channel Associated Signaling (CAS) multiframe alignment using the following G.732 compliant algorithm: signaling multiframe alignment is declared when at least one non-zero time slot 16 bit is observed to precede a time slot 16 containing the correct CAS alignment pattern, namely four zeros (“0000”) in the first four bit positions of timeslot 16.

Once signaling multiframe alignment has been found, the E1-FRMR sets the OOSMFV bit of the E1-FRMR Framing Status register to logic 0, and monitors the signaling multiframe alignment signal, indicating errors occurring in the 4-bit pattern, and indicating the debounced value of the Remote Signaling Multiframe Alarm bit (bit 6 of timeslot 16 of frame 0 of the multiframe). Using debounce, the Remote Signaling Multiframe Alarm bit has < 0.00001% probability of being falsely indicated in the presence of a 10^{-3} bit error rate.

The block declares loss of CAS multiframe alignment if two consecutive CAS multiframe alignment signals have been received in error, or additionally, if all the bits in time slot 16 are logic 0 for 1 or 2 (selectable) CAS multiframes. Loss of CAS multiframe alignment is also declared if basic frame alignment has been lost.

National Bit Extraction

The E1-FRMR extracts and assembles the submultiframe-aligned National bit codewords Sa4[1:4] , Sa5[1:4] , Sa6[1:4] , Sa7[1:4] and Sa8[1:4]. The

corresponding register values are updated upon generation of the CRC submultiframe interrupt.

This E1-FRMR also detects the V5.2 link ID signal, which is detected when 2 out of 3 Sa7 bits are zeros. Upon reception of this Link ID signal, the V52LINKV bit of the E1-FRMR Framing Status register is set to logic 1. This bit is cleared to logic 0 when 2 out of 3 Sa7 bits are ones.

Alarm Integration

The OOF and the AIS defects are integrated, verifying that each condition has persisted for 104 ms (± 6 ms) before indicating the alarm condition. The alarm is removed when the condition has been absent for 104 ms (± 6 ms).

The AIS alarm algorithm accumulates the occurrences of AISD (AIS detection). The E1-FRMR counts the occurrences of AISD over a 4 ms interval and indicates a valid AIS is present when 13 or more AISD indications (of a possible 16) have been received. Each interval with a valid AIS presence indication increments an interval counter which declares AIS Alarm when 25 valid intervals have been accumulated. An interval with no valid AIS presence indication decrements the interval counter. The AIS Alarm declaration is removed when the counter reaches 0. This algorithm provides a 99.8% probability of declaring an AIS Alarm within 104 ms in the presence of a 10^{-3} mean bit error rate.

The Red alarm algorithm monitors occurrences of OOF over a 4 ms interval, indicating a valid OOF interval when one or more OOF indications occurred during the interval, and indicating a valid in frame (INF) interval when no OOF indication occurred for the entire interval. Each interval with a valid OOF indication increments an interval counter which declares Red Alarm when 25 valid intervals have been accumulated. An interval with valid INF indication decrements the interval counter; the Red Alarm declaration is removed when the counter reaches 0. This algorithm biases OOF occurrences, leading to declaration of Red alarm when intermittent loss of frame alignment occurs.

The E1-FRMR can also be disabled to allow reception of unframed data.

9.3 Performance Monitor Counters (T1/E1-PMON)

The Performance Monitor Counters function is provided by the PMON block. The block accumulates CRC error events, Frame Synchronization bit error events, and Out Of Frame events, or optionally, Change of Frame Alignment (COFA) events with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second). When the transfer clock signal is applied, the PMON transfers the counter values into

holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. If the holding registers are not read between successive transfer clocks, an OVERRUN register bit is asserted.

Generation of the transfer clock within the TECT3 chip is performed by writing to any counter register location or by writing to the Global PMON Update register. The holding register addresses are contiguous to facilitate faster polling operations.

9.4 Bit Oriented Code Detector (RBOC)

The Bit Oriented Code detection function is provided by the RBOC block. This block detects the presence of 63 of the possible 64 bit oriented codes transmitted in the T1 Facility Data Link channel in ESF framing format, as defined in ANSI T1.403 and in TR-TSY-000194 or in the DS3 C-bit parity far-end alarm and control (FEAC) channel. The 64^{Th} code (111111) is similar to the HDLC flag sequence and is used by the RBOC to indicate no valid code received.

Bit oriented codes are received on the Facility Data Link channel or FEAC channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0). BOCs are validated when repeated at least 10 times. The RBOC can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Configuration/Interrupt Enable register. The RBOC declares that the code is removed if two code sequences containing code values different from the detected code are received in a moving window of ten code periods.

Valid BOC are indicated through the RBOC Interrupt Status register. The BOC bits are set to all ones (111111) if no valid code has been detected. An interrupt is generated to signal when a detected code has been validated, or optionally, when a valid code goes away (i.e. the BOC bits go to all ones).

9.5 HDLC Receiver (RDLC)

The RDLC is a microprocessor peripheral used to receive HDLC frames on the 4kHz ESF facility data link, the E1 Sa-bit data link, the DS3 C-bit parity Path Maintenance Data Link or a specified channel within a T1 or E1 stream.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-level FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status Register contains bits which indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The Status Register also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the Status Register indicates the FCS status and if the packet contained a non-integer number of bytes.

9.6 T1 Alarm Integrator (ALMI)

The T1 Alarm Integration function is provided by the ALMI block. This block detects the presence of Yellow, Red, and AIS Carrier Fail Alarms (CFA) in SF, or ESF formats. The alarm detection and integration is compatible with the specifications defined in ANSI T1.403 and TR-TSY-000191.

The ALMI block declares the presence of Yellow alarm when the Yellow pattern has been received for 425 ms (± 50 ms); the Yellow alarm is removed when the Yellow pattern has been absent for 425 ms (± 50 ms). The presence of Red alarm is declared when an out-of-frame condition has been present for 2.55 sec (± 40 ms); the Red alarm is removed when the out-of-frame condition has been absent for 16.6 sec (± 500 ms). The presence of AIS alarm is declared when an out-of-frame condition and all-ones in the PCM data stream have been present for 1.5 sec (±100 ms); the AIS alarm is removed when the AIS condition has been absent for 16.8 sec (±500 ms).

CFA alarm detection algorithms operate in the presence of a 10^{-3} bit error rate.

The ALMI also indicates the presence or absence of the Yellow, Red, and AIS alarm signal conditions over 40 ms, 40 ms, and 60 ms intervals, respectively, allowing an external microprocessor to integrate the alarm conditions via software with any user-specific algorithms. Alarm indication is provided through internal register bits.

9.7 Elastic Store (ELST)

The Elastic Store (ELST) synchronizes ingress frames to the common ingress clock and frame pulse (CICLK, CIFP) in the Clock Slave ingress modes or to the common ingress H-MVIP clock and frame pulse (CMV8MCLK, CMVFP, CMVFPC) in H-MVIP modes. The frame data is buffered in a two frame circular data buffer. Input data is written to the buffer using a write pointer and output data is read from the buffer using a read pointer.

When the elastic store is being used, if the average frequency of the incoming data is greater than the average frequency of the backplane clock, the write pointer will catch up to the read pointer and the buffer will be filled. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The subsequent ingress frame is deleted.

If the average frequency of the incoming data is less than the average frequency of the backplane clock, the read pointer will catch up to the write pointer and the buffer will be empty. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The previous ingress frame is repeated.

A slip operation is always performed on a frame boundary.

When the ingress timing is recovered from the receive data the elastic store can be bypassed to eliminate the 2 frame delay. In this configuration (the Clock Master ingress modes), the elastic store is used to synchronize the ingress frames to the transmit line clock so that per-DS0 loopbacks may be enabled.

To allow for the extraction of signaling information in the data channels, superframe identification is also passed through the ELST.

For payload conditioning, the ELST may optionally insert a programmable idle code into all channels when the framer is out of frame synchronization. This code is set to all 1’s when the ELST is reset.

If the data is required to pass through the TECT3 unchanged during an out-of-frame condition, then the elastic store may be bypassed.

9.8 Signaling Elastic Stores (RX-SIG-ELST and TX_SIG-ELST)

There are two additional elastic stores used to adapt the differences in rate between the CAS or CCS H-MVIP signaling rates and the serial clock and data or SBI data rates when in simultaneous SBI or serial clock and data with

signaling H-MVIP. These elastic stores are identical to the elastic store described in section 9.7.

When simultaneous SBI with CAS or CCS H-MVIP is selected by the SYSOPT[2:0] bits in the Global Configuration register these elastic stores eliminate the need for the H-MVIP interface clock and frame alignment to be externally synchronized to the rate and frame alignment of the individual links carries over the SBI interface. Any rate differences between the H-MVIP interface and an individual link will result in a controlled slip in the CAS or CCS data relative to the data channels of the individual T1 links.

When simultaneous serial clock and data with CCS H-MVIP is selected these elastic stores eliminate the need for the H-MVIP interface clock and frame alignment to be externally synchronized to the rate and frame alignment of the individual serial streams. As with simultaneous SBI mode, any rate differences between the H-MVIP interface and an individual link will result in a controlled slip in the CCS signaling relative to the data channels of the individual T1 links.

9.9 Signaling Extractor (SIGX)

The Signaling Extraction (SIGX) block provides channel associated signaling (CAS) extraction from an E1 signaling multi-frame or from ESF, and SF T1 formats.

In T1 mode, the SIGX block provides signaling bit extraction from the received data stream for ESF and SF framing formats. It selectively debounces the bits, and serializes the results onto the ISIG[x] outputs or CAS bits within the SBI Bus structure. Debouncing is performed on individual signaling bits. This ISIG[x] output is channel aligned with ID[x] output, and the signaling bits are repeated for the entire superframe, allowing downstream logic to reinsert signaling into any frame, as determined by system timing. The signaling data stream contains the A,B,C,D bits in the lower 4 channel bit locations (bits 5, 6, 7 and 8) in ESF framing format; in SF format the A and B bits are repeated in locations C and D (i.e. the signaling stream contains the bits ABAB for each channel).

The SIGX block contains three superframes worth of signal buffering to ensure that there is a greater than 95% probability that the signaling bits are frozen in the correct state for a 50% ones density out-of-frame condition, as specified in TR-TSY-000170 and BELL PUB 43801. With signaling debounce enabled, the per-channel signaling state must be in the same state for 2 superframes before appearing on the serial output stream.

The SIGX block provides one superframe or signaling-multiframe of signal freezing on the occurrence of slips. When a slip event occurs, the SIGX freezes

the output signaling for the entire superframe in which the slip occurred; the signaling is unfrozen when the next slip-free superframe occurs.

The SIGX also provides control over timeslot signaling bit fixing, data inversion and signaling debounce on a per-timeslot basis.

The SIGX block also provides an interrupt to indicate a change of signaling state on a per channel basis.

9.10 Receive Per-Channel Serial Controller (RPSC)

The RPSC allows data and signaling trunk conditioning to be applied on the ingress stream on a per-channel basis. It also allows per-channel control of data inversion, the extraction of clock and data on ICLK[x] and ID[x] (when the Clock Master: NxChannel mode is active), and the detection or generation of pseudo-random patterns. The RPSC operates on the data after its passage through ELST, so that data and signaling conditioning may overwrite the ELST trouble code.

9.11 Basic Transmitter (XBAS)

The T1 Basic Transmitter (XBAS) block generates the 1.544 Mbit/s T1 data stream according to SF or ESF frame formats.

In concert with the Transmit Per-Channel Serial Controller (TPSC), the XBAS block, provides per-channel control of idle code substitution, data inversion (either all 8 bits, sign bit magnitude or magnitude only), and zero code suppression. Three types of zero code suppression (GTE, Bell and "jammed bit 8") are supported and selected on a per-channel basis to provide minimum ones density control. An internal signaling control stream provides per-channel control of robbed bit signaling and selection of the signaling source. All channels can be forced into a trunk conditioning state (idle code substitution and signaling conditioning) by use of the Master Trunk Conditioning (MTRK) bit in the T1-XBAS Configuration Register.

A data link is provided for ESF mode. The data link sources include bit oriented codes and HDLC messages. Support is provided for the transmission of AIS or Yellow alarm signals for all formats.

The transmitter can be disabled for framing via the FDIS disable bit in the T1/E1 Transmit Framing and Bypass Options register. When transmitting ESF formatted data, the framing bit, datalink bit, or the CRC-6 bit from the egress stream can be by-passed to the output data stream via the same T1/E1 Transmit

Framing and Bypass Options register. Finally, the transmitter can be by-passed completely to provide a clear channel operating mode.

9.12 E1 Transmitter (E1-TRAN)

The E1 Transmitter (E1-TRAN) generates a 2048 kbit/s data stream according to ITU-T recommendations, providing individual enables for frame generation, CRC multiframe generation, and channel associated signaling (CAS) multiframe generation.

In concert with Transmit Per-Channel Serial Controller (TPSC), the E1-TRAN block provides per-timeslot control of idle code substitution, data inversion, digital milliwatt substitution, selection of the signaling source and CAS data. All timeslots can be forced into a trunk conditioning state (idle code substitution and signaling substitution) by use of the master trunk conditioning bit in the E1-TRAN Transmit Alarm/Diagnostic Control register.

Common Channel Signaling (CCS) is supported in time slot 16 through the Transmit Channel Insertion (TXCI) block. Support is provided for the transmission of AIS and TS16 AIS, and the transmission of remote alarm (RAI) and remote multiframe alarm signals.

The National Use bits (Sa-bits) can be sourced from the E1-TRAN National Bits Codeword registers as 4-bit codewords aligned to the submultiframe. Alternatively, the Sa-bits may individually carry data links sourced from the internal HDLC controller, or may be passed transparently from the ED[x] input.

9.13 Transmit Per-Channel Serial Controller (TPSC)

The Transmit Per-Channel Serial Controller allows data and signaling trunk conditioning or idle code to be applied on the transmit DS-1 stream on a per-channel basis. It also allows per-channel control of zero code suppression, data inversion, channel loopback (from the ingress stream), channel insertion, and the detection or generation of pseudo-random patterns.

The TPSC interfaces directly to the E1-TRAN and T1-XBAS block and provides serial streams for signaling control, idle code data and egress data control.

9.14 Signaling Aligner (SIGA)

The Signaling Aligner is a block that is only applicable in T1 operating modes. When enabled, the Signaling Aligner is positioned in the egress path before the T1-XBAS. Its purpose is to ensure that if the signaling on ESIG[x] is changed in the middle of a superframe, the XBAS completes transmitting the A,B,C, and D

bits for the current superframe before switching to the new values. This permits signaling integrity to be preserved independent of the superframe alignment of the T1-XBAS or the signaling data source.

9.15 Bit Oriented Code Generator (XBOC)

The Bit Oriented Code Generator function is provided by the XBOC block. This block transmits 63 of the possible 64 bit oriented codes in the Facility Data Link (FDL) channel in ESF framing format, as defined in ANSI T1.403-1989 or in the DS3 C-bit parity Far-End Alarm and Control (FEAC) channel. The 64th code (111111) is similar to the HDLC Flag sequence and is used in the XBOC to disable transmission of any bit oriented codes. When transmission is disabled the FDL or FEAC channel is set to all ones.

Bit oriented codes are transmitted on the T1 Facility Data Link or DS3 Far-End Alarm and Control channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. When driving the T1 facility data link the transmitted bit oriented codes have priority over any data transmitted except for ESF Yellow Alarm. The code to be transmitted is programmed by writing to the XBOC code registers when it is held until the last code has been transmitted at least 10 times. An interrupt or polling mechanism is used to determine when the most recent code written the XBOC register is being transmitted and a new code can be accepted.

9.16 HDLC Transmitters (TDPR)

The HDLC Transmitter (TDPR) provides a serial data link for the 4 kHz ESF facility data link, E1 Sa-bit data link, the DS3 C-bit parity path maintenance data link or a specified channel within a T1 or E1 stream. The TDPR is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) may be appended, followed by flags. If the TDPR transmit data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the TDPR continuously transmits the flag sequence (01111110) until data is ready to be transmitted. Data bytes to be transmitted are written into the Transmit Data Register. The TDPR performs a parallel-to-serial conversion of each data byte before transmitting it.

The default procedure provides automatic transmission of data once a complete packet is written. All complete packets of data will be transmitted. After the last data byte of a packet, the CRC word (if CRC insertion has been enabled) and a

flag, or just a flag (if CRC insertion has not been enabled) is transmitted. The TDPR then returns to the transmission of flag characters until the next packet is available for transmission. While working in this mode, the user must only be careful to avoid overfilling the FIFO; underruns cannot occur unless the packet is greater than 128 bytes long. The TDPR will force transmission if the FIFO is filled up regardless of whether or not the packet has been completely written into the FIFO.

The second procedure transmits data only when the FIFO depth has reached a user configured upper threshold. The TDPR will continue to transmit data until the FIFO depth has fallen below the upper threshold and the transmission of the last packet with data above the upper threshold has completed. In this mode, the user must be careful to avoid overruns and underruns. An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data.

Interrupts can also be generated if the FIFO underflows while transmitting a packet, when the FIFO falls below a lower threshold, when the FIFO is full, or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort characters can be continuously transmitted at any time by setting the ABT bit in the TDPR Configuration register. During packet transmission, an underrun situation can occur if data is not written to the TDPR Transmit Data register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDRI interrupt.

9.17 T1 Automatic Performance Report Generation (APRM)

In compliance with the ANSI T1.231, T1.403 and T1.408 standards, a performance report is generated each second for T1 ESF applications. The report conforms to the HDLC protocol and is inserted into the ESF facility data link.

The performance report can only be transmitted if the TDPR is configured to insert the ESF Facility Data Link and the PREN bit of the TDPR Configuration register is logic 1. The performance report takes precedence over incompletely written packets, but it does not pre-empt packets already being transmitted.

See the Operation section for details on the performance report encoding.

9.18 Receive and Transmit Digital Jitter Attenuator (RJAT, TJAT)

The Digital Jitter Attenuation function is provided by the DJAT blocks. Each framer in the TECT3 contains two separate jitter attenuators, one between the receive demultiplexed or demapped T1 or E1 link and the ingress interface (RJAT) and the other between the egress interface and the transmit T1 or E1 link to be multiplexed into DS3 (TJAT). Each DJAT block receives jittered data and stores the stream in a FIFO timed to the associated receive jittered clock. The jitter attenuated data emerges from the FIFO timed to the jitter attenuated clock. In the RJAT, the jitter attenuated clock (ICLK[x]) is referenced to the demultiplexed tributary receive clock. In the TJAT, the jitter attenuated transmit tributary clock feeding the M13 multiplexer may be referenced to either CTCLK, CECLK, or the tributary receive clock.

In T1 mode each jitter attenuator generates its output clock by adaptively dividing the 37.056 MHz XCLK signal according to the phase difference between the jitter attenuated clock and the input reference clock. Jitter fluctuations in the phase of the reference clock are attenuated by the phase-locked loop within each DJAT so that the frequency of the jitter attenuated clock is equal to the average frequency of the reference. To best fit the jitter attenuation transfer function recommended by TR 62411, phase fluctuations with a jitter frequency above 6.6 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 6.6 Hz are tracked by the jitter attenuated clock. The jitter attenuated clock (ICLK[x] for the RJAT and transmit clock for the TJAT) are used to read data out of the FIFO.

In E1 mode each jitter attenuator generates the jitter-free 2.048 MHz output clock by adaptively dividing the 49.152 MHz XCLK signal according to the phase difference between the jitter attenuated clock and input reference clock. Fluctuations in the phase of the input data clock are attenuated by the phase-locked loop within DJAT so that the frequency of the jitter attenuated clock is equal to the average frequency of the input data clock. Phase fluctuations with a jitter frequency above 8.8 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 8.8 Hz are tracked by the jitter attenuated clock. To provide a smooth flow of data out of DJAT, the jitter attenuated clock is used to read data out of the FIFO.

The TJAT and RJAT have programmable divisors in order to generate the jitter attenuated clock from the various reference sources. The divisors are set using the TJAT and RJAT Jitter Attenuator Divider N1 and N2 registers. The following formula must be met in order to select the values of N1 and N2:

$$Fin/(N1 + 1) = Fout/(N2 + 1)$$

where Fin is the input reference clock frequency and Fout is the output jitter attenuated clock frequency. The values on N1 and N2 can range between 1 and 256. Fin ranges from 8KHz to 2.048MHz in 8KHz increments.

If the FIFO read pointer comes within one bit of the write pointer, DJAT will track the jitter of the input clock. This permits the phase jitter to pass through unattenuated, inhibiting the loss of data.

Jitter Characteristics

Each DJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. In T1 mode each DJAT can accommodate up to 28 UIpp of input jitter at jitter frequencies above 6 Hz. For jitter frequencies below 6 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In E1 mode each DJAT can accommodate up to 35 UIpp of input jitter at jitter frequencies above 9 Hz. For jitter frequencies below 9 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In most applications the each DJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The DJAT blocks meet the stringent low frequency jitter tolerance requirements of AT&T TR 62411, ITU-T Recommendation G.823 and thus allow compliance with this standard and the other less stringent jitter tolerance standards cited in the references.

The DJAT exhibits negligible jitter gain for jitter frequencies below 6.6 Hz, and attenuates jitter at frequencies above 6.6 Hz by 20 dB per decade in T1 mode. It exhibits negligible jitter gain for jitter frequencies below 8.8 Hz, and attenuates jitter at frequencies above 8.8 Hz by 20 dB per decade in E1 mode. In most applications the DJAT Blocks will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through DJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of 24X (37.056 MHz or 49.152 MHz) digital phase locked loop for transmit clock generation. DJAT meets the jitter transfer requirements of AT&T TR 62411. The DJAT allows the implied T1 jitter attenuation requirements for a TE or NT1 given in ANSI Standard T1.408, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403 to be met. The DJAT meets the E1 jitter attenuation requirements of the ITU-T Recommendations G.737, G.738, G.739 and G.742.

Jitter Tolerance

Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For T1 modes the DJAT input jitter tolerance is 29 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 354 Hz. For E1 modes the input jitter tolerance is 35 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 308 Hz. In either mode jitter tolerance is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK divided by 24 and that of the input data clock.

Figure 8: DJAT Jitter Tolerance T1 Modes

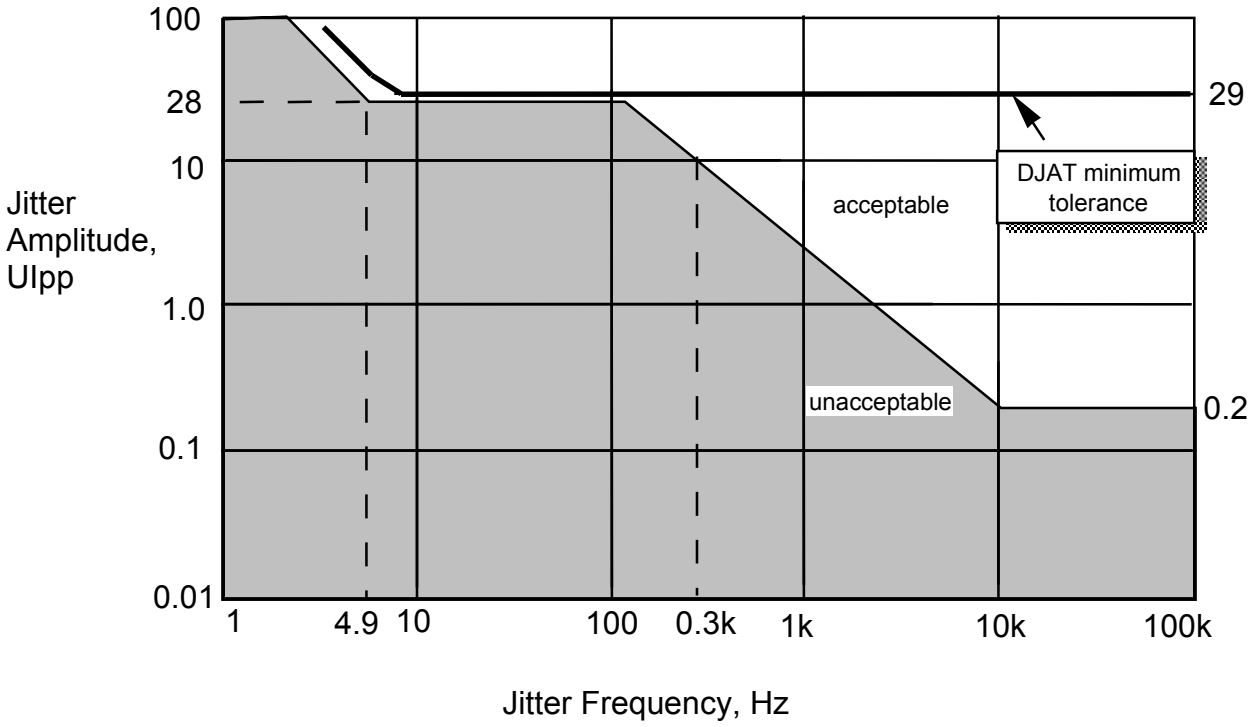
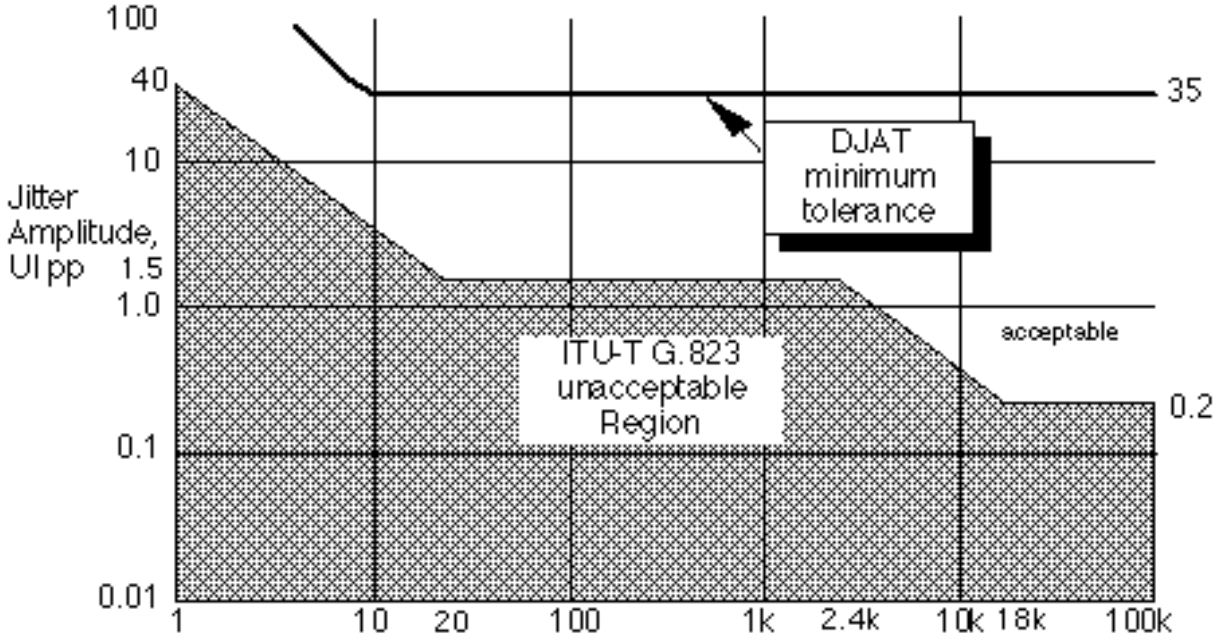


Figure 9: DJAT Jitter Tolerance E1 Modes



The accuracy of the XCLK frequency and that of the reference clock used to generate the jitter attenuated clock have an effect on the minimum jitter tolerance. Given that the DJAT PLL reference clock accuracy can be ±200 Hz from 1.544 MHz or be ±103 Hz from 2.048 MHz, and that the XCLK input accuracy can be ±100 ppm from 37.056 MHz or ±100 ppm from 49.152 MHz, the minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK ÷ 24 are shown in Figure 10 and Figure 11.

An XCLK input accuracy of ±100 ppm is only acceptable if an accurate line rate reference is provided. If TJAT is left to free-run without a reference, or referenced to a derivative of XCLK, then XCLK accuracy must be ±32 ppm.

Figure 10: DJAT Minimum Jitter Tolerance vs. XCLK Accuracy T1 Modes

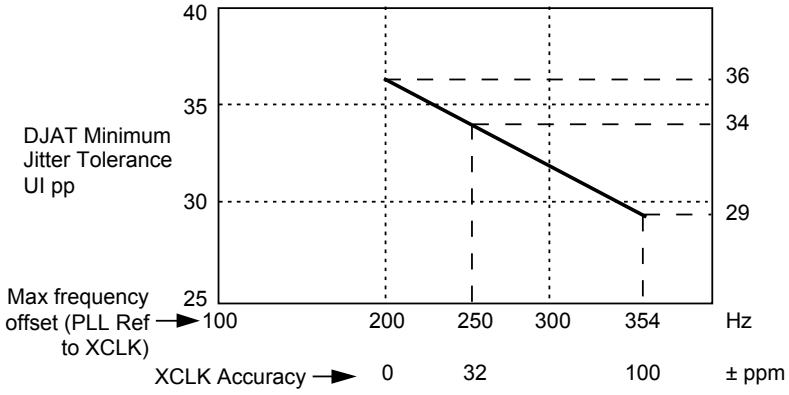
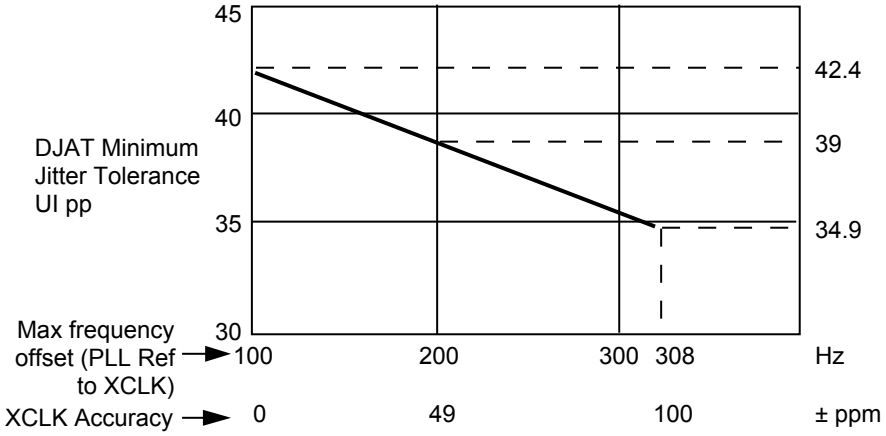


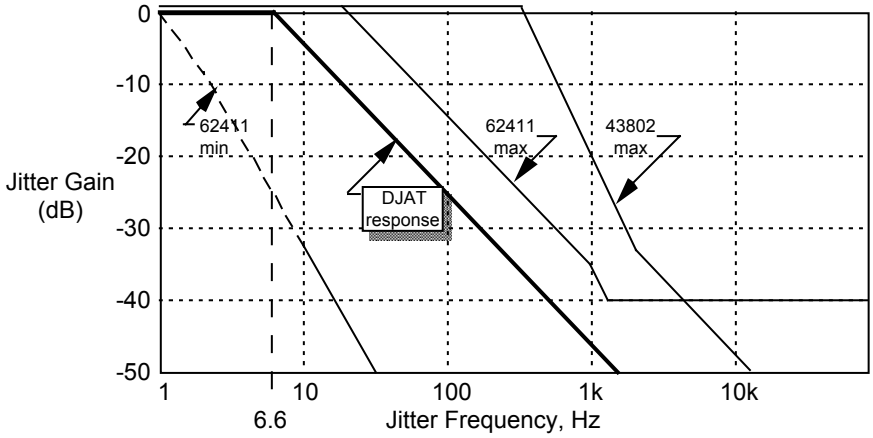
Figure 11: DJAT Minimum Jitter Tolerance vs. XCLK Accuracy E1 Modes



Jitter Transfer

The output jitter in T1 mode for jitter frequencies from 0 to 6.6 Hz is no more than 0.1 dB greater than the input jitter, excluding the residual jitter. Jitter frequencies above 6.6 Hz are attenuated at a level of 6 dB per octave, as shown in Figure 12.

Figure 12: DJAT Jitter Transfer T1 Modes



The output jitter in E1 mode for jitter frequencies from 0 to 8.8 Hz is no more than 0.1 dB greater than the input jitter, excluding the residual jitter. Jitter frequencies above 8.8 Hz are attenuated at a level of 6 dB per octave, as shown in Figure 13.

Figure 13: DJAT Jitter Transfer E1 Modes

Frequency Range

In the non-attenuating mode for T1 rates, that is, when the FIFO is within one UI of overrunning or under running, the tracking range is 1.48 to 1.608 MHz. The guaranteed linear operating range for the jittered input clock is 1.544 MHz ± 200 Hz with worst case jitter (29 UIpp) and maximum XCLK frequency offset (± 100 ppm). The nominal range is 1.544 MHz ± 963 Hz with no jitter or XCLK frequency offset.

In the non-attenuating mode for E1 rates the tracking range is 1.963 to 2.133 MHz. The guaranteed linear operating range for the jittered input clock is 2.048 MHz ± 1278 Hz with worst case jitter (42 UIpp) and maximum XCLK frequency offset (± 100 ppm).

9.19 Timing Options (TOPS)

The Timing Options block provides a means of selecting the source of the internal input clock to the TJAT block, the reference clock for the TJAT digital PLL, and the clock source used to derive the transmit clock to the M13 mux.

9.20 Pseudo Random Binary Sequence Generation and Detection (PRBS)

The Pseudo Random Binary Sequence Generator/Detector (PRBS) block is a software selectable PRBS generator and checker for 2^{11}-1, 2^{15}-1 or 2^{20}-1 PRBS polynomials for use in the T1 and E1 links. PRBS patterns may be generated in either the transmit or receive directions, and detected in the opposite direction.

The PRBS block can perform an auto synchronization to the expected PRBS pattern and accumulates the total number of bit errors in two 24-bit counters. The error count accumulates over the interval defined by to the Global PMON Update Register. When an accumulation is forced, the holding register is updated, and the counter reset to begin accumulating for the next interval. The counter is reset in such a way that no events are missed. The data is then available in the Error Count registers until the next accumulation.

9.21 Pseudo Random Pattern Generation and Detection (PRGD)

The Pseudo Random Pattern Generator/Detector (PRGD) block is a software programmable test pattern generator, receiver, and analyzer for the DS3 payload. Patterns may be generated in the transmit direction, and detected in the receive direction. Two types of ITU-T O.151 compliant test patterns are provided : pseudo-random and repetitive.

The PRGD can be programmed to generate any pseudo-random pattern with length up to 2^{32}-1 bits or any user programmable bit pattern from 1 to 32 bits in length. In addition, the PRGD can insert single bit errors or a bit error rate between 10^{-1} to 10^{-7}.

The PRGD can be programmed to check for the generated pseudo random pattern. The PRGD can perform an auto synchronization to the expected pattern and accumulates the total number of bits received and the total number of bit errors in two 32-bit counters. The counters accumulate either over intervals defined by writes to the Pattern Detector registers, upon writes to the Global PMON Update Register or automatically once a second. When an accumulation is forced, the holding registers are updated, and the counters reset to begin accumulating for the next interval. The counters are reset in such a way that no events are missed. The data is then available in the holding registers until the next accumulation.

9.22 DS3 Framer (DS3-FRMR)

The DS3 Framer (DS3-FRMR) Block integrates circuitry required for decoding a B3ZS-encoded signal and framing to the resulting DS3 bit stream. The DS3-FRMR is directly compatible with the M23 and C-bit parity DS3 applications.

The DS3-FRMR decodes a B3ZS-encoded signal and provides indications of line code violations. The B3ZS decoding algorithm and the LCV definition can be independently chosen through software. A loss of signal (LOS) defect is also detected for B3ZS encoded streams. LOS is declared when inputs RPOS and RNEG contain zeros for 175 consecutive RCLK cycles. LOS is removed when the ones density on RPOS and/or RNEG is greater than 33% for 175 ±1 RCLK cycles.

The framing algorithm examines five F-bit candidates simultaneously. When at least one discrepancy has occurred in each candidate, the algorithm examines the next set of five candidates. When a single F-bit candidate remains in a set, the first bit in the supposed M-subframe is examined for the M-frame alignment signal (i.e., the M-bits, M1, M2, and M3 are following the 010 pattern). Framing is declared, and out-of-frame is removed, if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits. During the examination of the M-bits, the X-bits and P-bits are ignored. The algorithm gives a maximum average reframe time of 1.5 ms.

While the DS3-FRMR is synchronized to the DS3 M-frame, the F-bit and M-bit positions in the DS3 stream are examined. An out-of-frame defect is detected when 3 F-bit errors out of 8 or 16 consecutive F-bits are observed (as selected by the M3O8 bit in the DS3 FRMR Configuration Register), or when one or more

M-bit errors are detected in 3 out of 4 consecutive M-frames. The M-bit error criteria for OOF can be disabled by the MBDIS bit in the DS3 Framer Configuration register. The 3 out of 8 consecutive F-bits out-of-frame ratio provides more robust operation, in the presence of a high bit error rate, than the 3 out of 16 consecutive F-bits ratio. Either out-of-frame criteria allows an out-of-frame defect to be detected quickly when the M-subframe alignment patterns or, optionally, when the M-frame alignment pattern is lost.

Also while in-frame, line code violations, M-bit or F-bit framing bit errors, and P-bit parity errors are indicated. When C-bit parity mode is enabled, both C-bit parity errors and far end block errors are indicated. These error indications, as well as the line code violation and excessive zeros indication, are accumulated over 1 second intervals with the Performance Monitor (PMON). Note that the framer is an off-line framer, indicating both OOF and COFA events. Even if an OOF is indicated, the framer will continue indicating performance monitoring information based on the previous frame alignment.

Three DS3 maintenance signals (a RED alarm condition, the alarm indication signal, and the idle signal) are detected by the DS3-FRMR. The maintenance detection algorithm employs a simple integrator with a 1:1 slope that is based on the occurrence of "valid" M-frame intervals. For the RED alarm, an M-frame is said to be a "valid" interval if it contains a RED defect, defined as an occurrence of an OOF or LOS event during that M-frame. For AIS and IDLE, an M-frame interval is "valid" if it contains AIS or IDLE, defined as the occurrence of less than 15 discrepancies in the expected signal pattern (1010... for AIS, 1100... for IDLE) while valid frame alignment is maintained. This discrepancy threshold ensures the detection algorithms operate in the presence of a 10^{-3} bit error rate. For AIS, the expected pattern may be selected to be: the framed "1010" signal; the framed arbitrary DS3 signal and the C-bits all zero; the framed "1010" signal and the C-bits all zero; the framed all-ones signal (with overhead bits ignored); or the unframed all-ones signal (with overhead bits equal to ones). Each "valid" M-frame causes an associated integration counter to increment; "invalid" M-frames cause a decrement. With the "slow" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 127, which results in a detection time of 13.5 ms. With the "fast" detection option, RED, AIS, or IDLE are declared when the respective counter saturates at 21, which results in a detection time of 2.23 ms (i.e., 1.5 times the maximum average reframe time). RED, AIS, or IDLE are removed when the respective counter decrements to 0. DS3 Loss of Frame detection is provided as recommended by ITU-T G.783 with programmable integration periods of 1ms, 2ms, or 3ms. While integrating up to assert LOF, the counter will integrate up when the framer asserts an Out of Frame condition and integrates down when the framer de-asserts the Out of Frame condition. Once an LOF is asserted, the framer must not assert OOF for the entire integration period before LOF is deasserted.

Valid X-bits are extracted by the DS3-FRMR to provide indication of far end receive failure (FERF). A FERF defect is detected if the extracted X-bits are equal and are logic 0 (X1=X2=0); the defect is removed if the extracted X-bits are equal and are logic 1 (X1=X2=1). If the X-bits are not equal, the FERF status remains in its previous state. The extracted FERF status is buffered for 2 M-frames before being reported within the DS3 FRMR Status register. This buffer ensures a better than 99.99% chance of freezing the FERF status on a correct value during the occurrence of an out of frame.

When the C-bit parity application is enabled, both the far end alarm and control (FEAC) channel and the path maintenance data link are extracted. Codes in the FEAC channel are detected by the Bit Oriented Code Detector (RBOC). HDLC messages in the Path Maintenance Data Link are received by the Data Link Receiver (RDLC).

The DS3-FRMR can be enabled to automatically assert the RAI indication in the outgoing transmit stream upon detection of any combination of LOS, OOF or RED, or AIS. The DS3-FRMR can also be enabled to automatically insert C-bit Parity FEBE upon detection of receive C-bit parity error.

The DS3-FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the DS3-FRMR. Access to these registers is via a generic microprocessor bus.

9.23 Performance Monitor Accumulator (DS3-PMON)

The Performance Monitor (PMON) Block interfaces directly with the DS3 Framer (DS3-FRMR). Saturating counters are used to accumulate:

- line code violation (LCV) events
- parity error (PERR) events
- path parity error (CPERR) events
- far end block error (FEBE) events
- excess zeros (EXZS)
- framing bit error (FERR) events

Due to the off-line nature of the DS3 Framer, PMON continues to accumulate performance meters even while the DS3-FRMR has declared OOF.

When an accumulation interval is signaled by a write to the PMON register address space, the PMON transfers the current counter values into microprocessor accessible holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed.

When counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled. If the holding registers have not been read since the last interrupt, an overrun status bit is set. In addition, a register is provided to indicate changes in the PMON counters since the last accumulation interval.

Whenever counter data is transferred into the holding registers, an interrupt is generated, providing the interrupt is enabled. If the holding registers have not been read since the last interrupt, an overrun status bit is set.

9.24 DS3 Transmitter (DS3-TRAN)

The DS3 Transmitter (DS3-TRAN) Block integrates circuitry required to insert the overhead bits into a DS3 bit stream and produce a B3ZS-encoded signal. The T3-TRAN is directly compatible with the M23 and C-bit parity DS3 formats.

When configured for the C-bit parity application, all overhead bits are inserted. When configured for the M23 application, all overhead bits except the stuff control bits (the C-bits) are inserted; the C-bits are inserted by the upstream MX23 TSB.

Status signals such as far end receive failure (FERF), the alarm indication signal, and the idle signal can be inserted when their transmission is enabled by internal register bits. FERF can also be automatically inserted on detection of any combination of LOS, OOF or RED, or AIS by the DS3-FRMR.

A valid pair of P-bits is automatically calculated and inserted by the DS3-TRAN. When C-bit parity mode is selected, the path parity bits, and far end block error (FEBE) indications are automatically inserted.

When enabled for C-bit parity operation, the FEAC channel is sourced by the XBOC bit-oriented code transmitter. The path maintenance data link messages are sourced by the TDPR data link transmitter.

The DS3-TRAN supports diagnostic modes in which it inserts parity or path parity errors, F-bit framing errors, M-bit framing errors, invalid X or P-bits, line code violations, or all-zeros.

9.25 M23 Multiplexer (MX23)

The M23 Multiplexer (MX23) integrates circuitry required to asynchronously multiplex and demultiplex seven DS2 streams into, and out of, an M23 or C-bit Parity formatted DS3 serial stream.

When multiplexing seven DS2 streams into an M23 formatted DS3 stream, the MX23 TSB performs rate adaptation to the DS3 by integral FIFO buffers, controlled by timing circuitry. The C-bits are also generated and inserted by the timing circuitry. Software control is provided to transmit DS2 AIS and DS2 payload loopback requests. The loopback request is coded by inverting one of the three C-bits (the default option is compatible with ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7). The TSB also supports generation of a C-bit Parity formatted DS3 stream by providing an internally generated DS2 rate clock corresponding to a 100% stuffing ratio. Integrated M13 applications are supported by providing an internally generated DS2 rate clock corresponding to a 39.1% stuffing ratio.

When demultiplexing seven DS2 streams from an M23 formatted DS3, the MX23 performs bit destuffing via interpretation of the C-bits. The MX23 also detects and indicates DS2 payload loopback requests encoded in the C-bits. As per ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7, the loopback command is identified as C3 being the inverse of C1 and C2. Because TR-TSY-000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames.

DS2 payload loopback can be activated or deactivated under software control. During payload loopback the DS2 stream being looped back still continues unaffected in the demultiplex direction to the DS2 Framer. All seven demultiplexed DS2 streams can also be replaced with AIS on an individual basis under register control or they can be configured to be replaced automatically on detection of out of frame, loss of signal, RED alarm or alarm indication signal.

9.26 DS2 Framer (DS2-FRMR)

The FRMR DS2 Framer integrates circuitry required for framing to a DS2 bit stream and is directly compatible with the M12 DS2 application. The FRMR can also be configured to frame to a G.747 bit stream.

The DS2 FRMR frames to a DS2 signal with a maximum average reframe time of less than 7 ms and frames to a G.747 signal with a maximum average reframe

time of 1 ms. In DS2 mode, both the F-bits and M-bits must be correct for a significant period of time before frame alignment is declared. In G.747 mode, frame alignment is declared if the candidate frame alignment signal has been correct for 3 consecutive frames (in accordance with CCITT Rec. G.747 Section 4). Once in frame, the DS2 FRMR provides indications of the M-frame and M-subframe boundaries, and identifies the overhead bit positions in the incoming DS2 signal or provides indications of the frame boundaries and overhead bit positions in the incoming G.747 signal.

Depending on configuration, declaration of DS2 out-of-frame occurs when 2 out of 4 or 2 out of 5 consecutive F-bits are in error (These two ratios are recommended in TR-TSY-000009 Section 4.1.2) or when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. The M-bit error criteria for OOF can be disabled via the MBDIS bit in the DS2 Framer configuration register. In G.747 mode, out-of-frame is declared when four consecutive frame alignment signals are incorrectly received (in accordance with CCITT Rec. G.747 Section 4). Note that the DS2 framer is an off-line framer, indicating both OFF and COFA. Error events continue to be indicated even when the FRMR is indicating OOF, based on the previous frame alignment.

The RED alarm and alarm indication signal are detected by the DS2 FRMR in 9.9 ms for DS2 format and in 6.9 ms for G.747 format. The framer employs a simple integration algorithm (with a 1:1 slope) that is based on the occurrence of "valid" DS2 M-frame or G.747 frame intervals. For the RED alarm, a DS2 M-frame (or G.747 frame, depending upon the framing format selected) is said to be a "valid" interval if it contains a RED defect, defined as the occurrence of an OOF event during that M-frame (or G.747 frame). For AIS, a DS2 M-frame (or G.747 frame) is said to be a "valid" interval if it contains AIS, defined as the occurrence of less than 9 zeros while the framer is out of frame during that M-frame (or G.747 frame). The discrepancy threshold ensures the detection algorithm operates in the presence of bit error rates of up to 10-3. Each "valid" DS2 M-frame (or G.747 frame) causes an integration counter to increment; "non-valid" DS2 M-frame (or G.747 frame) intervals cause a decrement. RED or AIS is declared if the associated integrator count saturates at 53, resulting in a detection time of 9.9 ms for DS2 and 6.9 ms for G.747. RED or AIS declaration is deasserted when the associated count decrements to 0.

The DS2 X-bit or G.747 remote alarm indication (RAI) bit is extracted by the DS2 FRMR to provide an indication of far end receive failure. The FERF status is set to the current X/RAI state only if the two successive X/RAI bits were in the same state. The extracted FERF status is buffered for 6 DS2 M-frames or 6 G.747 frames before being reported within the DS2 FRMR Status register. This buffer ensures a virtually 100% probability of freezing the FERF status in a valid state during an out of frame occurrence in DS2 mode, and ensures a better than 99.9% probability of freezing the valid status during an OOF occurrence in G.747

mode. When an OOF occurs, the FERF value is held at the state contained in the last buffer location corresponding to the previous sixth M-frame or G.747 frame. This location is not updated until the OOF condition is deasserted. Meanwhile, the last four of the remaining five buffer locations are loaded with the frozen FERF state while the first buffer location corresponding to the current M-frame/ G.747 frame is continually updated every M-frame/G.747 frame based on the above FERF definition. Once correct frame alignment has been found and OOF is deasserted, the first buffer location will contain a valid FERF status and the remaining five buffer locations are enabled to be updated every M-frame or G.747 frame.

DS2 M-bit and F-bit framing errors are indicated as are G.747 framing word errors (or bit errors) and G.747 parity errors. These error indications are accumulated for performance monitoring purposes in internal, microprocessor readable counters. The performance monitoring accumulators continue to count error indication even while the framer is indicating OOF.

The DS2 FRMR may be configured to generate interrupts on error events or status changes. All sources of interrupts can be masked or acknowledged via internal registers. Internal registers are also used to configure the DS2 FRMR.

9.27 M12 Multiplexer (MX12)

The MX12 M12 Multiplexer integrates circuitry required to asynchronously multiplex and demultiplex four DS1 streams into, and out of, an M12 formatted DS2 serial stream (as defined in ANSI T1.107 Section 7) and to support asynchronous multiplexing and demultiplexing of three 2048 kbit/s into and out of a G.747 formatted 6312 kbit/s high speed signal (as defined in CCITT Rec. G.747).

When multiplexing four DS1 streams into an M12 formatted DS2 stream, the MX12 TSB performs logical inversion on the second and fourth tributary streams. Rate adaptation to the DS2 is performed by integral FIFO buffers, controlled by timing circuitry. The FIFO buffers accommodate in excess of 5.0 UIpp of sinusoidal jitter on the DS1 clocks for all jitter frequencies. X, F, M, and C bits are also generated and inserted by the timing circuitry. Software control is provided to transmit Far End Receive Failure (FERF) indications, DS2 AIS, and DS1 payload loopback requests. The loopback request is coded by inverting one of the three C-bits (the default option is compatible with ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7).Two diagnostic options are provided to invert the transmitted F or M bits.

When demultiplexing four DS1 streams from an M12 formatted DS2, the MX12 performs bit destuffing via interpretation of the C-bits. The MX12 also detects and indicates DS1 payload loopback requests encoded in the C-bits. As per

ANSI T1.107 Section 7.2.1.1 and TR-TSY-000009 Section 3.7, the loopback command is identified as C3 being the inverse of C1 and C2. Because TR-TSY-000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames.

DS1 payload loopback can be activated or deactivated under software control. During payload loopback the DS1 stream being looped back still continues unaffected in the demultiplex direction. The second and fourth demultiplexed DS1 streams are logically inverted, and all four demultiplexed DS1 streams can be replaced with AIS on an individual basis.

Similar functionality supports CCITT Recommendation G.747. The FIFO is still required for rate adaptation. The frame alignment signal and parity bit are generated and inserted by the timing circuitry. Software control is provided to transmit Remote Alarm Indication (RAI), high speed signal AIS, and the reserved bit. A diagnostic option is provided to invert the transmitted frame alignment signal and parity bit.

When demultiplexing three 2048 kbit/s streams from a G.747 formatted 6312 kbit/s stream, the MX12 performs bit destuffing via interpretation of the C-bits. Tributary payload loopback can be activated or deactivated under software control. Although no remote loopback request has been defined for G.747, inversion of the third C-bit triggers a loopback request detection indication in anticipation of Recommendation G.747 refinement. All three demultiplexed 2048 kbit/s streams can be replaced with AIS on an individual basis.

9.28 Egress System Interface (ESIF)

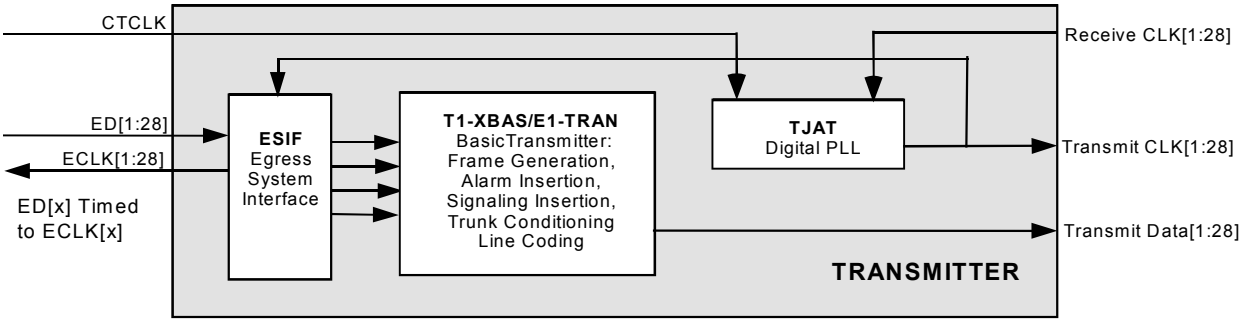
The Egress System Interface (ESIF) block provides system side serial clock and data access as well as H-MVIP access for up to 28 T1 or 21 E1 transmit streams. There are several master and slave clocking modes for serial clock and data system side access to the T1 and E1 streams. When enabled for 8.192Mb/s H-MVIP there are three separate interfaces for data, CAS signaling and CCS signaling. The H-MVIP signaling interfaces can be used in combination with the serial clock and data and SBI interface in certain applications. Control of the system side interface is global to TECT3 and is selected through the SYSOPT[2:0] bits in the Global Configuration register at address 0001H. The system interface options are serial clock and data, H-MVIP, SBI bus, SBI bus with CAS or CCS H-MVIP and serial clock and data with CCS H-MVIP.

Two Clock Master modes provide a serial clock and data egress interface with per link clocking provided by TECT3. The clock master modes are Clock Master:

NxChannel and Clock Master: Clear Channel. Four Clock slave modes provide three serial clock and data egress interfaces and a H-MVIP interface all with externally sourced clocking. The slave modes are Clock Slave: EFP Enabled, Clock Slave: External Signaling, Clock Slave: Clear Channel and Clock Slave: H-MVIP. The egress serial clock and data interface clocking modes are selected via the EMODE[2:0] bits in the T1/E1 Egress Serial Interface Mode Select register.

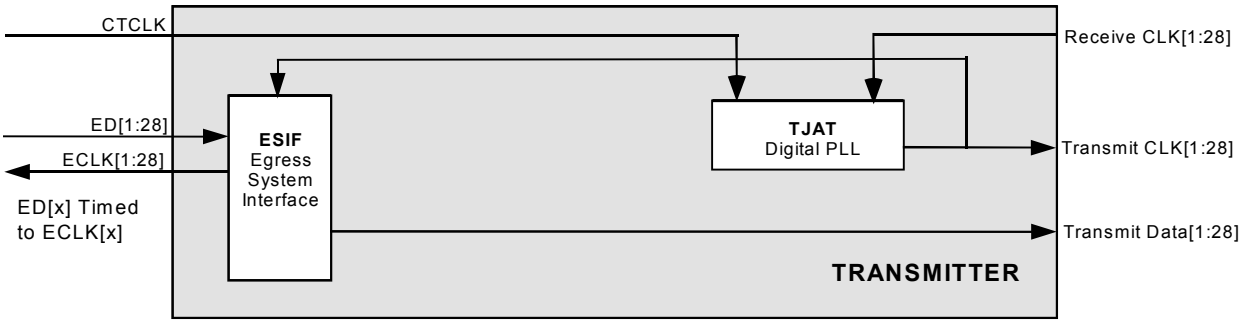
In all egress Clock Master modes the transmit clock can be sourced from either the common transmit clock, CTCLK, one of the two recovered clocks, RECVCLK1 and RECVCLK2, or the received clock for that link. The selection between CTCLK, RECVCLK1 and RECVCLK2 as the reference transmit clock is the same for all T1/E1 framers. Jitter attenuation can be applied to all master mode clocks with the TJAT.

Figure 14: Clock Master: NxChannel



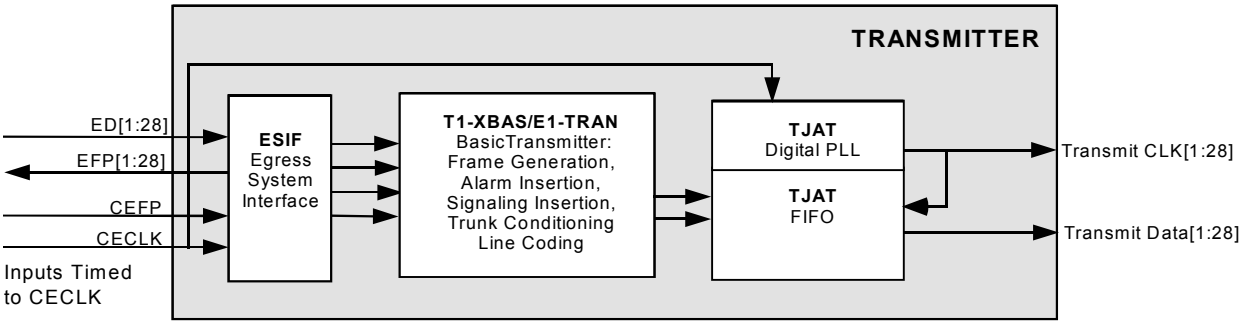
Clock Master: NxChannel mode does not indicate frame alignment to the upstream device. Instead, ECLK[x] is gapped on a per channel basis so that a subset of the 24 channels in a T1 frame or 32 channels in an E1 frame are inserted on ED[x]. Channel insertion is controlled by the IDLE_CHAN bits in the TPSC block's Egress Control Bytes. The framing bit position is always gapped, so the number of ECLK[x] pulses is controllable from 0 to 192 pulses per T1 frame or 0 to 256 pulses per E1 frame on a per-channel basis. The parity functions should not be enabled in NxChannel mode.

Figure 15: Clock Master: Clear Channel



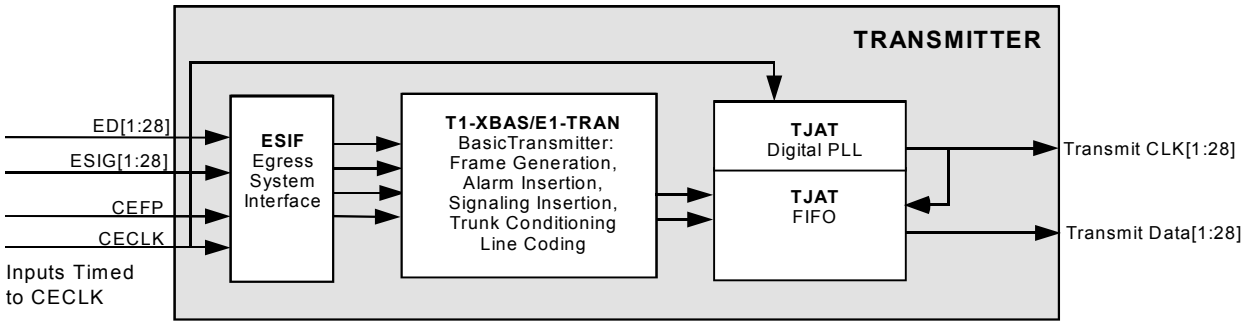
Clock Master: Clear Channel mode has no frame alignment therefore no frame alignment is indicated to the upstream device. ECLK[x] is a continuous clock at 1.544Mb/s for T1 links or 2.048Mb/s for E1 links.

Figure 16: Clock Slave: EFP Enabled



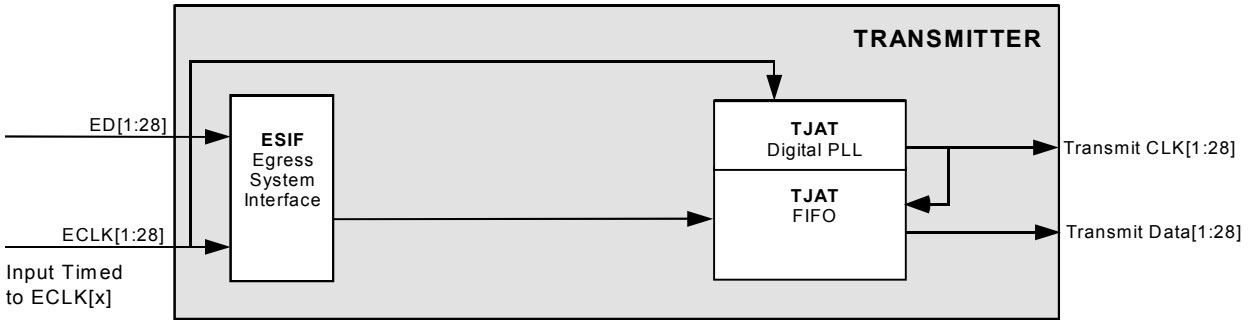
In Clock Slave: EFP Enabled mode, the egress interface is clocked by the common egress clock, CECLK. The transmitter is either frame-aligned or superframe-aligned to the common egress frame pulse, CEFP, via the CEMFP bit in the Master Egress Slave Mode Serial Interface Configuration register. EFP[x] is configurable to indicate the frame alignment or the superframe alignment of ED[x]. CECLK can be enabled to be either a 1.544 MHz clock for T1 links or a 2.048 MHz clock for T1 and E1 links. The CECLK2M bit in the Master Egress Slave Mode Serial Interface Configuration register selects the 2.048MHz clock for T1 operation.

Figure 17: Clock Slave: External Signaling



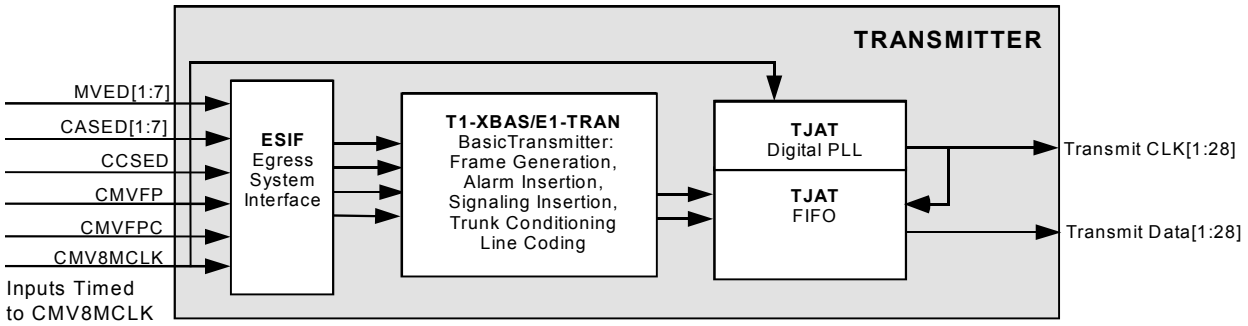
In Clock Slave: External Signaling mode, the egress interface is clocked by the common egress clock, CECLK. The transmitter is either frame-aligned or superframe-aligned to the common egress frame pulse, CEFP, via the CEMFP bit in the Master Egress Slave Mode Serial Interface Configuration register. The ESIG[x] signal contains the robbed-bit signaling data to be inserted into Transmit Data[x], with the four least significant bits of each channel on ESIG[x] representing the signaling state (ABCD or ABAB in T1 SF mode). EFP[x] is not available in this mode.

Figure 18: Clock Slave: Clear Channel



In Clock Slave: Clear Channel mode, the egress interface is clocked by the externally provided egress clock, ECLK[x]. ECLK[x] must be a 1.544 MHz clock for T1 links or a 2.048 MHz clock for E1 links. In this mode the T1/E1 framers are bypassed except for the TJAT which may or may not be bypassed depending on the setting of the TJATBYP bit in the T1/E1 Egress Line Interface Options register. Typically the TJAT would be bypassed unless jitter attenuation is required on ECLK[x].

Figure 19: Clock Slave: H-MVIP



When Clock Slave: H-MVIP mode is enabled a 8.192Mb/s H-MVIP egress interface multiplexes up to 672 channels from 28 T1s or 21 E1s, up to 672 channel associated signaling (CAS) channels from 28 T1s or 21 E1s and common channel signaling from up to 28 T1s or 21 E1s. The H-MVIP interfaces use common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

Seven H-MVIP data signals, MVED[1:7], share pins with serial PCM data inputs, ED[x], to provide H-MVIP access for up to 672 data channels. The H-MVIP mapping is fixed such that each group of four nearest neighbor T1 or E1 links make up the individual 8.192Mb/s H-MVIP signal. The multiplexed data input is shared with the lowest numbered T1 or E1 serial PCM link in the bundle, for example MVED[2] combines the DS0s or timeslots of ED[5,6,7,8] and is pin multiplexed with ED[5]. This mode is selected when the SYSOPT[2:0] bits in the Global Configuration register are set to H-MVIP.

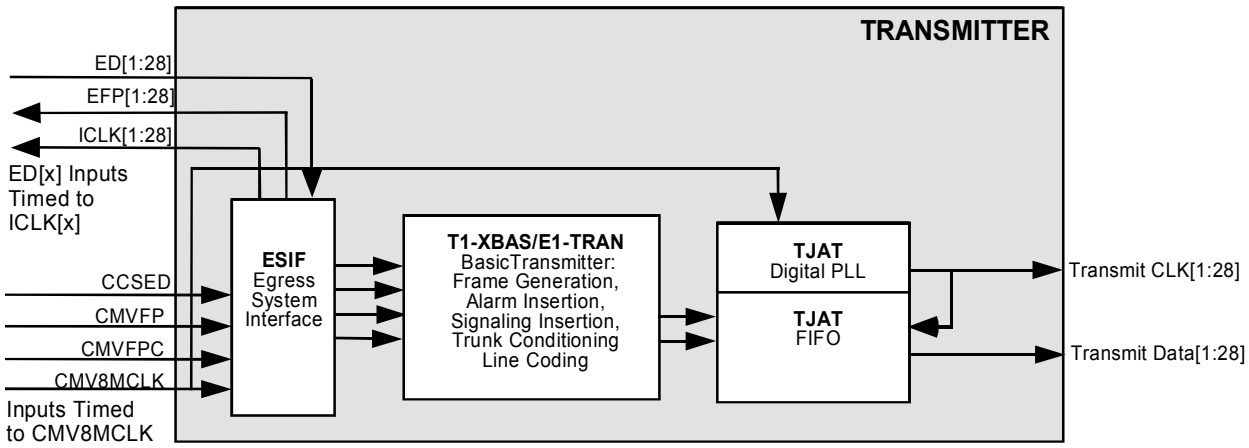
A separate seven signal H-MVIP interface is for access to the channel associated signaling for 672 channels. The CAS H-MVIP interface is time division multiplexed exactly the same way as the data channels. The CAS H-MVIP is synchronized with the H-MVIP data channels when SYSOPT[2:0] is set to H-MVIP mode. Over a T1 or E1 multi-frame the four CAS bits per channel are repeated with each data byte. Four stuff bits are used to pad each CAS nibble (ABCD bits) out to a full byte in parallel with each data byte. The egress CAS H-MVIP interface, CASED[1:7], is multiplexed with seven serial PCM egress data pins, ED[2,6,10,14,18,22,26].

The CAS H-MVIP interface can be used in parallel with the SBI Add bus as an alternative method for accessing the CAS bits while data transfer occurs over the SBI bus. This is selected when the SYSOPT[2:0] bits in the Global Configuration register are set to “SBI Interface with CAS or CCS H-MVIP Interface” and the ECCSEN bit in the T1/E1 Egress Serial Interface Mode Select register is set to 0.

A separate H-MVIP interface consisting of a single signal is used to time division multiplex the common channel signaling (CCS) for all T1s and E1s and additionally the V5 channels in E1 mode. The CCS H-MVIP interface, CCSED, is not multiplexed with any other pins. CCSED can be used in parallel with the Clock Slave:H-MVIP mode when SYSOPT[2:0] is set to "H-MVIP Interface" and the ECCSEN bit in the T1/E1 Egress Serial Interface Mode Select register is set to 1, a Clock Slave serial interface when SYSOPT[2:0] is set to "Serial Clock and Data Interface with CCS H-MVIP Interface", or the SBI Add bus when SYSOPT[2:0] is set to "SBI Interface with CAS or CCS H-MVIP Interface" and the ECCSEN bit is set to 1. The V5 channels in E1 mode can also be enabled over CCSEN when the ETS15EN and ETS31EN bits in the T1/E1 Egress Serial Interface Mode Select register are set to 1.

When accessing the CAS or CCS signaling via the H-MVIP interface in parallel with the SBI interface a transmit signaling elastic store is used to adapt any timing differences between the data interface and the CAS or CCS H-MVIP interface.

Figure 20: Clock Master: Serial Data and H-MVIP CCS



When Clock Master: Serial Data and H-MVIP CCS mode is enabled, payload data may be sourced through the egress serial interface, while common channel signaling is sourced in parallel through the H-MVIP interface.

The H-MVIP egress interface multiplexes common channel signaling from up to 28 T1s or 21 E1s. The H-MVIP interfaces use common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization. Common channel signaling over H-MVIP uses a Clock Slave serial interface, selected when SYSOPT[2:0] is set to "Serial Clock and Data Interface with CCS H-MVIP Interface". CCSED is a single dedicated input pin sampled by CMV8MCLK, used to time division multiplex the common channel signaling (CCS) for all T1s

and E1s and additionally the V5 channels in E1 mode. The V5 channels in E1 mode can also be enabled over CCSED when the ETS15EN and ETS31EN bits in the T1/E1 Egress Serial Interface Mode Select register are set to 1.

The ingress clock, ICLK[x], is a 1.544MHz or 2.048MHz clock generated from the 16.384MHz CMV8MCLK. (Note that in T1 mode, this clock does not divide down to T1 rate evenly, resulting in a gappy clock. The minimum period is 10 times that of CMV8MCLK.) ICLK[x] is pulsed for each bit in the 193 bit T1 or 256 bit E1 frame (i.e. NxDS0 controls are not applicable in this mode). Payload data on ID[x] is output relative to this clock. The ingress frame alignment is indicated by TECT3 on IFP[x], again timed to ICLK[x].

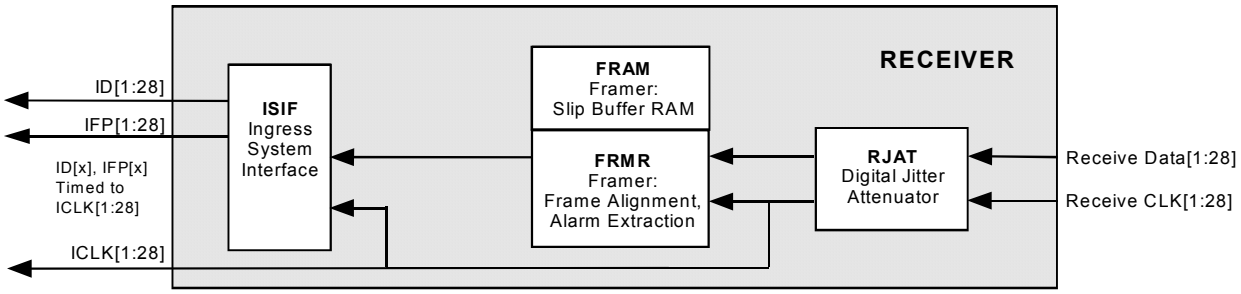
Note that several of the serial PCM egress data pins ED[x] are multiplexed with the egress data H-MVIP data interface. ED[1,5,9,13,17,21,25] share pins with the H-MVIP data signals MVED[1:7]. ED[2,6,10,14,18,22,26] share pins with the H-MVIP CAS signals CASED[1:7].

9.29 Ingress System Interface (ISIF)

The Ingress System Interface (ISIF) block provides system side serial clock and data access as well as H-MVIP access for up to 28 T1 or 21 E1 receive streams. There are several master and slave clock modes for serial clock and data system side access to the T1 and E1 streams. When enabled for 8.192Mb/s H-MVIP there are three separate interfaces for data and signaling. The H-MVIP signaling interfaces can be used in combination with the serial clock and data and SBI interface in certain applications. Control of the system side interface is global to TECT3 and is selected through the SYSOPT[2:0] bits in the Global Configuration register at address 0001H. The system interface options are serial clock and data, H-MVIP, SBI bus, SBI bus with CAS or CCS H-MVIP and serial clock and data with CCS H-MVIP.

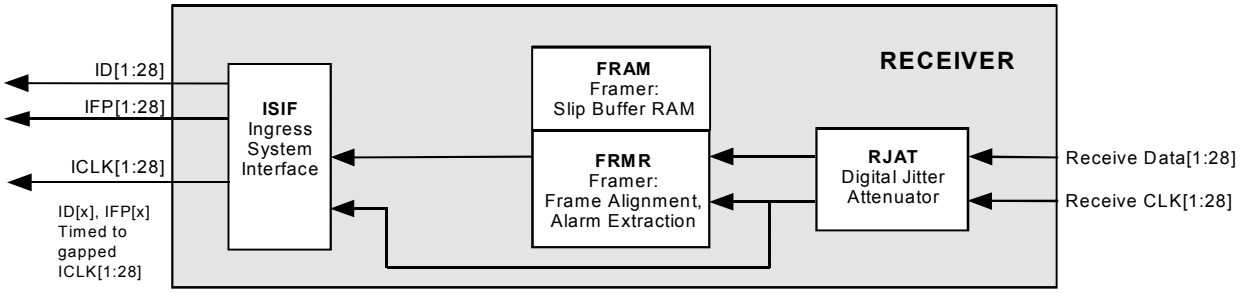
Three Clock Master modes provide a serial clock and data ingress interface with clocking provided by TECT3. The clock master modes are Clock Master: Full T1/E1, Clock Master : NxChannel, Clock Master: Clear Channel. Two Clock slave modes provide two serial clock and data ingress interfaces and a H-MVIP interface. All Clock slave modes accept externally sourced clocking. The clock slave modes are: Clock Slave: External Signaling or Clock Slave: H-MVIP. The ingress serial clock and data interface clocking modes are selected via the IMODE[1:0] bits in the T1/E1 Ingress Serial Interface Mode Select register. Clock Master: NxChannel and Clock Master: Full T1/E1 use the same IMODE[1:0] selection and are differentiated by the INXCHAN[1:0] bits in the same ragister as IMODE[1:0].

Figure 21: Clock Master: Full T1/E1



In Clock Master: Full T1/E1 mode, the elastic store is bypassed and the ingress clock (ICLK[x]) is a jitter attenuated version of the 1.544 MHz or 2.048 MHz receive clock coming from the M13 multiplex. Jitter attenuation is selectable by the RJATBYP bit in the T1/E1 Receive Options register. ICLK[x] is pulsed for each bit in the 193 bit T1 or 256 bit E1 frame. The ingress data appears on ID[x] and the ingress frame alignment is indicated by IFP[x]. In this mode, demultiplexed T1 or E1 data passes through the TECT3 unchanged during out-of-frame conditions, similar to an offline framer system. When the TECT3 is the clock master in the ingress direction, the elastic store is used to buffer between the ingress and egress clocks to facilitate per-Channel loopback.

Figure 22: Clock Master: NxChannel



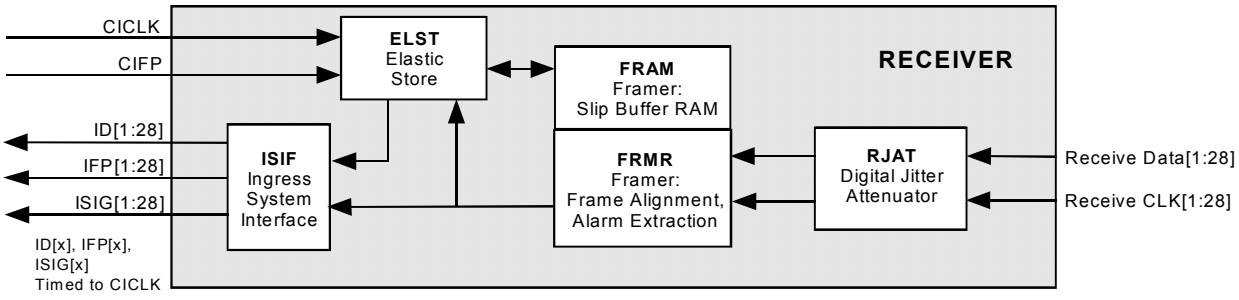
In Clock Master: NxChannel mode, ICLK[x] is a gapped version of the jitter attenuated 1.544 MHz or 2.048 MHz receive clock coming from the M13 multiplex. ICLK[x] is gapped on a per channel basis so that a subset of the 24 channels in the T1 frame or 32 channels in an E1 frame is extracted on ID[x]. IFP[x] indicates frame alignment but has no clock since it is gapped during the framing bits. Channel extraction is controlled by the RPSC block. The framing bit position is always gapped, so the number of ICLK[x] pulses is controllable from 0 to 192 pulses per T1 frame or 0 to 256 pulses per E1 frame on a per-channel basis. In this mode, demultiplexed or demapped T1 or E1 streams pass through

the TECT3 unchanged during out-of-frame conditions. The parity functions are not usable in NxChannel mode. When the TECT3 is the clock master in the ingress direction, the elastic store is used to buffer between the ingress and egress clocks to facilitate per-Channel loopback.

Figure 23: Clock Master: Clear Channel

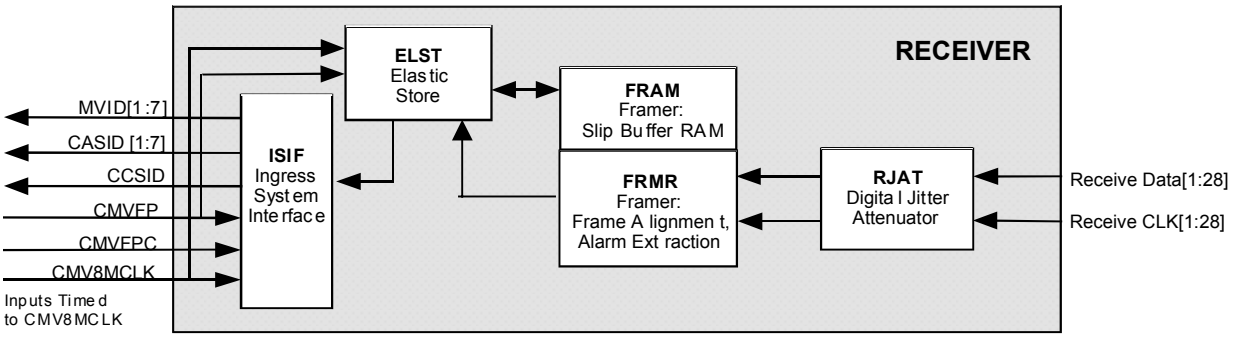
In Clock Master: Clear Channel mode, the elastic store is bypassed and the ingress clock (ICLK[x]) is a jitter attenuated version of the 1.544 MHz or 2.048 MHz receive clock coming from the M13 multiplex. The ingress data appears on ID[x] which no frame alignment indication. Per channel loopbacks are not available in Clear channel mode. The RCVCLRCH mode bit in the T1/E1 Receive Options register must be set to 1 in Clock master: Clear Channel mode.

Figure 24: Clock Slave: External Signaling



In Clock Slave: External Signaling mode, the elastic store is enabled to permit CICLK to specify the ingress-side timing. The ingress data on ID[x] and signaling ISIG[x] are bit aligned to the 1.544 MHz or 2.048 MHz common ingress clock (CICLK) and are frame aligned to the common ingress frame pulse (CIFP). CICLK can be enabled to be a 1.544 MHz clock or a 2.048 MHz clock. ISIG[x] contains the robbed-bit signaling state (ABCD or ABAB) in the lower four bits of each channel. IFP[x] indicates either the frame or superframe alignment on ID[x].

Figure 25: Clock Slave: H-MVIP



When Clock Slave: H-MVIP mode is enabled a 8.192Mb/s H-MVIP ingress interface multiplexes up to 672 channels from 28 T1s or 21 E1s, up to 672 channel associated signaling (CAS) channels from 28 T1s or 21 E1s and common channel signaling (CCS) from up to 28 T1s or 21 E1s. The H-MVIP interfaces use common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

The three ingress H-MVIP interfaces operate independently except that using any one of these forces the T1 or E1 framer to operate in synchronous mode, meaning that elastic stores are used.

Seven H-MVIP data signals, MVID[1:7], share pins with serial PCM data outputs, ID[x], to provide H-MVIP access for up to 672 data channels. The H-MVIP mapping is fixed such that each group of four nearest neighbor T1 or E1 links make up the individual 8.192Mb/s H-MVIP signal. The multiplexed data input is shared with the lowest numbered T1 or E1 serial PCM link in the bundle, for example MViD[2] combines the DS0s or timeslots of ID[5,6,7,8] and is pin multiplexed with ID[5]. This mode is selected when the SYSOPT[2:0] bits in the Global Configuration register are set to H-MVIP.

A separate H-MVIP interface consisting of seven pins is for access to the channel associated signaling for all of the 672 data channels. The CAS is time division multiplexed exactly the same way as the data channels and is synchronized with the H-MVIP data channels. Over a T1 or E1 multi-frame the four CAS bits per channel are repeated with each data byte. Four stuff bits are used to pad each CAS nibble (ABCD bits) out to a full byte in synchronization with each data byte. The ingress CAS H-MVIP interface, CASID[1:7], is multiplexed with seven serial PCM ingress data pins, ID[2,6,10,14,18,22,26].

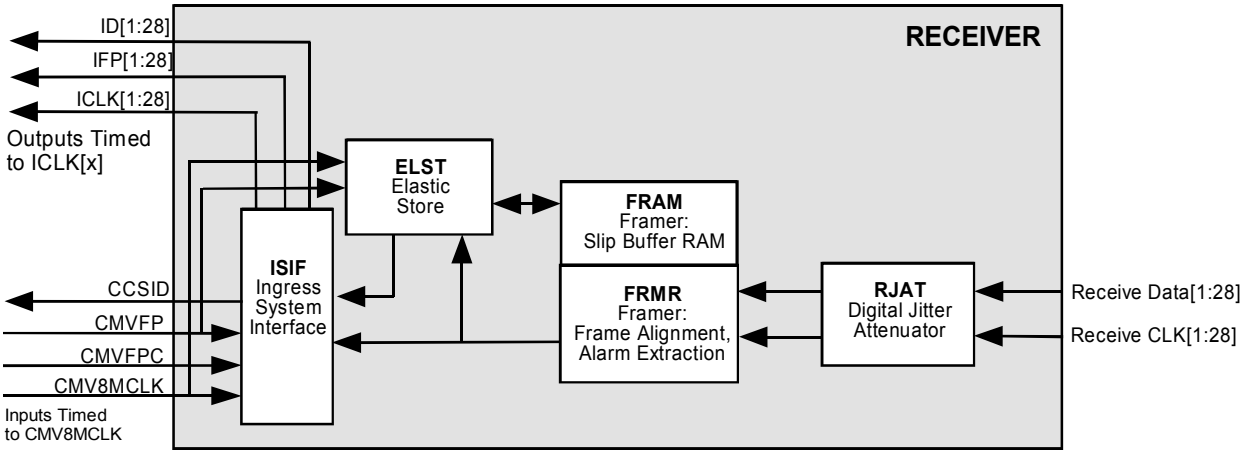
The CAS H-MVIP interface can be used in parallel with the SBI Drop bus as an alternative method for accessing the CAS bits while data transfer occurs over the

SBI bus. This is selected when the SYSOPT[2:0] bits in the Global Configuration register are set to “SBI Interface with CAS or CCS H-MVIP Interface” and the ICCSSEL bit in the T1/E1 Ingress Serial Interface Mode Select register is set to 0.

A separate H-MVIP interface consisting of a single signal is used to time division multiplex the common channel signaling (CCS) for all T1s and E1s and additionally the V5 channels in E1 mode. The CCS H-MVIP interface, CCSID, is not multiplexed with any other pins. CCSID can be used in parallel with the Clock Slave:H-MVIP mode when SYSOPT[2:0] is set to “H-MVIP Interface” and the ICCSSEL bit in the T1/E1 Ingress Serial Interface Mode Select register is set to 1, a Clock Slave serial interface when SYSOPT[2:0] is set to “Serial Clock and Data Interface with CCS H-MVIP Interface”, or the SBI Add bus when SYSOPT[2:0] is set to “SBI Interface with CAS or CCS H-MVIP Interface” and the ICCSSEL bit is set to 1.

When accessing the CAS or CCS signaling via the H-MVIP interface in parallel with serial clock and data or SBI interfaces a receive signaling elastic store is used to adapt any timing differences between the data interface and the CAS or CCS H-MVIP interface.

Figure 26: Clock Slave: Serial Data and H-MVIP CCS



When Clock Slave: H-MVIP mode is enabled, payload data may be extracted throught the ingress serial interface, while common channel signaling is extracted in parallel through the H-MVIP interface.

The H-MVIP ingress interface multiplexes common channel signalling from up to 28 T1s or 21 E1s. The H-MVIP interfaces use common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization. Common channel signaling over H-MVIP uses a Clock Slave serial interface, selected when

SYSOPT[2:0] is set to “Serial Clock and Data Interface with CCS H-MVIP Interface”. CCSID is a singal dedicated output pin, output relative to CMV8MCLK, used to time division multiplex the common channel signaling (CCS) for all T1s and E1s, and additionally the V5 channels in E1 mode.

The ingress clock, ICLK[x], is a 1.544MHz or 2.048MHz clock generated from the 16.384MHz CMV8MCLK. (Note that in T1 mode, this clock does not divide down to T1 rate evenly, resulting in a gappy clock. The minimum period is 10 times that of CMV8MCLK.) ICLK[x] is pulsed for each bit in the 193 bit T1 or 256 bit E1 frame (i.e. NxDS0 controls are not applicable in this mode). Payload data on ED[x] is sampled by this clock. The egress frame alignment is indicated by TECT3 on EFP[x], again timed to ICLK[x].

Note that several of the serial PMC ingress data pins ID[x] are multiplexed with the ingress data H-MVIP interface. ID[1,5,9,13,17,21,25] share pins with the H-MVIP data signals MVID[1:7]. ID[2,6,10,14,18,22,26] share pins with the H-MVIP CAS signals CASID[1:7]. Note also that in this mode, a receive signaling elastic store is used to adapt any timing differences between the data interface and the CCS H-MVIP interface.

9.30 Extract Scaleable Bandwidth Interconnect (EXSBI)

The Extract Scaleable Bandwidth Interconnect block demaps up to 28 1.544Mb/s links or a single 44.736Mb/s link from the SBI shared bus. The 1.544Mb/s links can be unframed when used in a straight multiplexer application, or they can be T1 framed and channelized for insertion into the DS3 multiplex. The 44.736Mb/s link can be DS3 unchannelized when the TECT3 is used as a DS3 framer.

All egress links extracted from the SBI bus can be timed from the source or from the TECT3. When Timing is from the source the EXSBI commands the PISO to generate 1.544Mb/s or 44.736Mb/s clocks slaved to the arrival rate of the data or from timing link rate adjustments provided from the source and carried with the links over the SBI bus. The 1.544Mb/s clock is synthesized from the 19.44MHz reference clock, SREFCLK, by dividing the clock by either 12 or 13 in a fixed sequence that produces the nominal 1.544Mb/s rate. Timing adjustments are made over 500uS intervals and are done by either advancing or retarding the phase or by adding or deleting a whole 1.544Mb/s clock cycle over the 500uS period.

The 44.736Mb/s clock is synthesized from the 51.84MHz or 44.928MHz reference clock, CLK52M. Using either reference clock frequency, the 44.736Mb/s rate is generated by gapping the reference clock in a fixed way. Timing adjustments are performed by adding or deleting four clocks over the 500uS period.

When the TECT3 is the SBI egress clock master for a link, clocks are sourced within the TECT3. Based on buffer fill levels, the EXSBI sends link rate adjustment commands to the link source indicating that it should send one additional or one fewer bytes of data during the next 500uS interval. Failure of the source to respond to these commands will ultimately result in overflows or underflows which can be configured to generate per link interrupts.

Channelized T1s extracted from the SBI bus optionally have the channel associated signaling (CAS) bits explicitly defined and carried in parallel with the DS0s, but only if the SBI interface is configured for synchronous mode operation.

Note that ITU-T G.747 mutiplexed E1 streams are not supported over the SBI interface. The E1 mode of operation is restricted to using the serial clock and data or H-MVIP system interfaces.

9.31 Insert Scaleable Bandwidth Interconnect (INSBI)

The Insert Scaleable Bandwidth Interconnect block maps up to 28 1.544Mb/s links or a single 44.736Mb/s link into the SBI shared bus. The 1.544Mb/s links can be unframed when sourced directly from the DS3 multiplexer, or they can be T1 channelized when sourced by the T1 framers. The 44.736Mb/s link can also be unframed when sourced directly from the DS3 interface. The 44.736Mb/s link can be an unchannelized DS3 when sourced from the DS3 framer.

Links inserted into the SBI bus can be timed from the TECT3 or from the far end. The INSBI makes link rate adjustments by adding or deleting an extra byte of data over a 500uS interval based on buffer fill levels. Timing adjustments made by the INSBI are detected by the receiving SBI interface by explicit signals in the SBI bus structure.

The INSBI optionally sends link rate information across the SBI bus. This information is used by the receiving SBI interface to create a recovered link clock which is based on small clock phase adjustments signaled by the INSBI.

Channelized T1s inserted into the SBI bus optionally have the channel associated signaling (CAS) bits explicitly defined and carried in parallel with the DS0s or timeslots, but only if the SBI interface is configured for synchronous mode operation. When enabled for CAS insertion the INSBI takes a byte serial stream of CAS bits from the SBISIPO and inserts them into the SBI bus structure.

Note that ITU-T G.747 mutiplexed E1 streams are not supported over the SBI interface. The E1 mode of operation is restricted to using the serial clock and data or H-MVIP system interfaces.

9.32 Scaleable Bandwidth Interconnect PISO (SBIPISO)

The Scaleable Bandwidth Interconnect Parallel to Serial converter (SBIPISO) generates up to 28 T1s or a DS3 serial clock and data signals from the byte serial stream provided by the Extract SBI block. The generated clock rate can be controlled with commands from the EXSBI. In clock slave mode the generated clock will be increased or decreased in small increments based on FIFO fill levels within the EXSBI or directly with clock rate commands from the far end device who is mastering the clock across the SBI bus. In clock master mode the SBIPISO controls the bit rate by accepting data from the EXSBI at the rate of the individual T1 or DS3 clocks sourced into it.

In addition the SBIPISO generates serial CAS signaling streams, frame pulses and multiframe pulses for all T1s and DS3.

9.33 Scaleable Bandwidth Interconnect SIPO (SBISIPO)

The Scaleable Bandwidth Interconnect Serial to Parallel converter (SBISIPO) sinks up to 28 T1s or a DS3 serial clock and data signals and generates a byte serial stream to the Insert SBI block. The SBISIPO measures the serial clock against the SBI reference clock and sends this information to the INSBI block and in turn across the SBI bus to the clock generation slave, SBIPISO. In this way an accurate representation of the input clock rate is communicated across the SBI bus.

In addition the SBISIPO generates byte serial streams from serial CAS signaling signals, frame pulses and multiframe pulses for all T1s and DS3.

9.34 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The TECT3 identification code is 383150CD hexadecimal.

9.35 Microprocessor Interface

The Microprocessor Interface Block provides normal and test mode registers, the interrupt logic, and the logic required to connect to the Microprocessor Interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the TECT3.

The Register Memory Map in Table 2 shows where the normal mode registers are accessed. The registers are organized so that backward software

compatibility with existing PMC devices is optimized. The resulting register organization splits into sections: Master configuration registers, 28 sets of T1/E1 Framer registers, DS3 M13 multiplexing registers and SBI registers.

On power up reset the TECT3 defaults to 28 T1 framers multiplexed into the M13 multiplexer using the DS3 M23 multiplex format. For proper operation some register configuration is necessary. System side access defaults to the SBI bus without any tributaries enabled which will leave the SBI Drop bus tristated. By default interrupts will not be enabled, automatic alarm generation is disabled, a dual rail DS3 LIU interface is expected and an external transmit reference clock is required.

Table 2: Register Memory Map

Address	Register
0000H	Global Reset
0001H	Global Configuration
0002H	Revision/Global PMON Update
0003H	Master Recovered Clock#1/Reference Clock Select
0004H	Recovered Clock#2 Select
0005H	Master Common Egress Serial and H-MVIP Interface Configuration
0006H	Master Common Ingress Serial and H-MVIP Interface Configuration
0007H-000FH	Reserved
00010H	Master Clock Monitor #1
0011H	Master Clock Monitor #2
0012H	Master Clock Monitor #3
0013H	Master Clock Monitor #4
0014H	Master Clock Monitor #5
0015H-001FH	Reserved
0020H	Master Interrupt Source
0021H	Master Interrupt Status T1/E1 #1-8

Address	Register
0022H	Master Interrupt Status T1/E1 #9-16
0023H	Master Interrupt Status T1/E1 #17-24
0024H	Master Interrupt Status T1 #25-28
0025H	Reserved
0026H	Master Interrupt Status Source SBI
0027H	Reserved
0028H	Master Interrupt Status DS3
0029H	Master Interrupt Status DS2
002AH	Master Interrupt Status MX12
002BH	Reserved
002CH	Master SBIDET0 Collision Detect LSB
002DH	Master SBIDET0 Collision Detect MSB
002EH	Master SBIDET1 Collision Detect LSB
002FH	Master SBIDET1 Collision Detect MSB
0030H-007FH	Reserved
0080H-00FFH	**T1/E1 Framer Slice #1**
0080H	T1/E1 Master Configuration
0081H	Reserved
0082H	T1/E1 Receive Options
0083H	T1/E1 Alarm Configuration
0084H	T1/E1 Egress Line Interface Configuration
0085H	T1/E1 Master Ingress Serial Interface Mode Select
0086H	T1/E1 Master Egress Serial Interface Mode Select
0087H	T1/E1 Master Ingress Parity and Alarm Enable
0088H	T1/E1 Master Egress Parity Enable
0089H	T1/E1 Master Serial Interface Configuration
008AH	T1/E1 Transmit Framing and Bypass Options

Address	Register
008BH	T1/E1 Interrupt Source #1
008CH	T1/E1 Interrupt Source #2
008DH	T1/E1 Diagnostics
008EH	T1/E1 PRBS Positioning and HDLC Control
008FH	Reserved
0090H	RJAT Interrupt Status
0091H	RJAT Reference Clock Divisor N1 Control
0092H	RJAT Output Clock Divisor N2 Control
0093H	RJAT Configuration
0094H	TJAT Interrupt Status
0095H	TJAT Reference Clock Divisor N1 Control
0096H	TJAT Output Clock Divisor N2 Control
0097H	TJAT Configuration
0098H	RX-ELST Configuration
0099H	RX-ELST Interrupt Enable/Status
009AH	RX-ELST Idle Code
009BH	RX-ELST Reserved
009CH	TX-ELST Configuration
009DH	TX-ELST Interrupt Enable/Status
009EH-009FH	TX-ELST Reserved
00A0H	RXCE Ingress Data Link Control
00A1H	RXCE Ingress Data Link Bit Select
00A2H-00A7H	RXCE Reserved
00A8H	TXCI Egress Data Link Control
00A9H	TXCI Egress Data Link Bit Select
00AAH-00AFH	TXCI Reserved

Address	Register
00B0H	RPSC Configuration
00B1H	RPSC µP Access Status
00B2H	RPSC Channel Indirect Address/Control
00B3H	RPSC Channel Indirect Data Buffer
00B4H	TPSC Configuration
00B5H	TPSC µP Access Status
00B6H	TPSC Channel Indirect Address/Control
00B7H	TPSC Channel Indirect Data Buffer
00B8H	PMON Interrupt Enable/Status
00B9H	PMON Framing Bit Error Count
00BAH	PMON OOF/COFA/Far End Block Error Count (LSB)
00BBH	PMON OOF/COFA/Far End Block Error Count (MSB)
00BCH	PMON Bit Error/CRCE Count (LSB)
00BDH	PMON Bit Error/CRCE Count (MSB)
00BEH	PMON Reserved
00BFH	PMON Reserved
00C0H	RDLC Configuration
00C1H	RDLC Interrupt Control
00C2H	RDLC Status
00C3H	RDLC Data
00C4H	RDLC Primary Address Match
00C5H	RDLC Secondary Address Match
00C6H-00C7H	Reserved
00C8H	TDPR Configuration
00C9H	TDPR Upper Transmit Threshold
00CAH	TDPR Lower Transmit Threshold
00CBH	TDPR Interrupt Enable

Address	Register
00CCH	TDPR Interrupt Status/UDR Clear
00CDH	TDPR Transmit Data
00CEH-00CFH	Reserved
00D0H	PRBS Generator/Checker Control
00D1H	PRBS Checker Interrupt Enable/Status
00D2H	PRBS Pattern Select
00D3H	PRBS Reserved
00D4H	PRBS Error Count Register #1
00D5H	PRBS Error Count Register #2
00D6H	PRBS Error Count Register #3
00D7H	PRBS Reserved
00D8H	SIGX Configuration/Change of Signaling State
00D9H	SIGX Channel Indirect Status/Change of Signaling State
00DAH	SIGX Channel Indirect Address/Control/ Change of Signaling State
00DBH	SIGX Channel Indirect Data Buffer/Change of Signaling State
00DCH	RX-SIG-ELST Configuration
00DDH	RX- SIG-ELST Interrupt Enable/Status
00DEH	RX- SIG-ELST Idle Code
00DFH	RX- SIG-ELST Reserved
00E0H	T1 ALMI Configuration
00E1H	T1 ALMI Interrupt Enable
00E2H	T1 ALMI Interrupt Status
00E3H	T1 ALMI Alarm Detection Status
00E4H	T1 XBOC Control
00E5H	T1 XBOC Code
00E6H	T1 RBOC Enable

Address	Register
00E7H	T1 RBOC Code Status
00E8H	T1 XBAS Configuration
00E9H	T1 XBAS Alarm Transmit
00EAH-00EBH	T1 XBAS Reserved
00ECH	T1 FRMR Configuration
00EDH	T1 FRMR Interrupt Enable
00EEH	T1 FRMR Interrupt Status
00EFH	T1 FRMR Reserved
00F0H	T1 APRM Configuration/Control
00F1H	T1 APRM Manual Load
00F2H	T1 APRM Interrupt Status
00F3H	T1 APRM One Second Content Octet 2
00F4H	T1 APRM One Second Content Octet 3
00F5H	T1 APRM One Second Content Octet 4
00F6H	T1 APRM One Second Content MSB (Octet 5)
00F7H	T1 APRM One Second Content LSB (Octet 6)
00E0H	E1 FRMR Frame Alignment Options
00E1H	E1 FRMR Maintenance Mode Options
00E2H	E1 FRMR Framing Status Interrupt Enable
00E3H	E1 FRMR Maintenance/Alarm Status Interrupt Enable
00E4H	E1 FRMR Framing Status Interrupt Indication
00E5H	E1 FRMR Maintenance/Alarm Status Interrupt Indication
00E6H	E1 FRMR Framing Status
00E7H	E1 FRMR Maintenance/Alarm Status
00E8H	E1 FRMR International/National Bits
00E9H	E1 FRMR CRC Error Count - LSB
00EAH	E1 FRMR CRC Error Count - MSB

Address	Register
00EBH	E1 FRMR National Bit Codeword Interrupt Enables
00ECH	E1 FRMR National Bit Codeword Interrupts
00EDH	E1 FRMR National Bit Codewords
00EEH	E1 FRMR Frame Pulse/Alarm Interrupt Enables
00EFH	E1 FRMR Frame Pulse/Alarm Interrupt
00F0H	E1 TRAN Configuration
00F1H	E1 TRAN Transmit Alarm/Diagnostic Control
00F2H	E1 TRAN International Control
00F3H	E1 TRAN Extra Bits Control
00F4H	E1 TRAN Interrupt Enable
00F5H	E1 TRAN Interrupt Status
00F6H	E1 TRAN National Bit Codeword Select
00F7H	E1 TRAN National Bit Codeword
00F8H-00FFH	Reserved
0100H-017FH	**T1/E1 Framer Slice #2**
0180H-01FFH	**T1/E1 Framer Slice #3**
0200H-027FH	**T1/E1 Framer Slice #4**
0280H-02FFH	**T1/E1 Framer Slice #5**
0300H-037FH	**T1/E1 Framer Slice #6**
0380H-03FFH	**T1/E1 Framer Slice #7**
0400H-047FH	**T1/E1 Framer Slice #8**
0480H-04FFH	**T1/E1 Framer Slice #9**

Address	Register
0500H-057FH	**T1/E1 Framer Slice #10**
0580H-05FFH	**T1/E1 Framer Slice #11**
0600H-067FH	**T1/E1 Framer Slice #12**
0680H-06FFH	**T1/E1 Framer Slice #13**
0700H-077FH	**T1/E1 Framer Slice #14**
0780H-07FFH	**T1/E1 Framer Slice #15**
0800H-087FH	**T1/E1 Framer Slice #16**
0880H-08FFH	**T1/E1 Framer Slice #17**
0900H-097FH	**T1/E1 Framer Slice #18**
0980H-09FFH	**T1/E1 Framer Slice #19**
0A00H-0A7FH	**T1/E1 Framer Slice #20**
0A80H-0AFFH	**T1/E1 Framer Slice #21**
0B00H-0B7FH	**T1 Framer Slice #22**
0B00H	T1/E1 Master Configuration
0B01H	Reserved
0B02H	T1/E1 Receive Options
0B03H	T1/E1 Ingress Line Interface Configuration
0B04H	T1/E1 Egress Line Interface Configuration
0B05H	T1/E1 Master Ingress Serial Interface Mode Select

Address	Register
0B06H	T1/E1 Master Egress Serial Interface Mode Select
0B07H	T1/E1 Master Ingress Parity and Alarm Enable
0B08H	T1/E1 Master Egress Parity Enable
0B09H	T1/E1 Master Serial Interface Configuration
0B0AH	T1/E1 Transmit Framing and Bypass Options
0B0BH	T1/E1 Interrupt Source #1
0B0CH	T1/E1 Interrupt Source #2
0B0DH	T1/E1 Diagnostics
0B0EH	T1/E1 PRBS Positioning and HDLC Control
0B0FH	Reserved
0B10H	RJAT Interrupt Status
0B11H	RJAT Reference Clock Divisor N1 Control
0B12H	RJAT Output Clock Divisor N2 Control
0B13H	RJAT Configuration
0B14H	TJAT Interrupt Status
0B15H	TJAT Reference Clock Divisor N1 Control
0B16H	TJAT Output Clock Divisor N2 Control
0B17H	TJAT Configuration
0B18H	RX-ELST Configuration
0B19H	RX-ELST Interrupt Enable/Status
0B1AH	RX-ELST Idle Code
0B1BH	RX-ELST Reserved
0B1CH	TX-ELST Configuration
0B1DH	TX-ELST Interrupt Enable/Status
0B1EH-0B1FH	TX-ELST Reserved
0B20H	RXCE Ingress Data Link Control
0B21H	RXCE Ingress Data Link Bit Select

Address	Register
0B22H-0B27H	RXCE Reserved
0B28H	TXCI Egress Data Link Control
0B29H	TXCI Egress Data Link Bit Select
0B2AH-0B2FH	TXCI Reserved
0B30H	RPSC Configuration
0B31H	RPSC µP Access Status
0B32H	RPSC Channel Indirect Address/Control
0B33H	RPSC Channel Indirect Data Buffer
0B34H	TPSC Configuration
0B35H	TPSC µP Access Status
0B36H	TPSC Channel Indirect Address/Control
0B37H	TPSC Channel Indirect Data Buffer
0B38H	PMON Interrupt Enable/Status
0B39H	PMON Framing Bit Error Count
0B3AH	PMON OOF/COFA/Far End Block Error Count (LSB)
0B3BH	PMON OOF/COFA/Far End Block Error Count (MSB)
0B3CH	PMON Bit Error/CRCE Count (LSB)
0B3DH	PMON Bit Error/CRCE Count (MSB)
0B3EH	PMON Reserved
0B3FH	PMON Reserved
0B40H	RDLC Configuration
0B41H	RDLC Interrupt Control
0B42H	RDLC Status
0B43H	RDLC Data
0B44H	RDLC Primary Address Match
0B45H	RDLC Secondary Address Match

Address	Register
0B46H-0B47H	Reserved
0B48H	TDPR Configuration
0B49H	TDPR Upper Transmit Threshold
0B4AH	TDPR Lower Transmit Threshold
0B4BH	TDPR Interrupt Enable
0B4CH	TDPR Interrupt Status/UDR Clear
0B4DH	TDPR Transmit Data
0B4EH-0B4FH	Reserved
0B50H	PRBS Generator/Checker Control
0B51H	PRBS Checker Interrupt Enable/Status
0B52H	PRBS Pattern Select
0B53H	PRBS Reserved
0B54H	PRBS Error Count Register #1
0B55H	PRBS Error Count Register #2
0B56H	PRBS Error Count Register #3
0B57H	PRBS Reserved
0B58H	SIGX Configuration/Change of Signaling State
0B59H	SIGX Channel Indirect Status/Change of Signaling State
0B5AH	SIGX Channel Indirect Address/Control/ Change of Signaling State
0B5BH	SIGX Channel Indirect Data Buffer/Change of Signaling State
0B5CH	RX-SIG-ELST Configuration
0B5DH	RX- SIG-ELST Interrupt Enable/Status
0B5EH	RX- SIG-ELST Idle Code
0B5FH	RX- SIG-ELST Reserved
0B60H	T1 ALMI Configuration

Address	Register
0B61H	T1 ALMI Interrupt Enable
0B62H	T1 ALMI Interrupt Status
0B63H	T1 ALMI Alarm Detection Status
0B64H	T1 XBOC Control
0B65H	T1 XBOC Code
0B66H	T1 RBOC Enable
0B67H	T1 RBOC Code Status
0B68H	T1 XBAS Configuration
0B69H	T1 XBAS Alarm Transmit
0B6AH-0B6BH	T1 XBAS Reserved
0B6CH	T1 FRMR Configuration
0B6DH	T1 FRMR Interrupt Enable
0B6EH	T1 FRMR Interrupt Status
0B6FH	T1 FRMR Reserved
0B70H	T1 APRM Configuration/Control
0B71H	T1 APRM Manual Load
0B72H	T1 APRM Interrupt Status
0B73H	T1 APRM One Second Content Octet 2
0B74H	T1 APRM One Second Content Octet 3
0B75H	T1 APRM One Second Content Octet 4
0B76H	T1 APRM One Second Content MSB (Octet 5)
0B77H	T1 APRM One Second Content LSB (Octet 6)
0B78H-0B7FH	Reserved
0B80H-0BFFH	**T1 Framer Slice #23**
0C00H-0C7FH	**T1 Framer Slice #24**

Address	Register
0C80H-0CFFH	**T1 Framer Slice #25**
0D00H-0D7FH	**T1 Framer Slice #26**
0D80H-0DFFH	**T1 Framer Slice #27**
0E00H-0E7FH	**T1 Framer Slice #28**
0E80H-0FFFH	Reserved
1000H-10FFH	**DS3 FRAMER and M13 Multiplexer**
1000H	DS3 Master Reset
1001H	DS3 Master Data Source
1002H	DS3 Master Unchannelized Interface Options
1003H	DS3 Master Transmit Line Options
1004H	DS3 Master Receive Line Options
1005H	DS3 Master Alarm Enable
1006H	DS2 Master Alarm Enable / DS3 Network Requirement Bit
1007H	Reserved
1008H	DS3 TRAN Configuration
1009H	DS3 TRAN Diagnostic
100AH-100BH	DS3 TRAN Reserved
100CH	DS3 FRMR Configuration
100DH	DS3 FRMR Interrupt Enable/Additional Configuration
100EH	DS3 FRMR Interrupt Status
100FH	DS3 FRMR Status
1010H	DS3 PMON Performance Meters
1011H	DS3 PMON Interrupt Enable/Status

Address	Register
1012H	DS3 PMON Reserved
1013H	DS3 PMON Reserved
1014H	DS3 PMON Line Code Violation Event Count LSB
1015H	DS3 PMON Line Code Violation Event Count MSB
1016H	DS3 PMON Framing Bit Error Event Count LSB
1017H	DS3 PMON Framing Bit Error Event Count MSB
1018H	DS3 PMON Excessive Zeros LSB
1019H	DS3 PMON Excessive Zeros MSB
101AH	DS3 PMON Parity Error Event Count LSB
101BH	DS3 PMON Parity Error Event Count MSB
101CH	DS3 PMON Path Parity Error Event Count LSB
101DH	DS3 PMON Path Parity Error Event Count MSB
101EH	DS3 PMON FEBE Event Count LSB
101FH	DS3 PMON FEBE Event Count MSB
1020H	DS3 TDPR Configuration
1021H	DS3 TDPR Upper Transmit Threshold
1022H	DS3 TDPR Lower Interrupt Threshold
1023H	DS3 TDPR Interrupt Enable
1024H	DS3 TDPR Interrupt Status/UDR Clear
1025H	DS3 TDPR Transmit Data
1026H-1027H	DS3 TDPR Reserved
1028H	DS3 RDLC Configuration
1029H	DS3 RDLC Interrupt Control
102AH	DS3 RDLC Status
102BH	DS3 RDLC Data
102CH	DS3 RDLC Primary Address Match
102DH	DS3 RDLC Secondary Address Match

Address	Register
102EH-102FH	DS3 RDLC Reserved
1030H	PRGD Control
1031H	PRGD Interrupt Enable/Status
1032H	PRGD Length
1033H	PRGD Tap
1034H	PRGD Error Insertion
1035H-1037H	PRGD Reserved
1038H	PRGD Pattern Insertion Register #1
1039H	PRGD Pattern Insertion Register #2
103AH	PRGD Pattern Insertion Register #3
103BH	PRGD Pattern Insertion Register #4
103CH	PRGD Pattern Detector Register #1
103DH	PRGD Pattern Detector Register #2
103EH	PRGD Pattern Detector Register #3
103FH	PRGD Pattern Detector Register #4
1040H	MX23 Configuration
1041H	MX23 Demux AIS Insert
1042H	MX23 Mux AIS Insert
1043H	MX23 Loopback Activate
1044H	MX23 Loopback Request Insert
1045H	MX23 Loopback Request Detect
1046H	MX23 Loopback Request Interrupt
1047H	MX23 Reserved
1048H	FEAC XBOC Control
1049H	FEAC XBOC Code
104AH	FEAC RBOC Configuration/Interrupt Enable
104BH	FEAC RBOC Interrupt Status

Address	Register
104CH-105FH	Reserved
1060H	DS2 FRMR #1 Configuration
1061H	DS2 FRMR #1 Interrupt Enable
1062H	DS2 FRMR #1 Interrupt Status
1063H	DS2 FRMR #1 Status
1064H	DS2 FRMR #1 Monitor Interrupt Enable/Status
1065H	DS2 FRMR #1 FERR Count
1066H	DS2 FRMR #1 PERR Count (LSB)
1067H	DS2 FRMR #1 PERR Count (MSB)
1068H-106FH	Reserved
1070H	MX12 #1 Configuration and Control
1071H	MX12 #1 Loopback Code Select
1072H	MX12 #1 Mux/Demux AIS Insert
1073H	MX12 #1 Loopback Activate
1074H	MX12 #1 Loopback Interrupt
1075H-1077H	MX12 #1 Reserved
1078H-107FH	Reserved
1080H-1087H	DS2 FRMR #2 Registers
1088H-108FH	Reserved
1090H-1097H	MX12 #2 Registers
1098H-109FH	Reserved
10A0H-10A7H	DS2 FRMR #3 Registers

Address	Register
10A8H-10AFH	Reserved
10B0H-10B7H	MX12 #3 Registers
10B8H-10BFH	Reserved
10C0H-10C7H	DS2 FRMR #4 Registers
10C8H-10CFH	Reserved
10D0H-10D7H	MX12 #4 Registers
10D8H-10DFH	Reserved
10E0H-10E7H	DS2 FRMR #5 Registers
10E8H-10EFH	Reserved
10F0H-10F7H	MX12 #5 Registers
10F8H-10FFH	Reserved
1100H-1107H	DS2 FRMR #6 Registers
1108H-110FH	Reserved
1110H-1117H	MX12 #6 Registers
1118H-111FH	Reserved
1120H-1127H	DS2 FRMR #7 Registers
1128H-112FH	Reserved

Address	Register
1130H-1137H	MX12 #7 Registers
1138H-16FFH	Reserved
1700H-179FH	**SBI Interface**
1700H	SBI Master Reset / Bus Signal Monitor
1701H	SBI Master Configuration
1702H	SBI Bus Master Configuration
1703H-170FH	SBI Reserved
1710H	EXSBI Control
1711H	EXSBI FIFO Underrun Interrupt Status
1712H	EXSBI FIFO Overrun Interrupt Status
1713H	EXSBI Tributary RAM Indirect Access Address
1714H	EXSBI Tributary RAM Indirect Access Control
1715H	EXSBI Reserved
1716H	EXSBI Tributary Control Indirect Access Data
1717H	EXSBI SBI Parity Error Interrupt Status
1718H-171DH	EXSBI Reserved
171EH	EXSBI Depth Check Interrupt Status
171FH	EXSBI Extract External ReSynch Interrupt Status
1720H	INSBI Control
1721H	INSBI FIFO Underrun Interrupt Status
1722H	INSBI FIFO Overrun Interrupt Status
1723H	INSBI Tributary Register Indirect Access Address
1724H	INSBI Tributary Register Indirect Access Control
1725H	INSBI Reserved
1726H	INSBI Tributary Control Indirect Access Data

Address	Register
1727H-172FH	INSBI Reserved
1731H	INSBI Depth Check Interrupt Status
1732H	INSBI Insert External ReSynch Interrupt Status
1733H-173FH	INSBI Reserved
1740H-175FH	SBI SIPO Reserved
1780H-179FH	SBI PISO Reserved
1780H-1FFFH	Reserved

For all register accesses, CSB must be low.

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the TECT3. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[13]) is low.

Notes on Normal Mode Register Bits:

1) Writing values into unused register bits typically has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bit must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2) All configuration bits that can be written into can also be read back. This allows the processor controlling the TECT3 to determine the programming state of the block.

3) Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4) Writing into read-only normal mode register bit locations does not affect TECT3 operation unless otherwise noted.

The register descriptions are contained in a separate TECT3 register description document.

11 TEST FEATURES DESCRIPTION

The TECT3 contains test features for both production testing and board testing.

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the TECT3. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[13]) is high.

Notes on Register Bits:

1) Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic one or a logic zero; hence unused bits should be masked off by software when read.

2) Writeable register bits are not initialized upon reset unless otherwise noted.

Register 2000H: Master Test Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2	R/W	IOTST	X
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	X

This register is used to select TECT3 test features. All bits, except for PMCTST, are reset to zero by a hardware reset of the TECT3; a software reset of the TECT3 does not affect the state of the bits in this register.

PMCTST:

The PMCTST bit is used to configure the TECT3 for PMC's manufacturing tests. When PMCTST is set to logic 1, the TECT3 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can only be cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin while IOTST is a logic 1. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the TECT3 to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads. When IOTST and PMCTST are both logic 0, the DBCTRL bit is ignored.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the TECT3 for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate

the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

HIZIO:

The HIZIO bit controls the tri-state modes of the output pins of the TECT3. While the HIZIO bit is a logic 1, all output pins of the TECT3, except the data bus, are held in a high-impedance state. The microprocessor interface is still active.

HIZDATA:

The HIZDATA bit controls the tri-state modes of the TECT3. While the HIZIO bit is a logic 1, all output pins of the TECT3, except the data bus, are held in a high-impedance state. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

11.1 JTAG Test Port

The TECT3 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 3: Instruction Register

Length - 3 bits

Instructions	Selected Register	Instruction Code IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 4: Identification Register

Length	32 bits
Version number	3H
Part Number	8315
Manufacturer's identification code	0CDH
Device identification	383150CDH

11.1.1 Boundary Scan Register

The boundary scan register is made up of 286 boundary scan cells, divided into inout observation (IN_CELL), output (OUT_CELL) and bidirectional (IO_CELL) cells. These cells are detailed in the following pages. The first 32 cells form the ID code register and carry the code 383150CDH. The cells are arranged as follows:

Table 5: Boundary Scan Chain

Pin/Enable	Register Bit	Cell Type	Device I.D.
HIZ	0	OUT_CELL	-
ICLK[28]	1	OUT_CELL	-
ICLK[27]	2	OUT_CELL	-
ICLK[20]	3	OUT_CELL	-
ICLK[19]	4	OUT_CELL	-
IFP[19]	5	OUT_CELL	-
ECLK[28]_OEN	6	OUT_CELL	-
ECLK[28]	7	IO_CELL	-
ECLK[27]_OEN	8	OUT_CELL	-
ECLK[27]	9	IO_CELL	-
ECLK[20]_OEN	10	OUT_CELL	-
ECLK[20]	11	IO_CELL	-
ECLK[19]_OEN	12	OUT_CELL	-
ECLK[19]	13	IO_CELL	-
ECLK[12]_OEN	14	OUT_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
ECLK[12]	15	IO_CELL	-
ECLK[11]_OEN	16	OUT_CELL	-
ECLK[11]	17	IO_CELL	-
IFP[12]	18	OUT_CELL	-
IFP[11]	19	OUT_CELL	-
ICLK[12]	20	OUT_CELL	-
ICLK[11]	21	OUT_CELL	-
ID[12]	22	OUT_CELL	-
ID[11]	23	OUT_CELL	-
ID[26]_CASID[7]	24	OUT_CELL	-
ID[25]_MVID[7]	25	OUT_CELL	-
ICLK[26]	26	OUT_CELL	-
ICLK[25]	27	OUT_CELL	-
IFP[26]	28	OUT_CELL	-
IFP[25]	29	OUT_CELL	-
ECLK[26]_OEN	30	OUT_CELL	-
ECLK[26]	31	IO_CELL	-
ECLK[25]_OEN	32	OUT_CELL	-
ECLK[25]	33	IO_CELL	-
ED[26]_CASED[7]	34	IN_CELL	-
ED[25]_MVED[7]	35	IN_CELL	-
ED[18]_CASED[5]	36	IN_CELL	-
CTCLK	37	IN_CELL	-
CECLK_CMV8MCLK	38	IN_CELL	-
CEFP_CMVFPB	39	IN_CELL	-
CICLK_CMVFPC	40	IN_CELL	-
CIFP	41	IN_CELL	-
CCSED	42	IN_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
ED[17]_MVED[5]	43	IN_CELL	-
CLK52M	44	IN_CELL	-
ED[10]_CASED[3]	45	IN_CELL	-
CCSID	46	OUT_CELL	-
ECLK[18]_OEN	47	OUT_CELL	-
ECLK[18]	48	IO_CELL	-
ECLK[17]_OEN	49	OUT_CELL	-
ECLK[17]	50	IO_CELL	-
ECLK[10]_OEN	51	OUT_CELL	-
ECLK[10]	52	IO_CELL	-
ED[9]_MVED[3]	53	IN_CELL	-
ICLK[18]	54	OUT_CELL	-
ICLK[17]	55	OUT_CELL	-
ID[18]_CASID[5]	56	OUT_CELL	-
ID[17]_MVID[5]	57	OUT_CELL	-
IFP[18]	58	OUT_CELL	-
IFP[17]	59	OUT_CELL	-
IFP[10]	60	OUT_CELL	-
IFP[9]	61	OUT_CELL	-
IFP[2]	62	OUT_CELL	-
ID[10]_CASID[3]	63	OUT_CELL	-
ID[9]_MVID[3]	64	OUT_CELL	-
ICLK[10]	65	OUT_CELL	-
ICLK[9]	66	OUT_CELL	-
ECLK[9]_OEN	67	OUT_CELL	-
ECLK[9]	68	IO_CELL	-
ECLK[2]_OEN	69	OUT_CELL	-
ECLK[2]	70	IO_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
ICLK[2]	71	OUT_CELL	-
ED[2]_CASED[1]_TFPI_TMFPI	72	IN_CELL	-
ECLK[1]_TGAPCLK_OEN	73	OUT_CELL	-
ECLK[1]_TGAPCLK	74	IO_CELL	-
ED[1]_MVED[1]_TDATI	75	IN_CELL	-
ID[1]_MVID[1]_RDATO	76	OUT_CELL	-
ID[2]_CASID[1]_ROVRHD	77	OUT_CELL	-
ICLK[1]_RSCLK	78	OUT_CELL	-
IFP[1]_RFPO_RMFPO	79	OUT_CELL	-
TICLK	80	IN_CELL	-
RCLK	81	IN_CELL	-
RPOS_RDAT	82	IN_CELL	-
RNEG_RLCV	83	IN_CELL	-
TCLK	84	OUT_CELL	-
TPOS_TDAT	85	OUT_CELL	-
TNEG_TMFP	86	OUT_CELL	-
UNCONNECTED	87	OUT_CELL	-
UNCONNECTED	88	OUT_CELL	-
UNCONNECTED	89	OUT_CELL	-
UNCONNECTED	90	OUT_CELL	-
UNCONNECTED	91	OUT_CELL	-
UNCONNECTED	92	OUT_CELL	-
UNCONNECTED	93	OUT_CELL	-
UNCONNECTED	94	OUT_CELL	-
UNCONNECTED	95	OUT_CELL	-
UNCONNECTED	96	OUT_CELL	-
UNCONNECTED	97	OUT_CELL	-
UNCONNECTED	98	OUT_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
UNCONNECTED	99	OUT_CELL	-
UNCONNECTED	100	OUT_CELL	-
UNCONNECTED	101	OUT_CELL	-
UNCONNECTED	102	OUT_CELL	-
UNCONNECTED	103	OUT_CELL	-
UNCONNECTED	104	OUT_CELL	-
UNCONNECTED	105	OUT_CELL	-
UNCONNECTED	106	OUT_CELL	-
UNCONNECTED	107	OUT_CELL	-
UNCONNECTED	108	OUT_CELL	-
LOGIC 0	109	IN_CELL	-
LOGIC 0	110	IN_CELL	-
LOGIC 0	111	IN_CELL	-
LOGIC 0	112	IN_CELL	-
LOGIC 0	113	IN_CELL	-
LOGIC 0	114	IN_CELL	-
LOGIC 0	115	IN_CELL	-
LOGIC 0	116	IN_CELL	-
LOGIC 0	117	IN_CELL	-
LOGIC 0	118	IN_CELL	-
LOGIC 0	119	IN_CELL	-
LOGIC 0	120	IN_CELL	-
LOGIC 0	121	IN_CELL	-
LOGIC 0	122	IN_CELL	-
LOGIC 0	123	IN_CELL	-
LOGIC 0	124	IN_CELL	-
LOGIC 0	125	IN_CELL	-
LOGIC 0	126	IN_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
LOGIC 0	127	IN_CELL	-
LOGIC 0	128	IN_CELL	-
LOGIC 0	129	IN_CELL	-
LOGIC 0	130	IN_CELL	-
ICLK[3]	131	OUT_CELL	-
ICLK[4]	132	OUT_CELL	-
ID[3]	133	OUT_CELL	-
ECLK[3]_OEN	134	OUT_CELL	-
ECLK[3]	135	IO_CELL	-
ECLK[4]_OEN	136	OUT_CELL	-
ECLK[4]	137	IO_CELL	-
ECLK[5]_OEN	138	OUT_CELL	-
ECLK[5]	139	IO_CELL	-
IFP[3]	140	OUT_CELL	-
IFP[4]	141	OUT_CELL	-
IFP[5]	142	OUT_CELL	-
IFP[6]	143	OUT_CELL	-
IFP[13]	144	OUT_CELL	-
IFP[14]	145	OUT_CELL	-
ICLK[5]	146	OUT_CELL	-
ICLK[6]	147	OUT_CELL	-
ECLK[6]_OEN	148	OUT_CELL	-
ECLK[6]	149	IO_CELL	-
ECLK[13]_OEN	150	OUT_CELL	-
ECLK[13]	151	IO_CELL	-
ECLK[14]_OEN	152	OUT_CELL	-
ECLK[14]	153	IO_CELL	-
ECLK[21]_OEN	154	OUT_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
ECLK[21]	155	IO_CELL	-
ECLK[22]_OEN	156	OUT_CELL	-
ECLK[22]	157	IO_CELL	-
ECLK[7]_OEN	158	OUT_CELL	-
ECLK[7]	159	IO_CELL	-
ECLK[8]_OEN	160	OUT_CELL	-
ECLK[8]	161	IO_CELL	-
IFP[21]	162	OUT_CELL	-
IFP[22]	163	OUT_CELL	-
ID[4]	164	OUT_CELL	-
ID[5]_MVID[2]	165	OUT_CELL	-
ID[6]_CASID[2]	166	OUT_CELL	-
ID[13]_MVID[4]	167	OUT_CELL	-
ID[14]_CASID[4]	168	OUT_CELL	-
ED[3]	169	IN_CELL	-
ED[4]	170	IN_CELL	-
ED[5]_MVED[2]	171	IN_CELL	-
ED[6]_CASED[2]	172	IN_CELL	-
ED[13]_MVED[4]	173	IN_CELL	-
ED[14]_CASED[4]	174	IN_CELL	-
ID[21]_MVID[6]	175	OUT_CELL	-
ID[22]_CASID[6]	176	OUT_CELL	-
ICLK[13]	177	OUT_CELL	-
ICLK[14]	178	OUT_CELL	-
IFP[7]	179	OUT_CELL	-
IFP[8]	180	OUT_CELL	-
IFP[15]	181	OUT_CELL	-
IFP[16]	182	OUT_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
IFP[23]	183	OUT_CELL	-
IFP[24]	184	OUT_CELL	-
ICLK[21]	185	OUT_CELL	-
ICLK[22]	186	OUT_CELL	-
ICLK[7]	187	OUT_CELL	-
ICLK[8]	188	OUT_CELL	-
ID[7]	189	OUT_CELL	-
ID[8]	190	OUT_CELL	-
ICLK[15]	191	OUT_CELL	-
ICLK[16]	192	OUT_CELL	-
ICLK[23]	193	OUT_CELL	-
ICLK[24]	194	OUT_CELL	-
ED[22]_CASED[6]	195	IN_CELL	-
ED[21]_MVED[6]	196	IN_CELL	-
RECVCLK1	197	OUT_CELL	-
RECVCLK2	198	OUT_CELL	-
XCLK	199	IN_CELL	-
ECLK[15]_OEN	200	OUT_CELL	-
ECLK[15]	201	IO_CELL	-
ECLK[16]_OEN	202	OUT_CELL	-
ECLK[16]	203	IO_CELL	-
ECLK[23]_OEN	204	OUT_CELL	-
ECLK[23]	205	IO_CELL	-
ECLK[24]_OEN	206	OUT_CELL	-
ECLK[24]	207	IO_CELL	-
RSTB	208	IN_CELL	-
A[13]	209	IN_CELL	-
A[12]	210	IN_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
A[11]	211	IN_CELL	-
A[10]	212	IN_CELL	-
A[9]	213	IN_CELL	-
A[8]	214	IN_CELL	-
A[7]	215	IN_CELL	-
A[6]	216	IN_CELL	-
A[5]	217	IN_CELL	-
A[4]	218	IN_CELL	-
A[3]	219	IN_CELL	-
A[2]	220	IN_CELL	-
A[1]	221	IN_CELL	-
A[0]	222	IN_CELL	-
RDB	223	IN_CELL	-
WRB	224	IN_CELL	-
ALE	225	IN_CELL	-
INTB	226	OUT_CELL	-
CSB	227	IN_CELL	-
D[0]_OEN	228	OUT_CELL	-
D[0]	229	IO_CELL	-
D[1]_OEN	230	OUT_CELL	-
D[1]	231	IO_CELL	-
D[2]_OEN	232	OUT_CELL	-
D[2]	233	IO_CELL	-
D[3]_OEN	234	OUT_CELL	-
D[3]	235	IO_CELL	-
D[4]_OEN	236	OUT_CELL	-
D[4]	237	IO_CELL	-
D[5]_OEN	238	OUT_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
D[5]	239	IO_CELL	-
D[6]_OEN	240	OUT_CELL	-
D[6]	241	IO_CELL	-
D[7]_OEN	242	OUT_CELL	-
D[7]	243	IO_CELL	-
ID[15]_SDDATA[0]_OEN	244	OUT_CELL	-
ID[15]_SDDATA[0]	245	OUT_CELL	-
ID[16]_SDDATA[1]_OEN	246	OUT_CELL	-
ID[16]_SDDATA[1]	247	OUT_CELL	-
ID[19]_SDDATA[2]_OEN	248	OUT_CELL	-
ID[19]_SDDATA[2]	249	OUT_CELL	-
ID[20]_SDDATA[3]_OEN	250	OUT_CELL	-
ID[20]_SDDATA[3]	251	OUT_CELL	-
ID[23]_SDDATA[4]_OEN	252	OUT_CELL	-
ID[23]_SDDATA[4]	253	OUT_CELL	-
ID[24]_SDDATA[5]_OEN	254	OUT_CELL	1
ID[24]_SDDATA[5]	255	OUT_CELL	0
ID[27]_SDDATA[6]_OEN	256	OUT_CELL	1
ID[27]_SDDATA[6]	257	OUT_CELL	1
ID[28]_SDDATA[7]_OEN	258	OUT_CELL	0
ID[28]_SDDATA[7]	259	OUT_CELL	0
IFP[20]_SDDP_OEN	260	OUT_CELL	1
IFP[20]_SDDP	261	OUT_CELL	1
IFP[28]_SDV5_OEN	262	OUT_CELL	0
IFP[28]_SDV5	263	OUT_CELL	0
IFP[27]_SDPL_OEN	264	OUT_CELL	0
IFP[27]_SDPL	265	OUT_CELL	0
SAJUST_REQ_OEN	266	OUT_CELL	1

Pin/Enable	Register Bit	Cell Type	Device I.D.
SAJUST_REQ	267	OUT_CELL	0
SBIACT_OEB	268	OUT_CELL	1
SBIACT	269	OUT_CELL	0
SBIDET[0]	270	IN_CELL	1
ED[7]_SBIDET[1]	271	IN_CELL	0
SREFCLK	272	IN_CELL	0
SC1FP_OEN	273	OUT_CELL	0
SC1FP	274	IO_CELL	1
ED[15]_SADATA[0]	275	IN_CELL	1
ED[16]_SADATA[1]	276	IN_CELL	0
ED[19]_SADATA[2]	277	IN_CELL	0
ED[20]_SADATA[3]	278	IN_CELL	0
ED[23]_SADATA[4]	279	IN_CELL	0
ED[24]_SADATA[5]	280	IN_CELL	0
ED[27]_SADATA[6]	281	IN_CELL	1
ED[28]_SADATA[7]	282	IN_CELL	1
ED[8]_SADP	283	IN_CELL	1
ED[12]_SAPL	284	IN_CELL	0
ED[11]_SAV5	285	IN_CELL	0
TDO		TAP Output	-
TDI		TAP Input	-
TCK		TAP Clock	-
TMS		TAP Input	-
TRSTB		TAP Input	-

Notes:

1. Register bit 285 is the first bit of the scan chain (closest to TDI).
2. Enable cell pinname_OEN, tristates pin pinname when set high.

3. Enable cell HIZ, tristates all pins that do not have an individual pinname_OEN enable signal.

12 OPERATION

12.1 DS3 Frame Format

The TECT3 provides support for both the C-bit parity and M23 DS3 framing formats. The DS3 frame format is shown in Figure 27.

Figure 27: DS3 Frame Structure

	84 bits	84 bits	84 bits	84 bits	84 bits	84 bits	84 bits	84 bits
M-subframe 1	X_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 2	X_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 3	P_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 4	P_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 5	M_1	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 6	M_2	F_1	C_1	F_2	C_2	F_3	C_3	F_4
M-subframe 7	M_3	F_1	C_1	F_2	C_2	F_3	C_3	F_4

X_X: X-Bit Channel

- Transmit: The TECT3 inserts the FERF signal on the X-bits. FERF generation is controlled by either the FERF bit of the DS3 TRAN Configuration register or by detection of OOF, RED, LOS and AIS, as configured by the TECT3 Master DS3 Alarm Enable register.
- Receive: The TECT3 monitors the state and detects changes in the state of the FERF signal on the X-bits.

P_X: P-Bit Channel

- Transmit: The TECT3 calculates the parity for the payload data over the previous M-frame and inserts it into the P1 and P2 bit positions.
- Receive: The TECT3 calculates the parity for the received payload. Errors are accumulated in the DS3 PMON Parity Error Event Count registers.

M_X: M-Frame Alignment Signal

- Transmit: The TECT3 generates the M-frame alignment signal (M1 = 0, M2 = 1, M3 = 0).
- Receive: The TECT3 finds M-frame alignment by searching for the F-bits and the M-bits. Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits. M-bit errors are counted in the DS3 PMON Framing Bit Error Event Count

registers. When one or more M-bit errors are detected in 3 out of 4 consecutive M-frames, an out-of-frame defect is asserted (if MBDIS in the DS3 Framer Configuration register is a logic 0).

F_X: M-Subframe Alignment Signal

- Transmit: The TECT3 generates the M-Subframe Alignment signal (F1=1, F2=0, F3=0, F4=1).
- Receive: The TECT3 finds M-frame alignment by searching for the F-bits and the M-bits. Out-of-frame is removed if the M-bits are correct for three consecutive M-frames while no discrepancies have occurred in the F-bits. F-bit errors are counted in the DS3 PMON Framing Bit Error Event Count registers. An out-of frame defect is asserted if 3 F-bit errors out of 8 or 16 consecutive F-bits are observed (as selected by the M3O8 bit in the DS3 FRMR Configuration register).

C_X: C-Bit Channels

- Transmit: When configured for M23 applications, the C-bits are forced to logic 1 with the exception of the C-bit Parity ID bit (the first C-bit of the first M-subframe), which is forced to toggle every M-frame.
  When configured for C-bit parity applications, the C-bit Parity ID bit is forced to logic 1. The second C-bit in M-subframe 1 is set to logic 1. The third C-bit in M-subframe 1 provides a far-end alarm and control (FEAC) signal. The FEAC channel is sourced by the DS3 XBOC block. The 3 C-bits in M-subframe 3 carry path parity information. The value of these 3 C-bits is the same as that of the P-bits. The 3 C-bits in M-subframe 4 are the FEBE bits. FEBE transmission is controlled by the DFEBE bit in the DS3 TRAN Diagnostic register and by the detection of receive framing bit and path parity errors. The 3 C-bits in M-subframe 5 contain the 28.2 kbit/s path maintenance datalink. These bits are inserted from the DS3 TDPR HDLC controller. The C-bits in M-subframes 2, 6, and 7 are unused and are set to logic 1.
- Receive: The CBITV register bit in the DS3 FRMR Status register is used to report the state of the C-bit parity ID bit, and hence whether a M23 or C-bit parity DS3 signal stream is being received. The FEAC channel on the third C-bit in M-subframe 1 is detected by the DS3 RBOC block. Path parity errors and detected FEBEs on the C-bits in M-subframes 3 and 4 are reported in the DS3 PMON Path Parity Error Event Count and FEBE Event Count registers respectively. The path maintenance datalink signal is extracted by theDS3 RDLC HDLC receiver (if enabled).

12.2 Servicing Interrupts

The TECT3 will assert INTB to logic 0 when a condition which is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

1. Read the bits of the TECT3 Master Interrupt Source register (0020H) to identify which of the eight interrupt registers (0021H-0028H) needs to be read to identify the interrupt. For example, a logic one read in the DS3INT register bit indicates that an interrupt identified in the Master Interrupt Source DS3 register produced the interrupt.

2. Read the bits of the second level Master Interrupt Source register to identify the interrupt source.

3. Service the interrupt.

4. If the INTB pin is still logic 0, then there are still interrupts to be serviced. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB

12.3 Using the Performance Monitoring Features

The PMON blocks are provided for performance monitoring purposes. The DS3 PMON block is used to monitor DS3 performance primitives. The PMON blocks within each T1/E1 Framer slice are used to monitor T1 or E1 performance primitives. The counters in the DS3 PMON block has been sized as not to saturate if polled every second. The T1/E1 PMON event counters are of sufficient length so that the probability of counter saturation over a one second interval is very small (less than 0.001%).

An accumulation interval is initiated by writing to one of the PMON event counter register addresses or by writing to the Master Revision/Global PMON Update register. After initiating an accumulation interval, 3.5 recovered clock periods (RCLK for the DS3 PMON) must be allowed to elapse to permit the PMON counter values to be properly transferred before the PMON registers may be read.

The odds of any one of the T1/E1 counters saturating during a one second sampling interval go up as the bit error rate (BER) increases. At some point, the probability of counter saturation reaches 50%. This point varies, depending upon the framing format and the type of event being counted. The BER at which the probability of counter saturation reaches 50% is shown for various counters in Table 6 for E1 mode, and in Table 7 for T1 mode.

Table 6: PMON Counter Saturation Limits (E1 mode)

Counter	BER
FER	4.0×10^{-3}
CRCE	cannot saturate
FEBE	cannot saturate

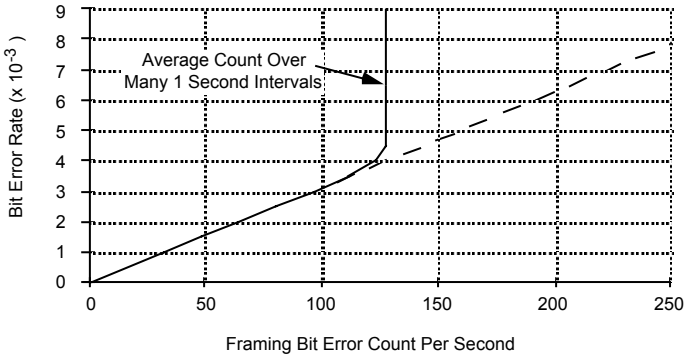
Table 7: PMON Counter Saturation Limits (T1 mode)

Counter	Format	BER
FER	SF	1.6×10^{-3}
	ESF	6.4×10^{-2}
CRCE	SF	1.28×10^{-1}
	ESF	cannot saturate

Below these 50% points, the relationship between the BER and the counter event count (averaged over many one second samples) is essentially linear. Above the 50% point, the relationship between BER and the average counter event count is highly non-linear due to the likelihood of counter saturation. The following figures show this relationship for various counters and framing formats. These graphs can be used to determine the BER, given the average event count. In general, if the BER is above 10^{-3}, the average counter event count cannot be used to determine the BER without considering the statistical effect of occasional counter saturation.

Figure 28 illustrates the expected count values for a range of Bit Error Ratios in E1 mode.

Figure 28: FER Count vs. BER (E1 mode)



Since the maximum number of CRC sub-multiframes that can occur in one second is 1000, the 10-bit FEBE and CRCE counters cannot saturate in one second. Despite this, there is not a linear relationship between BER and CRC-4 block errors due to the nature of the CRC-4 calculation. At BERs below 10^{-4}, there tends to be no more than one bit error per sub-multiframe, so the number of CRC-4 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above 10^{-4}, each CRC-4 error is often due to more than one bit error. Thus, the relationship between BER and CRCE count becomes non-linear above a 10^{-4} BER. This must be taken into account when using CRC-4 counts to determine the BER. Since FEBEs are indications of CRCEs at the far end, and are accumulated identically to CRCEs, the same explanation holds for the FEBE event counter.

The bit error rate for E1 can be calculated from the one-second PMON CRCE count by the following equation:

Bit Error Rate = 1 - 10$^{\left(\frac{\log\left(1-\frac{8}{8000}CRCE\right)}{8*256}\right)}$

Figure 29: CRCE Count vs. BER (E1 mode)

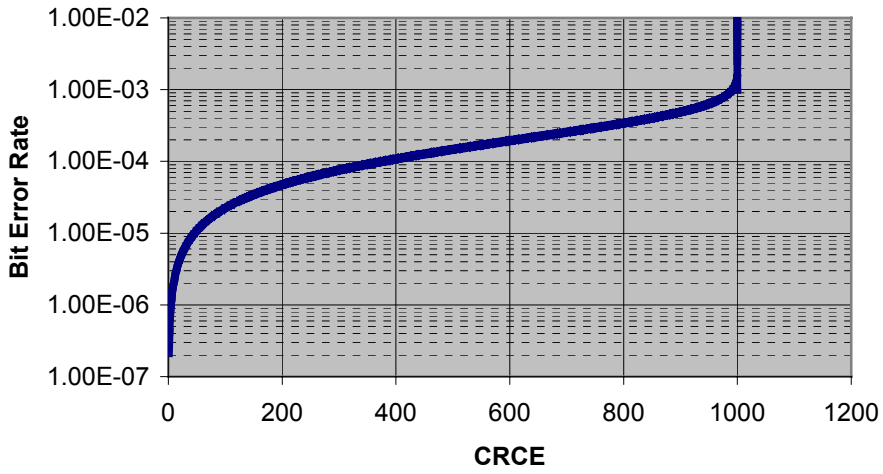
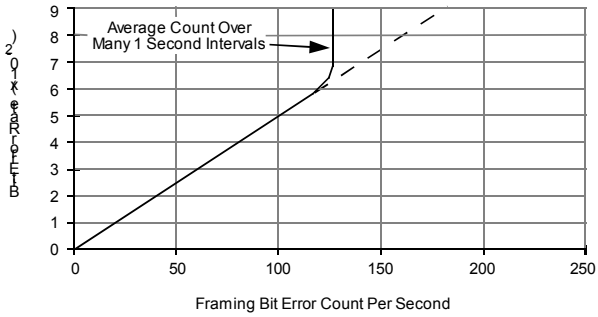


Figure 30 illustrates the expected count values for a range of Bit Error Ratios in T1 mode.

Figure 30: FER Count vs. BER (T1 ESF mode)

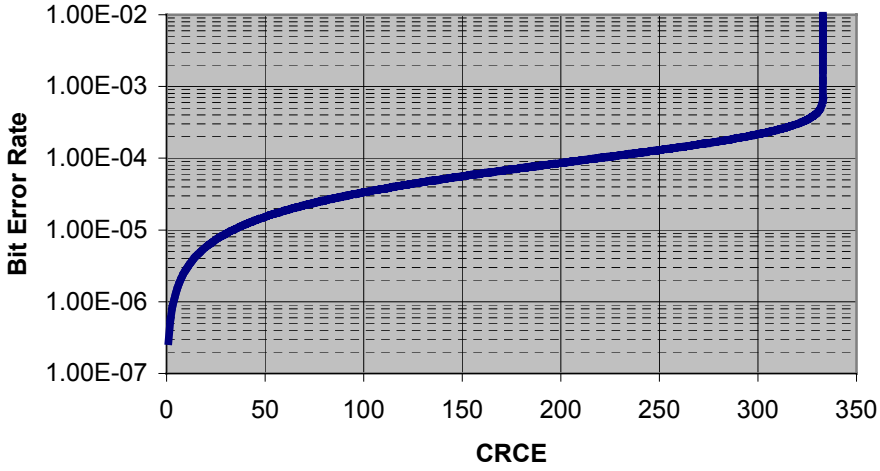


Since the maximum number of ESF superframes that can occur in one second is 333, the 9-bit BEE counter cannot saturate in one second in ESF framing format. Despite this, there is not a linear relationship between BER and BEE count, due to the nature of the CRC-6 calculation. At BERs below 10^{-4}, there tends to be no more than one bit error per superframe, so the number of CRC-6 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above 10^{-4}, each CRC-6 error is often due to more than one bit error. Thus, the relationship between BER and BEE count becomes non-linear above a 10^{-4} BER. This must be taken into account when using ESF CRC-6 counts to determine the BER.

The bit error rate for T1 ESF can be calculated from the one-second PMON CRCE count by the following equation:

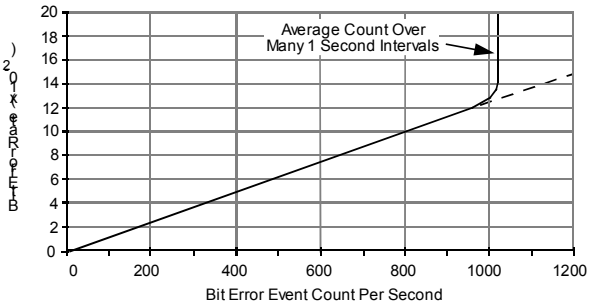
Bit Error Rate = 1 - 10 $^{\left(\frac{\log\left(1-\frac{24}{8000}BEE\right)}{24*193}\right)}$

Figure 31: CRCE Count vs. BER (T1 ESF mode)



For T1 SF format, the CRCE and FER counts are identical, but the FER counter is smaller and should be ignored.

Figure 32: CRCE Count vs. BER (T1 SF mode)



12.4 Using the Internal FDL Transmitter

It is important to note that access rate to the TDPR registers is limited by the rate of the internal high-speed system clock which is either the DS3, DS1 or E1 clock. Consecutive accesses to the TDPR Configuration, TDPR Interrupt Status/UDR

Clear, and TDPR Transmit Data register should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than 1/8 that of the selected TDPR high-speed system clock. This time is used by the high-speed system clock to sample the event, write the FIFO, and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the line clock) must be considered when determining the procedure used to read and write the TDPR registers.

Upon reset of the TECT3, the TDPR should be disabled by setting the EN bit in the TDPR Configuration Register to logic 0 (default value). An HDLC all-ones Idle signal will be sent while in this state. The TDPR is enabled by setting the EN bit to logic 1. The FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO. The TDPR is now ready to transmit.

To initialize the TDPR, the TDPR Configuration Register must be properly set. If FCS generation is desired, the CRC bit should be set to logic 1. If the block is to be used in interrupt driven mode, then interrupts should be enabled by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable register to logic 1. The TDPR operating parameters in the TDPR Upper Transmit Threshold and TDPR Lower Interrupt Threshold registers should be set to the desired values. The TDPR Upper Transmit Threshold sets the value at which the TDPR automatically begins the transmission of HDLC packets, even if no complete packets are in the FIFO. Transmission will continue until the current packet is transmitted and the number of bytes in the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC packets (packets with EOM attached) in its FIFO. Finally, the TDPR can be enabled by setting the EN bit to logic 1. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The TDPR can be used in a polled or interrupt driven mode for the transfer of data. In the polled mode the processor controlling the TDPR must periodically read the TDPR Interrupt Status register to determine when to write to the TDPR Transmit Data register. In the interrupt driven mode, the processor controlling the TDPR uses the INTB output, the one of the TECT3 Master Interrupt Source registers, and the TECT3 TDPR Interrupt Status registers to identify TDPR interrupts which determine when writes can or must be done to the TDPR Transmit Data register.

Interrupt Driven Mode:

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The

TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 1 so an interrupt on INTB is generated upon detection of a FIFO full state, a FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun. The following procedure should be followed to transmit HDLC packets:

1. Wait for a complete packet to be transmitted. Once data is available to be transmitted, then go to step 2.

2. Write the data byte to the TDPR Transmit Data register.

3. If all bytes of the packet have been written to the Transmit Data register, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

4. If there are more bytes in the packet to be sent, then go to step 2.

While performing steps 1 to 4, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine detailed in the following text should be followed immediately.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold register. Unless an error condition occurs, transmission will not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold limit. The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

TDPR Interrupt Routine:

Upon assertion of INTB, the source of the interrupt must first be identified by reading the TECT3 Master Interrupt Source register (0020H) followed by reading one of the second level master interrupt source registers T1E1INT1, T1E1INT2, T1E1INT3, T1E1INT4 or DS3INT. Once the source of the interrupt has been identified as the TDPR in use, then the following procedure should be carried out:

1. Read the TDPR Interrupt Status register.

2. If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted. When the UDRI bit transitions to logic 1, one Abort sequence and continuous flags will be transmitted. The TDPR FIFO is held in reset state. To re-enable the TDPR FIFO and to clear the underrun, the TDPR Interrupt Status/UDR Clear register should be written with any value.

3. If OVRI=1, then the FIFO has overflowed. The packet of which the last byte written into the FIFO belongs to, has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), OVRI is set, an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted. The FIFO is held in reset until a write to the TDPR Transmit Data register occurs. This write contains the first byte of the next packet to be transmitted.

4. If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written. When in this state, either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

5. If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. If there is more data to transmit, then it should be written to the TDPR Transmit Data register before an underrun occurs. If there is no more data to transmit, then an EOM should be set at the end of the last packet byte. Flags will then be transmitted once the last packet has been transmitted.

   If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

Polling Mode:

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 0 since packet transmission is set to work with a periodic polling procedure. The following procedure should be followed to transmit HDLC packets:

1. Wait until data is available to be transmitted, then go to step 2.

2. Read the TDPR Interrupt Status register.

3. If FULL=1, then the TDPR FIFO is full and no further bytes can be written. Continue polling the TDPR Interrupt Status register until either FULL=0 or BLFILL=1. Then, go to either step 4 or 5 depending on implementation preference.

4. If BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. Write the data into the TDPR Transmit Data register. Go to step 6.

5. If FULL=0, then the TDPR FIFO has room for at least 1 more byte to be written. Write the data into the TDPR Transmit Data register. Go to step 6.

6. If more data bytes are to be transmitted in the packet, then go to step 2.

If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

12.5 Using the Internal Data Link Receiver

It is important to note that the access rate to the RDLC registers is limited by the rate of the internal high-speed system clock which is either the DS3, DS1 or E1 system clock. Consecutive accesses to the RDLC Status and RDLC Data registers should be accessed at a rate no faster than 1/10 that of the selected RDLC high-speed system clock. This time is used by the high-speed system clock to sample the event and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read RDLC registers.

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register to logic 0 (default state). The RDLC Interrupt Control register should then be initialized to enable the INTB output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the RDLC Status register must be continuously polled to check the interrupt status (INTR) bit.

After the RDLC Interrupt Control register has been written, the RDLC can be enabled at any time by setting the EN bit in the RDLC Configuration register to logic 1. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer. This is done to provide alignment of link up status with the data read from the

FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO. This is done to provide alignment of link down status with the data read from the FIFO. It is up to the controlling processor to check the COLS bit in the RDLC Status register for a change in the link status. If the COLS bit is set to logic 1, the FIFO must be emptied to determine the current link status. The first flag and abort status encoded in the PBS bits is used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status register is being read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status register is read, the PKIN bit is cleared to logic 0 . If the RDLC Status register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled or interrupt driven mode for the transfer of frame data. In the polled mode, the processor controlling the RDLC must periodically read the RDLC Status register to determine when to read the RDLC Data register. In the interrupt driven mode, the processor controlling the RDLC uses the TECT3 INTB output and the TECT3 Master Interrupt Source registers to determine when to read the RDLC Data register.

In the case of interrupt driven data transfer from the RDLC to the processor, the INTB output of the TECT3 is connected to the interrupt input of the processor. The processor interrupt service routine verifies what block generated the interrupt by reading the TECT3 Master Interrupt Source register followed by one of the second level master interrupt source registers to identify one of the 29 HDLC receivers as the interrupt source. Once it has identified that the RDLC has generated the interrupt, it processes the data in the following order:

1. Read the RDLC Status register. The INTR bit should be logic 1.

2. If OVR = 1, then discard the last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

3. If COLS = 1, then set the EMPTY FIFO software flag.

4. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO

software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

5. Read the RDLC Data register.

6. Read the RDLC Status register.

7. If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.

8. If COLS = 1, then set the EMPTY FIFO software flag.

9. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.

10. Start the processing of FIFO data. Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

    If PBS[2:0] = 001, discard data byte read in step 5 and set the LINK ACTIVE software flag.

    If PBS[2:0] = 010, discard the data byte read in step 5 and clear the LINK ACTIVE software flag.

    If PBS[2:0] = 1XX, store the last byte of the packet, decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.

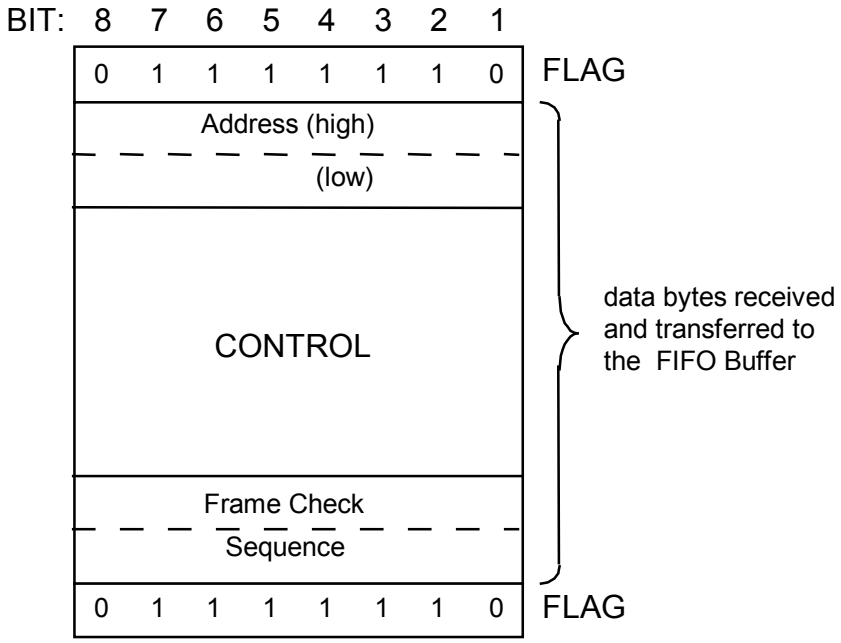
    If PBS[2:0] = 000, store the packet data.

11. If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, go to step 5 else clear the EMPTY FIFO software flag and leave this interrupt service routine to wait for the next interrupt.

The link state is typically a local software variable. The link state is inactive if the RDLC is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RDLC is receiving flags or data.

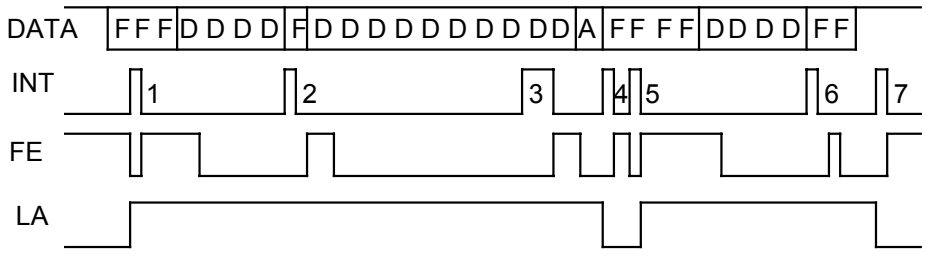
If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

Figure 33: Typical Data Frame



Bit 1 is the first serial bit to be received. When enabled, the primary, secondary and universal addresses are compared with the high order packet address to determine a match.

Figure 34: Example Multi-Packet Operational Sequence



F - flag sequence (01111110)
A - abort sequence (01111111)
D - packet data bytes
INT - active high interrupt output
FE - internal FIFO empty status
LA - state of the LINK ACTIVE software flag

Figure 34 shows the timing of interrupts, the state of the FIFO, and the state of the Data Link relative the input data sequence. The cause of each interrupt and

the processing required at each point is described in the following paragraphs. The actual interrupt signal, INTB, is active low and will be the inverse of the INT signal shown in Figure 16. Also in this example, the programmable fill level set point is set at 8 bytes by writing this value into the INTC[6:0] bits of the RDLC Interrupt Control register.

At points 1 and 5 the first flag after all ones or abort is detected. A dummy byte is written in the FIFO, FE goes low, and an interrupt goes active. When the interrupt is detected by the processor it reads the dummy byte, the FIFO becomes empty, and the interrupt is removed. The LINK ACTIVE (LA) software flag is set to logic 1.

At points 2 and 6 the last byte of a packet is detected and interrupt goes high. When the interrupt is detected by the processor, it reads the data and status registers until the FIFO becomes empty. The interrupt is removed as soon as the RDLC Status register is read, since the FIFO fill level of 8 bytes has not been exceeded. It is possible to store many packets in the FIFO and empty the FIFO when the FIFO fill level is exceeded. In either case the processor should use this interrupt to count the number of packets written into the FIFO. The packet count or a software time-out can be used as a signal to empty the FIFO.

At point 3 the FIFO fill level of 8 bytes is exceeded and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.

At points 4 or 7 an abort character is detected, a dummy byte is written into the FIFO, and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed. The LINK ACTIVE software flag is cleared.

12.6 T1 Automatic Performance Report Format

Table 8: Performance Report Message Structure and contents

Octet No.	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
1	FLAG							
2	SAPI						C/R	EA
3	TEI							EA
4	CONTROL							
5	G3	LV	G4	U1	U2	G5	SL	G6
6	FE	SE	LB	G1	R	G2	Nm	NI
7	G3	LV	G4	U1	U2	G5	SL	G6
8	FE	SE	LB	G1	R	G2	Nm	NI

9	G3	LV	G4	U1	U2	G5	SL	G6
10	FE	SE	LB	G1	R	G2	Nm	NI
11	G3	LV	G4	U1	U2	G5	SL	G6
12	FE	SE	LB	G1	R	G2	Nm	NI
13	FCS							
14	FCS							
15	FLAG							

Notes:

1. The order of transmission of the bits is LSB (Bit 1) to MSB (Bit 8).

Table 9: Performance Report Message Structure Notes

Octet No.	Octet Contents	Interpretation
1	01111110	Opening LAPD Flag
2	00111000 00111010	From CI: SAPI=14, C/R=0, EA=0 From carrier: SAPI=14,C/R=1,EA=0
3	00000001	TEI=0,EA=1
4	00000011	Unacknowledged Frame
5,6	Variable	Data for latest second (T')
7,8	Variable	Data for Previous Second(T'-1)
9,10	Variable	Data for earlier Second(T'-2)
11,12	Variable	Data for earlier Second(T'-3)
13,14	Variable	CRC16 Frame Check Sequence
15	01111110	Closing LAPD flag

Table 10: Performance Report Message Contents

Bit Value	Interpretation
G1=1	CRC ERROR EVENT =1
G2=1	1<CRC ERROR EVENT ≤5
G3=1	5<CRC ERROR EVENT ≤10

G4=1	10<CRC ERROR EVENT ≤100
G5=1	100<CRC ERROR EVENT ≤319
G6=1	CRC ERROR EVENT ≤ 320
SE=1	Severely Errored Framing Event ≥ 1(FE shall =0)
FE=1	Frame Synchronization Bit Error Event ≥1 (SE shall=0)
LV=1	Line code violation event ≥ 1
SL=1	Slip Event ≥ 1
LB=1	Payload Loopback Activated
U1,U2=0	Under Study For Synchronization.
R=0	Reserved (Default Value =0)
NmNI=00,01,10,11	One second Report Modulo 4 Counter

12.7 Using the Per-Channel Serial Controllers

12.7.1 Initialization

Before the TPSC (RPSC) block can be used, a proper initialization of the internal registers must be performed to eliminate erroneous control data from being produced on the block outputs. The output control streams should be disabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 0. Then, all 96 locations of the TPSC (RPSC) must be filled with valid data. Finally, the output streams can be enabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 1.

12.7.2 Direct Access Mode

Direct access mode to the TPSC or RPSC is not used in the TECT3. However, direct access mode is selected by default whenever the TECT3 is reset. The IND bit within the TPSC and RPSC Configuration Registers must be set to logic 1 after a reset is applied.

12.7.3 Indirect Access Mode

Indirect access mode is selected by setting the IND bit in the TPSC or RPSC Configuration Register to logic 1. When using the indirect access mode, the status of the BUSY indication bit should be polled to determine the status of the

microprocessor access: when the BUSY bit is logic 1, the TPSC or RPSC is processing an access request; when the BUSY bit is logic 0, the TPSC or RPSC has completed the request.

The indirect write programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.

2. Write the channel data to the TPSC (RPSC) Channel Indirect Data Buffer register.

3. Write RWB=0 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

4. Poll the BUSY bit until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 3 and remain at logic 1 until the request is complete.

5. If there is more data to be written, go back to step 1.

The indirect read programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.

2. Write RWB=1 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

3. Poll the BUSY bit, waiting until it goes to a logic 0. The BUSY bit will go to logic 1 immediately after step 2 and remain at logic 1 until the request is complete.

4. Read the requested channel data from the TPSC (RPSC) Channel Indirect Data Buffer register.

5. If there is more data to be read, go back to step 1.

12.8 T1/E1 Framer Loopback Modes

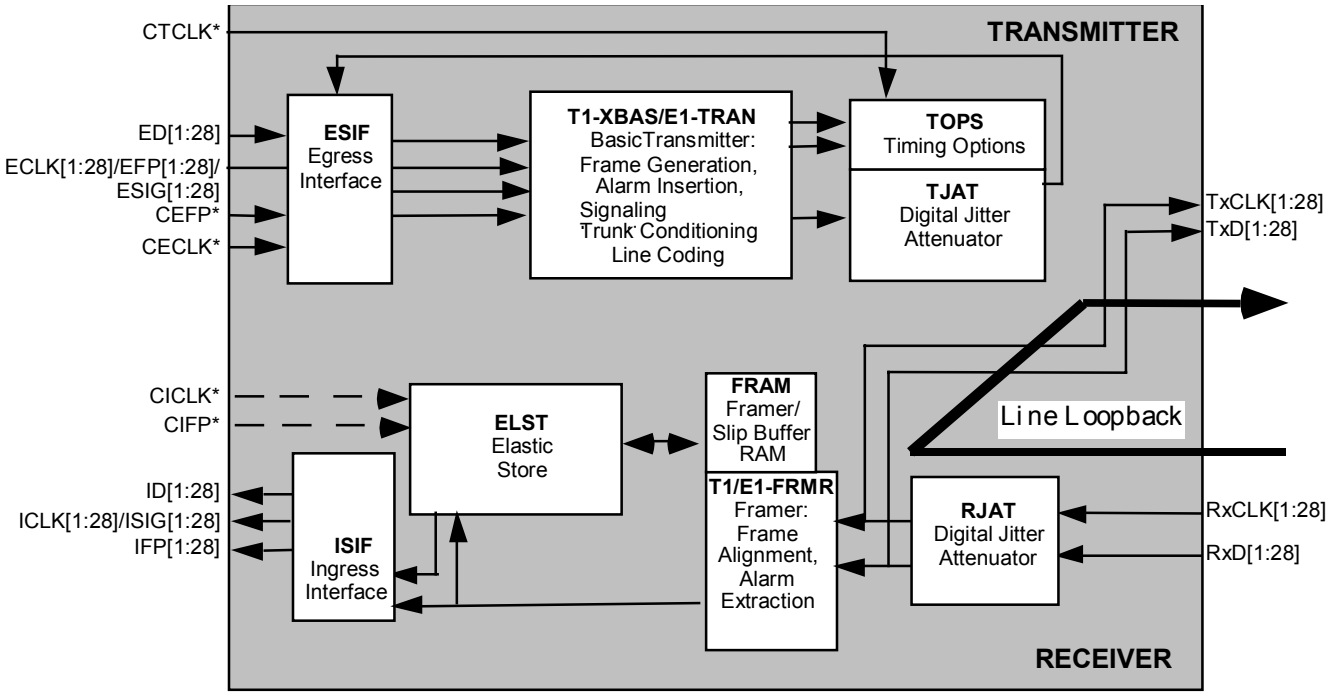
The TECT3 provides three loopback modes for T1/E1 links to aid in network and system diagnostics. The internal T1/E1 line loopback can be initiated at any time via the µP interface, but is usually initiated once an inband loopback activate code is detected. The system Diagnostic Digital loopback can be initiated at any time by the system via the µP interface to check the path of system data through

the framer. The payload can also be looped-back on a per-DS0 basis to allow network testing without taking an entire DS1 off-line.

T1/E1 Line Loopback

T1/E1 Line loopback is initiated by setting the LLOOP bit to a 1 in the T1/E1 Diagnostics register (000DH + N*80H, N=1 to 28). When in line loopback mode the appropriate T1/E1 framer in the TECT3 is configured to internally connect the jitter-attenuated clock and data from the RJAT to the transmit clock and data (shown as TxD[x] and TxCLK[x] in the lineloopback diagram) going to the M13 mux. The RJAT may be bypassed if desired. Conceptually, the data flow through a single T1/E1 framer in this loopback condition is illustrated in Figure 35.

Figure 35: T1/E1 Line Loopback

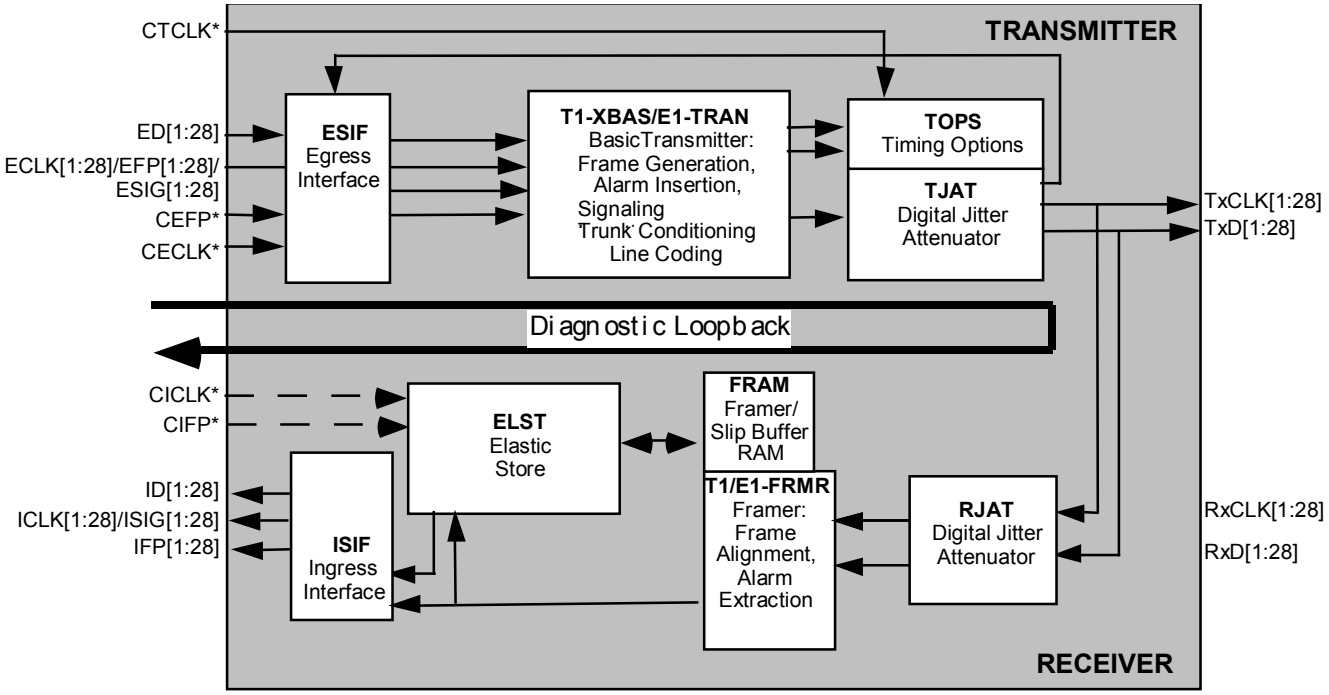


T1/E1 Diagnostic Digital Loopback

When Diagnostic Digital loopback is initiated, by writing a 1 to the DLOOP bit in the T1/E1 Diagnostics register (000DH + N*80H, N=1 to 28), the appropriate T1/E1 framer in the TECT3 is configured to internally connect its transmit clock and data (shown as TxD[x] and TxCLK[x] in the diagnostic loopback figure) to the

receive clock and data (shown as RxD[x] and RxCLK[x] in the diagnostic loopback figure) The data flow through a single T1/E1 framer in this loopback condition is illustrated in Figure 36.

Figure 36: T1/E1 Diagnostic Digital Loopback

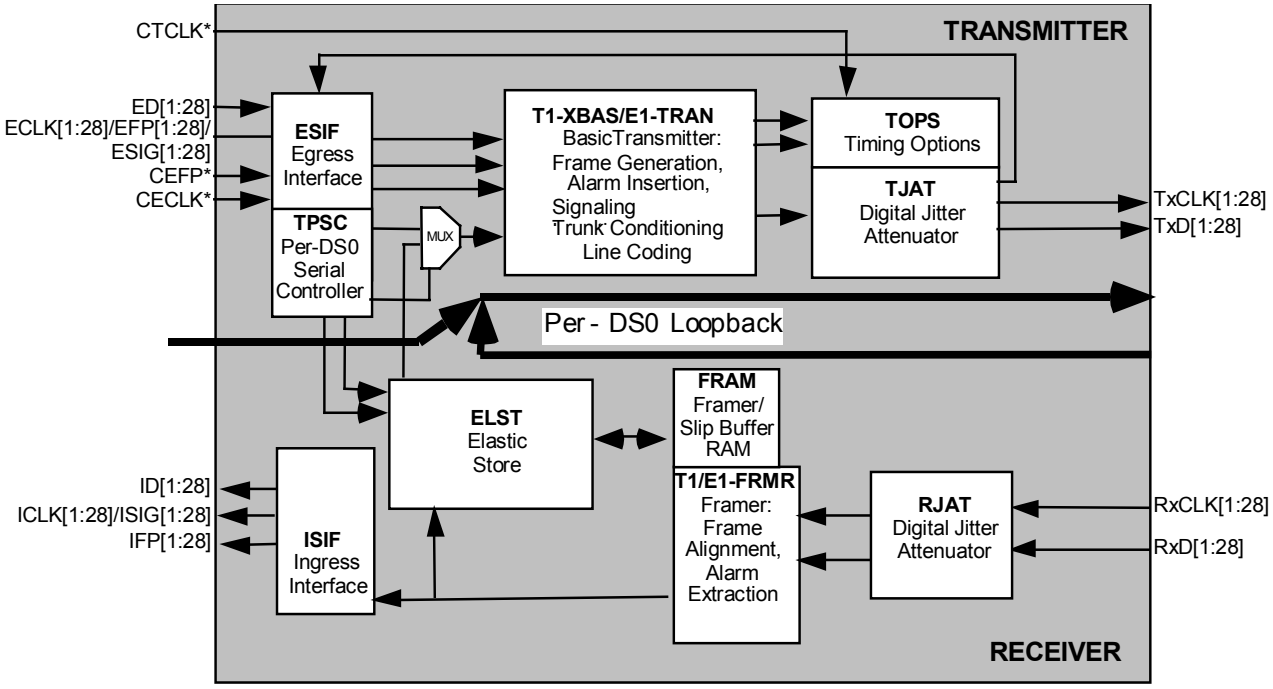


Per-Channel Loopback

The T1/E1 payload may be looped-back on a per-channel basis through the use of the TPSC. If all channels are looped-back, the result is very similar to Payload Loopback on other PMC framers. In order for per-channel loopback to operate correctly, the Ingress Interface must be in Clock Master mode. The LOOP bit must be set to logic 1 in the TPSC Internal Registers for each channel desired to be looped back, and the PCCE bit must be set to logic 1 in the TPSC Configuration register. When all these configurations have been made, the ingress DS0s or timeslots selected will overwrite their corresponding egress channels; the remaining egress channels will pass through intact. Note that because the egress and ingress streams will not be superframe aligned, that any robbed-bit signaling in the ingress stream may not fall in the correct frame once looped-back, and that egress robbed-bit signaling will overwrite the looped-back channel data if signaling insertion is enabled. PRBS generation and detection is

not available in payload loopback mode. The data flow in per-channel loopback is illustrated in Figure 37.

Figure 37: Per-Channel Loopback



12.9 DS3 Loopback Modes

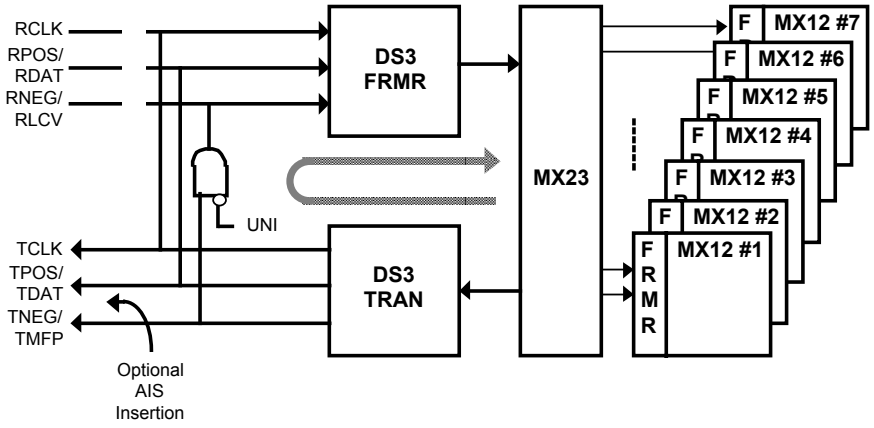
The TECT3 provides three DS3 M13 multiplexer loopback modes to aid in network and system diagnostics at the DS3 interface. The DS3 loopbacks can be initiated via the µP interface whenever the DS3 framer/M13 multiplexer is enabled. The DS3 Master Data Source register controls the DS3 loopback modes.

DS3 Diagnostic Loopback

DS3 Diagnostic Loopback allows the transmitted DS3 stream to be looped back into the receive DS3 path, overriding the DS3 stream received on the RDAT/RPOS and RNEG/RLCV inputs. The RCLK signal is also substituted with the transmit DS3 clock, TCLK. While this mode is active, AIS may be substituted for the DS3 payload being transmitted on the TPOS/TDAT and TNEG/TMFP outputs. The configuration of the receive interface determines how the TNEG/TMFP signal is handled during loopback: if the UNI bit in the DS3 FRMR register is set, then the receive interface is configured for RDAT and RLCV,

therefore the TNEG/TMFP signal is suppressed during loopback so that transmit MFP indications will not be seen nor accumulated as input LCVs. If the UNI bit is clear, then the interface is configured for bipolar signals RPOS and RNEG, therefore the TNEG is fed directly to the RNEG input. This diagnostic loopback can be used when configured as a multiplexer or as a framer only. The DS3 loopback mode is shown diagrammatically in Figure 38.

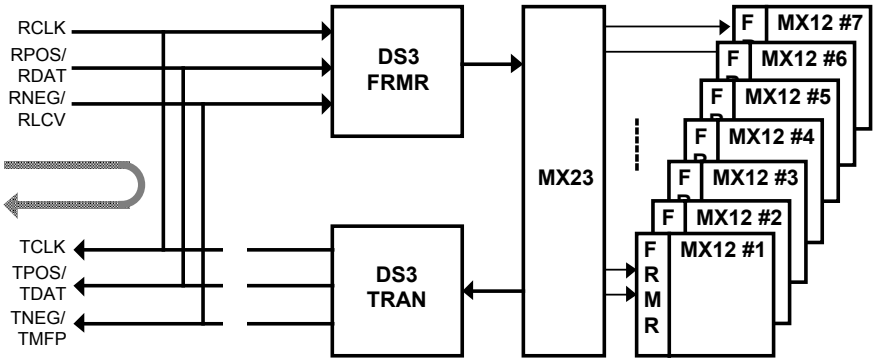
Figure 38: DS3 Diagnostic Loopback Diagram



DS3 Line Loopback

DS3 Line Loopbacks allow the received DS3 streams to be looped back into the transmit DS3 paths, overriding the DS3 streams created internally by the multiplexing of the lower speed tributaries. The transmit signals on TPOS/TDAT and TNEG/TMFP are substituted with the receive signals on RPOS/RDAT and RNEG/RLCV. The TCLK signal is also substituted with the receive DS3 clock, RCLK. While this mode is active, AIS may be substituted for the DS3 payload being transmitted on the TPOS/TDAT and TNEG/TMFP outputs. Note that the transmit interface must be configured to be the same as the DS3 FRMR receive interface for this mode to work properly. The DS3 line loopback mode is shown diagrammatically in Figure 39. There is a second form of line loopback which only loops back the DS3 payload. In this mode the DS3 framing overhead is regenerated for the received DS3 stream and then retransmitted. Line loopback is selected with the LLOOP bit in the DS3 Master Data source register and payload loopback is selected by the PLOOP bit in the same register.

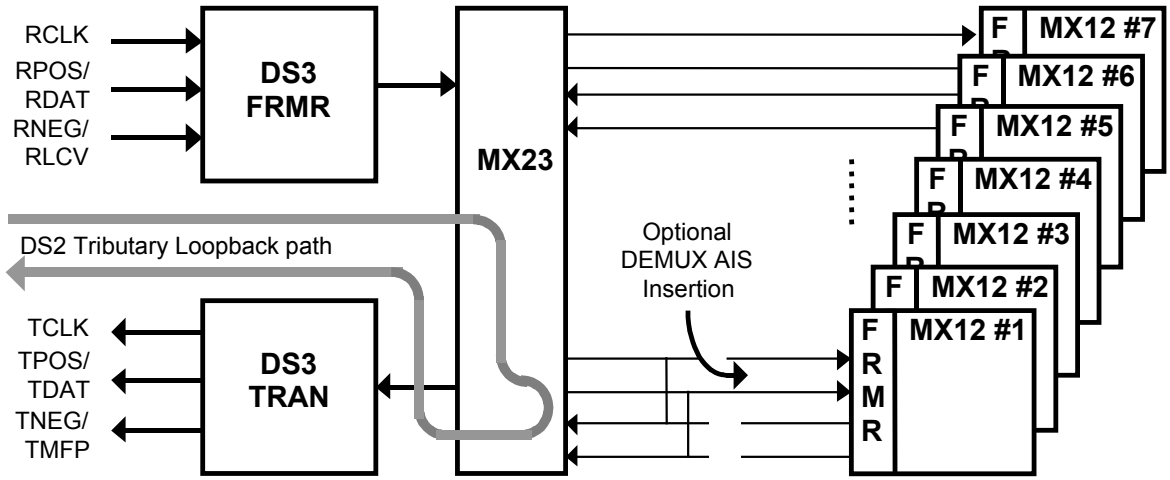
Figure 39: DS3 Line Loopback Diagram



DS2 Demultiplex Loopback

DS2 Demultiplex Loopbacks allow each of the seven demultiplexed DS2 streams to be looped back into the MX23 and multiplexed up into the transmit DS3 stream. This overrides the tributary DS2 streams coming from the MX12s. The DS2 loopback mode is shown diagrammatically in Figure 40 and is enabled via the MX23 Loopback Activate register.

Figure 40: DS2 Loopback Diagram



.

12.10 SBI Bus Data Formats

The TECT3 uses the Scaleable Bandwidth Interconnect (SBI) bus as a high density link interconnect with devices processing T1s and DS3s. The SBI bus is a multi-point to multi-point bus capable of interconnecting up to three TECT3 devices in parallel with other link layer or tributary processing devices.

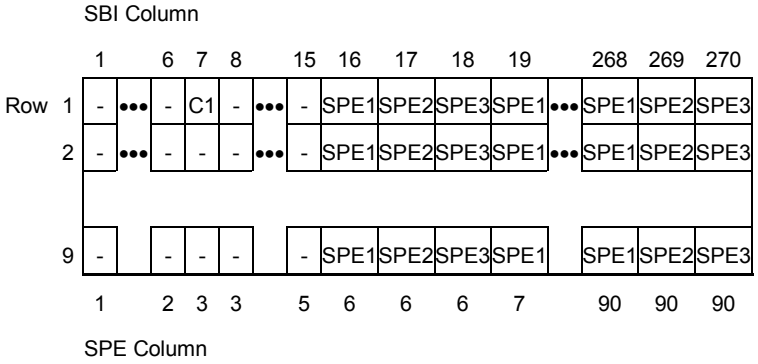
Multiplexing Structure

The SBI structure uses a locked SONET/SDH structure fixing the position of the TU-3 relative to the STS-3/STM-1. The SBI is also of fixed frequency and alignment as determined by the reference clock (SREFCLK) and frame indicator signal (SC1FP). Frequency deviations are compensated by adjusting the location of the T1/DS3 channels using floating tributaries as determined by the V5 indicator and payload signals (SDV5, SAV5, SDPL and SAPL).

Table 11 shows the bus structure for carrying T1 and DS3 tributaries in a SDH STM-1 like format. Up to 84 T1s or 3 DS3s are carried within the octets labeled SPE1, SPE2 and SPE3 in columns 16-270. All other octets are unused and are of fixed position. The frame signal (SC1FP) occurs during the octet labeled C1 in Row 1 column 7.

The multiplexed links are separated into three Synchronous Payload Envelopes called SPE1, SPE2 and SPE3. Each envelope carries up to 28 T1s or a DS3. SPE1 carries the T1s numbered 1,1 through 1,28 or DS3 number 1,1. SPE2 carries T1s numbered 2,1 through 2,28 or DS3 number 2,1. SPE3 carries T1s numbered 3,1 through 3,28 or DS3 number 3,1. The most significant bit in all formats is the first bit of transmission.

Table 11: Structure for Carrying Multiplexed Links



The TECT3, when enabled for SBI interconnection, will add and drop either 28 T1s or a DS3 into one of the three Synchronous Payload Envelopes, SPE1, SPE2 or SPE3.

Tributary Numbering

Tributary numbering for T1 uses the SPE number, followed by the Tributary number within that SPE and are numbered sequentially. Table 12 shows the T1 column numbering and relates the tributary number to the SPE column numbers and overall SBI column structure. Numbering for DS3 follows the same naming convention even though there is only one DS3 per SPE. SBI columns 16-18 are unused for T1 tributaries.

Table 12: T1 Tributary Column Numbering

T1#	SPE1 Column	SPE2 Column	SPE3 Column	SBI Column
1,1	7,35,63			19,103,187
2,1		7,35,63		20,104,188
3,1			7,35,63	21,105,189
1,2	8,36,64			22,106,190
2,2		8,36,64		23,107,191
•••				
1,28	34,62,90			100,184,268
2,28		34,62,90		101,185,269
3,28			34,62,90	102,186,270

SBI Timing Master Modes

The TECT3 supports both synchronous and asynchronous SBI timing modes. Synchronous modes apply only to T1 tributaries and are used with ingress elastic stores to rate adapt the receive tributaries to the fixed SBI data rate. Asynchronous modes allow T1 and DS3 to float within the SBI structure to accommodate differences in timing. Note that Synchronous mode SBI timing operation is required for support of Channel Associated Signaling (CAS).

In synchronous SBI mode the T1 DS0s are in a fixed format and do not move relative to the SBI structure. The SBI frame pulse, SC1FP, in synchronous mode can be enabled to indicate CAS signaling multi-frame alignment by pulsing once every 12th 2KHz SC1FP frame pulse period. SREFCLK sets the ingress rate from the receive elastic store.

In Asynchronous modes timing is communicated across the Scaleable Bandwidth Interconnect by floating data structures within the SBI. Payload indicator signals in the SBI control the position of the floating data structure and therefore the timing. When sources are running faster than the SBI the floating payload structure is advanced by an octet be passing an extra octet in the V3 octet locations (H3 octet for DS3 mappings). When the source is slower than the SBI bus, the floating payload is retarded by leaving the octet after the V3 or H3 octet unused. Both these rate adjustments are indicated by the SBI control signals.

On the DROP BUS the TECT3 is timing master as determined by the arrival rate of data over the SBI.

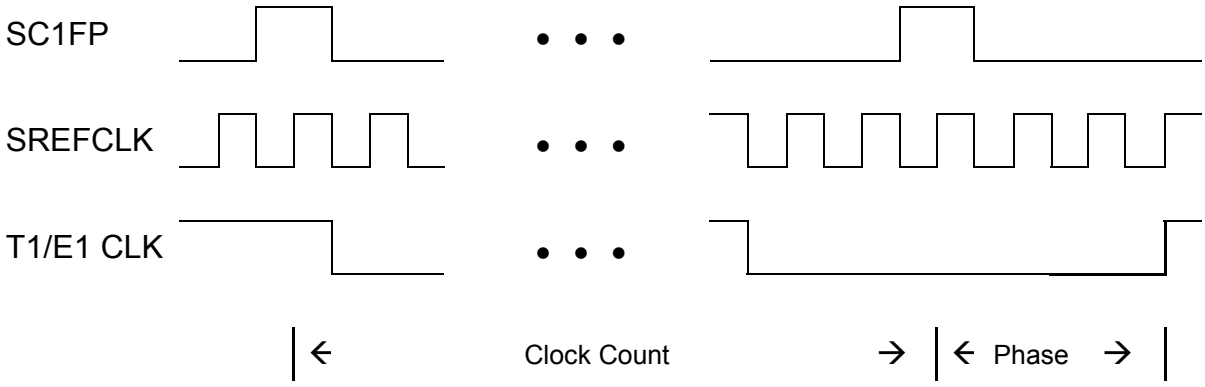
On the ADD BUS the TECT3 can be either the timing master or the timing slave. When the TECT3 is the timing slave it receives its transmit timing information from the arrival rate of data across the SBI ADD bus. When the TECT3 is the timing master it signals devices on the SBI ADD bus to speed up or slow down with the justification request signal, SAJUST_REQ. The TECT3 as timing master indicates a speedup request to a Link Layer SBI device by asserting the justification request signal high during the V3 or H3 octet. When this is detected by the Link Layer it will speed up the channel by inserting extra data in the next V3 or H3 octet. The TECT3 indicates a slowdown request to the Link Layer by asserting the justification request signal high during the octet after the V3 or H3 octet. When detected by the Link Layer it will retard the channel by leaving the octet following the next V3 or H3 octet unused. Both advance and retard rate adjustments take place in the frame or multi-frame following the justification request.

SBI Link Rate Information

The TECT3 SBI bus provides a method for carrying link rate information between devices. This is optional on a per channel basis. Two methods are specified, one for T1 channels and the second for DS3 channels. These methods use the reference 19.44MHz SBI clock and the SC1FP frame synchronization signal to measure channel clock ticks and clock phase for transport across the bus.

The T1 method allows for a count of the number of T1 rising clock edges between 2 KHz SC1FP frame pulses. This count is encoded in ClkRate[1:0] to indicate that the nominal number of clocks, one more than nominal or one less than nominal should be generated during the SC1FP period. This method also counts the number of 19.44MHz clock rising edges after sampling SC1FP high to the next rising edge of the T1 clock, giving the ability to control the phase of the generated clock. The link rate information passed across the SBI bus via the V4 octet and is shown in Table 13. Table 14 shows the encoding of the clock count, ClkRate[1:0], passed in the link rate octet.

Table 13: SBI T1 Link Rate Information



Link Rate Octet	Bit #	7	6	5:4	3:0
T1/E1 Format		ALM	0	ClkRate[1:0]	Phase[3:0]

Table 14: SBI T1 Clock Rate Encoding

ClkRate[1:0]	T1 Clocks / 2KHz
“00” – Nominal	772
“01” – Fast	773

“1x” – Slow	771

The method for transferring DS3 link rate information across the SBI passes the encoded count of DS3 clocks between 2KHz SC1FP pulses in the same method used for T1 tributaries, but does not pass any phase information. The other difference from T1 link rate is that ClkRate[1:0] indicates whether the nominal number of clocks are generated or if four fewer or four extra clocks are generated during the SC1FP period. The format of the DS3 link rate octet is shown in Table 15. This is passed across the SBI via the Linkrate octet which follows the H3 octet in the column, see Table 19. Table 16 shows the encoding of the clock count, ClkRate[1:0], passed in the link rate octet.

Table 15: DS3 Link Rate Information

Link Rate Octet	Bit #	7	6	5:4	3:0
DS3 Format		0	0	ClkRate[1:0]	Unused

Table 16: DS3 Clock Rate Encoding

ClkRate[1:0]	DS3 Clocks / 2KHz
“00” – Nominal	22368
“01” – Fast	22372
“1x” – Slow	22364

SBI Alarms

The TECT3 transfers alarm conditions across the SBI bus for T1 tributaries. The TECT3 does not support alarm conditions across the SBI bus for DS3.

Table 13 show the alarm indication bit, ALM, as bit 7 of the Link Rate Octet. Devices connecting to the TECT3 which do not support alarm indications must set this bit to 0 on the SBI ADD bus.

The presence of an alarm condition is indicated by the ALM bit set high in the Link Rate Octet. The absence of an alarm condition is indicated by the ALM bit set low in the Link Rate Octet. In the egress direction the TECT3 can be configured to use the alarm bit to force AIS on a per link basis.

T1 Tributary Mapping

Table 17 shows the format for mapping 84 T1s within the SPE octets. The DS0s and framing bits within each T1 are easily located within this mapping for channelized T1 applications. It is acceptable for the framing bit to not carry a valid framing bit on the Add Bus since the physical layer device will provide this information. Unframed T1s use the exact same format for mapping 84 T1s into the SBI except that the T1 tributaries need not align with the frame bit and DS0 locations. The V1,V2 and V4 octets are not used to carry T1 data and are either reserved or used for control across the interface. When enabled, the V4 octet is the Link Rate octet of Tables 1 and 3. It carries alarm and clock phase information across the SBI bus. The V1 and V2 octets are unused and should be ignored by devices listening to the SBI bus. The V5 and R octets do not carry any information and are fixed to a zero value. The V3 octet carries a T1 data octet but only during rate adjustments as indicated by the V5 indicator signals, DV5 and AV5, and payload signals, SDPL and SAPL. The PPSSSSFR octets carry channel associated signaling (CAS) bits and the T1 framing overhead. The DS0 octets are the 24 DS0 channels making up the T1 link.

The V1,V2,V3 and V4 octets are fixed to the locations shown. All the other octets, shown shaded for T1#1,1, float within the allocated columns maintaining the same order and moving a maximum of one octet per 2KHz multi-frame. The position of the floating T1 is identified via the V5 Indicator signals, SDV5 and SAV5, which locate the V5 octet. When the T1 tributary rate is faster than the SBI nominal T1 tributary rate, the T1 tributary is shifted ahead by one octet which is compensated by sending an extra octet in the V3 location. When the T1 tributary rate is slower than the nominal SBI tributary rate the T1 tributary is shifted by one octet which is compensated by inserting a stuff octet in the octet immediately following the V3 octet and delaying the octet that was originally in that position.

Table 17: T1 Framing Format

	COL #	**T1#1,1**	T1#2,1-3,28	**T1#1,1**	T1#2,1-3,28	**T1#1,1**	T1#2,1-3,28
ROW #	1-18	19	20-102	103	104-186	187	188-270
1	Unused	V1	V1	V5	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-

9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V2	V2	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V3	V3	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V4	V4	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-

The $P_1P_0S_1S_2S_3S_4$FR octet carries T1 framing in the F bit and channel associated signaling in the $P_1P_0$and $S_1S_2S_3S_4$bits. Channel associated signaling is optional. The R bit is reserved and is set to 0. The P_1P_0bits are used to indicate the phase of the channel associated signaling and the $S_1S_2S_3S_4$ bits are the channel associated signaling bits for the 24 DS0 channels in the T1. Table 18 shows the channel associated signaling bit mapping and how the phase bits locate the sixteen state CAS mapping as well as T1 frame alignment for super frame and extended superframe formats. When using four state CAS then the signaling bits are A1-A24, B1-B24, A1-B24, B1-B24 in place of are A1-A24, B1-

B24, C1-C24, D1-D24. When using 2 state CAS there are only A1-A24 signaling bits.

Table 18: T1 Channel Associated Signaling bits

				SF	ESF	
S_1	S_2	S_3	S_4	F	F	P_1 P_0
A1	A2	A3	A4	F1	M1	00
A5	A6	A7	A8	S1	C1	00
A9	A10	A11	A12	F2	M2	00
A13	A14	A15	A16	S2	F1	00
A17	A18	A19	A20	F3	M3	00
A21	A22	A23	A24	S3	C2	00
B1	B2	B3	B4	F4	M4	01
B5	B6	B7	B8	S4	F2	01
B9	B10	B11	B12	F5	M5	01
B13	B14	B15	B16	S5	C3	01
B17	B18	B19	B20	F6	M6	01
B21	B22	B23	B24	S6	F3	01
C1	C2	C3	C4	F1	M7	10
C5	C6	C7	C8	S1	C4	10
C9	C10	C11	C12	F2	M8	10
C13	C14	C15	C16	S2	F4	10
C17	C18	C19	C20	F3	M9	10
C21	C22	C23	C24	S3	C5	10
D1	D2	D3	D4	F4	M10	11
D5	D6	D7	D8	S4	F5	11
D9	D10	D11	D12	F5	M11	11
D13	D14	D15	D16	S5	C6	11
D17	D18	D19	D20	F6	M12	11
D21	D22	D23	D24	S6	F6	11

Note that in synchronous mode, the SF/ESF F-bits may have arbitrary alignment with respect to the P_1P_0 phase alignment bits, due to possible frame slips at the T1 level. However, CAS is always aligned to the P_1P_0 bits (i.e. in either synchronous or asynchronous mode).

T1 tributary asynchronous timing is compensated via the V3 octet. T1 tributary link rate adjustments are optionally passed across the SBI via the V4. T1 tributary alarm conditions are optionally passed across the SBI bus via the link rate octet in the V4 location.

In synchronous mode the T1 tributary mapping is fixed to that shown in Table 17 and rate justifications are not possible using the V3 octet. The clock rate

information within the link rate octet in the V4 location is not used in synchronous mode.

DS3 Tributary Mapping

Table 19 shows a DS3 tributary mapped within the first synchronous payload envelope SPE1. The V5 indicator pulse identifies the V5 octet. The DS3 framing format does not follow an 8KHz frame period so the floating DS3 multi-frame located by the V5 indicator, shown in heavy border grey region in Table 19, will jump around relative to the H1 frame on every pass. In fact the V5 indicator will often be asserted twice per H1 frame, as is shown by the second V5 octet in Table 19. The V5 indicator and payload signals indicate negative and positive rate adjustments which are carried out by either putting a data byte in the H3 octet or leaving empty the octet after the H3 octet.

Table 19: DS3 Framing Format

	SPE COL #		DS3 1	DS3 2-56	DS3 57	DS3 58-84	DS3 Col 85
ROW	SBI COL# 1,4,7,10	13	16	•••	184	•••	268
1	Unused	**H1**	V5	DS3	DS3	DS3	DS3
2	Unused	**H2**	DS3	DS3	DS3	DS3	DS3
3	Unused	**H3**	DS3	DS3	DS3	DS3	DS3
4	Unused	**Linkrate**	DS3	DS3	DS3	DS3	DS3
5	Unused	Unused	DS3	DS3	DS3	DS3	DS3
6	Unused	Unused	DS3	DS3	DS3	DS3	DS3
7	Unused	Unused	DS3	DS3	DS3	DS3	DS3
8	Unused	Unused	DS3	DS3	V5	DS3	DS3
9	Unused	Unused	DS3	DS3	DS3	DS3	DS3

Because the DS3 tributary rate is less than the rate of the grey region, padding octets are interleaved with the DS3 tributary to make up the difference in rate. Interleaved with every DS3 multi-frame are 35 stuff octets, one of which is the V5 octet. These 35 stuff octets are spread evenly across seven DS3 subframes. Each DS3 subframe is eight blocks of 85 bits. The 85 bits making up a DS3 block are padded out to be 11 octets. Table 20 shows the DS3 block 11 octet format where R indicates a stuff bit, F indicates a DS3 framing bit and I indicates DS3 information bits. Table 21 shows the DS3 multi-frame format that is packed into the grey region of Table 19. In this table V5 indicates the V5 octet which is also a stuff octet, R indicates a stuff octet and B indicates the 11 octet DS3 block. Each row in Table 21 is a DS3 multi-frame. The DS3 multi-frame stuffing format is identical for 5 multi-frames and then an extra stuff octet after the V5 octet is added every sixth frame.

Table 20: DS3 Block Format

Octet #	1	2	3	4	5	6	7	8	9	10	11
Data	RRRFIIII	8*I	8*I	8*I	8*I	8*I	8*I	8*I	8*I	8*I	8*I

Table 21: DS3 Multi-frame Stuffing Format

V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B

DS3 asynchronous timing is compensated via the H3 octet. DS3 link rate adjustments are optionally passed across the SBI via the Linkrate octet.

12.11 H-MVIP Data Format

The H-MVIP data and Channel Associated Signaling interfaces on the TECT3 are able to carry all the DS0s for 28 T1s or all timeslots for 21 E1s. When Carrying timeslots from E1s the H-MVIP frame is completely filled with 128 timeslots from four E1s but when carrying DS0s from four T1s there are not enough DS0s to completely fill the 128 byte frame. Table 22 shows how the DS0s and CAS bits of four T1s are formatted in the 128 timeslot H-MVIP frame. Table 23 shows the timeslot and CAS bit H-MVIP format when in G.747 mode. The CAS bits are carried in bits 5,6,7 and 8 of each byte on the CASID[1:7] and CASED[1:7] H-MVIP buses.

Table 22: Data and CAS T1 H-MVIP Format

Timeslot Number	First T1 DS0 Number	Second T1 DS0 Number	Third T1 DS0 Number	Fourth T1 DS0 Number
0-3	Undefined	Undefined	Undefined	Undefined
4-7	1	1	1	1
8-11	2	2	2	2
12-15	3	3	3	3
16-19	Undefined	Undefined	Undefined	Undefined

20-23	4	4	4	4
24-27	5	5	5	5
28-31	6	6	6	6
32-35	Undefined	Undefined	Undefined	Undefined
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
108-111	21	21	21	21
112-115	Undefined	Undefined	Undefined	Undefined
116-119	22	22	22	22
120-123	23	23	23	23
124-127	24	24	24	24

Table 23: Data and CAS E1 H-MVIP Format in G.747 mode

Timeslot Number	First E1 TS Number	Second E1 TS Number	Third E1 TS Number	Fourth E1 TS Number
0-3	0	0	0	undefined
4-7	1	1	1	undefined
8-11	2	2	2	undefined
12-15	3	3	3	undefined
16-19	4	4	4	undefined
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
120-123	30	30	30	undefined
124-127	31	31	31	undefined

The H-MVIP Common Channel Signaling interface on TECT3 carries at most 63 timeslots when in E1 mode, timeslot 16 for ISDN signaling, timeslot 15 and timeslot 31 for V5.2 interfaces. In T1 mode the CCS H-MVIP interface only carries 28 full timeslots. Table 24 shows the H-MVIP format for carrying 28 common channeling signaling channels when in T1 mode. Table 25 shows the

H-MVIP format for carrying 63 E1 common channeling signaling channels when in G.747 mode . These formats are fixed so when a signaling or V5.2 channel is not in use the H-MVIP timeslot is undefined.

Table 24: CCS T1 H-MVIP Format

H-MVIP Timeslot Number	T1 Number
0	1
1	2
2	3
3	4
4	5
•	•
•	•
•	•
26	27
27	28
28	undefined
29	undefined
•	•
•	•
•	•
127	undefined

Table 25: CCS E1 H-MVIP Format in G.747 Mode

H-MVIP Timeslot Number	E1 Number TS 16	E1 Number TS 15	E1 Number TS 31
0	1		
1	2		
2	3		
3	undefined		
4	4		

5	5		
6	6		
7	undefined		
•	•		
•	•		
•	•		
24	19		
25	20		
26	21		
27	undefined		
•	•		
•	•		
•	•		
31	undefined		
32		1	
33		2	
34		3	
35		undefined	
•		•	
•		•	
•		•	
58		21	
59		undefined	
•		•	
•		•	
•		•	
63		undefined	
64			1
65			2

66			3
67			undefined
•			•
•			•
•			•
90			21
91			undefined
•			•
•			•
•			•
127			undefined

12.12 Serial Clock and Data Format

The Serial Clock and Data interfaces are able to carry the complete payload for 28 T1s or 21 E1s. Each T1 or E1 is assigned to one transmit pin and one receive data pin for the payload. As appropriate, additional pins may exist for the T1/E1 clock, signaling bits and/or frame pulse, depending on the specific interface mode selected. The formatting of these bits is outlined in greater deail in the Functional Timing section of this document.

In T1 mode, all 28 sets of clock and data pins are used in each direction.

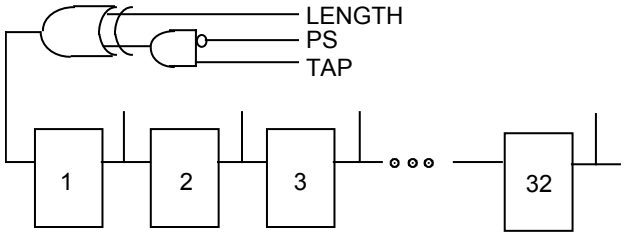
In normal E1 mode, the first 21 sets of clock and data pins are used in each direction. The clock and data pins numbered between 22 and 28 are not defined, as the 22nd through 28th framer blocks are not used in this mode.

In ITU-T G.747 mutiplexed E1 mode, every fourth set of clock and data pins are not used in each direction. (i.e. Pins 1-3, 5-7, 9-11, 13-15, 17-19, 21-23, 25-27 are defined while pins 4, 8, 12, 16, 20, 24, and 28 are not defined.) This is because the 4th, 8th, 12th, 16th, 20th, 24th and 28th framer blocks are not used in this mode.

12.13 PRGD Pattern Generation

The pattern generator can be configured to generate pseudo random patterns or repetitive patterns as shown in Figure 41 below:

Figure 41: PRGD Pattern Generator



The pattern generator consists of a 32 bit shift register and a single XOR gate. The XOR gate output is fed into the first stage of the shift register. The XOR gate inputs are determined by values written to the length register (PL[4:0]) and the tap register (PT[4:0], when the PS bit is low). When PS is high, the pattern detector functions as a recirculating shift register, with length determined by PL[4:0].

Generating and detecting repetitive patterns

When a repetitive pattern (such as 1-in-8) is to be generated or detected, the PS bit must be set to logic 1. The pattern length register must be set to (N-1), where N is the length of the desired repetitive pattern. Several examples of programming for common repetitive sequences are given below in the Common Test Patterns section.

For pattern generation, the desired pattern must be written into the PRGD Pattern Insertion registers. The repetitive pattern will then be continuously generated. The generated pattern will be inserted in the output data stream, but the phase of the pattern cannot be guaranteed.

For pattern detection, the PRGD will determine if a repetitive pattern of the length specified in the pattern length register exists in the input stream. It does so by loading the first N bits from the data stream, and then monitoring to see if the pattern loaded repeats itself error free for the subsequent 48 bit periods. It will repeat this process until it finds a repetitive pattern of length N, at which point it begins counting errors (and possibly re-synchronizing) in the same way as for pseudo-random sequences. Note that the PRGD does NOT look for the pattern loaded into the Pattern Insertion registers, but rather automatically detects any repetitive pattern of the specified length. The precise pattern detected can be determined by initiating a PRGD update, setting PDR[1:0] = 00 in the PRGD Control register, and reading the Pattern Detector registers (which will then contain the 32 bits detected immediately prior to the strobe).

Common Test Patterns

The PRGD can be configured to monitor the standardized pseudo random and repetitive patterns described in ITU-T O.151. The register configurations required to generate these patterns and others are indicated in Table 26 and Table 27 below:

Table 26: Pseudo Random Pattern Generation (PS bit = 0)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
2^3 -1	00	02	FF	FF	FF	FF	0	0
2^4 -1	00	03	FF	FF	FF	FF	0	0
2^5-1	01	04	FF	FF	FF	FF	0	0
2^6 -1	04	05	FF	FF	FF	FF	0	0
2^7 -1	00	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Activate)	03	06	FF	FF	FF	FF	0	0
2^7 -1 (Fractional T1 LB Deactivate)	03	06	FF	FF	FF	FF	1	1
2^9 -1 (O.153)	04	08	FF	FF	FF	FF	0	0
2^{10} -1	02	09	FF	FF	FF	FF	0	0
2^{11} -1 (O.152, O.153)	08	0A	FF	FF	FF	FF	0	0
2^{15} -1 (O.151)	0D	0E	FF	FF	FF	FF	1	1
2^{17} -1	02	10	FF	FF	FF	FF	0	0
2^{18} -1	06	11	FF	FF	FF	FF	0	0
2^{20} -1 (O.153)	02	13	FF	FF	FF	FF	0	0
2^{20} -1 (O.151 QRSS bit=1)	10	13	FF	FF	FF	FF	0	0
2^{21} -1	01	14	FF	FF	FF	FF	0	0
2^{22} -1	00	15	FF	FF	FF	FF	0	0
2^{23} -1 (O.151)	11	16	FF	FF	FF	FF	1	1
2^{25} -1	02	18	FF	FF	FF	FF	0	0
2^{28} -1	02	1B	FF	FF	FF	FF	0	0
2^{29} -1	01	1C	FF	FF	FF	FF	0	0

2^{31} -1	02	1E	FF	FF	FF	FF	0	0

Table 27: Repetitive Pattern Generation (PS bit = 1)

Pattern Type	TR	LR	IR#1	IR#2	IR#3	IR#4	TINV	RINV
All ones	00	00	FF	FF	FF	FF	0	0
All zeros	00	00	FE	FF	FF	FF	0	0
Alternating ones/zeros	00	01	FE	FF	FF	FF	0	0
Double alternating ones/zeros	00	03	FC	FF	FF	FF	0	0
3 in 24	00	17	22	00	20	FF	0	0
1 in 16	00	0F	01	00	FF	FF	0	0
1 in 8	00	07	01	FF	FF	FF	0	0
1 in 4	00	03	F1	FF	FF	FF	0	0
Inband loopback activate	00	04	F0	FF	FF	FF	0	0
Inband loopback deactivate	00	02	FC	FF	FF	FF	0	0

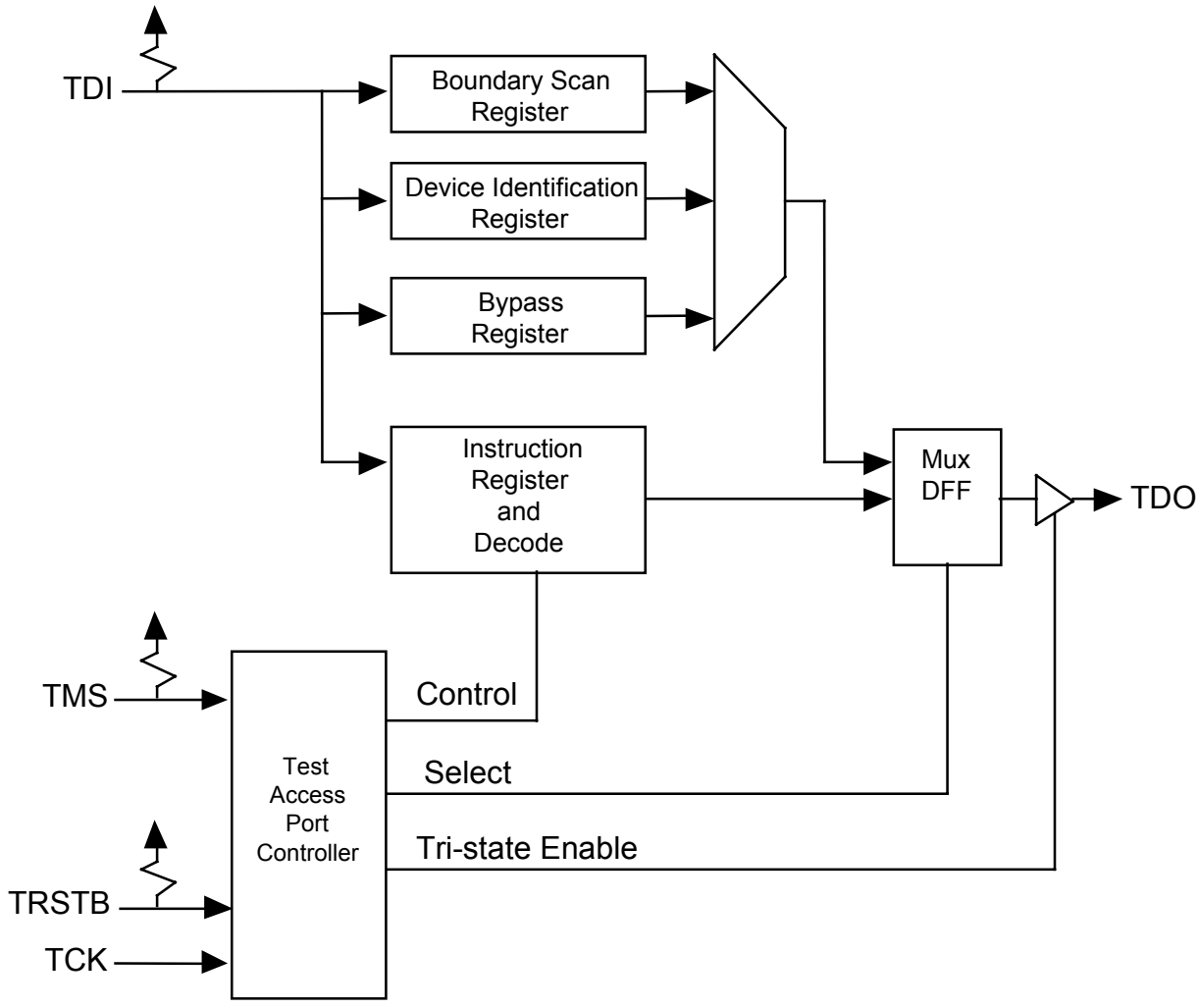
Notes for the Pseudo Random and Repetitive Pattern Generation Tables

1. The PS bit and the QRSS bit are contained in the PRGD Control register
2. TR = PRGD Tap Register
3. LR = PRGD Length Register
4. IR#1 = PRGD Pattern Insertion #1 Register
5. IR#2 = PRGD Pattern Insertion #2 Register
6. IR#3 = PRGD Pattern Insertion #3 Register
7. IR#4 = PRGD Pattern Insertion #4 Register
8. The TINV bit and the RINV bit are contained in the PRGD Control register

12.14 JTAG Support

The TECT3 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 42: Boundary Scan Architecture



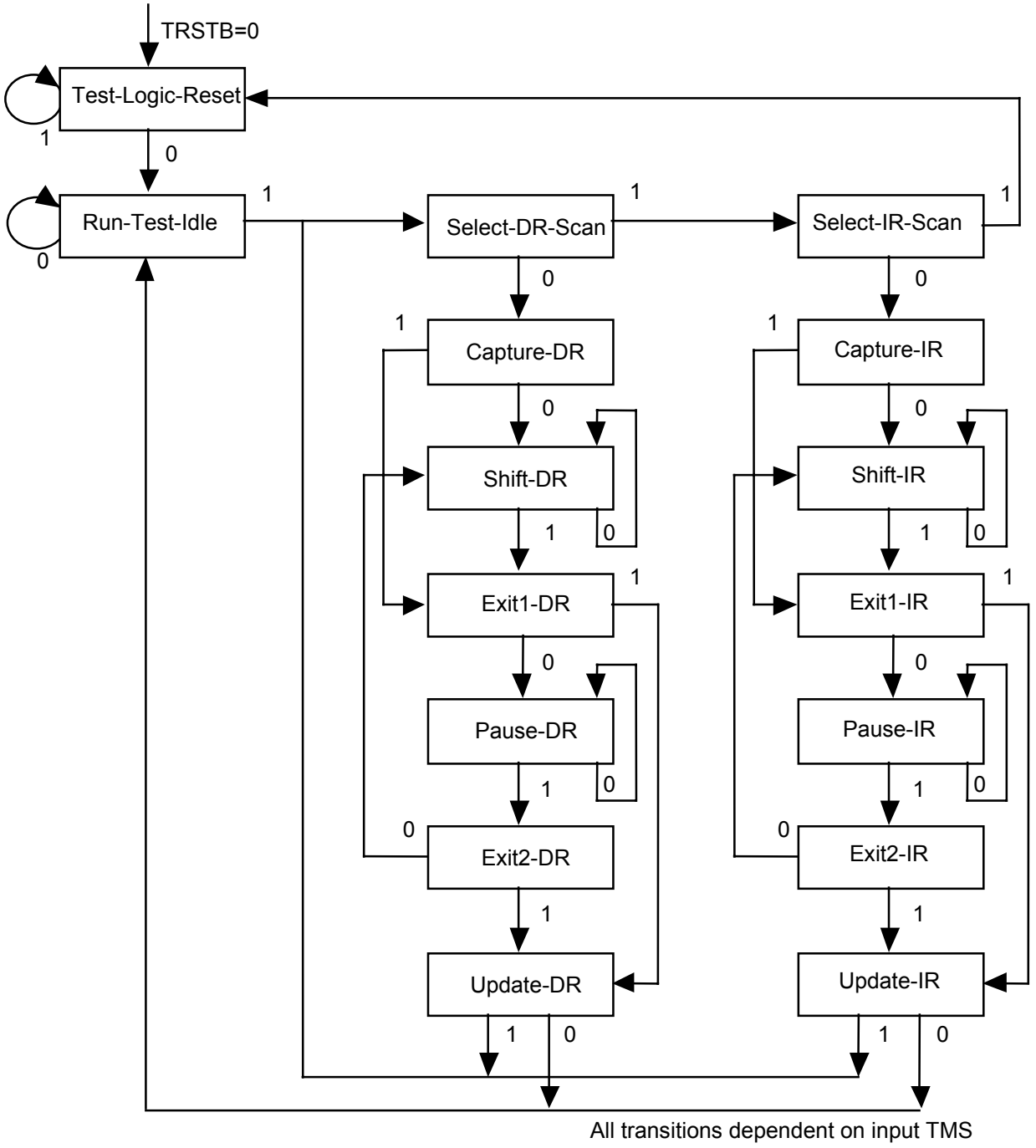
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI, and forced onto all digital outputs.

12.14.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 43: TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out of the output, TDO, using the Shift-DR state.

Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table in the JTAG Test Port section 11.2.

Figure 44: Input Observation Cell (IN_CELL)

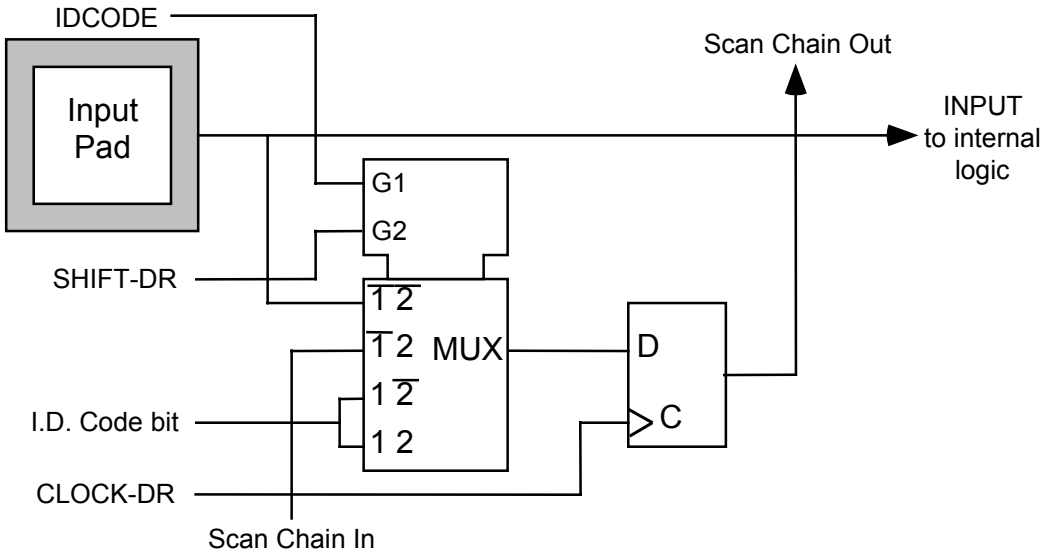


Figure 45: Output Cell (OUT_CELL)

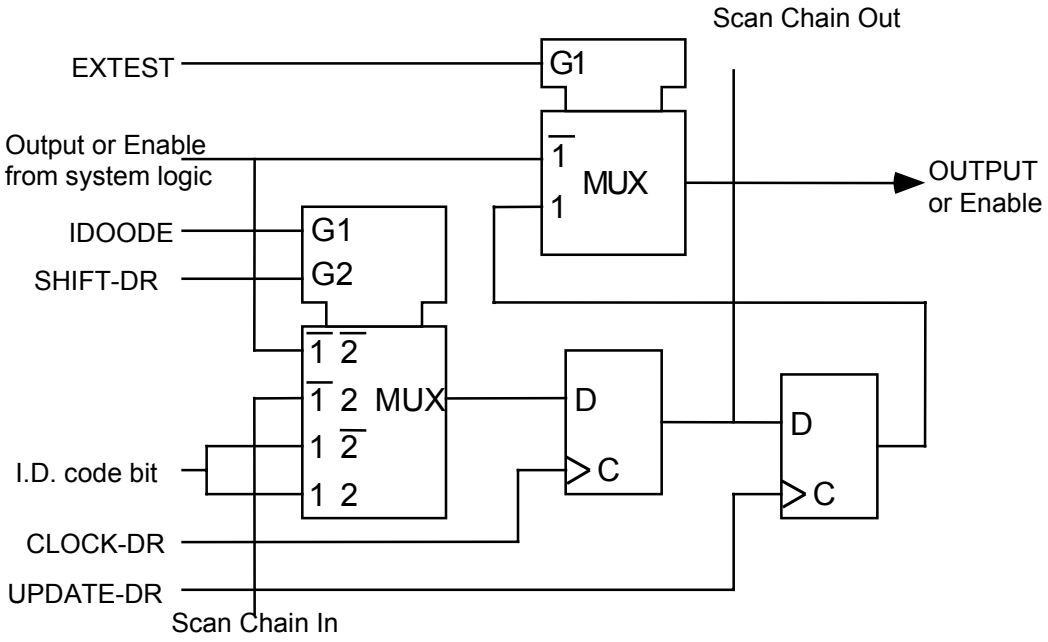


Figure 46: Bidirectional Cell (IO_CELL)

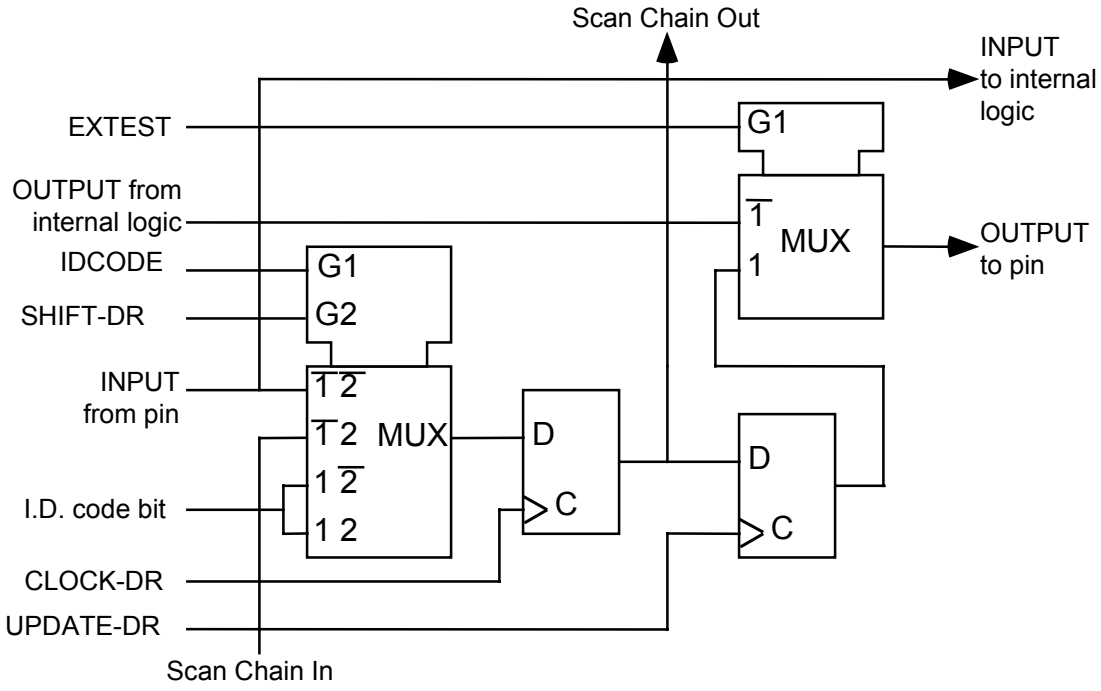
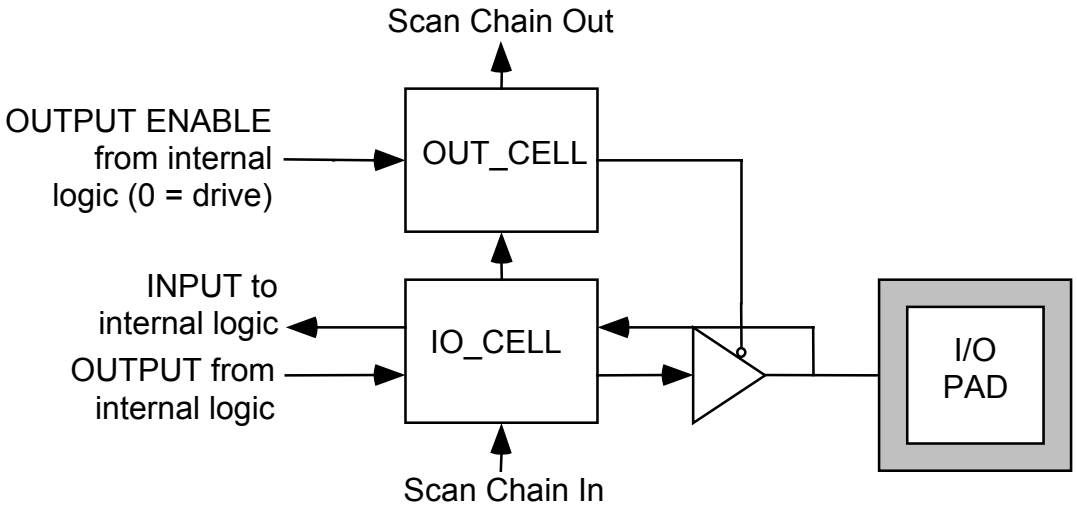


Figure 47: Layout of Output Enable and Bidirectional Cells

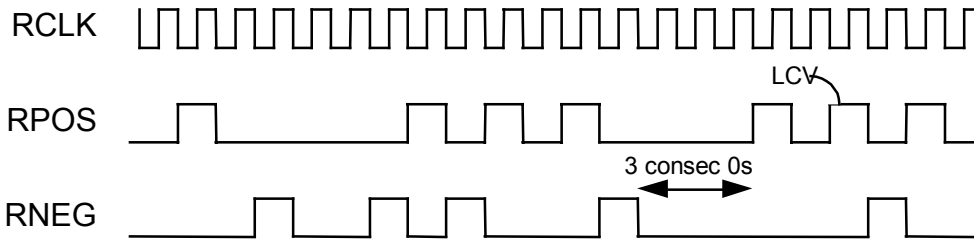


13 FUNCTIONAL TIMING

13.1 DS3 Line Side Interface Timing

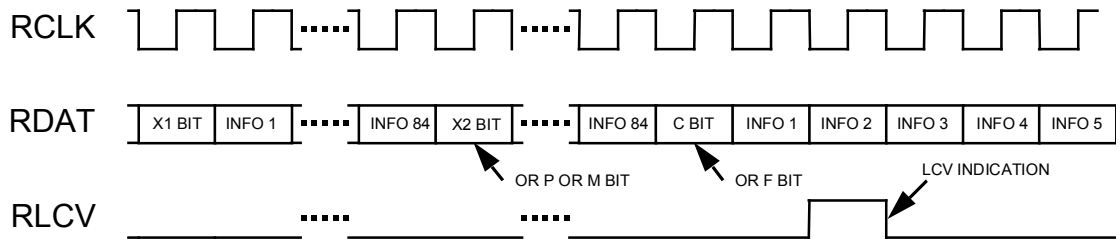
All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the TECT3 registers are set to their default states).

Figure 48: Receive Bipolar DS3 Stream



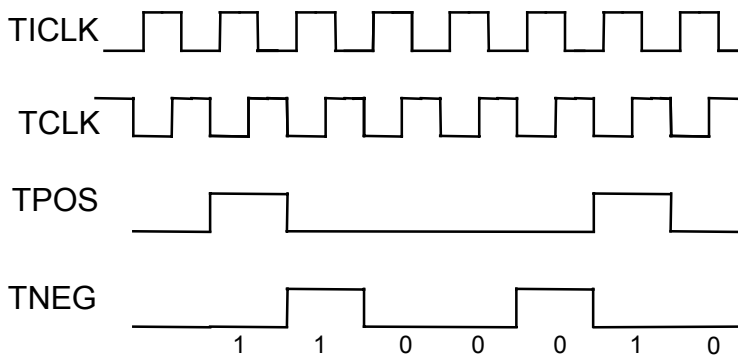
The Receive Bipolar DS3 Stream diagram (Figure 48) shows the operation of the TECT3 while processing a B3ZS encoded DS3 stream on inputs RPOS and RNEG. It is assumed that the first bipolar violation (on RNEG) illustrated corresponds to a valid B3ZS signature. A line code violation is declared upon detection of three consecutive zeros in the incoming stream, or upon detection of a bipolar violation which is not part of a valid B3ZS signature.

Figure 49: Receive Unipolar DS3 Stream



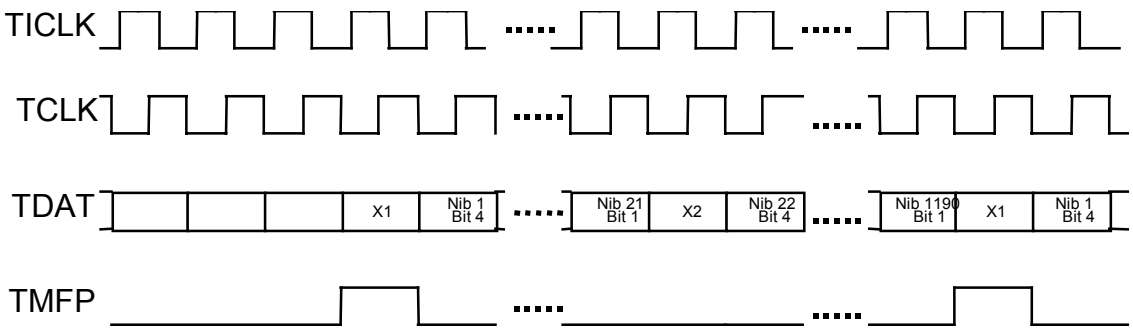
The Receive Unipolar DS3 Stream diagram (Figure 49) shows the complete DS3 receive signal on the RDAT input. Line code violation indications, detected by an upstream B3ZS decoder, are indicated on input RLCV. RLCV is sampled each bit period. The PMON Line Code Violation Event Counter is incremented each time a logic 1 is sampled on RLCV.

Figure 50: Transmit Bipolar DS3 Stream



The Transmit Bipolar DS3 Stream diagram (Figure 50) illustrates the generation of a bipolar DS3 stream. The B3ZS encoded DS3 stream is present on TPOS and TNEG. These outputs, along with the transmit clock, TCLK, can be directly connected to a DS3 line interface unit. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

Figure 51: Transmit Unipolar DS3 Stream



The Transmit Unipolar DS3 Stream diagram (Figure 51) illustrates the unipolar DS3 stream generation. The TMFP output marks the M-frame boundary, X1 bit, in the transmit stream. Note that TCLK is a flow through version of TICLK; a variable propagation delay exists between these two signals.

13.2 DS3 System Side Interface Timing

Figure 52: Framer Mode DS3 Transmit Input Stream

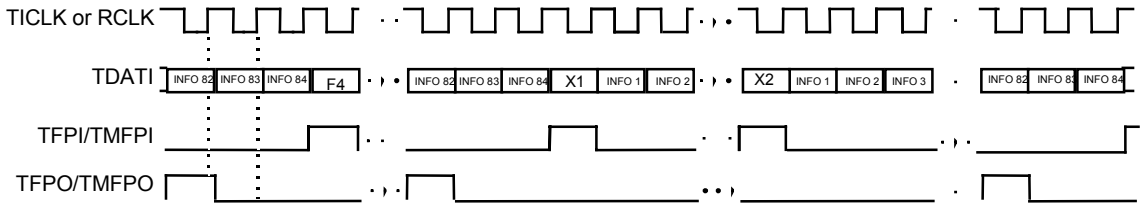
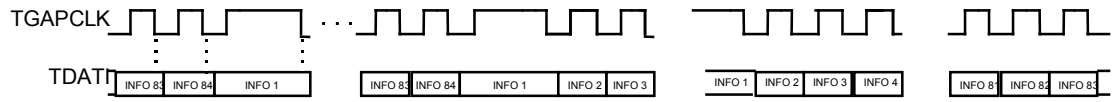


Figure 53: Framer Mode DS3 Transmit Input Stream With TGAPCLK



The Framer Mode DS3 Transmit Input Stream diagram (Figure 52) shows the expected format of the inputs TDATI and TFPI/TMFPI along with TICLK and the output TFPO/TMFPO when the OPMODE[1:0] bits are set to “DS3 Framer Only mode” in the Global Configuration register. If the TXMFPI bit in the DS3 Master Unchannelized Interface Options register is logic 0, then TFPI is valid, and the TECT3 will expect TFPI to pulse for every DS3 overhead bit with alignment to TDATI. If the TXMFPI register bit is logic 1, then TMFPI is valid, and the TECT3 will expect TMFPI to pulse once every DS3 M-frame with alignment to TDATI. If the TXMFPO bit in the DS3 Master Unchannelized Interface Options register is logic 0, then TFPO is valid, and the TECT3 will pulse TFPO once every 85 TICLK cycles, providing upstream equipment with a reference DS3 overhead pulse. If the TXMFPO register bit is logic 1, then TMFPO is valid and the TECT3 will pulse TMFPO once every 4760 TICLK cycles, providing upstream equipment with a reference M-frame pulse. The alignment of TFPO or TMFPO is arbitrary. There is no set relationship between TFPO/TMFPO and TFPI/TMFPI. When the DS3 interface is loop timed by setting the LOOPT bit in the DS3 Master Data Source register, RCLK replaces TICLK as the transmit timing reference and all timing is relative to RCLK.

The TGAPCLK output is available in place of TFPO/TMFPO when the TXGAPEN bit in the DS3 Master Unchannelized Interface Options register is set to logic 1, as in Figure 53. TGAPCLK remains high during the overhead bit positions. TDATI is sampled on the active edge of TGAPCLK when TXGAPEN is set to logic 1 and on the active edge of TICLK when TXGAPEN is set to logic 0. The TDATIFALL bit in the DS3 Master Unchannelized Interface Options register selects the active edge of TICLK or TGAPCLK for sampling TDATI.

Figure 54: Framer Mode DS3 Receive Output Stream

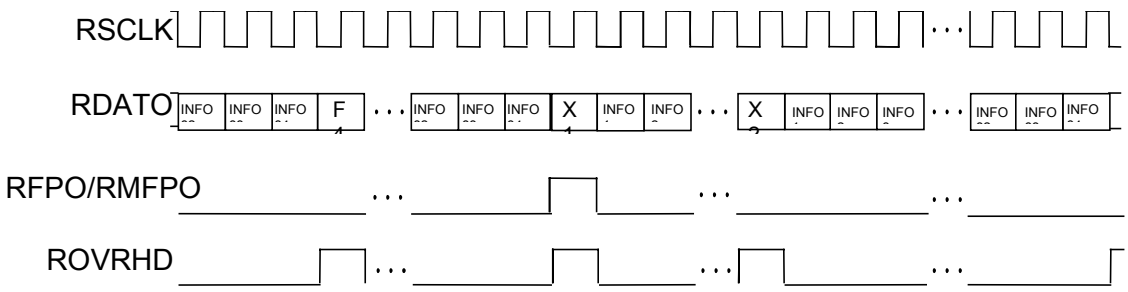
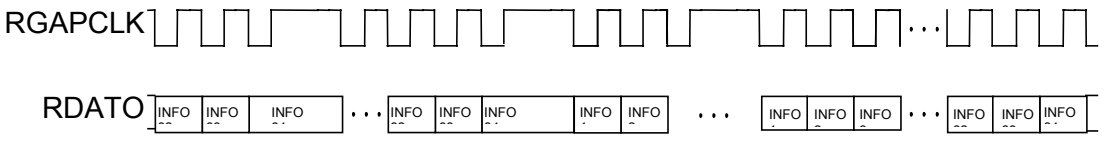


Figure 55: Framer Mode DS3 Receive Output Stream with RGAPCLK



The DS3 Framer Only Mode Receive Output Stream diagram (Figure 54) shows the format of the outputs RDATO, RFPO/RMFPO, RSCLK ROVRHD when the OPMODE[1:0] bits are set to “DS3 Framer Only mode” in the Global Configuration register. Figure 54 shows the data streams when the TECT3 is configured for the DS3 receive format. If the RXMFPO bit in the DS3 Master Unchannelized Interface Options register is logic 0, RFPO is valid and will pulse high for one RSCLK cycle on first bit of each M-subframe with alignment to the RDATO data stream. If the RXMFPO register bit is a logic 1 (as shown Figure 54), RMFPO is valid and will pulse high on the X1 bit of the RDATO data output stream. ROVRHD will be high for every overhead bit position on the RDATO data stream. Figure 55 shows the output data stream with RGAPCLK in place of RSCLK when the RXGAPEN bit in the DS3 Master Unchannelized Interface Options register set to logic 1. RGAPCLK remains high during the overhead bit positions.

13.3 SBI DROP Bus Interface Timing

Figure 56: SBI DROP Bus T1 Functional Timing

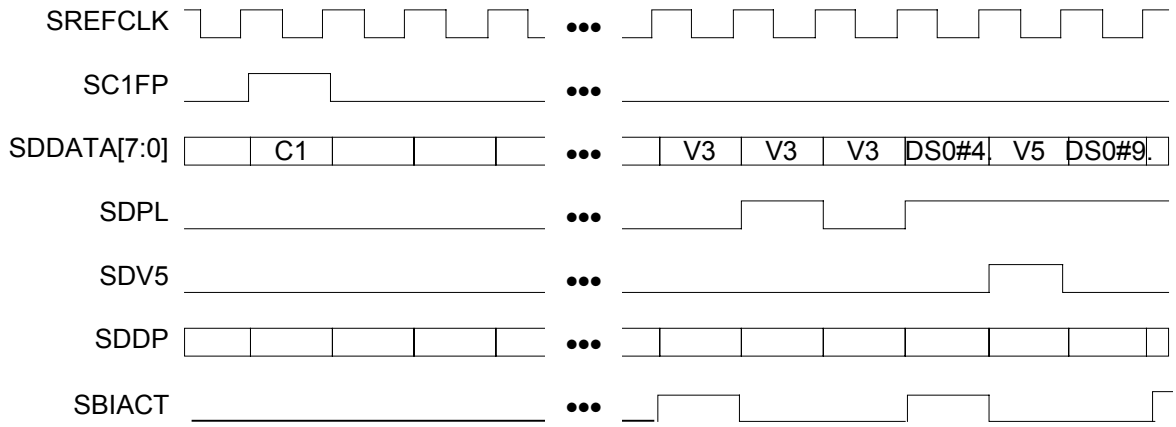


Figure 56 illustrates the operation of the SBI DROP Bus, using a negative justification on the second to last V3 octet as an example. The justification is indicated by asserting SDPL high during the V3 octet. The timing diagram also shows the location of one of the tributaries by asserting SDV5 high during the V5 octet. The SBIACT signal is shown for the case in which TECT3 is driving SPE#1 onto the SBI DROP bus.

Figure 57: SBI DROP Bus DS3 Functional Timing

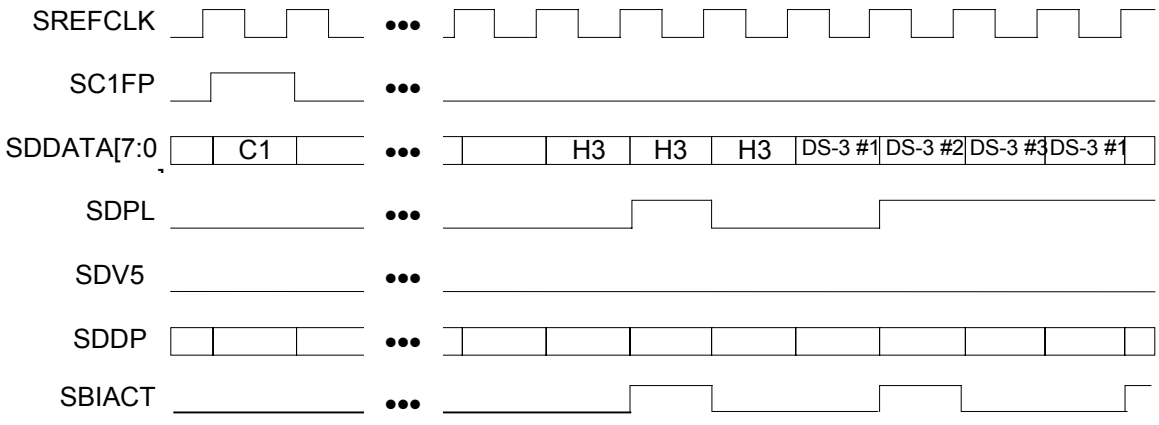


Figure 57 shows three DS-3 tributaries mapped onto the SBI bus. A negative justification is shown for DS-3 #2 during the H3 octet with SDPL asserted high. A positive justification is shown for DS-3#1 during the first DS-3#1 octet after H3 which has SDPL asserted low. The SBIACT signal is shown for the case in which TECT3 is driving SPE#2 (DS-3#2) onto the SBI DROP bus.

13.4 SBI ADD Bus Interface Timing

The SBI ADD bus functional timing for the transfer of tributaries, whether T1 or DS3, is the same as for the SBI DROP bus. The only difference is that the SBI ADD bus has one additional signal: the SAJUST_REQ output. The SAJUST_REQ signal is used to by the TECT3 in SBI master timing mode to provide transmit timing to SBI link layer devices.

Figure 58: SBI ADD Bus Justification Request Functional Timing

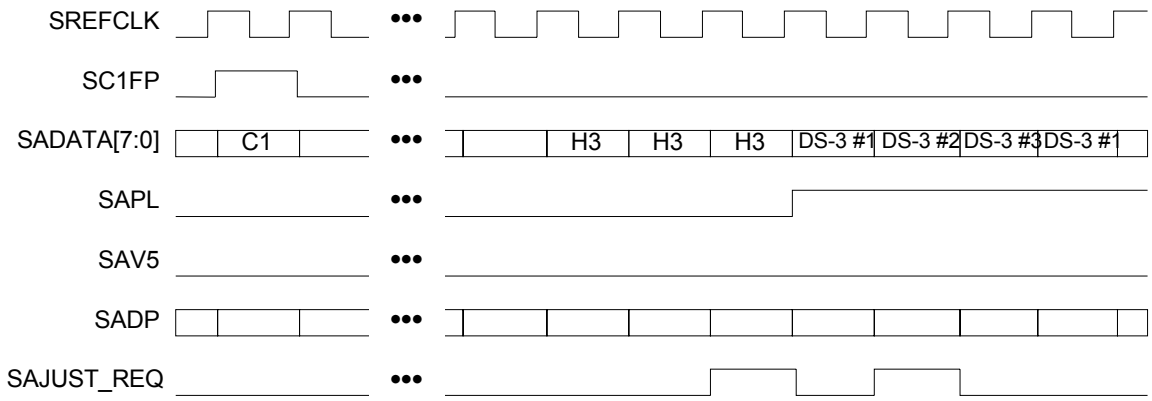
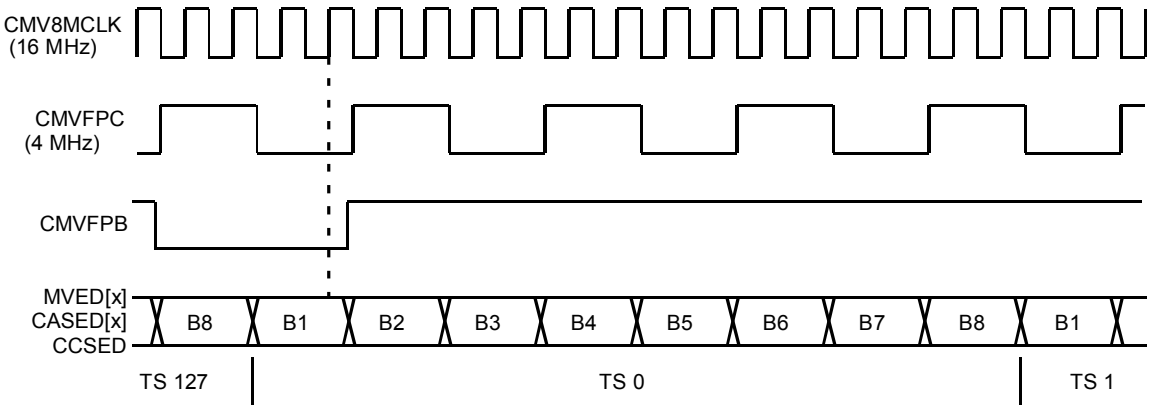


Figure 58 illustrates the operation of the SBI ADD Bus, using positive and negative justification requests as an example. (The responses to the justification requests would take effect during the next multi-frame.) The negative justification request occurs on the DS-3#3 tributary when SAJUST_REQ is asserted high during the H3 octet. The positive justification occurs on the DS-3#2 tributary when SAJUST_REQ is asserted high during the first DS-3#2 octet after the H3 octet.

13.5 Egress H-MVIP Link Timing

The timing relationship of the common 8M H-MVIP clock, CMV8MCLK, frame pulse clock, CMVFPC, data, MVED[x], CASED[x] or CCSED, and frame pulse, CMVFPB, signals of a link configured for 8.192 Mbps H-MVIP operation with a type 0 frame pulse is shown in Figure 59. The falling edges of each CMVFPC are aligned to a falling edge of the corresponding CMV8MCLK for 8.192 Mbps H-MVIP operation. The TECT3 samples CMVFPB low on the falling edge of CMVFPC and references this point as the start of the next frame. The TECT3 samples the data provided on MVED[x], CASED[x] and CCSED at the ¾ point of the data bit using the rising edge of CMV8MCLK as indicated for bit 1 (B1) of time-slot 1 (TS 1) in Figure 59. B1 is the most significant bit and B8 is the least significant bit of each octet.

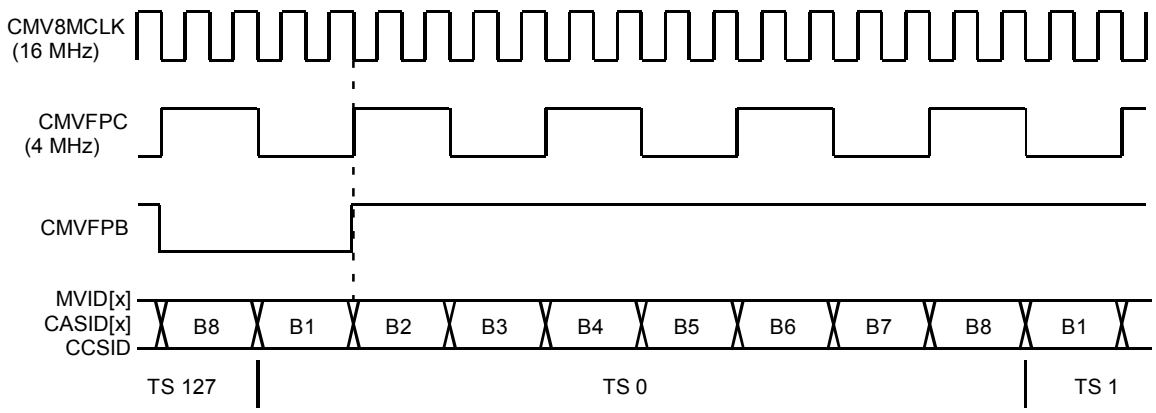
Figure 59: Egress 8.192 Mbps H-MVIP Link Timing



13.6 Ingress H-MVIP Link Timing

The timing relationship of the common 8M H-MVIP clock, CMV8MCLK, frame pulse clock, CMVFPC, data, MVID[x], CASID[x] or CCSID, and frame pulse, CMVFPB, signals of a link configured for 8.192 Mbps H-MVIP operation with a type 0 frame pulse is shown in Figure 60. The falling edges of each CMVFPC are aligned to a falling edge of the corresponding CMV8MCLK for 8.192 Mbps H-MVIP operation. The TECT3 samples CMVFPB low on the falling edge of CMVFPC and references this point as the start of the next frame. The TECT3 updates the data provided on MVID[x], CASID[x] and CCSID on every second falling edge of CMV8MCLK as indicated for bit 2 (B2) of time-slot 1 (TS 1) in Figure 60. The first bit of the next frame is updated on MVID[x], CASID[x] and CCSID on the falling CMV8MCLK clock edge for which CMVFPB is also sampled low. B1 is the most significant bit and B8 is the least significant bit of each octet.

Figure 60: Ingress 8.192 Mbps H-MVIP Link Timing



13.7 Egress Serial Clock and Data Interface Timing

By convention in the following functional timing diagrams, the first bit transmitted in each channel shall be designated bit 1 and the last shall be designated bit 8. Each of the Ingress and Egress Master and Clock Modes apply to both T1 and E1 configurations with the exception of the 2.048MHz T1 Clock Slave Modes.

Figure 61: T1 Egress Interface Clock Master: NxChannel Mode

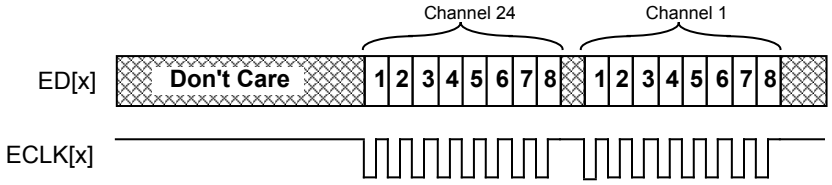
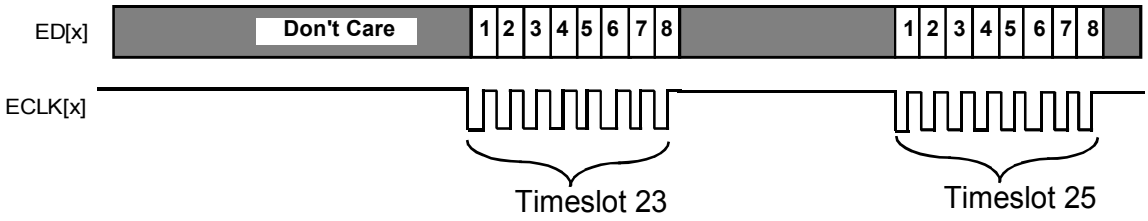
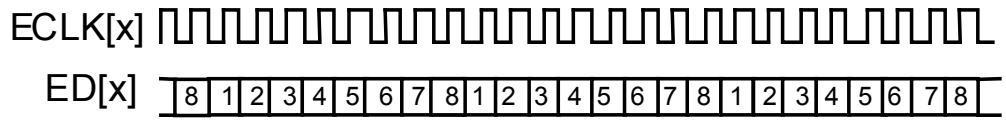


Figure 62: E1 Egress Interface Clock Master : NxChannel Mode



The Egress Interface Options register is programmed to select NxChannel mode. The TPSC egress control bytes are programmed to insert the desired channels. In Figure 61, the egress control bytes for T1 channels 1 and 24 are configured to insert these channels. In Figure 62, the egress control bytes for E1 channels 23 and 25 are configured to insert these channels. ECLK[x] is gapped so that it is only active for those channels with the associated IDLE_CHAN bit cleared (logic 0). The remaining channels (with IDLE_CHAN set) contain the per-channel idle code as defined in the associated Idle Code byte. When the EDE bit in the T1/E1 Serial Interface Configuration register is set to logic 0, then ED[x] is sampled on the falling edge of ECLK[x], and the functional timing is described by Figure 61 with the ECLK[x] signal inverted.

Figure 63: T1 and E1 Egress Interface Clock Master: Clear Channel Mode



The Egress Interface is configured for the Clock Master: Clear Channel mode by writing to EMODE[2:0] in theT1/E1 Egress Serial Interface Mode Select register. ED[x] is sampled on the rising edge of the ECLK[x] output. When the the EDE bit in the T1/E1 Serial Interface Configuration register is set to logic 0, then ED[x] is sampled on the falling edge of ECLK[x], and the functional timing is described by Figure 63 with the ECLK[x] signal inverted.

Figure 64: T1 Egress Interface Clock Slave: EFP Enabled mode

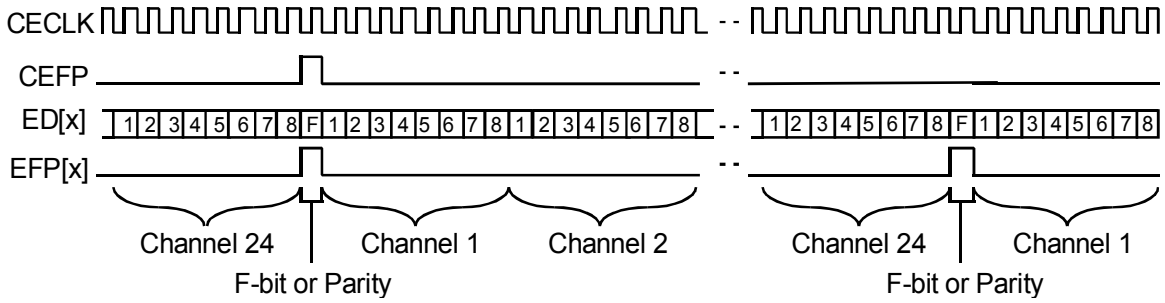
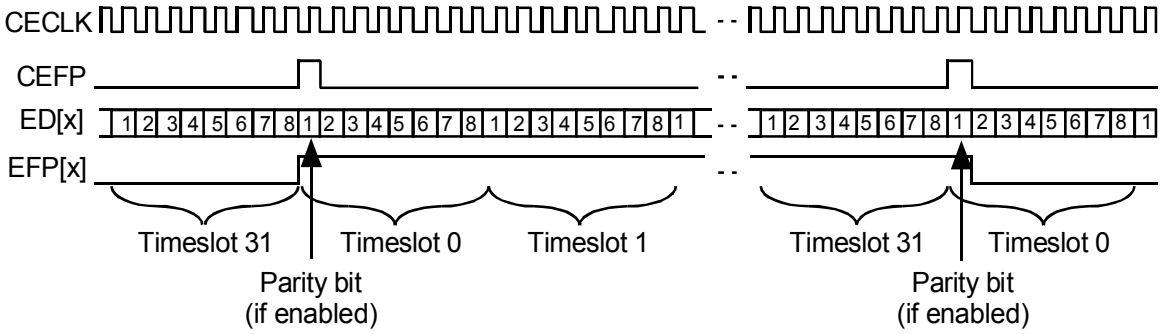


Figure 65: E1 Egress Interface Clock Slave : EFP Enabled Mode



The Egress Interface is configured for the Clock Slave: EFP Enabled mode by writing to EMODE[2:0] in theT1/E1 Egress Serial Interface Mode Select register. ED[x] is sampled on the active edge of CECLK and EFP[x] is updated on the falling edge of CECLK.

In T1 mode, Figure 64, the CEMFP bit is written to logic 1 in the Master Egress Slave Mode Serial Interface Configuration register, so that CEFP must pulse once every 12 or 24 frames (for SF and ESF, respectively) on the first frame bit of the multiframe. If parity checking is enabled, a parity bit should be inserted on ED[x] in the first bit of each frame. The EFP[x] output will pulse high to mark the F-bit of each frame in order to indicate frame alignment to an upstream device. EFP[x] may be configured to mark superframe alignment instead by setting the EMFP bit in the T1/E1 Serial Interface Configuration register.

In E1 mode EFP[x] may be chosen to indicate alignment of every frame or the composite CRC and Signaling multiframe alignment as shown in Figure 65, by setting the EMFP bit in the T1/E1 Serial Interface Configuration register. If parity checking is enabled, a parity bit should be inserted on ED[x] in the first bit of each frame.

Figure 66: T1 Egress Interface Clock Slave: External Signaling mode

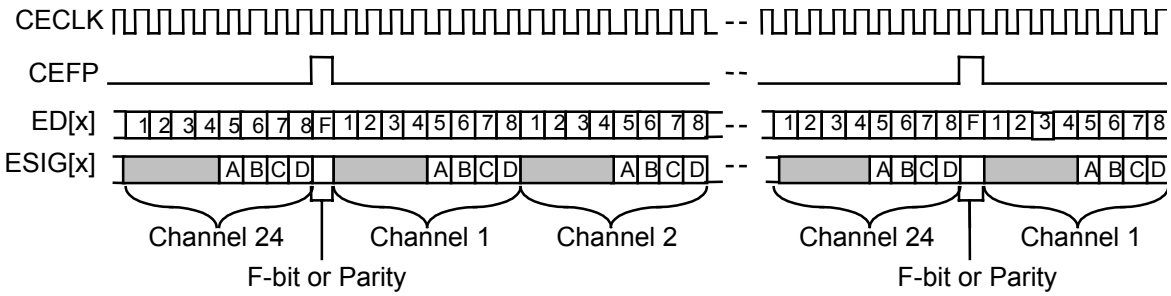
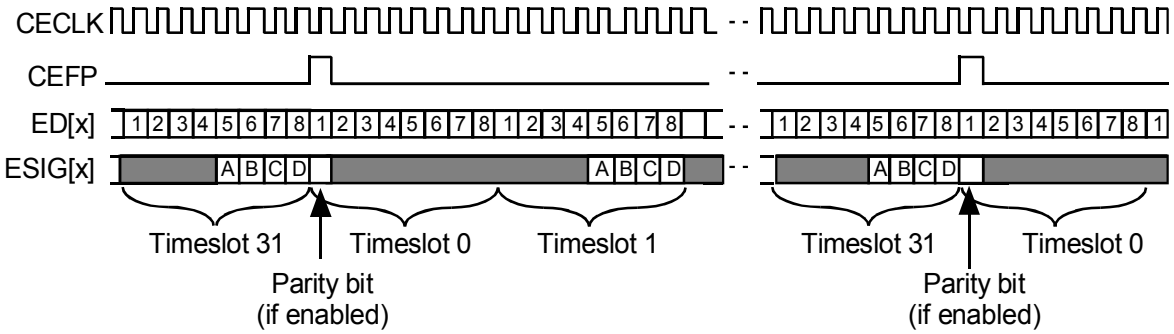
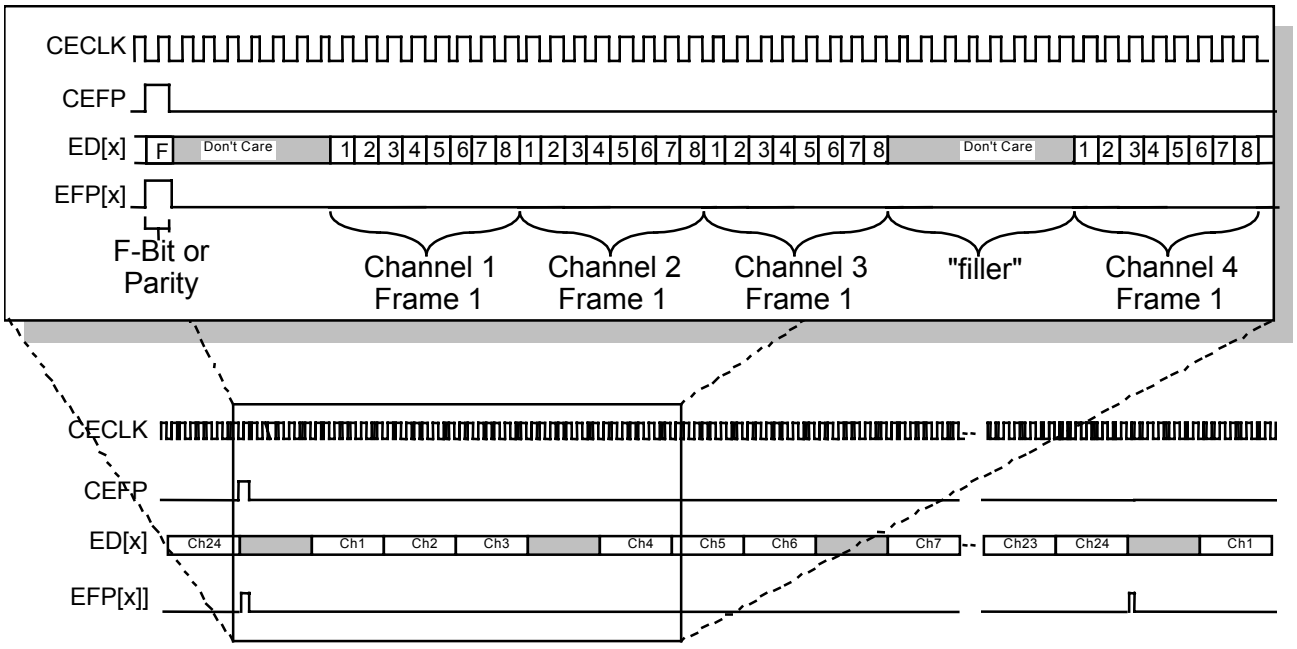


Figure 67: E1 Egress Interface Clock Slave : External Signaling Mode



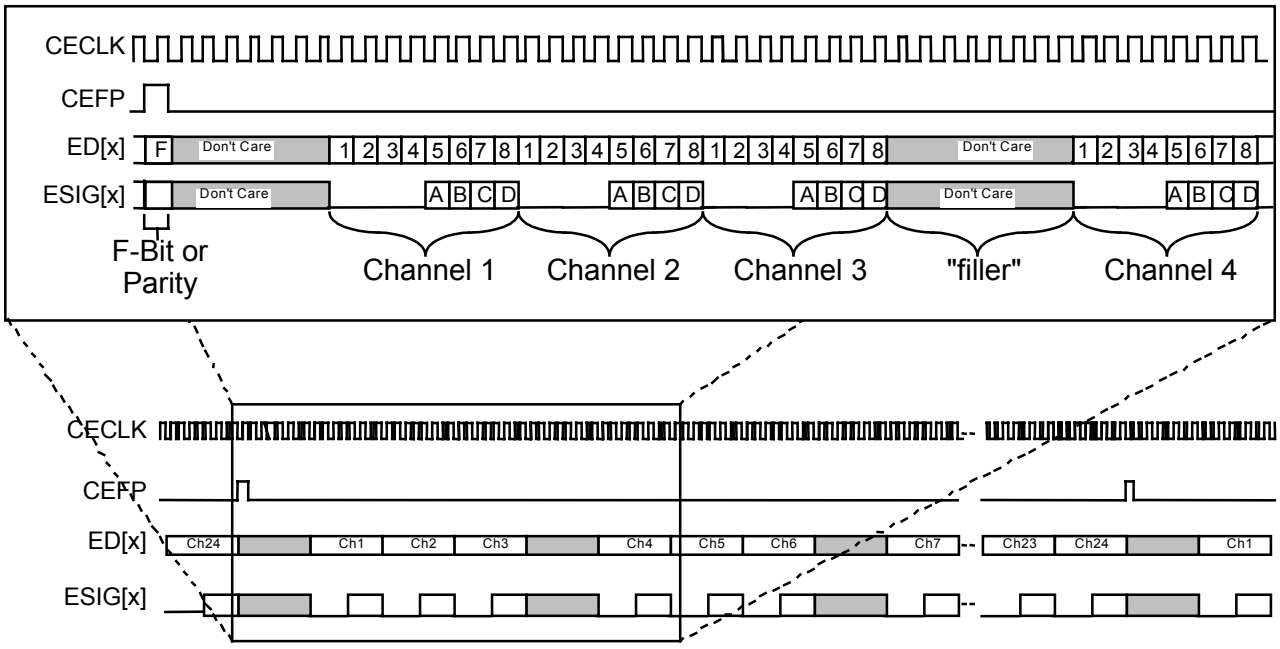
The Egress Interface is configured for the Clock slave: External Signaling Mode by writing to EMODE[2:0] in theT1/E1 Egress Serial Interface Mode Select register. ED[x] is clocked in on the active edge of CECLK. Frame alignment is specified by pulses on CEFP. ESIG[x] should carry the signaling bits for each channel in bits 5,6,7 and 8. These signaling bits will be inserted into the data stream by the T1 or E1 transmitter. If parity checking is enabled, a parity bit should be inserted on ED[x] and ESIG[x] in the first bit of each frame. The parity operates on all bits in the ED[x] and ESIG[x] streams, including the unused bits on ESIG[x].

Figure 68: T1 Egress Interface 2.048 MHz Clock Slave: EFP Enabled Mode



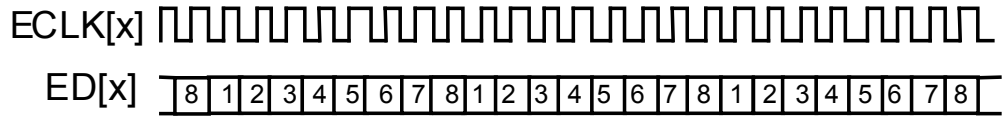
The Egress Interface is configured for the Clock Slave: EFP Enabled Mode by writing to EMODE[2:0] in theT1/E1 Egress Serial Interface Mode Select register. The 2.048 MHz internally gapped clock mode is selected by writing CECLK2M to logic 1 in the Master Egress Slave Mode Serial Interface register. In Figure 68, CEFP is configured for superframe alignment by writing CEMFP to logic 1 in the Master Egress Slave Mode Serial Interface register, so that the CEFP input must pulse once every 12 or 24 frames (for SF and ESF, respectively) on the first F-bit of the multiframe to specify superframe alignment, instead of once every frame to specify frame alignment. If parity checking is enabled, a parity bit should be inserted on ED[x] in the first bit of each frame. The EFP[x] output will pulse high to mark the F-bit of each frame in order to indicate frame alignment to an upstream device. EFP[x] may be configured to mark superframe alignment instead by setting the EMFP bit in the T1/E1 Serial Interface Configuration register. The values of the don't-care bits are not important, except that they will be used in the backplane parity check if it is enabled.

Figure 69: T1 Egress Interface 2.048 MHz Clock Slave: External Signaling Mode



The Egress Interface is configured for the 2.048 MHz Clock Slave: External Signaling Mode by writing to EMODE[2:0] in theT1/E1 Egress Serial Interface Mode Select register. The 2.048 MHz internally gapped clock mode is selected by writing CECLK2M to logic 1 in the Master Egress Slave Mode Serial Interface register. In the illustrated case, CEFP specifies frame alignment and is required to pulse high for one cycle every frame. ESIG[x] should carry the signaling bits for each channel in bits 5,6,7 and 8; the signaling bits will be inserted into the data stream by the transmitter. If parity checking is enabled, a parity bit should be inserted on ED[x] and ESIG[x] in the first bit of each frame. The values of the don't-care bits are not important, except that they will be used in the backplane parity check if it is enabled.

Figure 70: T1 and E1 Egress Interface Clock Slave: Clear Channel Mode



The Egress Interface is configured for the Clock Slave: Clear Channel mode by writing to EMODE[2:0] in theT1/E1 Egress Serial Interface Mode Select register. ED[x] is clocked in on the rising edge of the ECLK[x] input. When the EDE bit in the T1/E1 Serial Interface Configuration register is set to logic 0, then ED[x] is sampled on the falling edge of ECLK[x], and the functional timing is described by Figure 70 with the ECLK[x] signal inverted.

13.8 Ingress Serial Clock and Data Interface Timing

Figure 71: T1 Ingress Interface Clock Master : Full Channel Mode

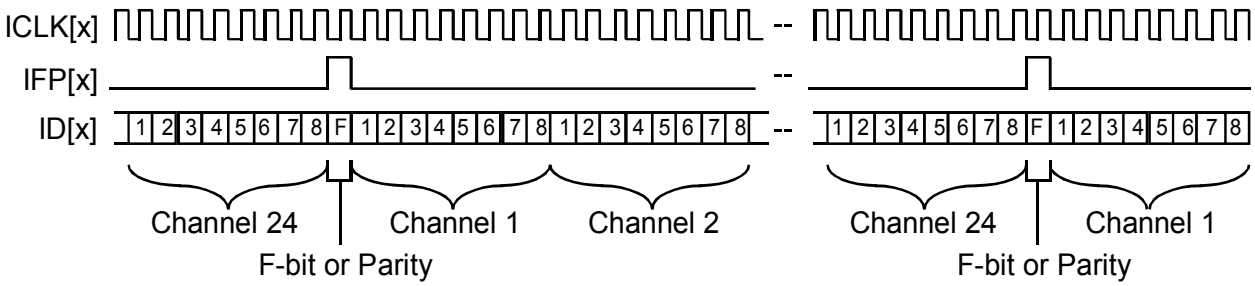
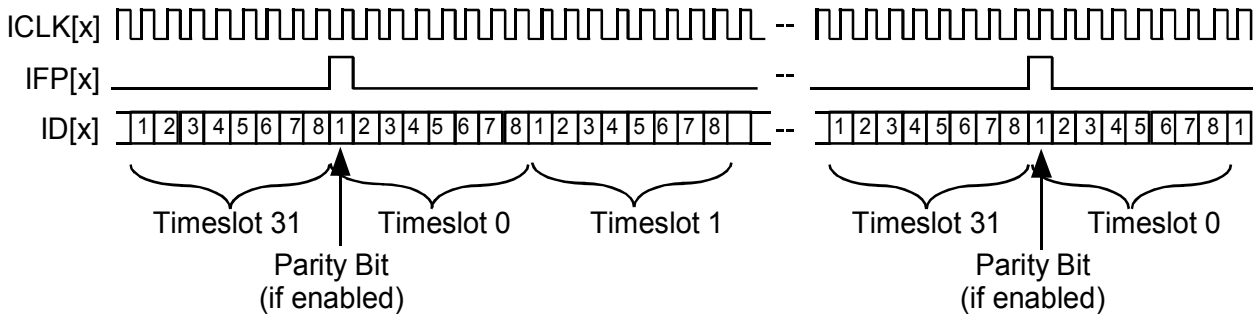


Figure 72: E1 Ingress Interface Clock Master : Full Channel Mode



The IMODE[1:0] bits in the T1/E1 Ingress Serial Interface Mode Select register are programmed to select the Clock Master: Full Channel mode. IFP[x] is set high for one ICLK[x] period every frame. When the IMFP bit in the T1/E1 Serial Interface Configuration register are set to 1, IFP[x] pulses on the superframe frame boundaries (i.e. once every 12 or 24 frame periods when configured for T1 operation or once every CRC or signaling multiframe when configured for E1 operation). The IMFPCFG[1:0] bits select whether IFP[x] indicates E1 CRC, signaling or both CRC and signaling multiframe boundaries. If ALTIFP=1, IFP[x] pulses on every second frame or the multiframe boundary.

Figure 73: T1 Ingress Interface Clock Master: NxChannel Mode

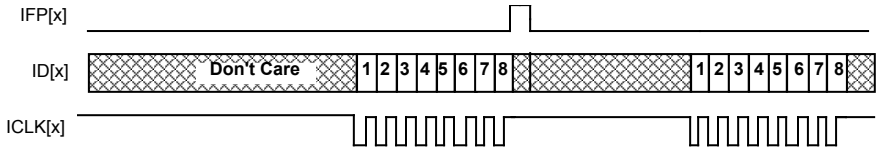
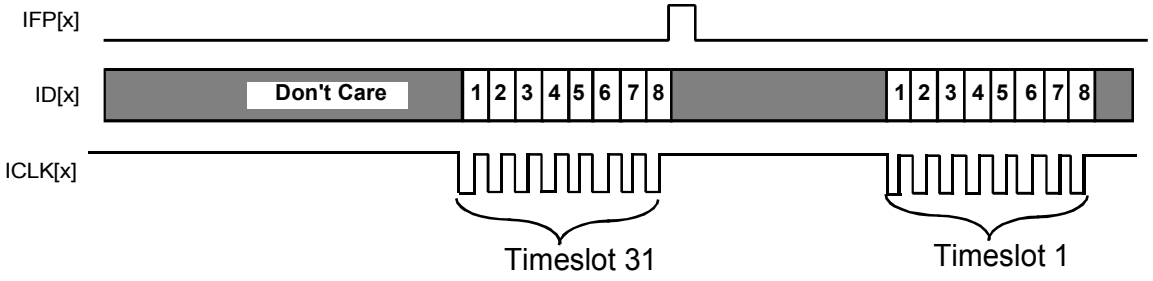
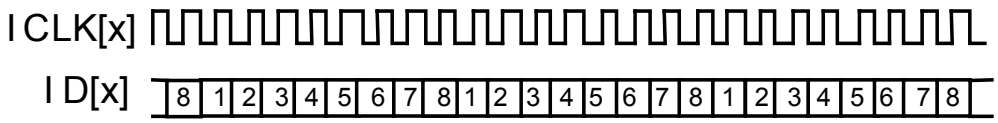


Figure 74: E1 Ingress Interface Clock Master: NxChannel Mode



The IMODE[1:0] bits in the T1/E1 Ingress Serial Interface Mode Select register are programmed to select NxChannel mode. The RPSC ingress control bytes are programmed to extract the desired channels. In Figure 73, the ingress control bytes for T1 channels 2 and 24 are extracted. In Figure 74, the ingress control bytes for E1 channels 31 and 1 are extracted. ICLK[x] is gapped so that it is only active for those channels with the associated DTRKC bit set to 0. If either IMFP or ALTIFP is set, then IFP[x] will pulse only during the appropriate frames. When the IDE bit in the T1/E1 Serial Interface Configuration register bit is set, then ID[x] is updated on the rising edge of ICLK[x] and the functional timing is described by with ICLK[x] inverted.

Figure 75: T1 and E1 Ingress Interface Clock Master: Clear Channel Mode



The Ingress Interface is configured for the Clock Slave: Clear Channel mode by writing to IMODE[1:0] in the T1/E1 Ingress Serial Interface Mode Select register. ID[x] is updated on the falling edge of the ICLK[x] input. When the IDE bit in the T1/E1 Serial Interface Configuration register is set to logic 1, then ID[x] is updated on the rising edge of ICLK[x], and the functional timing is described by Figure 75 with the ICLK[x] signal inverted.

Figure 76: T1 Ingress Interface Clock Slave: External Signaling Mode

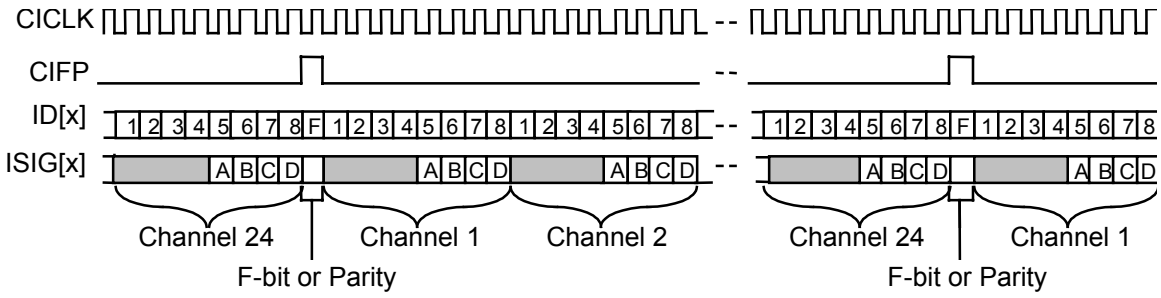
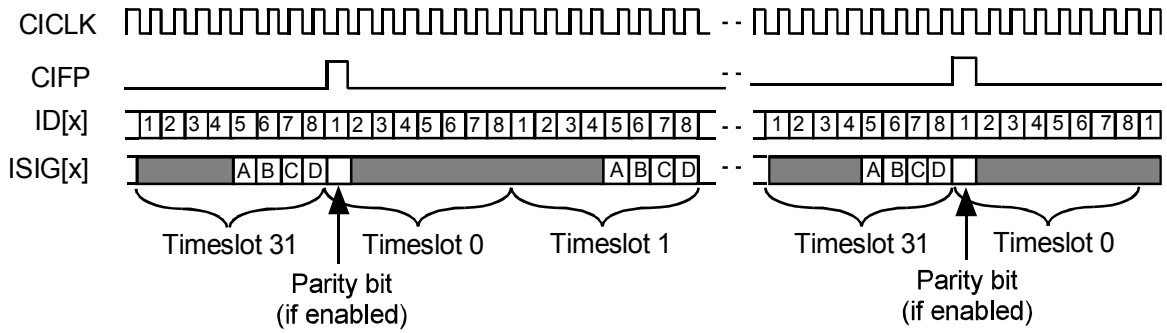
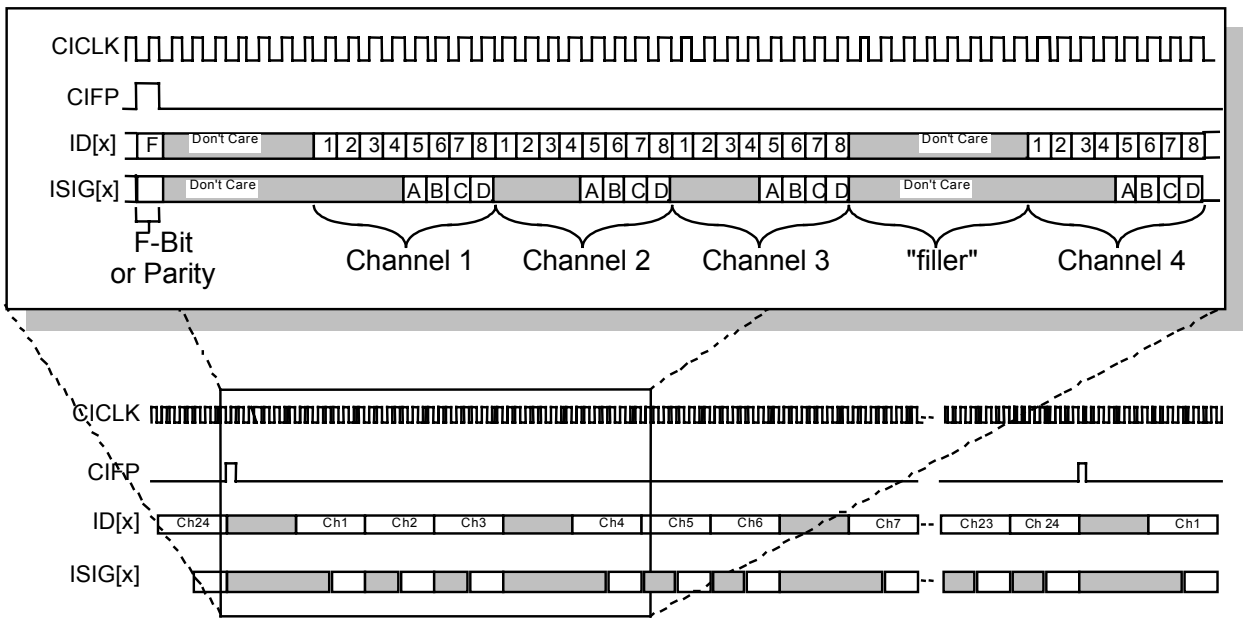


Figure 77: E1 Ingress Interface Clock Slave: External Signaling Mode



The Ingress Interface is programmed for Clock Slave mode by setting the IMODE[1:0] bits in the T1/E1 Ingress Serial Interface Mode Select register. ID[x] is timed to the active edge of CICLK, and is frame-aligned to CIFP. CIFP need not be provided every frame. ID[x] and ISIG[x] may be configured to carry a parity bit during the first bit of each frame. In External Signaling Mode, ISIG[x] is active and is aligned as shown.

Figure 78: T1 Ingress Interface 2.048 MHz Clock Slave: External Signaling Mode



The Ingress Interface is programmed for Clock Slave mode by setting the IMODE[1:0] in the T1/E1 Ingress Serial Interface Mode Select register. The 2.048 MHz internally-gapped clock mode is selected by setting the CICLK2M bit to logic 1 in the Master Ingress Slave Mode Serial Interface Configuration register. ID[x] is timed to the active edge of CICLK, and is frame-aligned to CIFP. CIFP need not be provided every frame. ID[x] and ISIG[x] may be configured to carry a parity bit during the first bit of each frame. The values of the filler bits will depend on the exact configuration of the TECT3, and they will be included in the parity calculation.

14 ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 28: Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Ambient Temperature under Bias		-40 to +85	°C
Storage Temperature	T_{ST}	-40 to +125	°C
Supply Voltage	$V_{DD2.5}$	-0.3 to + 3.5	V_{DC}
Supply Voltage	$V_{DD3.3}$	-0.3 to + 4.6	V_{DC}
Supply Voltage	V_{DDQ}	-0.3 to + 4.6	V_{DC}
Voltage on Any Pin (note 3)	V_{IN}	-0.3 to + 5.5	V_{DC}
Static Discharge Voltage		±1000	V
Latch-Up Current		±100	mA
DC Input Current	I_{IN}	±20	mA
Lead Temperature		+230	°C
Junction Temperature	T_J	+150	°C

Notes on Power Supplies:

1. VDD3.3 and VDDQ should power up before VDD2.5.
2. VDD3.3 and VDDQ should not be allowed to drop below the VDD2.5 voltage level except when VDD2.5 is not powered.
3. All pins on the TECT3 are 5V tolerant.

15 D.C. CHARACTERISTICS

T_A = -40°C to +85°C, $V_{DD3.3}$ = 3.3V ±10%, $V_{DD2.5}$ = 2.5V ±8% (Typical Conditions: T_A = 25°C, $V_{DD3.3}$ = 3.3V, V_{DDQ} = 3.3V, $V_{DD2.5}$ = 2.5V)

Table 29: D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDD3.3	Power Supply	2.97	3.3	3.63	Volts	
VDDQ	Power Supply	2.97	3.3	3.63	Volts	
VDD2.5	Power Supply	2.3	2.5	2.7	Volts	
VIL	Input Low Voltage	-0.5		0.6	Volts	Guaranteed Input LOW Voltage
VIH	Input High Voltage	2.0		5.5	Volts	Guaranteed Input HIGH Voltage
VOL	Output or Bidirectional Low Voltage			0.4	Volts	VDD = min, IOL = -4mA for D[7:0], LAOE, RECVCLK1, RECVCLK2, MVID[7:0], CASID[7:0], CCSID, TCLK, TPOS/TDAT, TNEG/TMFP, RGAPCLK/RSCLK, RDATAO, RFPO/RMFPO, ROVRHD, TFPO/TMFPO/TGAPCLK, SBIACT, IOL = -8mA for SDDATA[7:0], SDDP, SDPL, SDV5, SAJUST_REQ, SC1FP, IOL = -2mA for others. Note 3
VOH	Output or Bidirectional High Voltage	2.4			Volts	VDD = min, IOH = 4mA for D[7:0], LAOE, RECVCLK1, RECVCLK2, MVID[7:0], CASID[7:0], CCSID, TCLK, TPOS/TDAT, TNEG/TMFP, RGAPCLK/RSCLK, RDATAO, RFPO/RMFPO, ROVRHD, TFPO/TMFPO/TGAPCLK, SBIACT, IOH = 8mA for SDDATA[7:0], SDDP, SDPL, SDV5, SAJUST_REQ, SC1FP, IOH = 2mA for others. Note 3

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VT+	Reset Input High Voltage	2.0		5.5	Volts	TTL Schmidt
VT-	Reset Input Low Voltage	-0.2		0.6	Volts	
VTH	Reset Input Hysteresis Voltage	1.2	0.5		Volts	
IILPU	Input Low Current	+10		+100	µA	VIL = GND. Notes 1, 3,4
IIHPU	Input High Current	-10		+10	µA	VIH = VDD. Notes 1, 3
IIL	Input Low Current	-10		+10	µA	VIL = GND. Notes 2, 3
IIH	Input High Current	-10		+10	µA	VIH = VDD. Notes 2, 3
CIN	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
COUT	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
CIO	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
IDDOP1	Operating Current		 30	270	mA mA	VDD2.5 = 2.7V VDD3.3 = 3.63 V Outputs Unloaded, DS3 to M13 multiplexing, SBI backplane with H-MVIP CAS mode.

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Typical values are given as a design aid. The product is not tested to the typical values given in the data sheet.

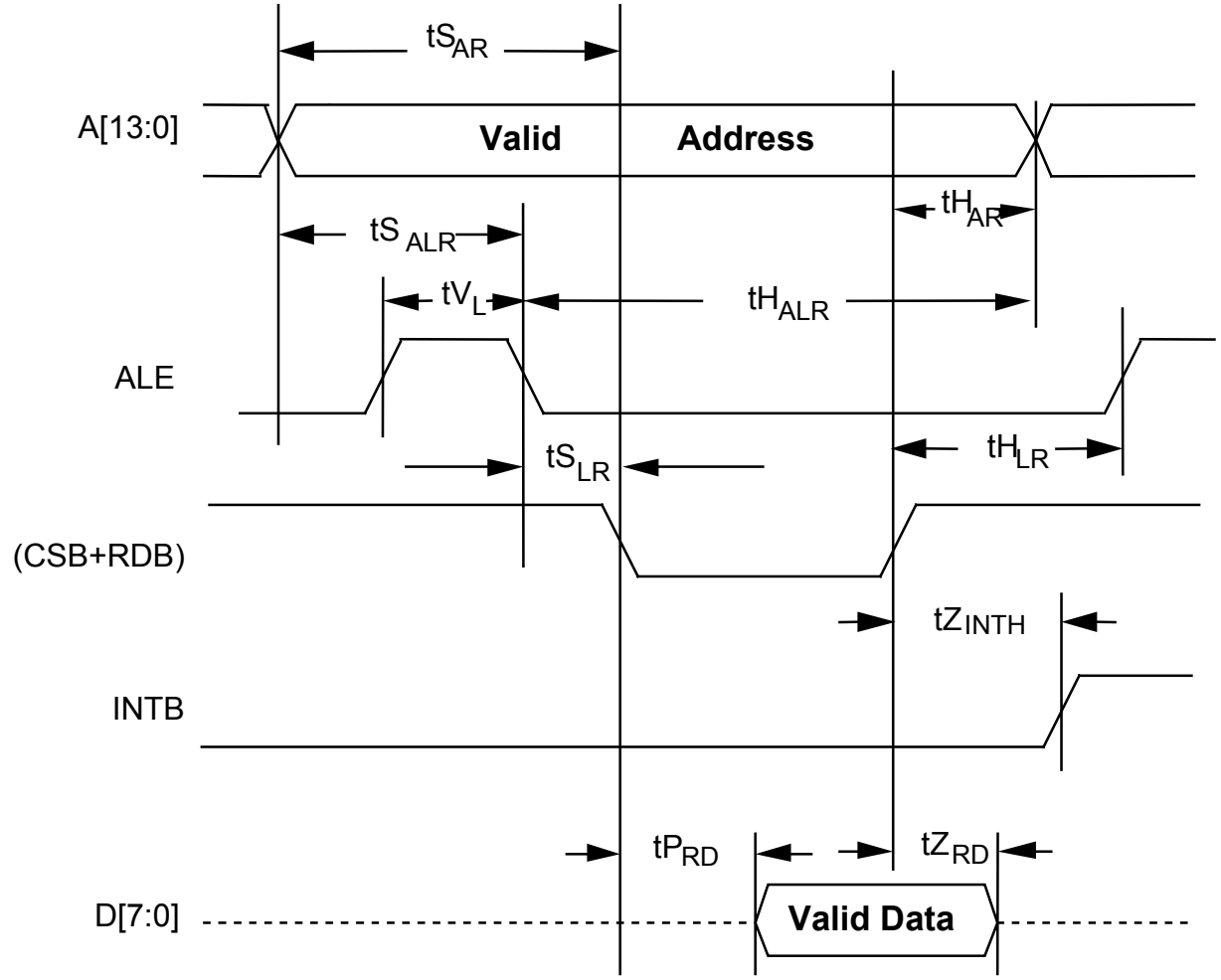
16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, $V_{DD3.3}$ = 3.3V ±10%, $V_{DD2.5}$ = 2.5V ±8%)

Table 30: Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
tSAR	Address to Valid Read Set-up Time	10		ns
tHAR	Address to Valid Read Hold Time	5		ns
tSALR	Address to Latch Set-up Time	10		ns
tHALR	Address to Latch Hold Time	10		ns
tVL	Valid Latch Pulse Width	20		ns
tSLR	Latch to Read Set-up	0		ns
tHLR	Latch to Read Hold	5		ns
tPRD	Valid Read to Valid Data Propagation Delay		40	ns
tZRD	Valid Read Negated to Output Tri-state		20	ns
tZINTH	Valid Read Negated to Output Tri-state		50	ns

Figure 79: Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALR, tHALR, tVL, and tSLR are not applicable.

5. Parameter tHAR is not applicable if address latching is used.

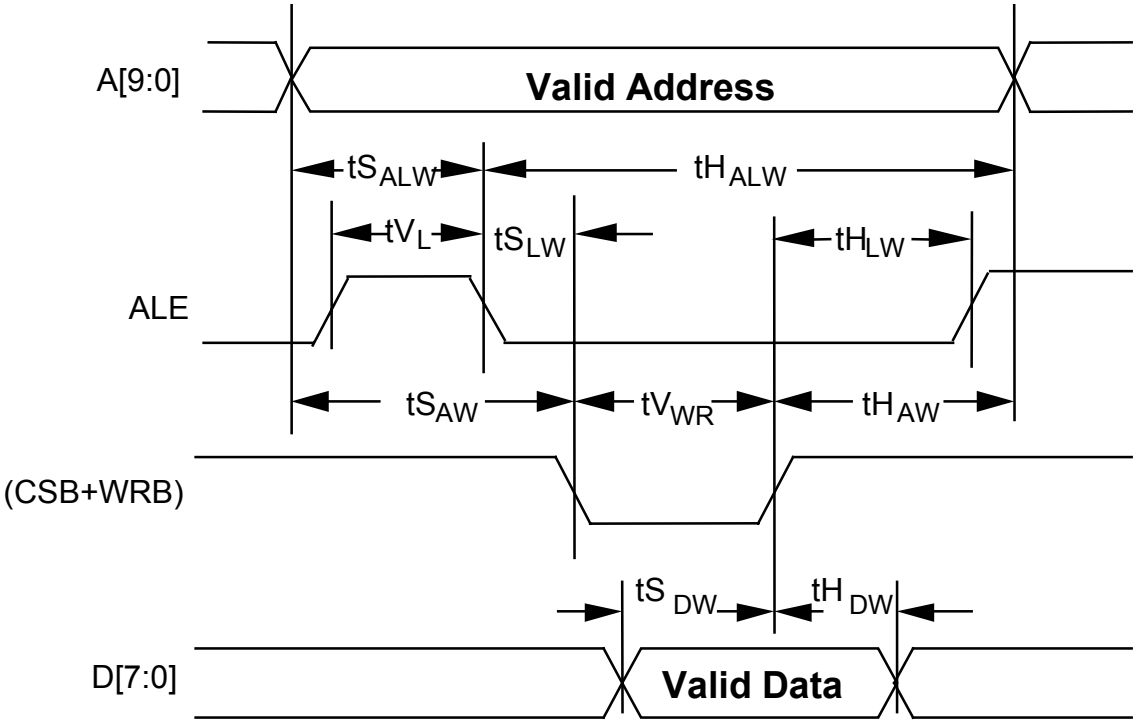
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 31: Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tSAW	Address to Valid Write Set-up Time	10		ns
tSDW	Data to Valid Write Set-up Time	20		ns
tSALW	Address to Latch Set-up Time	10		ns
tHALW	Address to Latch Hold Time	10		ns
tVL	Valid Latch Pulse Width	20		ns
tSLW	Latch to Write Set-up	0		ns
tHLW	Latch to Write Hold	5		ns
tHDW	Data to Valid Write Hold Time	5		ns
tHAW	Address to Valid Write Hold Time	5		ns
TVWR	Valid Write Pulse Width	40		ns

Figure 80: Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALW, tHALW, tVL, tSLW and tHLW are not applicable.
3. Parameter tHAW is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

17 TECT3 TIMING CHARACTERISTICS

(T_A = -40°C to +85°C $V_{DD3.3}$ = 3.3V ±10%, $V_{DD2.5}$ = 2.5V ±8%)

Table 32: RTSB Timing

Symbol	Description	Min	Max	Units
tVRSTB	RSTB Pulse Width	100		ns

Figure 81: RSTB Timing

Table 33: DS3 Transmit Interface Timing

Symbol	Description	Min	Max	Units
f_{TICLK}	TICLK Frequency		52	MHz
$t0_{TICLK}$	TICLK minimum pulse width low	7.7		ns
$t1_{TICLK}$	TICLK minimum pulse width high	7.7		ns
tS_{TFPI}	TFPI/TMFPI to TICLK Set-up Time (LOOPT=0) TFPI/TMFPI to RCLK Set-up Time (LOOPT=1) (See Note 1)	5 5		ns
tH_{TFPI}	TFPI/TMFPI to TICLK Hold Time (LOOPT=0) TFPI/TMFPI to RCLK Hold Time (LOOPT=1) (See Note 2)	1 1		ns
TS_{TDATI}	TDATI to TICLK Set-up Time (LOOPT = 0) TDATI to RCLK Set-up Time (LOOPT = 1) (See Note 1)	5 5		ns
TH_{TDATI}	TDATI to TICLK Hold Time (LOOPT = 0) TDATI to RCLK Hold Time (LOOPT = 1)	1 1		ns

	(See Note 2)			
TP_{TFPO}	TICLK High to TPFO Prop Delay (See Note 3 and 4)	2	16	ns
TS_{TGAP}	TDATI to TGAPCLK Set-up Time (See Notes 1 and 5)	3		ns
TH_{TGAP}	TDATI to TGAPCLK Hold Time (See Note 2 and 5)	2		ns
TP_{TCLK}	TICLK Edge to TCLK Edge Prop Delay (See Notes 3 and 4)	2	13	ns
TP_{TPOS}	TCLK Edge to TPOS/TDAT Prop Delay (See Notes 3 and 4)	-1	5	ns
TP_{TNEG}	TCLK Edge to TNEG/TMFP Prop Delay (See Notes 3 and 4)	-1	5	ns
tP_{TPOS2}	TICLK High to TPOS/TDAT Prop Delay (See Notes 3 and 4)	2	13	ns
TP_{TNEG2}	TICLK High to TNEG/TMFP Prop Delay (See Notes 3 and 4)	2	13	ns

Notes on DS3 Transmit Interface Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

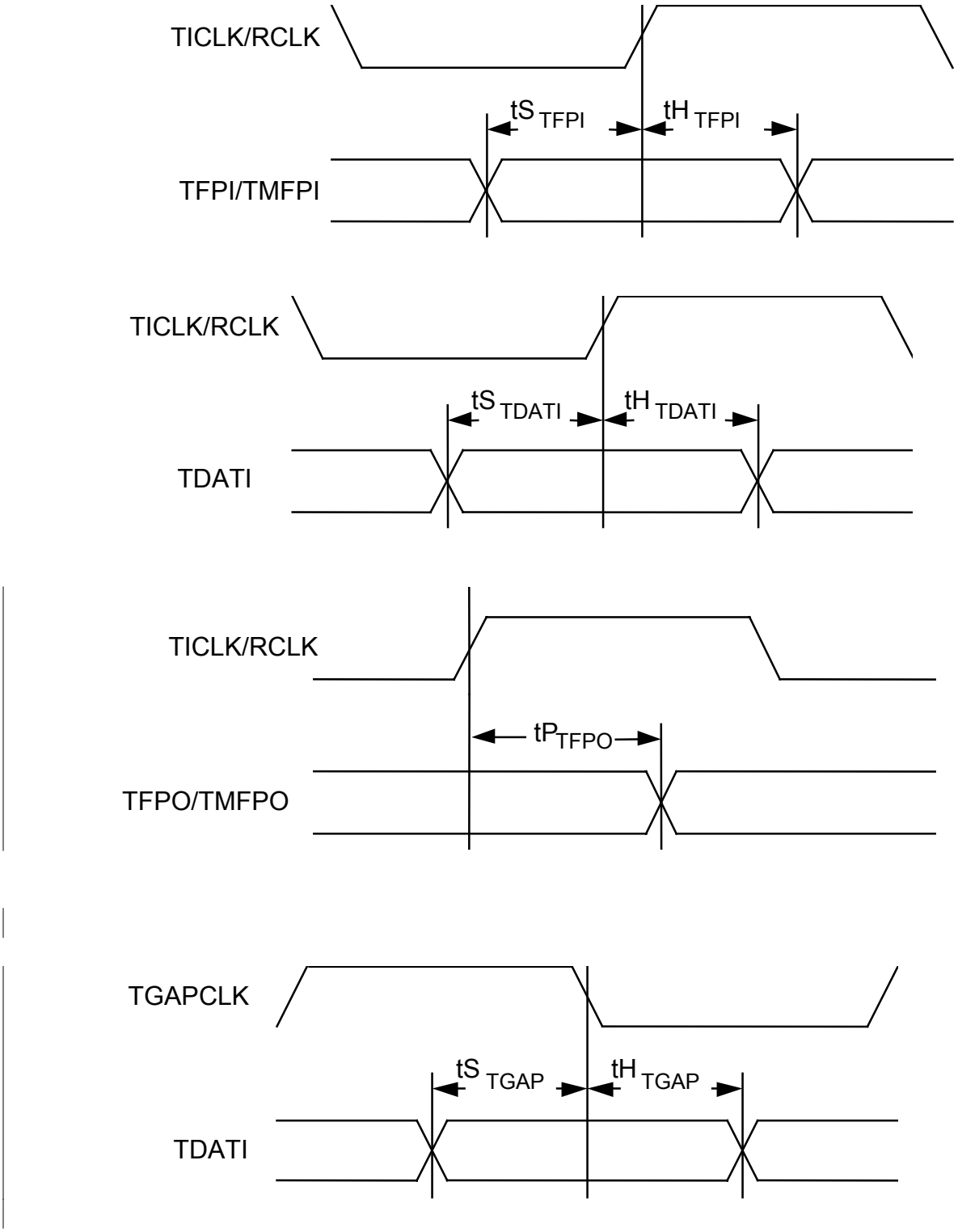
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

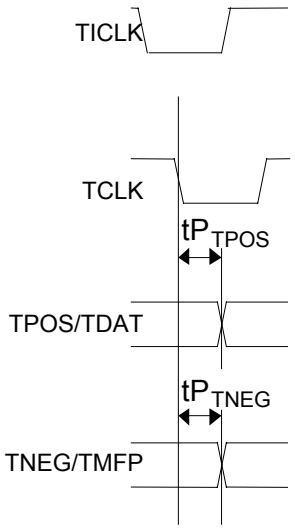
4. Maximum and minimum output propagation delays are measured with a 20 pF load on all the outputs.

5. Setup and hold times relative to TGAPCLK are measured with a 20 pF load on aTGAPCLK.

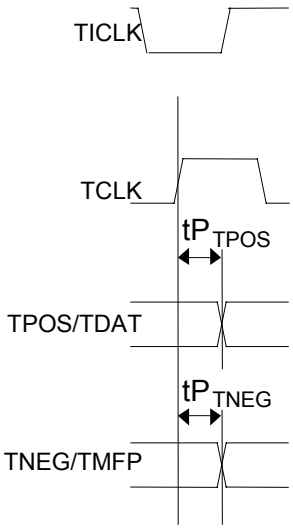
Figure 82: DS3 Transmit Interface Timing



TICLK=0, TRISE=0



TICLK=0, TRISE=1



TICLK=1, TRISE=X

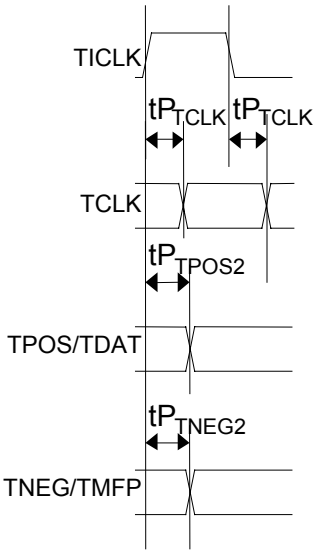


Table 34: DS3 Receive Interface Timing

Symbol	Description	Min	Max	Units
f_{RCLK}	RCLK Frequency		52	MHz
$t0_{RCLK}$	RCLK minimum pulse width low	7.7		ns
$t1_{RCLK}$	RCLK minimum pulse width high	7.7		ns
tS_{RPOS}	RPOS/RDAT Set-up Time (See Note 1)	4		ns
tH_{RPOS}	RPOS/RDAT Hold Time (See Note 2)	1		ns
tS_{RNEG}	RNEG/RLCV Set-Up Time (See Note 1)	4		ns
tH_{RNEG}	RNEG/RLCV Hold Time (See Note 2)	1		ns
tP_{RDATO}	RSCLK Edge to RDATO Prop Delay (See Notes 3 and 4)	2	12	ns
tP_{RFPO}	RSCLK Edge to RFPO/RMFPO Prop Delay (See Notes 3 and 4)	2	12	ns
tP_{ROVRHD}	RSCLK Edge to ROVRHD Prop Delay (See Notes 3 and 4)	2	12	ns
tP_{RGAP}	RGAPCLK Edge to RDATO[x] Prop Delay (See Notes 3 and 4)	3	11	ns

Notes on DS3 Transmit Interface Timing:

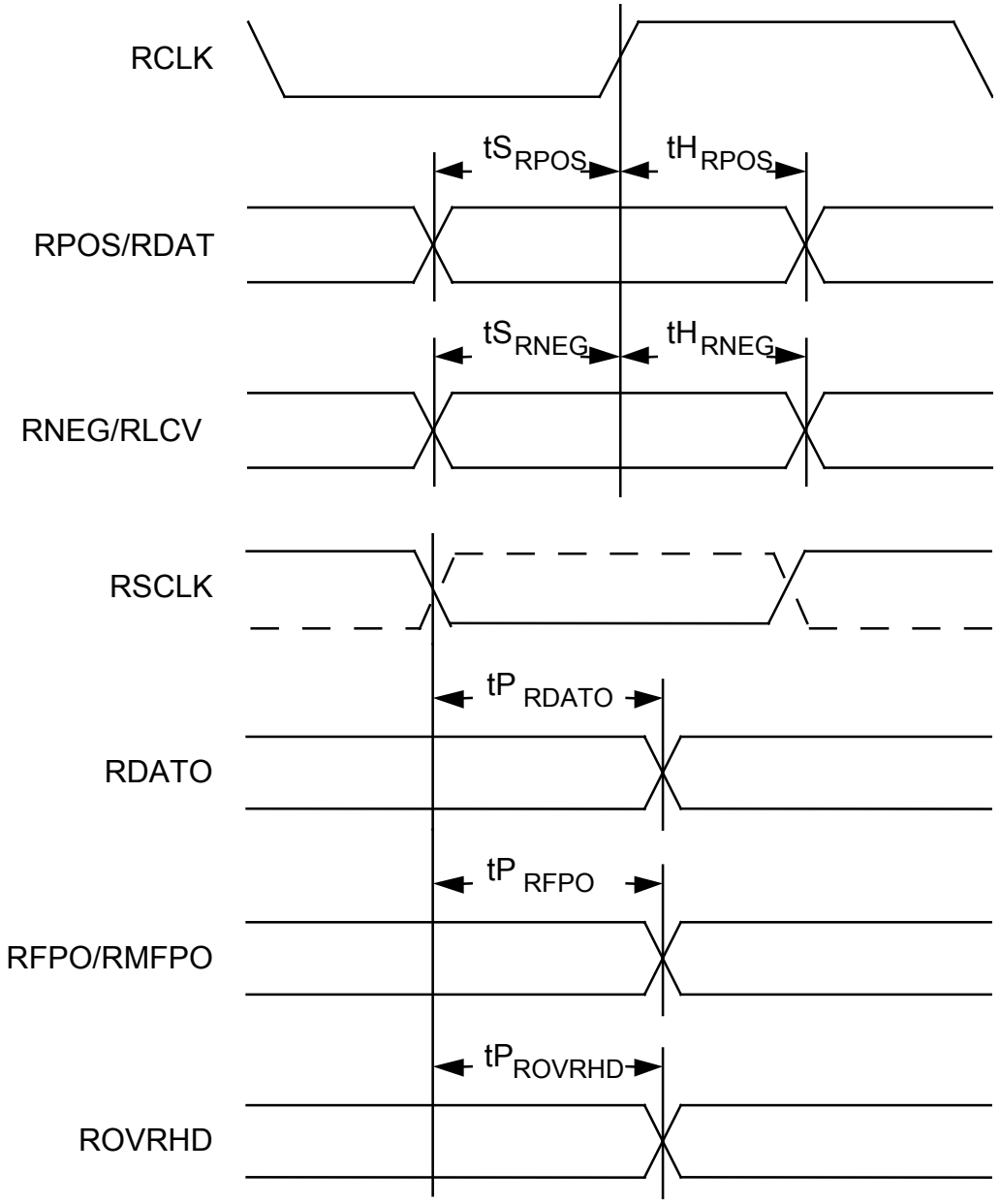
1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

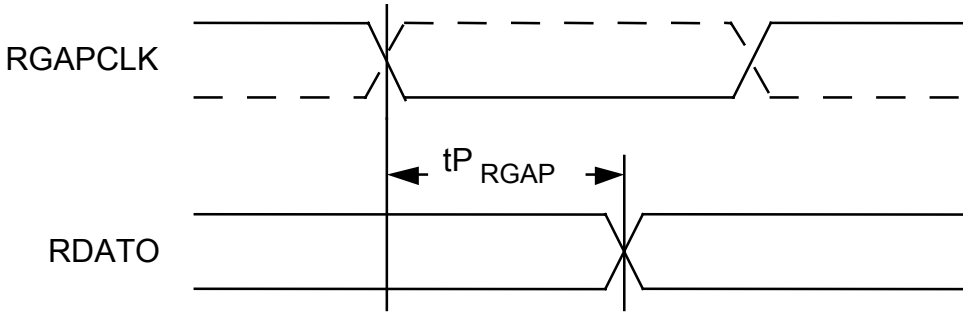
3. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

4. Maximum and minimum output propagation delays are measured with a 50 pF load on all the outputs.

Figure 83: DS3 Receive Interface Timing



Dashed line RSCLK represents behaviour when RSCLKR register bit = 1.



Dashed line RSCLK represents behaviour
when RSCLKR register bit = 1.

Table 35: SBI ADD BUS Timing (Figure 84)

Symbol	Description	Min	Max	Units
	SREFCLK Frequency	19.44 -50 ppm	19.44 +50 ppm	MHz
	SREFCLK Duty Cycle	40	60	%
tS_{SBIADD}	All SBI ADD BUS Inputs Set-Up Time to SREFCLK (See Note 1)	4		ns
tH_{SBIADD}	All SBI ADD BUS Inputs Hold Time to SREFCLK (See Note 2)	0.75		ns
tP_{SBIADD}	SREFCLK to SAJUST_REQ Valid (See Notes 3 and 4)	2	20	ns
tZ_{SBIADD}	SREFCLK to SAJUST_REQ Tristate (See Note 5)	2	20	ns

Notes on SBI Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

4. Maximum and minimum output propagation delays are measured with a 100 pF load on all the outputs.

5. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to the point where the total current delivered through the output is less than or equal to the leakage current.

Figure 84: SBI ADD BUS Timing

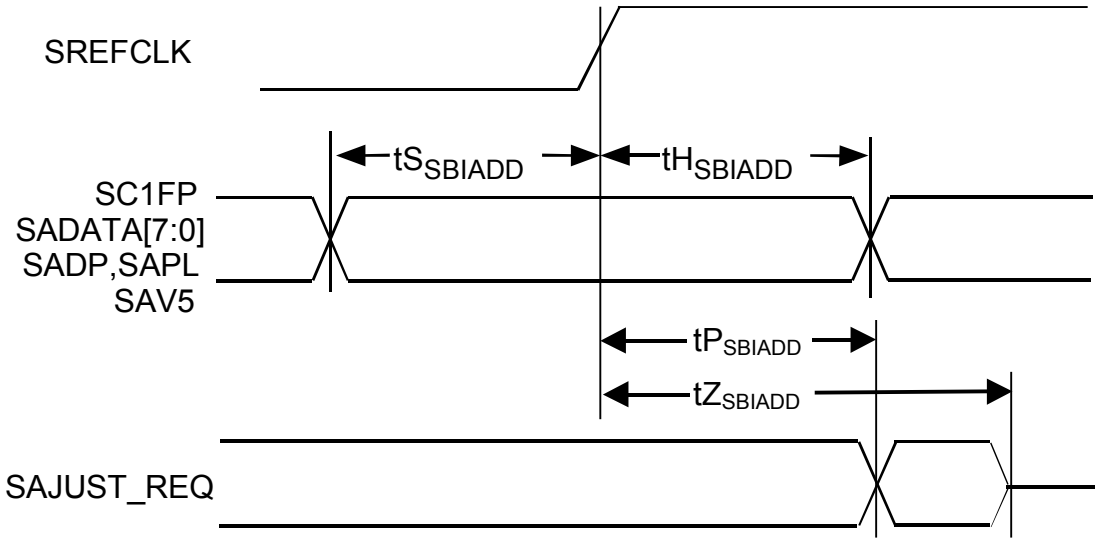


Table 36: SBI DROP BUS Timing (Figure 85 to Figure 86)

Symbol	Description	Min	Max	Units
$tP_{SBIDROP}$	SREFCLK to SBI DROP BUS Outputs Valid (See Notes 1 and 2)	2	20	ns
tP_{SBIACT}	SREFCLK to SBIACT Output Valid (See Notes 1 and 3)	2	19	ns
$tZ_{SBIDROP}$	SREFCLK to All SBI DROP BUS Outputs Tristate (See Note 4)	2	12	ns
TP_{OUTEN}	SBIDET[1] and SBIDET[0] low to All SBI DROP BUS Outputs Valid (See Notes 1 and 2)	2	15	ns
tZ_{OUTEN}	SBIDET[1] and SBIDET[0] high to All SBI DROP BUS Outputs Tristate (See Note 4)	2	12	ns
tS_{DET}	SBIDET[n] Set-Up Time to SREFCLK (See Notes 5)	4		ns
tH_{DET}	SBIDET[n] Hold Time to SREFCLK (See Notes 6)	0		ns

Notes on SBI Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum and minimum output propagation delays are measured with a 100 pF load on all the outputs.

3. Maximum and minimum output propagation delay is measured with a 50pF load.

4. Output tristate delay is the time in nanoseconds from the 1.4 Volt point of the reference signal to the point where the total current delivered through the output is less than or equal to the leakage current.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Figure 85: SBI DROP BUS Timing

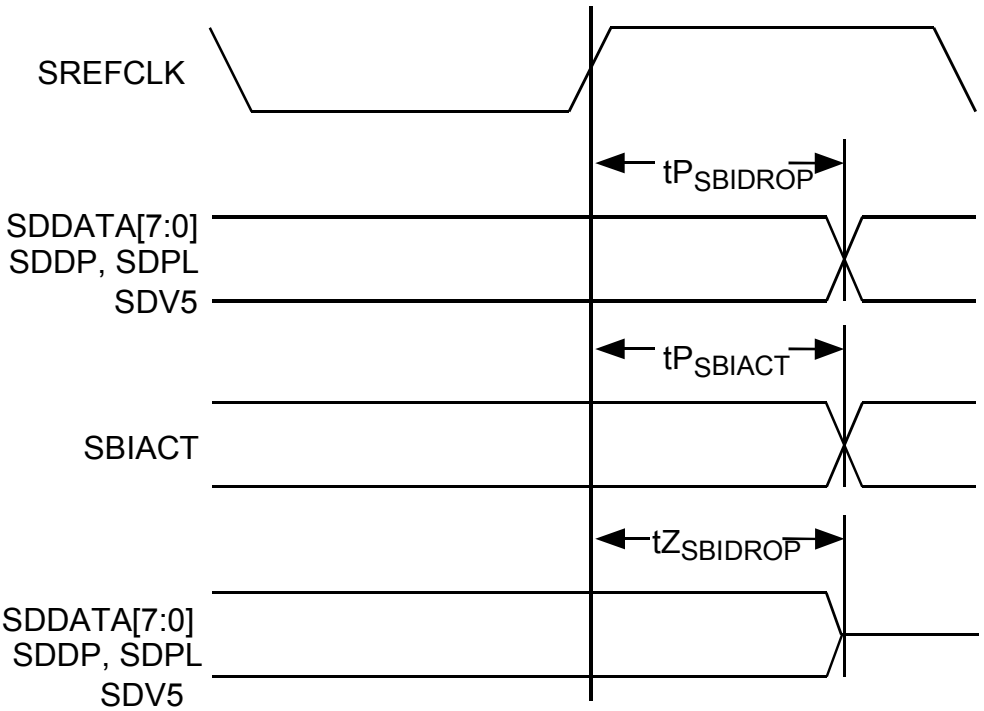


Figure 86: SBI DROP BUS Collision Avoidance Timing

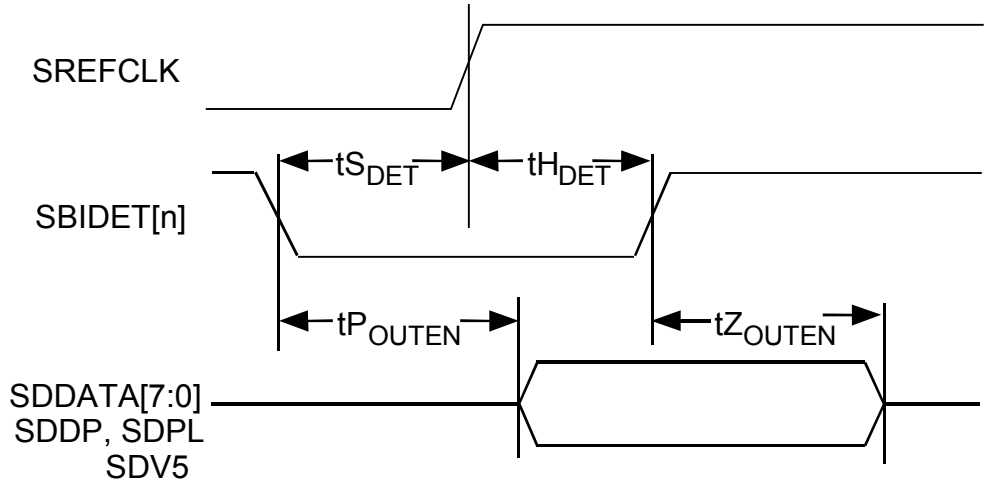


Table 37: H-MVIP Egress Timing (Figure 87)

Symbol	Description	Min	Max	Units
	CMV8MCLK Frequency (See Note 3)	16.368	16.400	MHz
	CMV8MCLK Duty Cycle	40	60	%
	CMVFPC Frequency (See Note 4)	4.092	4.100	MHz
	CMVFPC Duty Cycle	40	60	%
tP_{MVC}	CMV8MCLK to CMVFPC skew	-10	10	ns
TS_{HMVED}	MVED[7:1], CASED[7:1], CCSED Set-Up Time	5		ns
tH_{HMVED}	MVED[7:1], CASED[7:1], CCSED Hold Time	5		ns
TS_{MVFPB}	CMVFPB Set-Up Time (See Note 1)	5		ns
TH_{MVFPB}	CMVFPB Hold Time (See Note 2)	5		ns

Notes on H-MVIP Egress Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

3. Measured between any two CMV8MCLK falling edges.

4. Measured between any two CMVFPC falling edges.

Figure 87: H-MVIP Egress Data & Frame Pulse Timing

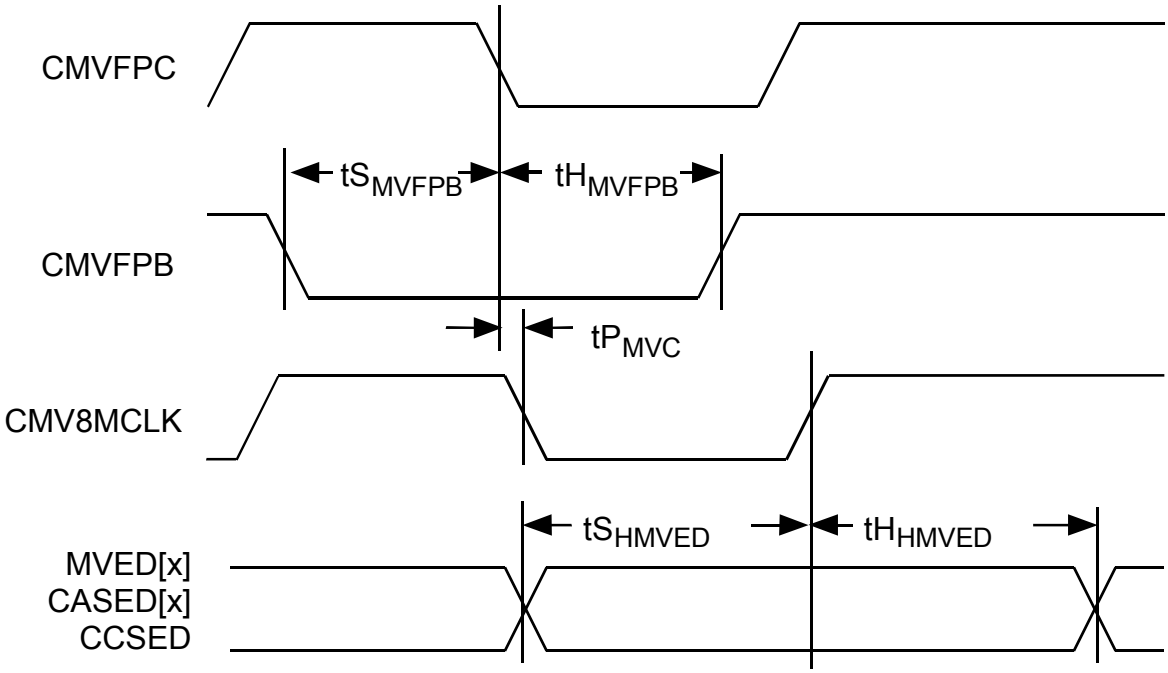


Table 38: H-MVIP Ingress Timing (Figure 88)

Symbol	Description	Min	Max	Units
tP_{HMVID}	CMV8MCLK Low to MVID[7:1], CASID[7:1], CCSID Valid (See Notes 1 and 2)	5	25	ns

Notes on H-MVIP Ingress Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum and minimum output propagation delays are measured with a 50 pF load on all the outputs.

Figure 88: H-MVIP Ingress Data Timing

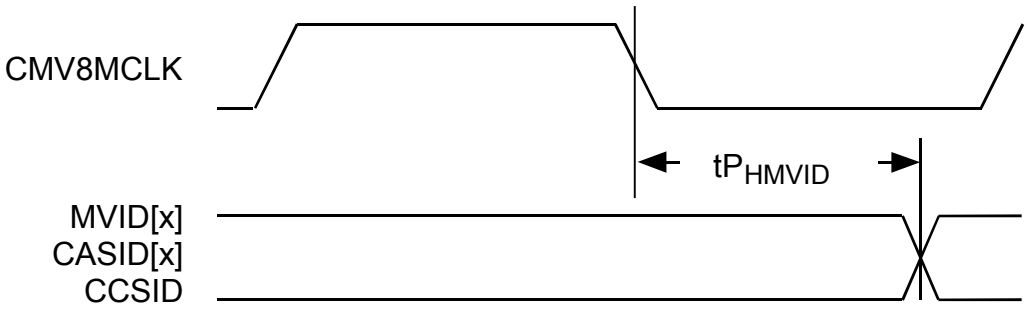


Table 39: XCLK Input (Figure 89)

Symbol	Description	Min	Max	Units
t_{LXCLK}	XCLK Low Pulse Width[4]	8		ns
t_{HXCLK}	XCLK High Pulse Width[4]	8		ns
t_{XCLK}	XCLK Period (typically 1/37.056 MHz ± 32 ppm for T1 operation or 1/49.152 MHz for E1 operation)[5]	20		ns

Figure 89: XCLK Input Timing

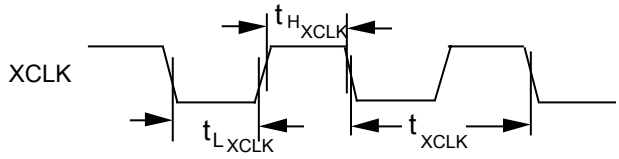


Table 40: Egress Interface Timing - Clock Slave: EFP Enabled Mode (Figure 90)

Symbol	Description	Min	Max	Units
	Common Egress Clock Frequency[1,2](Typically 1.544 MHz ± 130 ppm or 2.048 MHz ± 130 ppm for T1 modes and 2.048 MHz ±50ppm for E1 modes)	1.5	2.1	MHz
$t1_{CECLK}$	Common Egress High Pulse Width[2,4] (XCLK = 37.056 MHz)	167		ns
$t0_{CECLK}$	Common Egress Low Pulse Width[2,4] (XCLK = 37.056 MHz)	167		ns
$t1_{CECLK}$	Common Egress High Pulse Width[2,4] (XCLK = 49.152 MHz)	145		ns
$t0_{CECLK}$	Common Egress Low Pulse Width[2,4] (XCLK = 49.152 MHz)	145		ns
tS_{CECLK}	CECLK to Input Set-up Time[7,9]	20		ns
tH_{CECLK}	CECLK to Input Hold Time[8,9]	20		ns
tP_{EFP1}	CECLK to EFP[x] Propagation delay[9,10,11]	5	100	ns

Figure 90: Egress Interface Timing - Clock Slave: EFP Enabled Mode

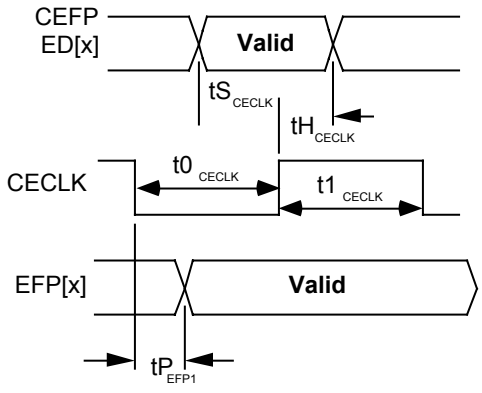


Table 41: Egress Interface Timing - Clock Slave: External Signaling (Figure 91)

Symbol	Description	Min	Max	Units
	Common Egress Clock Frequency[1,2](Typically 1.544 MHz ± 130 ppm or 2.048 MHz ± 130 ppm for T1 modes and 2.048 MHz ±50ppm for E1 modes)	1.5	2.1	MHz
$t1_{CECLK}$	Common Egress High Pulse Width[2,4] (XCLK = 37.056 MHz)	167		ns
$t0_{CECLK}$	Common Egress Low Pulse Width[2,4] (XCLK = 37.056 MHz)	167		ns
$t1_{CECLK}$	Common Egress High Pulse Width[2,4] (XCLK = 49.152 MHz)	145		ns
$t0_{CECLK}$	Common Egress Low Pulse Width[2,4] (XCLK = 49.152 MHz)	145		ns
tS_{CECLK}	CECLK to Input Set-up Time[7,9]	20		ns
tH_{CECLK}	CECLK to Input Hold Time[8,9]	20		ns

Figure 91: Egress Interface Timing - Clock Slave: External Signaling Mode

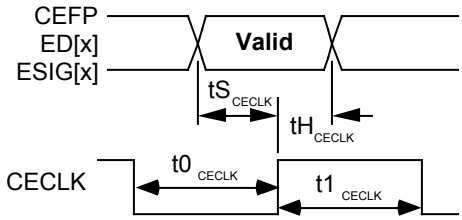


Table 42: Egress Interface Input Timing - Clock Master : NxChannel Mode (Figure 92)

Symbol	Description	Min	Max	Units
tSECLK	ECLK[x] to ED[x] Set-up Time[7,9]	30		ns
tHECLK	ECLK[x] to ED[x] Hold Time[8,9]	30		ns

Figure 92: Egress Interface Input Timing - Clock Master : NxChannel Mode

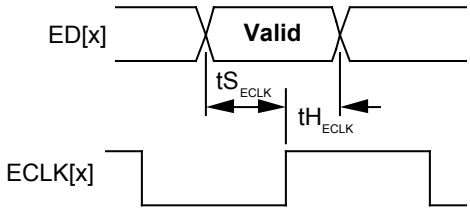
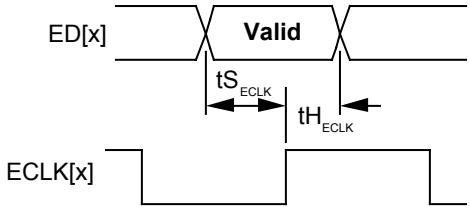


Table 43: Egress Interface Input Timing - Clock Master : Clear Channel Mode (Figure 92)

Symbol	Description	Min	Max	Units
tSECLK	ECLK[x] to ED[x] Set-up Time[7,9]	30		ns
tHECLK	ECLK[x] to ED[x] Hold Time[8,9]	30		ns

Figure 93: Egress Interface Input Timing - Clock Master : Clear Channel Mode

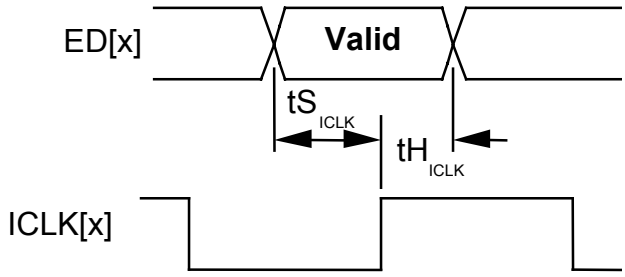


Note: ECLK[x] is an output derived from CECLK or CTCLK.

Table 44: Egress Interface Input Timing - Clock Master : Serial Data and H-MVIP CCS Mode (Figure 92)

Symbol	Description	Min	Max	Units
tSICLK	ICLK[x] to ED[x] Set-up Time[7,9]	30		ns
tHICLK	ICLK[x] to ED[x] Hold Time[8,9]	30		ns

Figure 94: Egress Interface Input Timing - Clock Master : Serial Data and H-MVIP CCS Mode

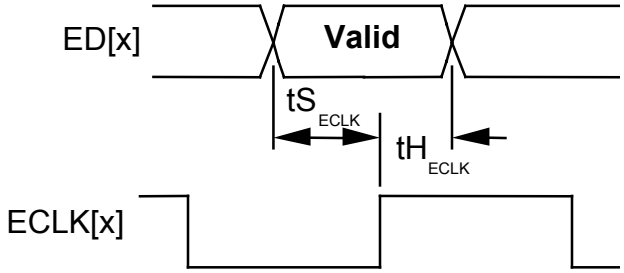


Note: ICLK[x] is an output derived from CMV8MCLK.

Table 45: Egress Interface Input Timing - Clock Slave : Clear Channel Mode (Figure 92)

Symbol	Description	Min	Max	Units
tSECLK	ECLK[x] to ED[x] Set-up Time[7,9]	30		ns
tHECLK	ECLK[x] to ED[x] Hold Time[8,9]	30		ns

Figure 95: Egress Interface Input Timing - Clock Slave : Clear Channel Mode



Note: ECLK[x] is an input.

Table 46: Ingress Interface Timing - Clock Slave Modes (Figure 96)

Symbol	Description	Min	Max	Units
	Common Ingress Clock Frequency[1,2] (Typically 1.544 MHz ± 130 ppm or 2.048 MHz ± 130 ppm for T1 modes and 2.048 MHz ±50ppm for E1 modes)	1.5	2.1	MHz
$t1_{CICLK}$	Common Ingress High Pulse Width[2,4] (XCLK = 37.056 MHz)	167		ns
$t0_{CICLK}$	Common Ingress Low Pulse Width[2,4] (XCLK = 37.056 MHz)	167		ns
$t1_{CICLK}$	Common Ingress High Pulse Width[2,4] (XCLK = 49.152 MHz)	145		ns
$t0_{CICLK}$	Common Ingress Low Pulse Width[2,4] (XCLK = 49.152 MHz)	145		ns
tSCICLK	CICLK to CIFP Set-up Time[7,9]	20		ns
tHCICLK	CICLK to CIFP Hold Time[8,9]	20		ns
tPCICLK	CICLK to Ingress Output Prop. Delay[9,10,11]	5	100	ns

Figure 96: Ingress Interface Timing - Clock Slave Modes

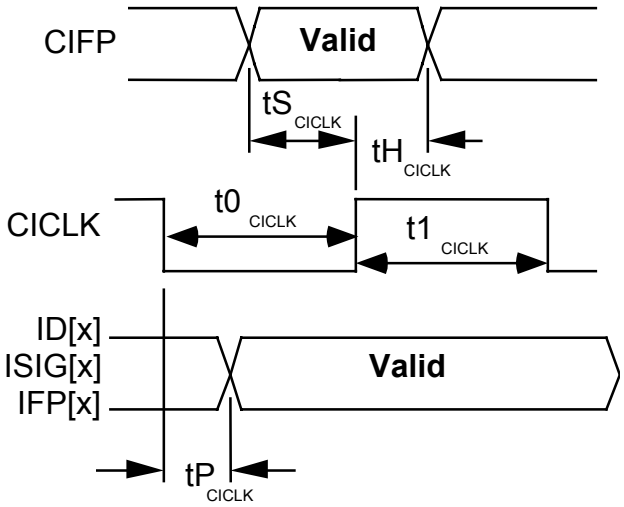


Table 47: Ingress Interface Timing - Clock Master Modes (Figure 97)

Symbol	Description	Min	Max	Units
tP_{ICLK}	ICLK[x] to Ingress Output Prop. Delay[9,10,11]	-20	20	ns

Figure 97: Ingress Interface Timing - Clock Master Modes

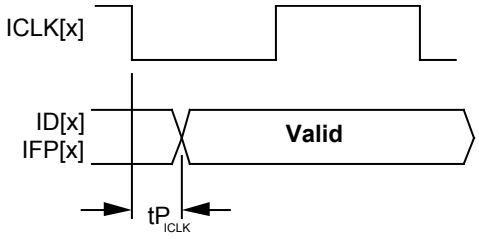
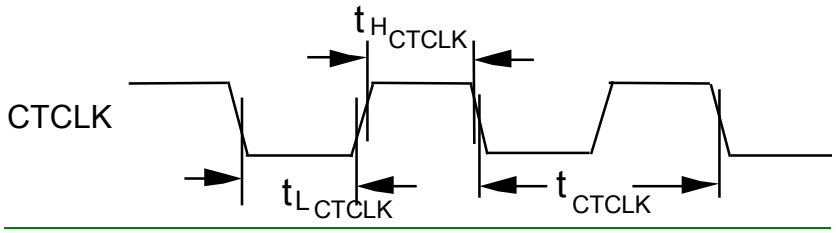


Table 48: Transmit Line Interface Timing (Figure 98)

Symbol	Description	Min	Max	Units
	CTCLK Frequency (when used for TJAT REF), typically 1.544 MHz± 130 ppm for T1 operation or 2.048 MHz± 50 ppm for E1 operation[2,3,6]	1.5	2.1	MHz
t_{HCTCLK}	CTCLK High Duration[4] (when used for TJAT REF)	100		ns
t_{LCTCLK}	CTCLK Low Duration[4] (when used for TJAT REF)	100		ns

Figure 98: Transmit Line Interface Timing



Notes on Ingress and Egress Serial Interface Timing:

1. CECLK and CICLK can be gapped and/or jittered clock signals subject to the minimum high and low times shown. These specifications correspond to nominal XCLK input frequencies.

2. Guaranteed by design for nominal XCLK input frequency (37.056 MHz ±100 ppm for T1 modes and 49.152 MHz ±50ppm for E1 modes).

3. CTCLK can be a jittered clock signal subject to the minimum high and low times shown. These specifications correspond to nominal XCLK input frequency of 37.056 MHz ±100 ppm for T1 modes and 49.152 MHz ±50ppm for E1 modes.

4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

5. XCLK frequency must be 24x the line rate ±32 ppm when TJAT is free-running or referenced to a derivative of XCLK. XCLK may be ± 100 ppm if an accurate reference is provided to TJAT.

6. CTCLK can be a jittered clock signal subject to the minimum high and low durations tHCTCLK, tLCTCLK. These durations correspond to nominal XCLK input frequency.

7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

9. Setup, hold, and propagation delay specifications are shown relative to the default active clock edge, but are equally valid when the opposite edge is selected as the active edge.

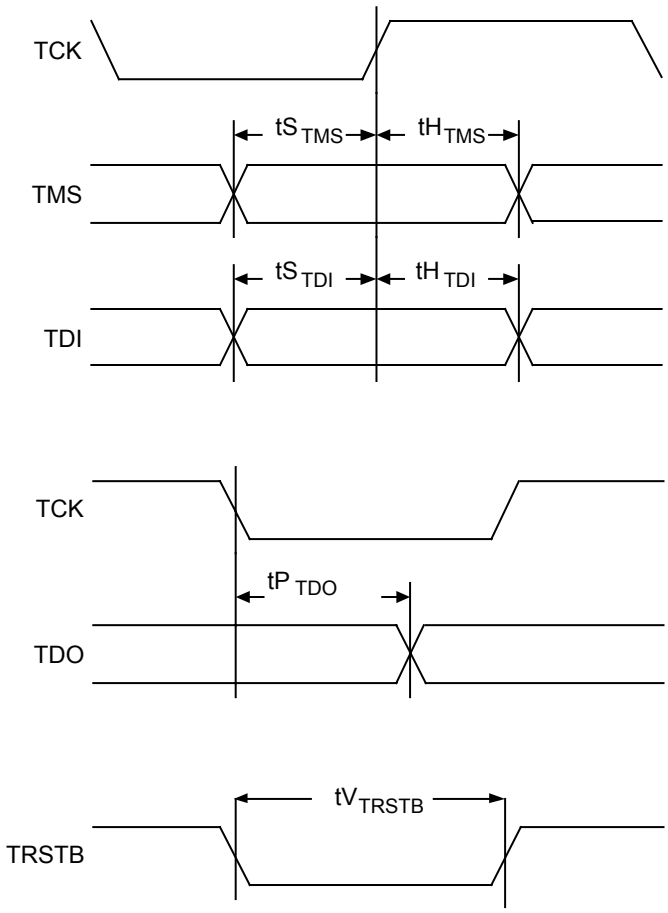
10. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

11. Output propagation delays are measured with a 50 pF load on all outputs with the exception of the high speed DS3 outputs (TCLK, TPOS/TDAT, TNEG/TMFP). The TCLK, TPOS/TDAT, TNEG/TMFP output propagation delays are measured with a 20 pF load.

Table 49: JTAG Port Interface

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	100		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	100		ns
tP_{TDO}	TCK Low to TDO Valid	2	100	ns
tV_{TRSTB}	TRSTB Pulse Width	100		ns

Figure 99: JTAG Port Interface Timing



18 ORDERING AND THERMAL INFORMATION

Table 50: Ordering and Thermal Information

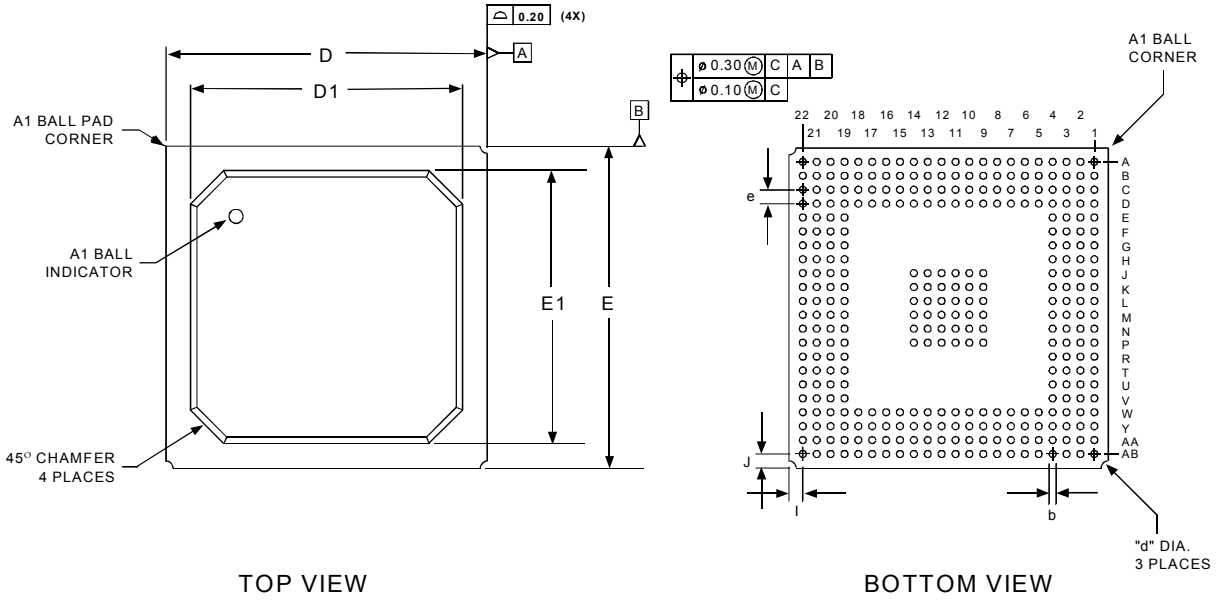
Part No.	Description
PM4328-PI	324 Plastic Ball Grid Array (PBGA)

Table 51: Thermal information – Theta Ja vs. Airflow

		Forced Air (Linear Feet per Minute)				
Theta JA (°C/W) @ specified power	Convection	100	200	300	400	500
Dense Board	35.3	31.0	27.9	25.9	24.5	23.6
JEDEC Board	20.5	18.8	17.7	16.8	16.3	15.8

19 MECHANICAL INFORMATION

Figure 100: 324 Pin PBGA 23x23mm Body



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES COPLANARITY.
3) DIMENSION bbb DENOTES PARALLEL.

PACKAGE TYPE : 324 PLASTIC BALL GRID ARRAY - PBGA																	
BODY SIZE : 23 x 23 x 2.28 MM (4 layer)																	
Dim.	A (2 layer)	A (4 layer)	A1	A2	D	D1	C (2 layer)	C (4 layer)	E	E1	l	J	b	d	e	aaa	bbb
Min	1.82	2.07	0.40	1.12	-	19.00	0.30	0.55	-	19.00	-	-	0.50	-	-	-	-
Nom.	2.03	2.28	0.50	1.17	23.00	19.50	0.36	0.61	23.00	19.50	1.00	1.00	0.63	1.00	1.00	-	-
Max.	2.22	2.49	0.60	1.22	-	20.20	0.40	0.67	-	20.20	-	-	0.70	-	-	0.15	0.35

NOTES

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

PMC-2011596(R1) ref PMC-2011465 (R1) Issue date: August 2001