NEC

MOS INTEGRATED CIRCUIT

μPD78F0701Y

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F0701Y is a μPD780701Y sub-series product of the 78K/0 series. The μPD78F0701Y features a DCAN controller and an IEBus™ controller. It also features flash memory as internal ROM. Programs can be written into the flash memory without having to remove it from the board.

The functions of the μPD78F0701Y are described in the following user's manuals. Be sure to read these manuals when designing a system based on the μPD78F0701Y.

μPD780701Y Sub-Series User's Manual : U13781E
78K/0 Series User's Manual, Instruction : U12326E

FEATURES

- Built-in IEBus (Inter Equipment Bus™) controller
- Built-in DCAN (Direct Storage Controller Area Network) controller
- Pin-compatible with masked ROM versions (other than the V_{PP} pin)
- Flash memory : 60K bytes (supported for self-programming)
- Internal high-speed RAM : 1,024 bytes
- Internal expansion RAM : 2,048 bytes
- ★ • Buffer RAM for DCAN : 288 bytes
- ★ • Can be operated within the same power supply voltage ranges as masked ROM versions (V_{DD} = 3.5 to 5.5 V)

Remark For differences between flash memory versions and masked ROM versions, see **Chapter 1**.

APPLICATIONS

Car audio systems, etc.

ORDERING INFORMATION

Part number	Package
μPD78F0701YGC-8BT	80-pin plastic QFP (14 × 14 mm)

Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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Printed in Japan

The mark ★ shows major revised points.

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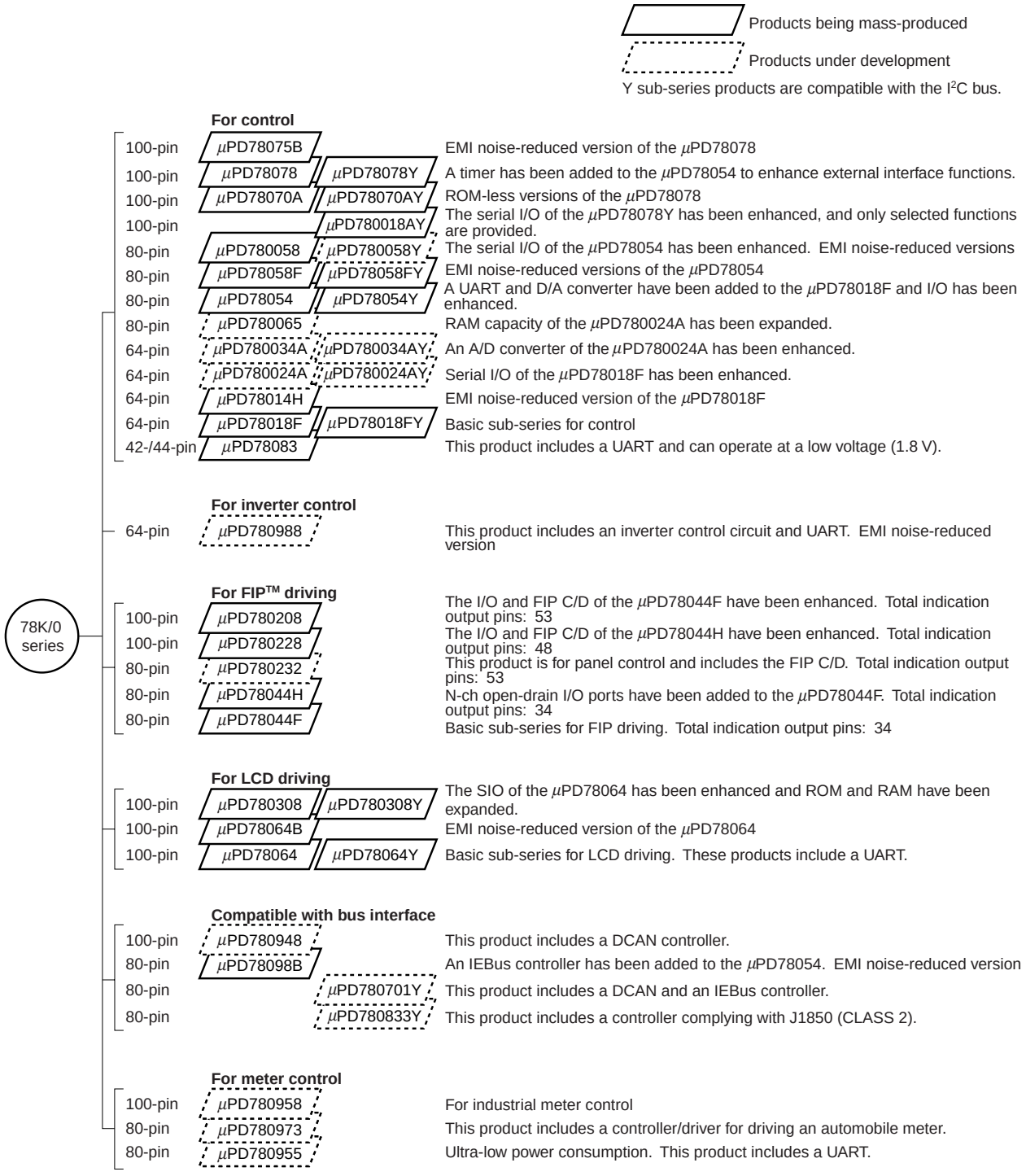
★ 78K/0 SERIES DEVELOPMENT

The 78K/0 series products are shown below. The sub-series names are indicated in frames.

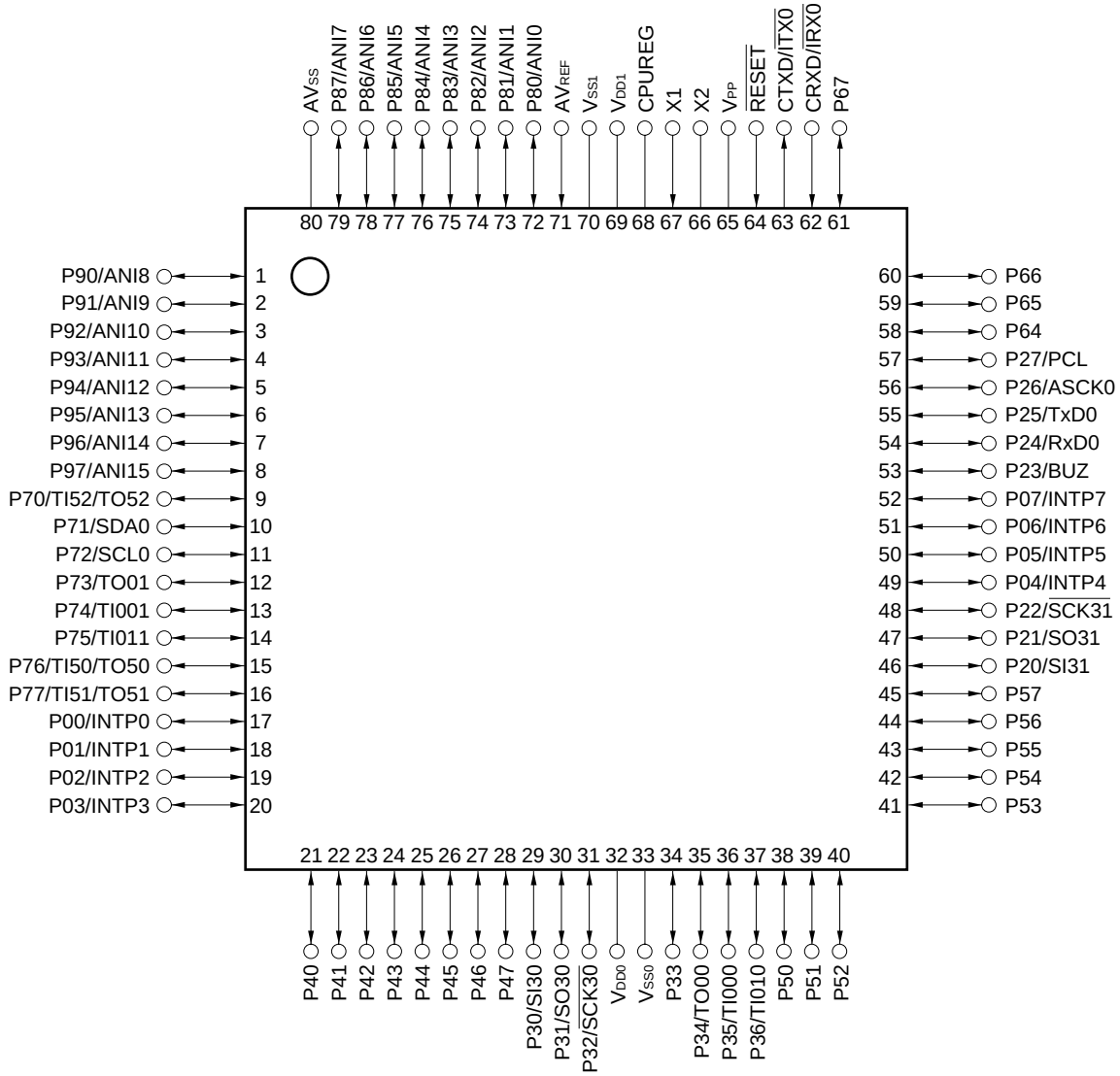


FUNCTIONS

Item		Function
Internal memory	Flash memory	60K bytes
	High-speed RAM	1,024 bytes
	Extended RAM	2,048 bytes
★	Buffer RAM for DCAN	288 bytes
Minimum instruction execution time		On-chip minimum instruction execution time modification function • 0.32 μs/0.64 μs/1.27 μs/2.54 μs/5.09 μs (operation with system clock running at 6.29 MHz)
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction set		• 16-bit operations • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulations (such as set, reset, test, and Boolean operation)
I/O ports		Total : 67 • CMOS I/O : 56 • TTL input/CMOS output : 8 • N-ch open-drain I/O : 3
A/D converters		• 16 channels with 8-bit resolution • Power failure detection function
Serial interface		• Three-wire serial I/O mode : 2 channels • UART mode : 1 channel • I^2C bus mode : 1 channel
Timers		• 16-bit timer/event counters : 2 channels • 8-bit timer/event counters : 3 channels • Watch timer : 1 channel • Watchdog timer : 1 channel
Timer output		5 lines (8-bit PWM output: 3 lines)
DCAN controller		1 channel
IEBus controller		Effective transmission rate: 18 kbps
Clock output		49.2 kHz, 98.3 kHz, 197 kHz, 393 kHz, 786 kHz, 1.57 MHz, 3.15 MHz, 6.29 MHz (operation with system clock running at 6.29 MHz)
Buzzer output		0.768 kHz, 1.54 kHz, 3.07 kHz, 6.14 kHz (operation with system clock running at 6.29 MHz)
Vectored interrupt sources	Maskable	Internal: 20, External: 8
	Nonmaskable	Internal: 1
	Software	1
★ Power supply voltage		V_{DD} = 3.5 to 5.5 V
Operating ambient temperature		T_A = -40°C to +85°C
Package		80-pin plastic QFP (14 × 14 mm)

PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic QFP (14 × 14 mm)
  μPD78F0701YGC-8BT



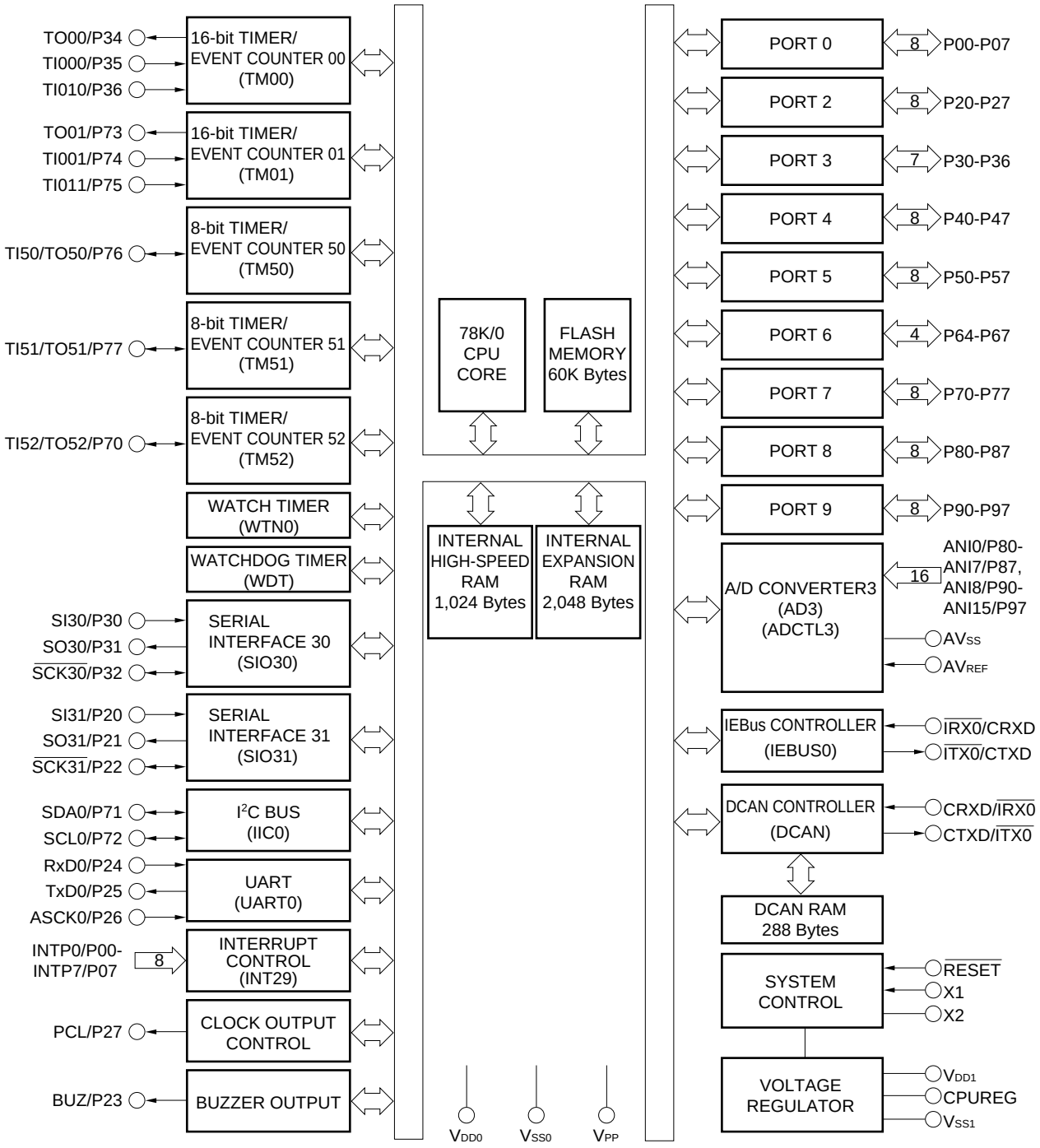
Cautions 1. In normal operation mode, connect the V_{PP} pin directly to the V_{SS0} or V_{SS1} pin.

2. Connect the AV_{SS} pin to the V_{SS0} pin.

3. Connect the AV_{REF} pin to the V_{DD0} pin.

ANI0-ANI15	: Analog Input	P90-P97	: Port 9
ASCK0	: Asynchronous Serial Clock	PCL	: Programmable Clock
AV_{REF}	: Analog Reference Voltage	$\overline{RESET}$	: Reset
AV_{SS}	: Analog Ground	RxD0	: Receive Data (for UART0)
BUZ	: Buzzer Output	$\overline{SCK30}$, $\overline{SCK31}$	: Serial Clock (for SIO30, SIO31)
CPUREG	: Regulator for CPU Power Supply	SCL0	: Serial Clock (for IIC0)
CRXD	: CAN Receive Data	SDA0	: Serial Data
CTXD	: CAN Transmit Data	SI30, SI31	: Serial Input
INTP0-INTP7	: Interrupt from Peripherals	SO30, SO31	: Serial Output
$\overline{IRX0}$	: IEBus Receive Data	TI000, TI010, TI001,	
$\overline{ITX0}$	: IEBus Transmit Data	TI011, TI50, TI51,	
P00-P07	: Port 0	TI52	: Timer Input
P20-P27	: Port 2	TO00, TO01, TO50,	
P30-P36	: Port 3	TO51, TO52	: Timer Output
P40-P47	: Port 4	TxD0	: Transmit Data (for UART0)
P50-P57	: Port 5	V_{DD0}, V_{DD1}	: Power Supply
P64-P67	: Port 6	V_{PP}	: Programming Power Supply
P70-P77	: Port 7	V_{SS0}, V_{SS1}	: Ground
P80-P87	: Port 8	X1, X2	: Crystal

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN THE μPD78F0701Y AND MASKED ROM VERSIONS

The μPD78F0701Y is a product provided with flash memory that enables writing, erasing, and rewriting of programs without being removed from the board.

Table 1-1 shows the differences between the flash memory version (μPD78F0701Y) and masked ROM versions (μPD780701Y and μPD780702Y).

Table 1-1. Differences between the μPD78F0701Y and Masked ROM Versions

Item		μPD78F0701Y	μPD780701Y	μPD780702Y
Internal ROM type		Flash memory	Masked ROM	
IC pin		Not provided	Provided	
V_{PP} pin		Provided	Not provided	
Built-in bus controller		DCAN controller and IEBus controller	DCAN controller	IEBus controller
	TX pin	DCAN or IEBus output (switched by software)	DCAN output	IEBus output
	RX pin	DCAN or IEBus input (switched by software)	DCAN input	IEBus input
Electrical characteristics		Refer to the data sheet of individual products.		

Caution The flash memory versions and masked ROM versions have different noise immunity and noise radiation characteristics. Do not use ES products for evaluation when considering switching from flash memory versions to those using masked ROM upon the transition from preproduction to mass-production. CS products (masked ROM versions) should be used in this case.

2. PIN FUNCTIONS

2.1 Port Pins (1/2)

	Pin name	I/O	Function		When reset	Also used as
	P00-P07	I/O	Port 0 8-bit input/output port Can be set to either input or output in 1-bit units. Whether an on-chip pull-up resistor is to be used can be specified by software.		Input	INTP0-INTP7
	P20	I/O	Port 2 8-bit input/output port Can be set to either input or output in 1-bit units. Whether an on-chip pull-up resistor is to be used can be specified by software.		Input	SI31
	P21					SO31
	P22					$\overline{\text{SCK31}}$
★	P23					BUZ
	P24					RxD0
	P25					TxD0
	P26					ASCK0
	P27					PCL
★	P30	I/O	Port 3 7-bit input/output port Can be set to either input or output in 1-bit units.	Whether an on-chip pull-up resistor is to be used can be specified by software.	Input	SI30
	P31					SO30
	P32					$\overline{\text{SCK30}}$
	P33			N-ch open-drain input/output port (15-V withstand voltage) Can directly drive LEDs.		-
★	P34			Whether an on-chip pull-up resistor is to be used can be specified by software.		TO00
	P35					TI000
	P36					TI010
★	P40-P47	I/O	Port 4 8-bit input/output port Can be set to either input or output in 1-bit units. Whether an on-chip pull-up resistor is to be used can be specified by software. When a falling edge is detected, the interrupt request flag (KRIF) is set to 1.		Input	-
★	P50-P57	I/O	Port 5 8-bit input/output port TTL-level input and CMOS output Can be set to either input or output in 1-bit units. Whether an on-chip pull-up resistor is to be used can be specified by software.		Input	-
★	P64-P67	I/O	Port 6 4-bit input/output port Can be set to either input or output in 1-bit units. Whether an on-chip pull-up resistor is to be used can be specified by software.		Input	-

2.1 Port Pins (2/2)

Pin name	I/O	Function		When reset	Also used as
★ P70	I/O	Port 7 8-bit input/output port Can be set to either input or output in 1-bit units.	Whether an on-chip pull-up resistor is to be used can be specified by software.	Input	TI52/TO52
P71			N-ch open-drain input/output port (5-V withstand voltage)		SDA0
P72					SCL0
P73			Whether an on-chip pull-up resistor is to be used can be specified by software.		TO01
P74					TI001
P75					TI011
P76					TI50/TO50
P77					TI51/TO51
P80-P87	I/O	Port 8 8-bit input/output port Can be set to either input or output in 1-bit units.		Input	ANI0-ANI7
P90-P97	I/O	Port 9 8-bit input/output port Can be set to either input or output in 1-bit units.		Input	ANI8-ANI15

2.2 Non-Port Pins (1/2)

Pin name	I/O	Function	When reset	Also used as
INTP0-INTP7	Input	External interrupt input for which effective edges (rising and/or falling edges) can be specified.	Input	P00-P07
SI30	Input	Serial data input to serial interface	Input	P30
SI31				P20
SO30	Output	Serial data output to serial interface	Input	P31
SO31				P21
SDA0	I/O	Serial data input/output to serial interface	Input	P71
$\overline{\text{SCK30}}$	I/O	Serial clock input/output to serial interface	Input	P32
$\overline{\text{SCK31}}$				P22
SCL0				P72
RxD0	Input	Serial data input to asynchronous serial interface	Input	P24
TxD0	Output	Serial data output to asynchronous serial interface	Input	P25
ASCK0	Input	Serial clock input to asynchronous serial interface	Input	P26
CRXD	Input	DCAN controller (DCAN) data input	Input	$\overline{\text{IRX0}}$
CTXD	Output	DCAN controller (DCAN) data output	Output	$\overline{\text{ITX0}}$
$\overline{\text{IRX0}}$	Input	IEBus controller (IEBUS0) data input	Input	CRXD
$\overline{\text{ITX0}}$	Output	IEBus controller (IEBUS0) data output	Output	CTXD

2.2 Non-Port Pins (2/2)

Pin name	I/O	Function	When reset	Also used as
TI000	Input	External count clock input to 16-bit timer (TM00)	Input	P35
TI010		External count clock input to 16-bit timer (TM00)		P36
TI001		External count clock input to 16-bit timer (TM01)		P74
TI011		External count clock input to 16-bit timer (TM01)		P75
TI50		External count clock input to 8-bit timer (TM50)		P76/TO50
TI51		External count clock input to 8-bit timer (TM51)		P77/TO51
TI52		External count clock input to 8-bit timer (TM52)		P70/TO52
TO00	Output	16-bit timer (TM00) output	Input	P34
TO01		16-bit timer (TM01) output		P73
TO50		8-bit timer (TM50) output		P76/TI50
TO51		8-bit timer (TM51) output		P77/TI51
TO52		8-bit timer (TM52) output		P70/TI52
PCL	Output	Clock output	Input	P27
BUZ	Output	Buzzer output	Input	P23
ANI0-ANI7	Input	A/D converter (AD3) analog input	Input	P80-P87
ANI8-ANI15				P90-P97
AV_{REF}	Input	A/D converter (AD3) reference voltage and analog power supply	-	-
AV_{SS}	-	A/D converter (AD3) ground potential	-	-
X1	Input	Connected to crystal for system clock oscillation	-	-
X2	-		-	-
$\overline{\text{RESET}}$	Input	System reset input	Input	-
CPUREG	-	CPU supply voltage regulator. Connect this pin to the V_{SS0} or V_{SS1} pin through a 0.1-μF capacitor.	-	-
V_{DD0}	-	Positive supply voltage for ports	-	-
V_{DD1}	-	Positive supply voltage (except ports and analog section)	-	-
V_{SS0}	-	Ground potential for ports	-	-
V_{SS1}	-	Ground potential (except ports and analog section)	-	-
V_{PP}	-	This pin applies a high voltage when a program is written or verified. In normal operation mode, connect this pin directly to the V_{SS0} or V_{SS1} pin.	-	-

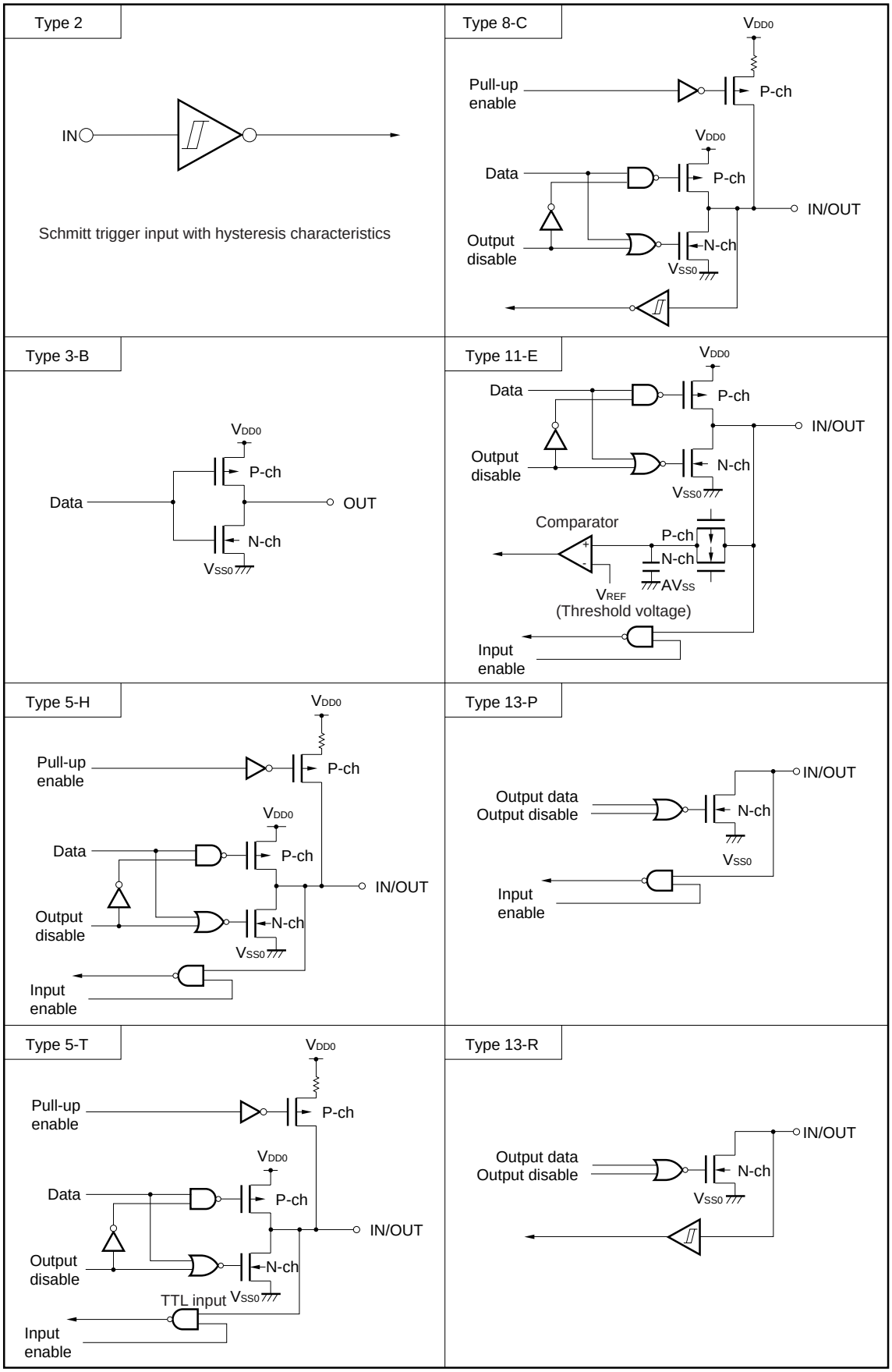
2.3 Pin Input/Output Circuits and Handling of Unused Pins

Table 2-1 lists the types of input/output circuits for each pin and explains how unused pins are handled.
Figure 2-1 shows the configuration of each type of input/output circuit.

Table 2-1. Types of Input/Output Circuit for Each Pin and Handling of Unused Pins

Pin name	I/O circuit type	I/O	Recommended connection of unused pins
P00/INTP0-P07/INTP7	8-C	I/O	Connect these pins to the V_{SS0} pin via respective resistors.
P20/SI31			Connect these pins to the V_{DD0} or V_{SS0} pin via respective resistors.
P21/SO31	5-H		
P22/$\overline{SCK31}$	8-C		
P23/BUZ	5-H		
P24/RxD0	8-C		
P25/TxD0	5-H		
P26/ASCK0	8-C		
P27/PCL	5-H		
P30/SI30	8-C		
P31/SO30	5-H		
P32/$\overline{SCK30}$	8-C		
P33	13-P		Connect this pin to the V_{DD0} pin via resistors.
P34/TO00	5-H		Connect these pins to the V_{DD0} or V_{SS0} pin via respective resistors.
P35/TI000	8-C		
P36/TI010			
P40-P47	5-H		Connect these pins to the V_{DD0} pin via respective resistors.
P50-P57	5-T		Connect these pins to the V_{DD0} or V_{SS0} pin via respective resistors.
P64-P67	5-H		
P70/TI52/TO52			
P71/SDA0	13-R		Connect these pins to the V_{DD0} pin via respective resistors.
P72/SCL0			
P73/TO01	5-H		Connect these pins to the V_{DD0} or V_{SS0} pin via respective resistors.
P74/TI001	8-C		
P75/TI011			
P76/TI50/TO50			
P77/TI51/TO51			
P80/ANI0-P87/ANI7	11-E		
P90/ANI8-P97/ANI15			
CRXD/$\overline{IRX0}$	2	Input	Connect this pin to the V_{DD0} or V_{SS0} pin via resistors.
CTXD/$\overline{ITX0}$	3-B	Output	Leave this pin open.
$\overline{RESET}$	2	Input	-
AV_{REF}	-		Connect this pin to the V_{DD0} pin.
AV_{SS}		-	Connect this pin to the V_{SS0} pin.
V_{PP}			Connect this pin directly to the V_{SS0} or V_{SS1} pin.

Figure 2-1. Pin Input/Output Circuits



★ 3. SELECTING INTERNAL BUS CONTROLLERS (DCAN and IEBus)

The μPD78F0701Y has two internal bus controllers: a DCAN controller and IEBus controller. These bus controllers cannot be used simultaneously.

By default, the DCAN controller is selected.

The IEBus controller is selected by making the IEBus unit active (by setting bit 7 (ENIEBUS) of the IEBus control register 0 (BRC0) to 1).

The default statuses of the interrupt request signals and pins differ depending on which of the internal bus controllers is used.

Table 3-1 shows the default statuses of the interrupt request signals and pins.

Table 3-1. Default Statuses of Interrupt Request Signals and Pins

Item	Using DCAN controller	Using IEBus controller
Default status of CTXD/ITX0 pin	High level	Low level
Interrupt request signals[Note]	INTCR	INTIE1
	INTCT	INTIE2
	INTCE	None

Note The statuses of the flags corresponding to the interrupt signals also differ.

★ 4. MEMORY SIZE SELECT REGISTER (IMS)

The memory size select register (IMS) selects the internal memory size.
This register is set by an 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input sets IMS to CFH.

Caution Use IMS with its default value (CFH). Do not set any other values for the IMS.

Figure 4-1. Format of Memory Size Select Register (IMS)

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
1	1	1	1	60K bytes
Other settings				Not to be set

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
1	1	0	1,024 bytes
Other settings			Not to be set

★ 5. INTERNAL EXPANSION RAM SIZE SELECT REGISTER (IXS)

The internal expansion RAM size select register (IXS) selects the internal expansion RAM capacity.
This register is set by a 1-bit or 8-bit memory manipulation instruction.
$\overline{\text{RESET}}$ input sets IXS to 0CH.

Caution Set IXS to 08H as the default status of the program. Because IXS is set to 0CH at a reset, set it to 08H after a reset.

Figure 5-1. Format of Internal Expansion RAM Size Select Register (IXS)

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
IXS	0	0	0	IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0CH	R/W

IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	Internal expansion RAM capacity selection
0	1	0	0	0	2,048 bytes
Other settings					Not to be set

★ 6. FLASH MEMORY PROGRAMMING

The flash memory can be written even while the device is mounted on the target system (on-board write). To write a program into the flash memory, connect the dedicated flash writer (Flashpro III (model number: FL-PR3 and PG-FP3)) to both the host machine and target system.

A program can also be written by using an adapter, for flash memory writing, connected to the Flashpro III.

Remark The FL-PR3 is manufactured by Naito Densei Machida Mfg. Co., Ltd.

6.1 Selecting the Transmission Method

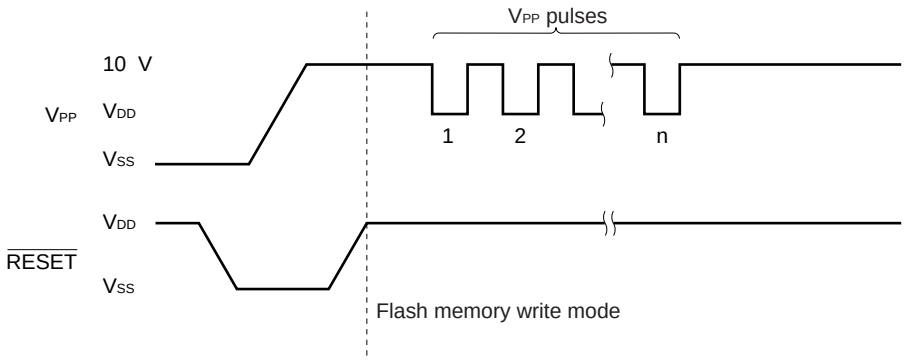
The Flashpro III writes into flash memory by means of serial transmission. The transmission method to be used for writing is selected from those listed in Table 6-1. To select a transmission method, use the format shown in Figure 6-1, according to the number of V_{PP} pulses listed in Table 6-1.

Table 6-1. Transmission Methods

Transmission method	Number of channels	Pins	Number of V_{PP} pulses
Three-wire serial I/O	2	SI30/P30 SO30/P31 $\overline{SCK30}$/P32	0
		SI31/P20 SO31/P21 $\overline{SCK31}$/P22	1
I^2C bus	1	SDA0/P71 SCL0/P72	4
UART	1	RxD0/P24 TxD0/P25	8

Caution To select a transmission method, always use the corresponding number of V_{PP} pulses listed in Table 6-1.

Figure 6-1. Format of Transmission Method Selection



6.2 Flash Memory Programming Functions

Flash memory writing and other operations can be performed by transmitting/receiving commands and data according to the selected transmission method. Table 6-2 lists the main flash memory programming functions.

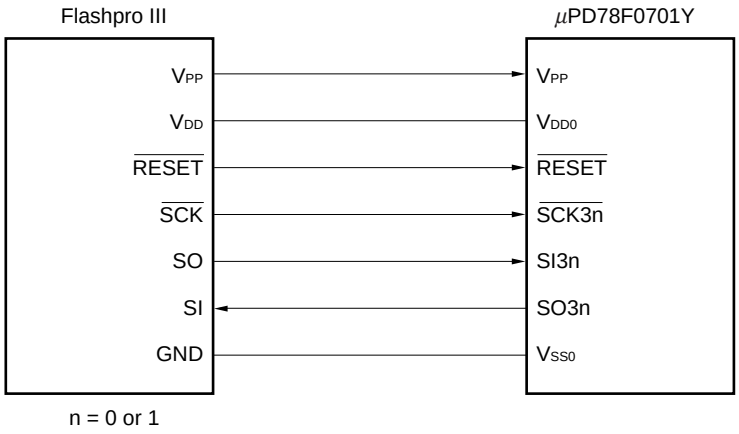
Table 6-2. Main Flash Memory Programming Functions

Function	Description
Reset	Stops writing or detects communication synchronization.
Batch verify	Compares the entire contents of memory with the input data.
Batch internal verify	Compares the entire contents of memory in different modes.
Batch erase	Erases the entire contents of memory.
Batch blank check	Checks that the entire contents of memory have been erased.
High-speed write	Writes to the flash memory according to the specified write start address and number of data bytes to be written.
Continuous write	Continues writing based on the information input by using the high-speed write function.
Batch prewrite	Writes 00H into the entire contents of memory.
Status	Checks the current operation mode and whether the operation has terminated.
Oscillation frequency setting	Inputs the frequency information of the resonator.
Erase time setting	Inputs the memory erase time.
Baud rate setting	Sets the communication rate in UART mode.
I^2C communication mode setting	Sets standard or high-speed mode upon communication via I^2C.
Silicon signature read	Outputs the device name, memory capacity, and device block information.

6.3 Connecting the Flashpro III

The connection between the Flashpro III and μPD78F0701Y varies with the transmission method. Figures 6-2 to 6-4 show the connection for each transmission method.

Figure 6-2. Flashpro III Connection in Three-Wire Serial I/O Mode



n = 0 or 1

Figure 6-3. Flashpro III Connection in I²C Bus Mode

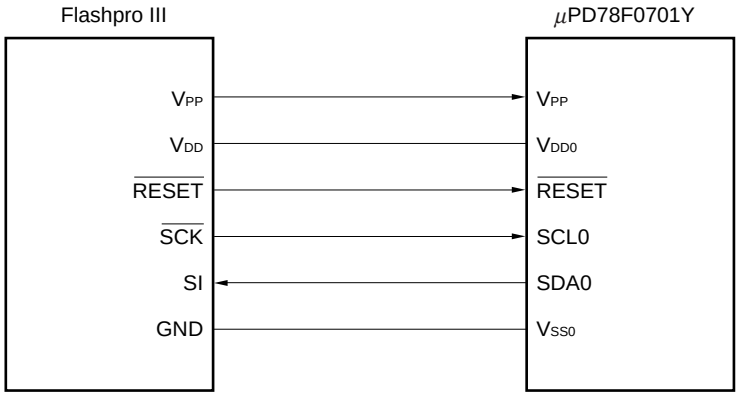
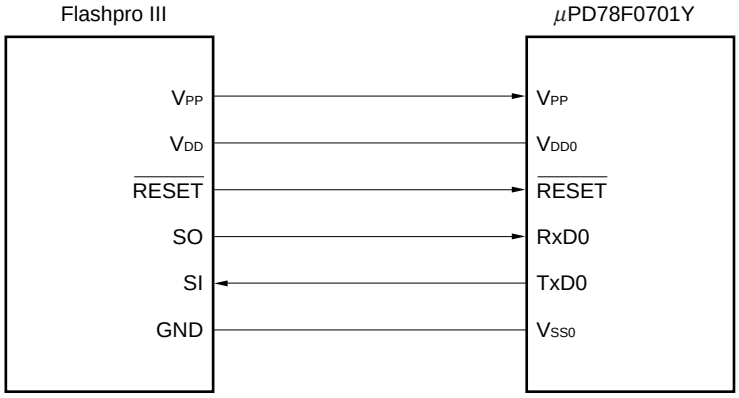


Figure 6-4. Flashpro III Connection in UART Mode



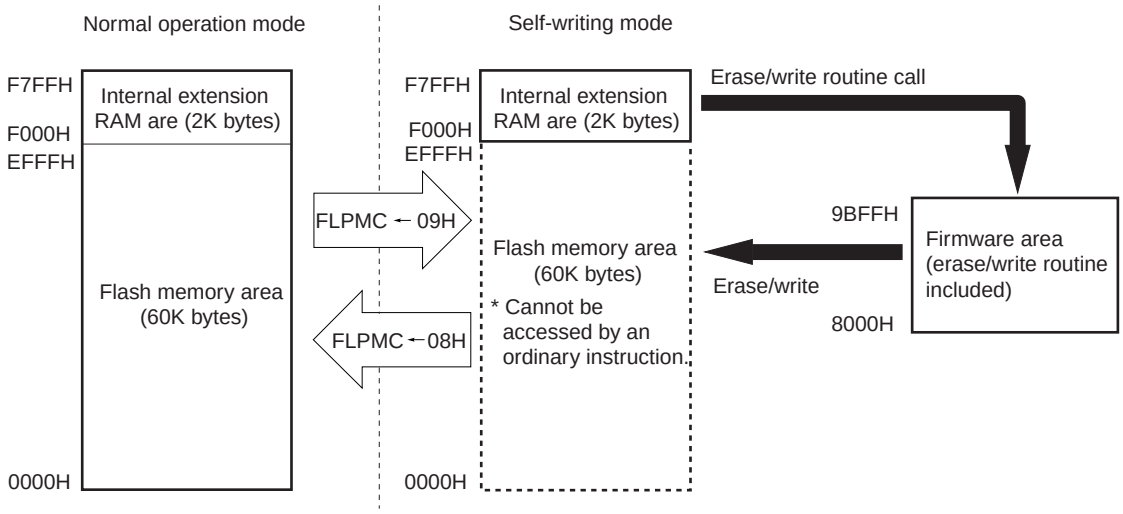
★ 6.4 Flash Memory Programming by Self-Writing

The flash memory of the μPD78F0701Y can be rewritten by a program.

(1) Configuration of flash memory

Figure 6-5 shows the configuration of the flash memory.

Figure 6-5. Configuration of Flash Memory



(2) Flash programming mode control register (FLPMC)

The flash programming mode control register (FLPMC) is used to select an operation mode and check the status of the V_{PP} pin.

This register is set with a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets FLPMC to 08H.

Figure 6-6. Format of Flash Programming Mode Control Register (FLPMC)

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
FLPMC	0	0	0	0	1	VPP	0	FLSPM0	FFCDH	08H Note 1	R/W Note 2

VPP	Applied voltage of V_{PP} pin
0	The voltage necessary for erasing/writing flash memory is not applied to the V_{PP} pin.
1	A voltage higher than that on the V_{DD} pin is applied to the V_{PP} pin.

FLSPM0	Operation mode selection
0	Normal operation mode
1	Self-writing mode

Notes 1. Bit 2 changes depending on the level of the V_{PP} pin.

2. Bit 2 is a read-only bit.

Cautions 1. Clear bits 1 and 4 to 7 to 0, and set bit 3 to 1.

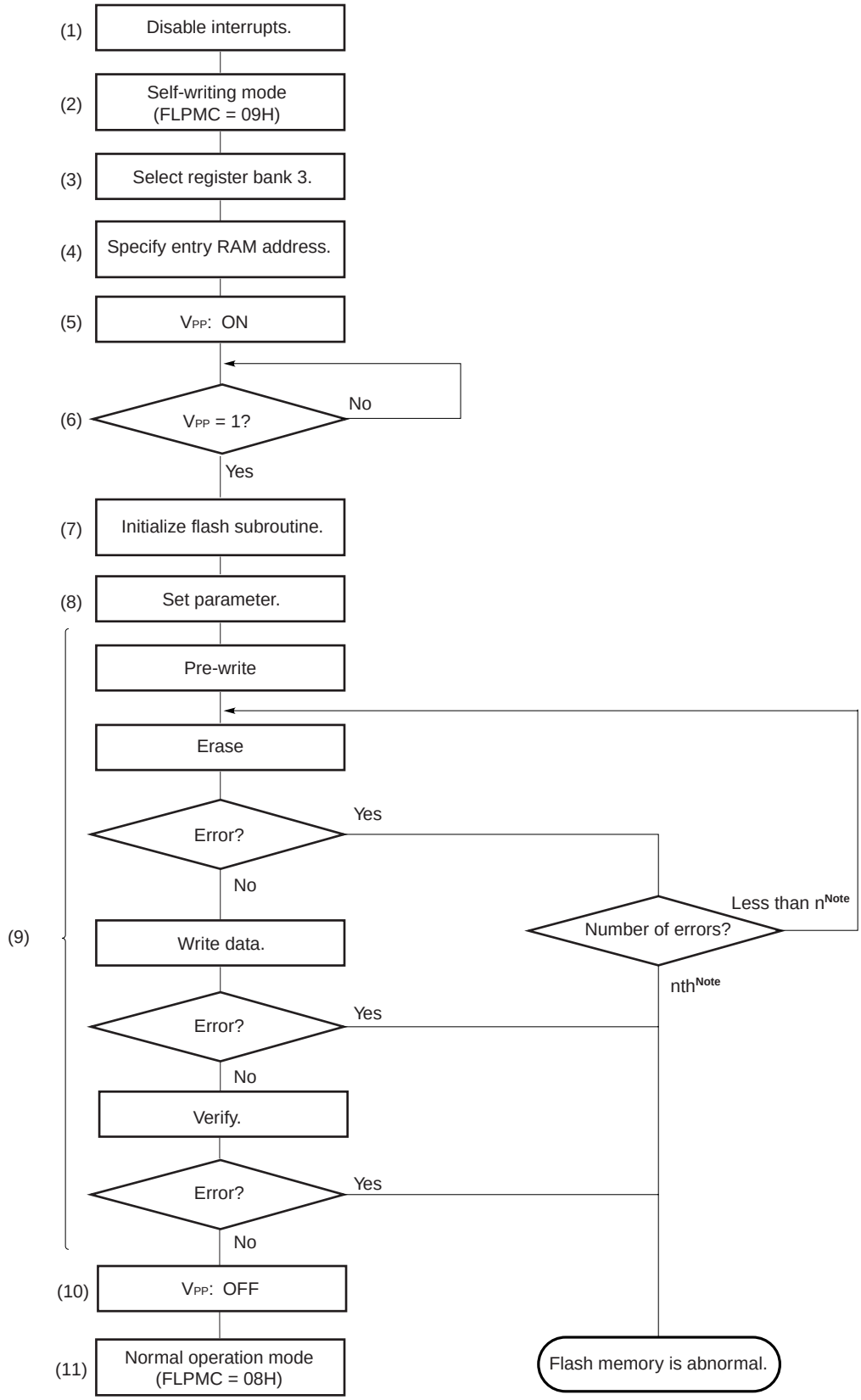
2. The VPP bit indicates the status of the voltage applied to the V_{PP} pin. When the VPP bit is "0", the voltage necessary for erasing/writing the flash memory is not applied to the V_{PP} pin. However, the voltage necessary for erasing/writing is not always applied even when the VPP bit is "1". Configure the hardware so that the necessary voltage is accurately applied to the V_{PP} pin. To check whether the necessary voltage is also applied to the V_{PP} pin by software, not only by hardware, use an external hardware detection circuit and its output signals.

(3) Self writing procedure

The procedure for self writing the flash memory is as follows (see Figure 6-7):

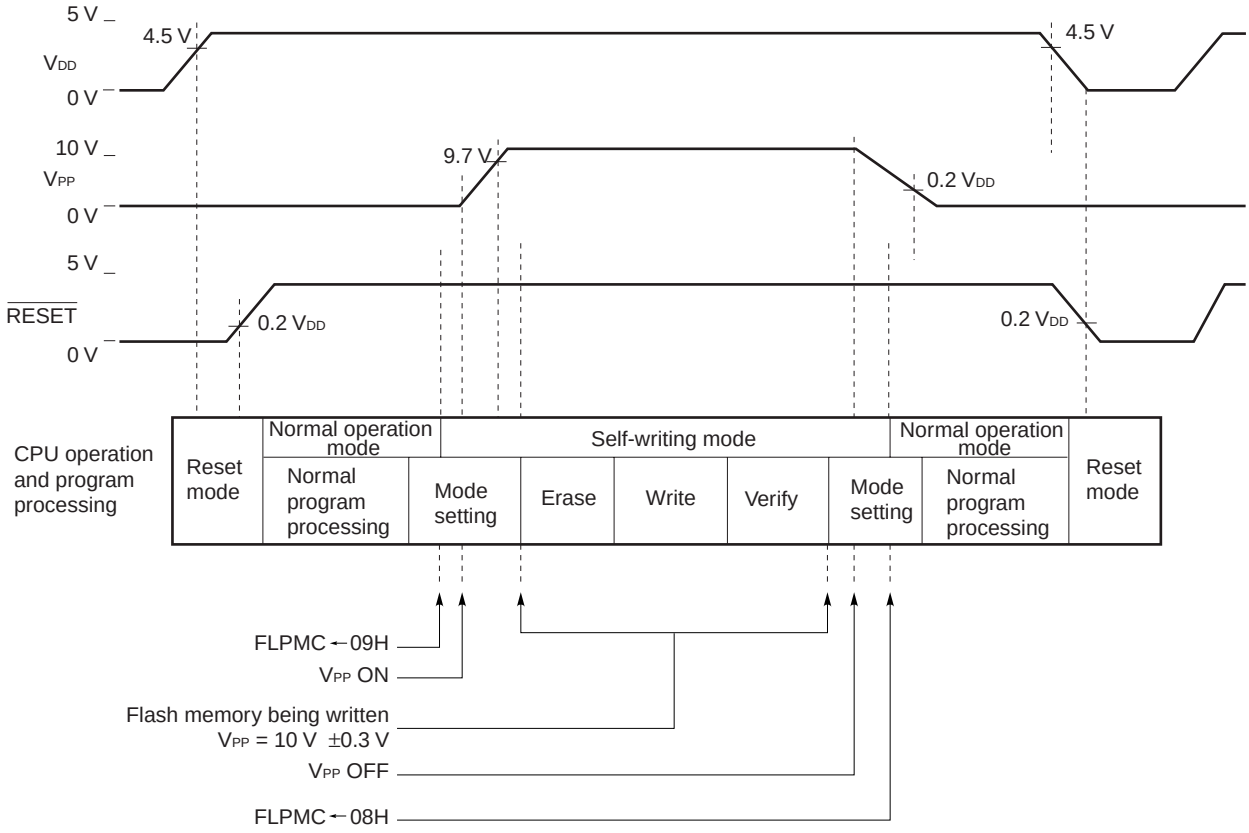
(1) Disable the interrupts.
(2) Set self-writing mode (FLPMC = 09H).
(3) Select register bank 3.
(4) Specify the first address of the entry RAM to the HL register.
(5) V_{PP}: ON (ON signal for power IC).
(6) Check the V_{PP} level.
(7) Initialize the flash subroutine.
(8) Set the parameters.
(9) Control the flash memory (erasing, writing, etc.).
(10) V_{PP}: OFF (OFF signal for power IC).
(11) Normal operation mode (FLPMC = 08H)

Figure 6-7. Self-Programming Flowchart



Note This differs depending on the user program.

Figure 6-8. Self-Writing Timing



(4) CPU resources

The CPU resources used for self-writing the flash memory are as follows:

- Register bank: BANK3 (8 bytes)
  B register: Status flag
  C register: Function number
  HL register: Entry RAM area first address
- Stack area: 16 bytes MAX.
- Write data storage area: 1 to 256 bytes
- Entry RAM area: 32 bytes
  RAM area used by self-writing subroutine.
  Can be specified by user by using HL register.
- Status flag

7	6	5	4	3	2	1	0
Parameter setting error	-	-	Verify error	Write error	-	Blank check error	-

(5) Entry RAM area

Table 6-3 shows the contents of the entry RAM area.

Table 6-3. Entry RAM Area

Offset value	Contents
+0	Reserved area (1 byte)
+1	Reserved area (1 byte)
+2	Flash memory start address (2 bytes)
+4	Flash memory end address (2 bytes)
+6	Number of bytes written to flash memory (1 byte)
+7	Write time data (1 byte)
+8	Erase time data (3 bytes)
+11	Reserved area (3 bytes)
+14	Write data storage buffer first address (2 bytes)
+16	Total number of blocks (1 byte)
+17	Total number of areas (1 byte)
+18 :	Reserved area (14 bytes)

Example: When the value of the HL register in register bank 3 is 0FD00H
0FD00H: Status
0FD02H: Flash memory start address
0FD06H: Number of bytes written to flash memory
:

The following explains the entry RAM area in detail.

(a) Flash memory start address

Flash memory address value used for _FlashByteWrite subroutine

(b) Flash memory end address

Flash memory address value used for _FlashGetInfo subroutine

(c) Number of bytes written to flash memory

Area number and number of bytes written to flash memory

(d) Write time

Set one of the following values according to the operating frequency.

f_X (MHz)	Set value
1.00 to 1.28	20H
1.29 to 2.56	40H
2.57 to 5.12	60H
5.13 to 8.38	80H

(e) Erase time data

Set value = Erase time (s) × Operating frequency/2^9 + 1

(Erase time range: 0.5 to 20 s)

Example: When the erase time is two seconds and the operating frequency is 6.29 MHz

Set value = 2 × 6,291,456/512 + 1

= 24,577 (decimal)

= 6001H (hexadecimal)

(f) Write data storage buffer first address

This area stores the first address of the write data storage buffer area. The data (write data) in the RAM addressed by using the data in this area is written into flash memory (_FlashByteWrite subroutine). Up to 256 bytes of write data can be specified with the data in this area as the first address.

(g) Total number of blocks

Total number of flash memory blocks stored by _FlashGetInfo subroutine

(h) Total number of areas

Total number of flash memory areas stored by _FlashGetInfo subroutine

(6) Self-writing subroutine

Table 6-4 lists the subroutines to be used for self-writing and their functions.

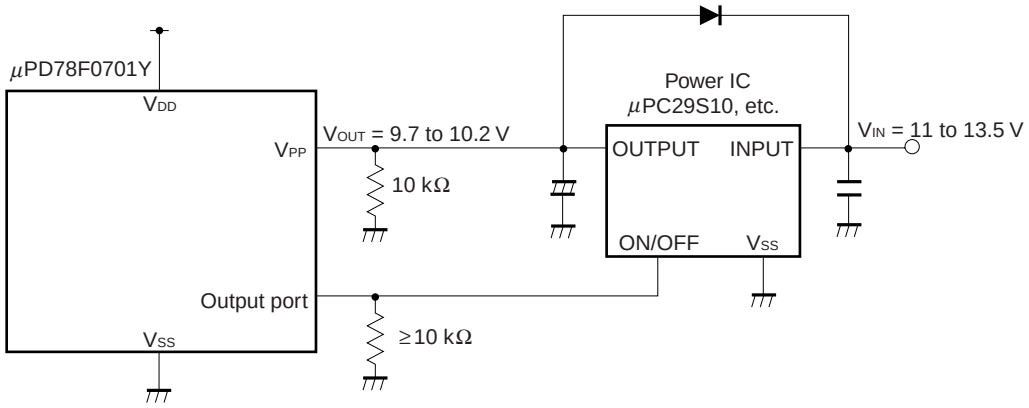
Table 6-4. Self-Writing Subroutines

Function No.		Subroutine name	Function
Decimal	Hexa-decimal		
0	00H	_FlashEnv	Initializes flash subroutine.
1	01H	_FlashSetEnv	Sets parameter.
2	02H	_FlashGetInfo	Reads flash memory information.
16	10H	_FlashAreaBlankCheck	Blank check of specified area
32	20H	_FlashAreaPreWrit	Pre-write of specified area
48	30H	_FlashAreaErase	Erases specified area
80	50H	_FlashByteWrite	Successive write in byte units
96	60H	_FlashAreaIVerify	Internal verification of specified area

(7) Configuration of self-writing circuit

Figure 6-9 shows the configuration of the self-writing circuit.

Figure 6-9. Configuration of Self-Writing Circuit



★ 7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

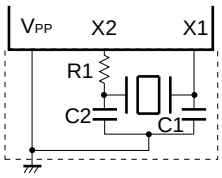
Parameter	Symbol	Conditions		Rated value	Unit
Supply voltage	V_{DD}	$V_{DD} = AV_{REF}$		-0.3 to +6.5	V
	AV_{REF}				
	V_{PP}			-0.3 to +10.5	V
	AV_{SS}			-0.3 to +0.3	V
Input voltage	V_{I1}	P00-P07, P20-P27, P30-P32, P34-P36, P40-P47, P50-P57, P64-P67, P70-P77, P80-P87, P90-P97, CRXD/$\overline{IRX0}$, X1, X2, $\overline{RESET}$		-0.3 to V_{DD} + 0.3	V
	V_{I2}	P33	N-ch open drain	-0.3 to +16	V
Output voltage	V_O	P00-P07, P20-P27, P30-P36, P40-P47, P50-P57, P64-P67, P70-P77, P80-P87, P90-P97, CTXD/$\overline{ITX0}$		-0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P80-P87, P90-P97	Analog input pin	AV_{SS} - 0.3 to AV_{REF} + 0.3 and -0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	P00-P07, P20-P27, P30-P32, P34-P36, P40-P47, P50-P57, P64-P67, P70, P73-P77, P80-P87, P90-P97, CTXD/$\overline{ITX0}$ per pin		-10	mA
		Total for all pins		-30	mA
Low-level output current	I_{OL} Note	P00-P07, P20-P27, P30-P32, P34-P36, P40-P47, P50-P57, P64-P67, P70-P77, P80-P87, P90-P97, CTXD/$\overline{ITX0}$ per pin	Peak value	20	mA
			rms value	10	mA
		P33	Peak value	30	mA
			rms value	15	mA
		Total for all pins	Peak value	100	mA
			rms value	60	mA
Operating ambient temperature	T_A			-40 to +85	°C
Programming ambient temperature				-10 to +55	°C
Storage temperature	T_{stg}	Before 2,000 hours elapses after flash memory programming was performed		-65 to +150	°C
		After flash memory programming was performed and 2,000 hours or more has elapsed		-65 to +125	°C

Note To obtain the rms value, calculate [rms value] = [peak value] $\times \sqrt{\text{duty}}$.

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

Remark Unless otherwise specified, the characteristics of a dual-function pin are the same as those of the corresponding port pin.

CHARACTERISTICS OF THE SYSTEM CLOCK OSCILLATION CIRCUIT (T_A = -40°C to +85°C, V_{DD} = 3.5 to 5.5 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillation frequency (f_X)[Note 1]			6.29[Note 2]		MHz
		Oscillation settling time[Note 3]				30	ms

Notes 1. Only the characteristics of the oscillation circuit are indicated.

2. 6.29 = 6.291456 (MHz)

3. Time required for oscillation to settle once a reset sequence ends or STOP mode is deselected.

Caution When using the system clock oscillation circuit, observe the following conditions for the wiring of that section enclosed in dotted lines in the above diagrams, so as to avoid the influence of the wiring capacitance.

- **Keep the wiring as short as possible.**
- **Do not allow signal wires to cross one another.**
- **Keep the wiring away from wires that carry a high, non-stable current.**
- **Keep the grounding point of the capacitors at the same level as V_{SS1}.**
- **Do not connect the grounding point to a grounding wire that carries a high current.**
- **Do not extract a signal from the oscillation circuit.**

DC CHARACTERISTICS (T_A = -40°C to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	P21, P23, P25, P27, P31, P34, P40-P47, P64-P67, P73, P80-P87, P90-P97		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00-P07, P20, P22, P24, P26, P30, P32, P35, P36, P70-P72, P74-P77, CRXD/$\overline{IRX0}$, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P50-P57		2.3		V_{DD}	V
	V_{IH4}	P33	N-ch open drain	0.7V_{DD}		15	V
	V_{IH5}	X1, X2		V_{DD} - 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	P21, P23, P25, P27, P31, P34, P40-P47, P64-P67, P73, P80-P87, P90-P97		0		0.3V_{DD}	V
	V_{IL2}	P00-P07, P20, P22, P24, P26, P30, P32, P35, P36, P70-P72, P74-P77, CRXD/$\overline{IRX0}$, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	P50-P57		0		0.75	V
	V_{IL4}	P33	N-ch open drain	0		0.3V_{DD}	V
	V_{IL5}	X1, X2		0		0.4	V
High-level output voltage	V_{OH1}	I_{OH} = -1 mA	P00-P07, P20-P27, P30-P32, P34-P36, P40-P47, P50-P57, P64-P67, P70, P73-P77, P80-P87, P90-P97, CTXD/$\overline{ITX0}$	V_{DD} - 1.0		V_{DD}	V
	V_{OH2}	I_{OH} = -100 μA		V_{DD} - 0.5		V_{DD}	V
Low-level output voltage	V_{OL1}	I_{OL} = 15 mA	P33		0.4	2.0	V
	V_{OL2}	I_{OL} = 1.6 mA	P71, P72			0.4	V
	V_{OL3}	I_{OL} = 1 mA	P00-P07, P20-P27, P30-P32, P34-P36, P40-P47, P50-P57, P64-P67, P70, P73-P77, P80-P87, P90-P97, CTXD/$\overline{ITX0}$			1.0	V
	V_{OL4}	I_{OL} = 100 μA				0.5	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	P00-P07, P20-P27, P30-P32, P34-P36, P40-P47, P50-P57, P64-P67, P70-P77, P80-P87, P90-P97, CRXD/$\overline{IRX0}$, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P33			80	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	P00-P07, P20-P27, P30-P32, P34-P36, P40-P47, P50-P57, P64-P67, P70-P77, P80-P87, P90-P97, CRXD/$\overline{IRX0}$, $\overline{RESET}$			-3	μA
	I_{LIL2}		X1, X2			-20	μA
	I_{LIL3}		P33 (during other than input instruction execution[Note])			-3	μA

Note During input instruction execution, a leakage current of -200 μA (MAX.) is input to P33 for one clock (during no wait).

Remark Unless otherwise specified, the characteristics of a dual-function pin are the same as those of the corresponding port pin.

DC CHARACTERISTICS (T_A = -40°C to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level output leakage current	I_{LOH}	$V_{OUT} = V_{DD}$	P00-P07, P20-P27, P30-P36, P40-P47, P50-P57, P64-P67, P70-P77, P80-P87, P90-P97, CTXD/$\overline{ITX0}$			3	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V	P00-P07, P20-P27, P30-P36, P40-P47, P50-P57, P64-P67, P70-P77, P80-P87, P90-P97, CTXD/$\overline{ITX0}$			-3	μA
Software pull-up resistor	R_1	V_{IN} = 0 V	P00-P07, P20-P27, P30-P32, P34-P36, P40-P47, P50-P57, P64-P67, P70, P73-P77	15	30	90	kΩ
Power supply current Note 1	I_{DD1}	6.29-MHz crystal oscillation operating mode			4.0	20	mA
	I_{DD2}	6.29-MHz crystal oscillation HALT mode Note 2			500	1,000	μA
	I_{DD3}	STOP mode			0.1	30	μA

Notes 1. The current flowing through the V_{DD1} pin. The power supply current does not include the current flowing through the A/D converter and on-chip pull-up resistors.

2. During low-speed mode operation (when 04H is loaded into the processor clock control register (PCC)). The power supply current does not include the current for peripheral circuit operation.

Remark Unless otherwise specified, the characteristics of a dual-function pin are the same as those of the corresponding port pin.

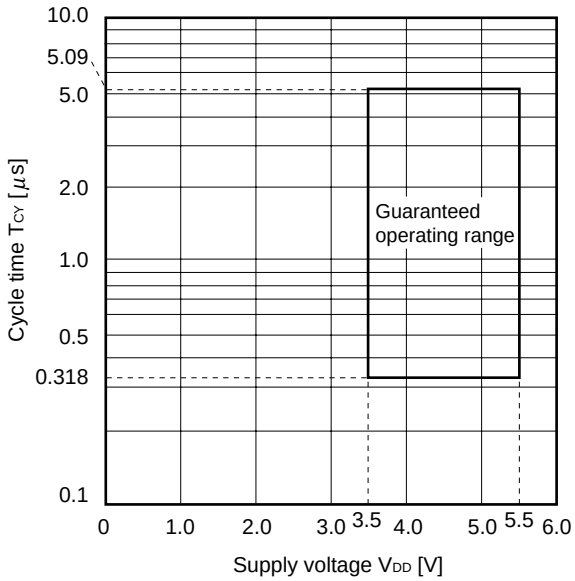
AC CHARACTERISTICS

(1) Basic operations (T_A = -40°C to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	System clock operation (at f_X = 6.291456 MHz)	0.318		5.09	μs
TI000, TI010, TI001, and TI011 input high/low level width	t_{TIH0} t_{TIL0}		$4/f_{sam}$ + 0.25 Note			μs
TI50, TI51, and TI52 input frequency	f_{TI5}				2	MHz
TI50, TI51, and TI52 input high/low level width	t_{TIH5} t_{TIL5}		200			ns
Interrupt request input high/low level width	t_{INTH} t_{INTL}	INTP0 to INTP7, P40 to P47	10			μs
$\overline{RESET}$ low level width	t_{RSL}		10			μs

Note $f_X/2$, $f_X/4$, or $f_X/64$ can be selected as f_{sam} by using bits 0 and 1 (PRM0n0 and PRM0n1) of the prescaler mode register 0n (PRM0n). If the valid edge of TI00n is selected as the count clock, however, $f_{sam} = f_X/8$ (n = 0 or 1).

T_{CY} vs V_{DD} (with system clock running)



(2) Serial interface (T_A = -40°C to +85°C, V_{DD} = 3.5 to 5.5 V)

(a) Three-wire serial I/O mode ($\overline{SCK30}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY1}		1.9			μs
$\overline{SCK30}$ high/low level width	t_{KH1} t_{KL1}		t_{KCY1}/2 - 50			ns
SI30 setup time (for $\overline{SCK30}$ ↑)	t_{SIK1}		100			ns
SI30 hold time (for $\overline{SCK30}$ ↑)	t_{KSI1}		400			ns
Delay from $\overline{SCK30}$ ↓ to SO30 output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the capacitance of the $\overline{SCK30}$ and SO30 output line.

(b) Three-wire serial I/O mode ($\overline{SCK30}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK30}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK30}$ high/low level width	t_{KH2} t_{KL2}		400			ns
SI30 setup time (for $\overline{SCK30}$ ↑)	t_{SIK2}		100			ns
SI30 hold time (for $\overline{SCK30}$ ↑)	t_{KSI2}		400			ns
Delay from $\overline{SCK30}$ ↓ to SO30 output	t_{KSO2}	C = 100 pF[Note]			300	ns

Note C is the capacitance of the SO30 output line.

(c) Three-wire serial I/O mode ($\overline{\text{SCK31}}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK31}}$ cycle time	t_{KCY3}		1.9			μs
$\overline{\text{SCK31}}$ high/low level width	t_{KH3} t_{KL3}		t_{KCY1}/2 - 50			ns
SI31 setup time (for $\overline{\text{SCK31}}$ ↑)	t_{SIK3}		100			ns
SI31 hold time (for $\overline{\text{SCK31}}$ ↑)	t_{KSI3}		400			ns
Delay from $\overline{\text{SCK31}}$ ↓ to SO31 output	t_{KSO3}	C = 100 pF[Note]			300	ns

Note C is the capacitance of the $\overline{\text{SCK31}}$ and SO31 output line.

(d) Three-wire serial I/O mode ($\overline{\text{SCK31}}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK31}}$ cycle time	t_{KCY4}		800			ns
$\overline{\text{SCK31}}$ high/low level width	t_{KH4} t_{KL4}		400			ns
SI31 setup time (for $\overline{\text{SCK31}}$ ↑)	t_{SIK4}		100			ns
SI31 hold time (for $\overline{\text{SCK31}}$ ↑)	T_{KSI4}		400			ns
Delay from $\overline{\text{SCK31}}$ ↓ to SO31 output	t_{KSO4}	C = 100 pF[Note]			300	ns

Note C is the capacitance of the SO31 output line.

(e) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					38,836	bps

(f) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY3}		800			ns
ASCK0 high/low level width	t_{KH3}, t_{KL3}		400			ns
Transfer rate					39,063	bps

(g) I^2C bus mode

Parameter		Symbol	Standard mode		High-speed mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{SCL}	0	100	0	400	kHz
Bus free time (between stop-start conditions)		t_{BUF}	4.7	-	1.3	-	μs
Hold time Note 1		$t_{HD:STA}$	4.0	-	0.6	-	μs
SCL0 clock low level width		t_{LOW}	4.7	-	1.3	-	μs
SCL0 clock high level width		t_{HIGH}	4.0	-	0.6	-	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	-	0.6	-	μs
Data hold time	CBUS-compatible master	$t_{HD:DAT}$	5.0	-	-	-	μs
	I^2C bus		0 Note 2	-	0 Note 2	0.9 Note 3	μs
Data setup time		$t_{SU:DAT}$	250	-	100 Note 4	-	ns
SDA0 and SCL0 signal rising time		t_R	-	1,000	-	300	ns
SDA0 and SCL0 signal falling time		t_F	-	300	-	300	ns
Stop condition setup time		$t_{SU:STO}$	4.0	-	0.6	-	μs
Pulse width of spikes controlled by the input filter		t_{SP}	-	-	0	50	ns
Capacitive load of each bus line		Cb	-	400	-	400	pF

Notes 1. In the start condition, the first clock pulse is generated after this period of time.

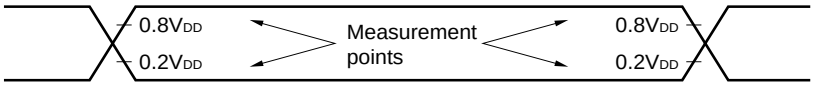
2. To fill the undefined area of the SCL0 falling edge (at $V_{IHmin.}$ of the SCL0 signal), the device needs to internally provide a hold time of at least 300 ns for the SDA0 signal.

3. If the device does not extend the low hold time (t_{LOW}) of the SCL0 signal, the maximum data hold time ($t_{HD:DAT}$) only needs to be satisfied.

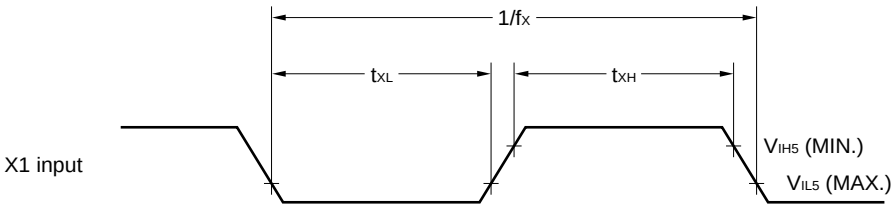
4. High-speed mode I^2C bus can be used in standard mode I^2C bus system. In this case, the following conditions must be satisfied:

- When the device does not extend the low hold time of the SCL0 signal
  $t_{SU:DAT} \geq 250$ ns
- When the device extends the low hold time of the SCL0 signal
  Before SCL0 is released ($t_{Rmax.} + t_{SU:DAT} = 1{,}000 + 250 = 1{,}250$ ns: for standard mode I^2C bus system), the next data bit must be sent onto the SDA0 line.

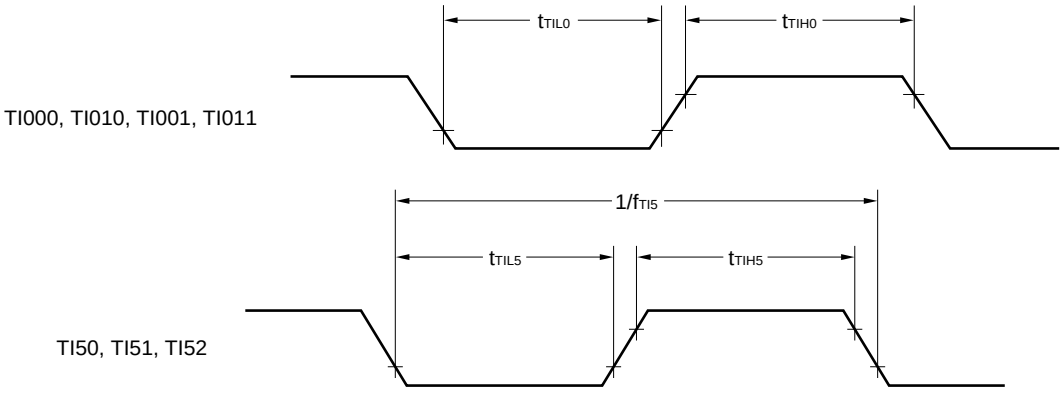
AC TIMING MEASUREMENT POINTS (except the X1 inputs)



CLOCK TIMING

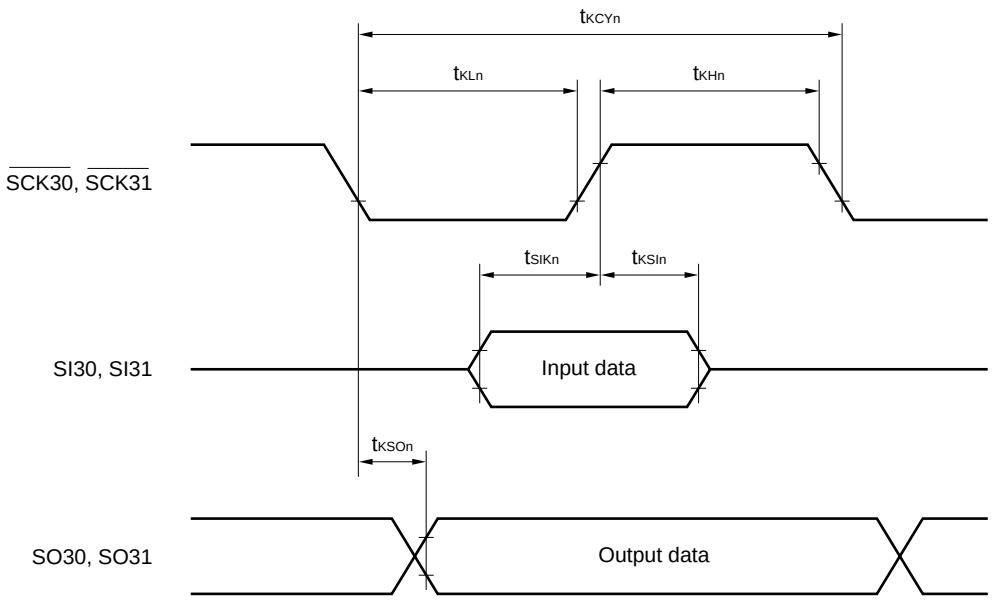


TI TIMING



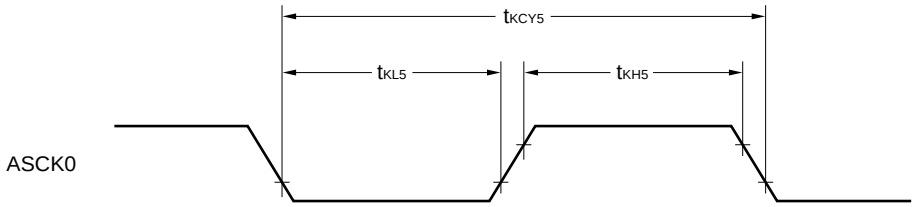
SERIAL TRANSFER TIMING

Three-Wire Serial I/O Mode:

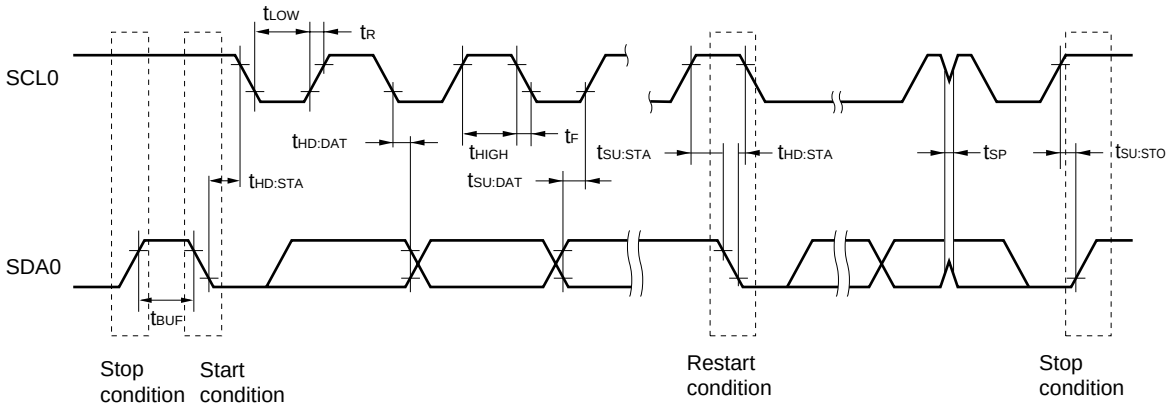


n = 1-4

UART Mode (External Clock Input):



I²C Bus Mode:



IEBus 0 CONTROLLER CHARACTERISTICS (T_A = -40°C to +85°C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IEBus system clock frequency	f_S	Fixed to mode 1		6.29		MHz
Driver delay (from $\overline{ITX0}$ output to bus line)	t_{DTX}	C = 50 pF[Note] The μPC2590 is used as a driver/receiver.			1.5	μs
Receiver delay (from bus line to $\overline{IRX0}$ input)	t_{DRX}	The μPC2590 is used as a driver/receiver.			0.7	μs
Transmission delay on bus	t_{DBUS}	The μPC2590 is used as a driver/receiver.			0.85	μs

Note C is the load capacitance of the $\overline{ITX0}$ output line.

Remarks 1. Although the IEBus standard recommends the 6.0-MHz system clock frequency, the μPD78F0701Y guarantees normal operation of the IEBus controller at 6.29 MHz.

2. f_S: System clock frequency of the IEBus controller

A/D CONVERTER CHARACTERISTICS (T_A = -40°C to +85°C, V_{DD} = AV_{REF} = 3.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error[Note]					±0.6	%
Conversion time	t_{CONV}		14		100	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
AV_{REF} resistance	R_{AIREF}		T.B.D	28	T.B.D	kΩ

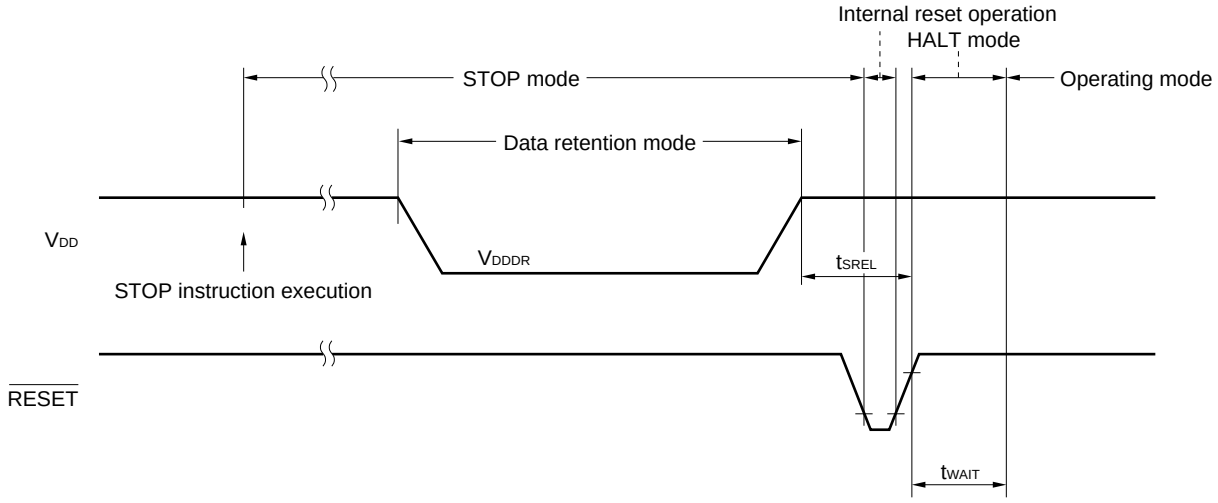
Note No quantization error (±0.2%) is included. This parameter is indicated as the ratio to the full-scale value.

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = -40°C to +85°C)

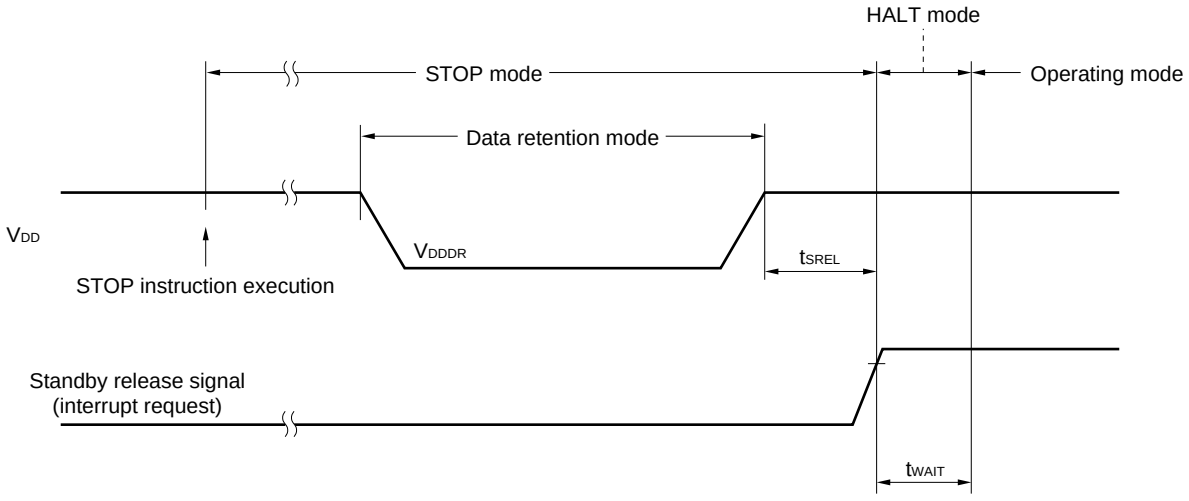
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation settling time	t_{WAIT}	Released by $\overline{RESET}$		$2^{17}/f_X$		ms
		Released by interrupt		**Note**		ms

Note Selection of $2^{12}/f_X$, $2^{14}/f_X$, $2^{19}/f_X$, or $2^{21}/f_X$ is available by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation settling time selection register (OSTS).

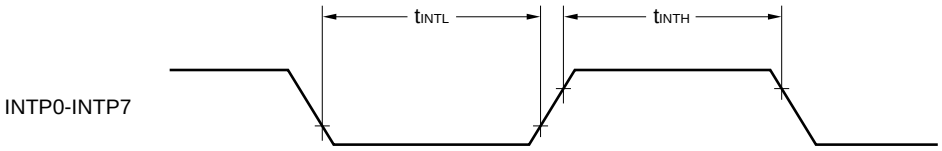
DATA RETENTION TIMING (STOP mode release by $\overline{RESET}$)



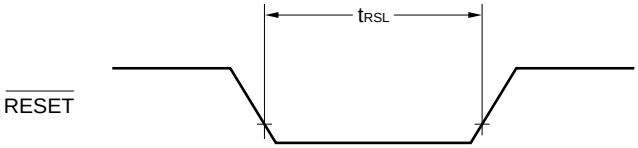
DATA RETENTION TIMING (standby release signal: STOP mode release by interrupt signal)



INTERRUPT REQUEST INPUT TIMING

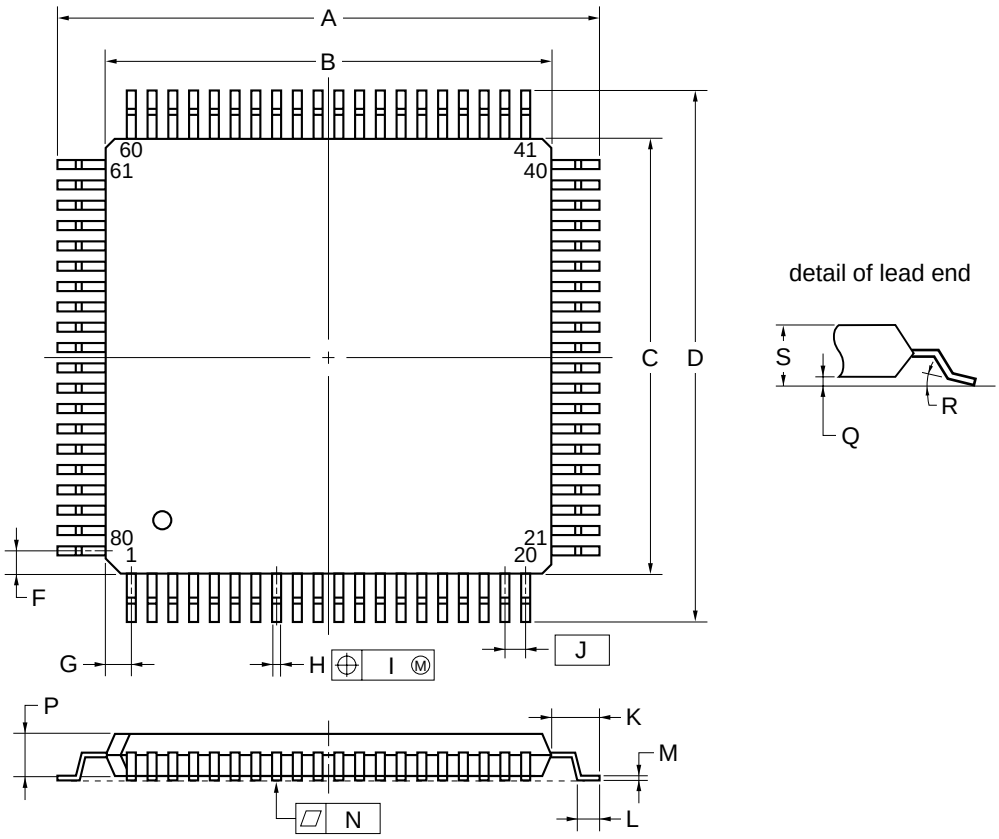


$\overline{\text{RESET}}$ INPUT TIMING



8. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD78F0701Y.
Be sure to see notes described in **(5)**.

(1) Language processing software

RA78K/0	Assembler package used in common with the 78K/0 series
CC78K/0	C compiler package used in common with the 78K/0 series
DF780701[Note]	Device file for the μPD780701Y sub-series
CC78K/0-L	C compiler library source file used in common with the 78K/0 series

Note Under development

(2) Flash memory write tools

★	Flashpro III (model No. FL-PR3, PG-FP3)	Flash writer used only for microcontrollers with internal flash memory
	FA-80GC	Flash memory write adapter. Connect this adapter to the Flashpro III. This adapter is dedicated to the 80-pin plastic QFP (GC-8BT type).
★	Floashpro III controller	Program controlled by a personal computer and which is supported by Flashpro III. Runs under Windows™ 95, etc.

(3) Debugging tools

- **When in-circuit emulator IE-78K0-NS is used**

	IE-78K0-NS	In-circuit emulator used in common with the 78K/0 series
	IE-70000-MC-PS-B	Power supply unit for the IE-78K0-NS
	IE-70000-98-IF-C	Interface adapter required when a PC-9800 series computer (other than a notebook type) is used as the host machine (C bus supported)
★	IE-70000-CD-IF-A	PC card and interface cable required when a notebook-type computer is used as the host machine (PCMCIA socket supported)
	IE-70000-PC-IF-C	Interface adapter required when an IBM PC/AT™ or compatible is used as the host machine (ISA bus supported)
★	IE-70000-PCI-IF	Interface adapter when using PC that incorporates PCI bus as host machine
	IE-780701-NS-EM1[Note]	Emulation board used to emulate the μPD780701Y sub-series products
	NP-80GC	Emulation probe dedicated to the 80-pin plastic QFP (GC-8BT type)
	EV-9200GC-80	Conversion socket for connecting the target system board created for the 80-pin plastic QFP (GC-8BT type) with the NP-80GC
	ID78K0-NS	Integrated debugger for IE-78K0-NS
	SM78K0	System simulator used in common with the 78K/0 series
	DF780701[Note]	Device file for the μPD780701Y sub-series

Note Under development

- **When in-circuit emulator IE-78001-R-A is used**

IE-78001-R-A	In-circuit emulator used in common with the 78K/0 series
★ IE-70000-98-IF-C	Interface adapter required when a PC-9800 series computer (other than a notebook type) is used as the host machine (C bus supported)
★ IE-70000-PC-IF-C	Interface adapter required when an IBM PC/AT or compatible is used as the host machine (ISA bus supported)
★ IE-70000-PCI-IF	Interface adapter when using PC that incorporates PCI bus as host machine
IE-78000-R-SV3	Interface adapter and cable required when an EWS is used as the host machine
IE-780701-NS-EM1[Note]	Emulation board used to emulate the μPD780701Y sub-series
IE-78K0-R-EX1	Emulation probe conversion board required when the IE-780701-NS-EM1 is used with the IE-78001-R-A
EP-78230GC-R	Emulation probe dedicated to the 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket for connecting the target system board created for the 80-pin plastic QFP (GC-8BT type) with the EP-78230GC-R
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator used in common with the 78K/0 series
DF780701[Note]	Device file for the μPD780701Y sub-series

Note Under development

(4) Real-time OS

RX78K/0	Real-time OS for the 78K/0 series
MX78K0	OS for the 78K/0 series

(5) Notes on using development tools

- ID78K0-NS, ID78K0, and SM78K0 are to be used in combination with DF780701.
- CC78K/0 and RX78K/0 are to be used in combination with RA78K/0 and DF780701.
- FL-PR3, FA-80GC, and NP-80GC are manufactured by Naito Densei Machida Mfg. Co., Ltd. (044-822-3813). Contact NEC sales representatives for purchase.
- For third party development tools, refer to the **78K/0 Series Selection Guide** (U11126E).
- The host machines and OSs supporting each software product are as follows:

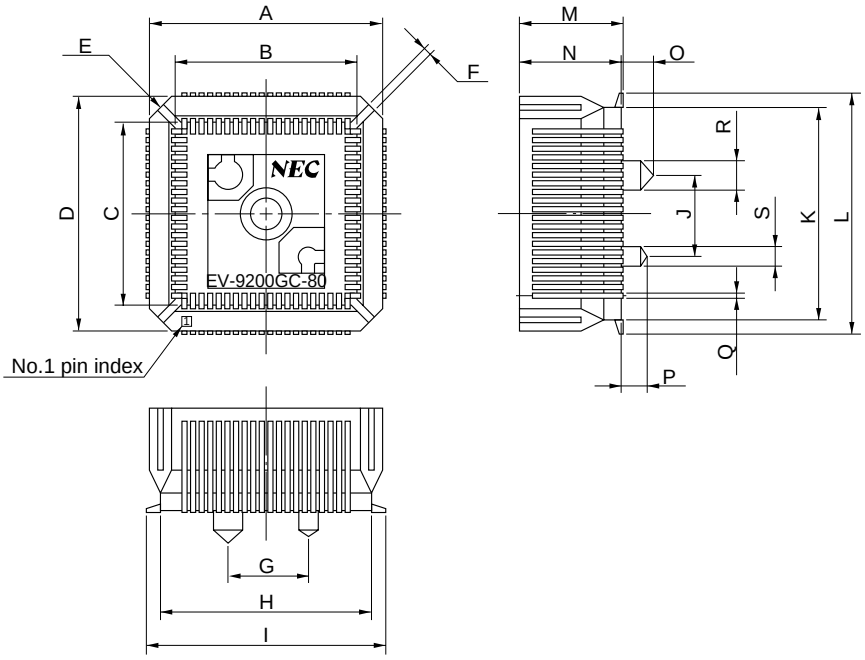
Host machine [OS] / Software	PC PC-9800 series [Windows] IBM PC/AT and compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	O[Note]	O
CC78K/0	O[Note]	O
ID78K0-NS	O	-
ID78K0	O	O
SM78K0	O	-
RX78K/0	O[Note]	O
MX78K0	O[Note]	O

Note DOS-based software

PACKAGE DRAWINGS OF THE CONVERSION SOCKET (EV-9200GC-80) AND RECOMMENDED PATTERN ON BOARDS

Figure A-1. Package Drawings of the EV-9200GC-80 (Reference)

Based on EV-9200GC-80
(1) Package drawing (in mm)

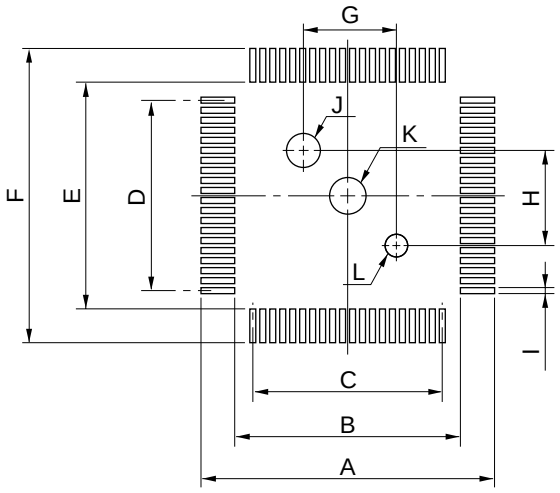


EV-9200GC-80-G0E

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
O	8.0	0.315
N	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	1.5	0.059

Figure A-2. Recommended Pattern for Mounting the EV-9200GC-80 on Boards (Reference)

Based on EV-9200GC-80
(2) Pad drawing (in mm)



EV-9200GC-80-P1E

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
D	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}$ $0.748=0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
H	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

APPENDIX B RELATED DOCUMENTS

- **Documents related to devices**

	Document name	Document No.	
		Japanese	English
★	μPD780701Y Sub-Series User's Manual	U13781J	U13781E
★	μPD780701Y, 780702Y Preliminary Product Information	U13920J	U13920E
★	μPD78F0701Y Preliminary Product Information	U13563J	This manual
	78K/0 Series User's Manual, Instruction	U12326J	U12326E

- **Documents related to development tools (user's manual)**

Document name		Document No.	
		Japanese	English
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Language	U11801J	U11801E
	Structured Assembly Language	U11789J	U11789E
RA78K Series Structured Assembler Preprocessor		U12323J	EEU-1402
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming Know-How	U13034J	U13034E
IE-78K0-NS		To be created	To be created
IE-78001-R-A		To be created	To be created
IE-78K0-R-EX1		To be created	To be created
IE-780701-NS-EM1		To be created	To be created
EP-78230		EEU-985	EEU-1515
SM78K0 System Simulator Windows Base	Reference	U10181J	U10181E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K0-NS Integrated Debugger Windows Base	Reference	U12900J	U12900E
ID78K0 Integrated Debugger EWS Base	Reference	U11151J	-
ID78K0 Integrated Debugger Windows Base	Guide	U11649J	U11649E
ID78K0 Integrated Debugger PC Base	Reference	U11539J	U11539E

- **Documents related to software to be incorporated into the product (user's manual)**

Document name		Document No.	
		Japanese	English
78K/0 Series Real-Time OS	Basic	U11537J	U11537E
	Installation	U11536J	U11536E
OS for 78K/0 Series MX78K0	Basic	U12257J	U12257E

- **Other documents**

Document name	Document No.	
	Japanese	English
★ NEC IC Package Manual (CD-ROM)	-	C13388E
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Semiconductor Device Quality Control/Reliability Handbook	C12769J	-
Guide for Products Related to Micro-Computer: Other Companies	U11416J	-

Caution The above documents may be revised without notice. Use the latest versions when you design an application system.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Caution This product contains an I^2C bus interface circuit.
When using the I^2C bus interface, notify its use to NEC when ordering custom code. NEC can guarantee the following only when the customer informs NEC of the use of the interface:
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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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800-729-9288

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Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
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- Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
- Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.

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