Advance Data Sheet
January 1992

AT&T Microelectronics

ATT7C342 High-Speed CMOS 1 Mbit (64K x 16) SRAM Synchronous, Pipelined Architecture TTL Compatible Common I/O

Features

- High speed—10 ns maximum access times
- Fast read/write cycle times: 20 ns min (50 MHz)
- Ideally suited as high-speed cache memory for RISC applications
- Internal self-timed write pulse generation
- Fully pipelined architecture
- Registered addresses, data I/O, and control inputs
- Low-power operation
- Advanced 0.5 µm CMOS technology
- Available in 52-pin, PLCC package

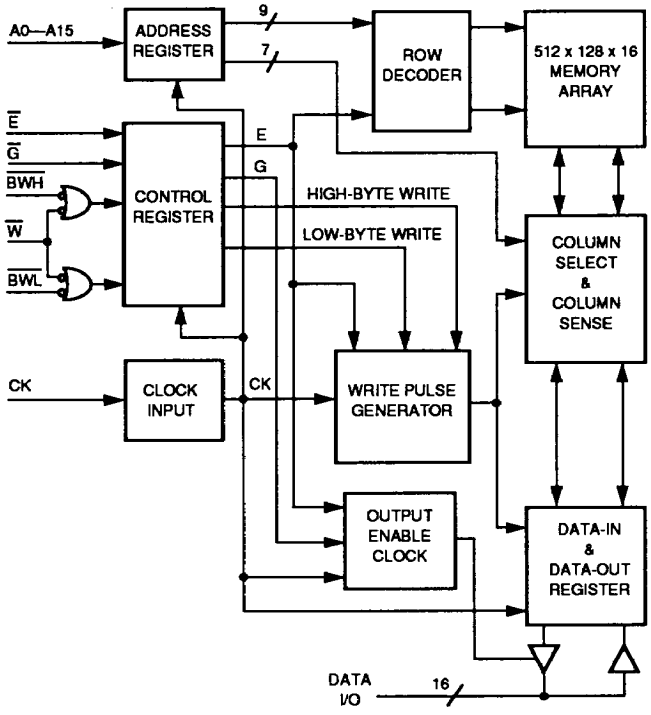
Description

The ATT7C342 devices are high-performance, CMOS static RAMs organized as 65,536 words by 16 bits. The data-in and data-out signals share I/O pins. The device has single chip enable and an output enable. The output is 3-stated when either chip enable or output enable is high.

The address (A0—A15), data-in outputs (I/O0—I/O15), write enable ($\overline{WE}$), high byte write enable ($\overline{BWH}$), low byte write enable ($\overline{BWL}$), chip enable ($\overline{CE}$), and output enable ($\overline{OE}$) are latched, positive edge-triggered registers.

Output registers provide full pipelined operation. At the rising edge of the clock, the output from the previous cycle is presented.

Inputs and outputs are TTL compatible. Operation is from a single 5 V power supply. Power consumption is 625 mW (typical) at 20 ns cycle time. Dissipation drops to 500 µW (typical) when the memory is in standby mode.



Pin Information

Table 1. Pin Descriptions

Pin	Function
A0—A15	Address Inputs
I/O0—I/O15	Data Input/Output
CLK	Clock Input
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{BWL}$	Lower Byte Write Enable
$\overline{BWH}$	Upper Byte Write Enable
GND	Ground
Vcc	+5 V Supply
NC	No Connection

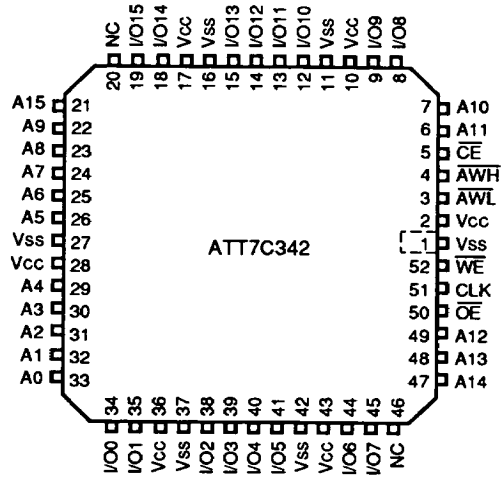


Figure 2. Pin Diagram

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those indicated in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	150	°C
Operating Ambient Temperature	T_A	–55	125	°C
Supply Voltage with Respect to Ground	Vcc	–0.5	7.0	V
Input Signal with Respect to Ground	—	–3.0	7.0	V
Signal Applied to High-impedance Output	—	–3.0	7.0	V
Output Current into Low Outputs	—	—	25	mA
Latch-up Current	—	>200	—	mA

Handling Precautions

The ATT7C342 device includes internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation	0 °C to 70 °C	4.5 V ≤ Vcc ≤ 5.5 V

Electrical Characteristics

Over all Recommended Operating Conditions.

Table 2. General Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage:						
High	V_{OH}	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4	—	—	V
Low	V_{OL}	I_{OL} = 8.0 mA, V_{CC} = 4.5 V	—	—	0.4	V
Input Voltage:						
High	V_{IH}	—	2.0	—	V_{CC} + 0.3	V
Low	V_{IL}	—	–1.0	—	0.8	V
Input Current	I_{IX}	Ground ≤ V_{IN} ≤ V_{CC}	–10	—	10	µA
Output Leakage Current	I_{OZ}	$\overline{CE}$ is high	–10	—	10	µA
Vcc Current:						
Active[1]	I_{CC1}	—	—	150	300	mA
Inactive[2]	I_{CC2}	—	—	50	80	mA
Standby[3]	I_{CC3}	—	—	100	1,000	µA
Capacitance:						
Input	C_I	—	—	—	5	pF
Output	C_O	—	—	—	7	pF

1. Tested with outputs open, all address and data inputs at TTL level, and the clock running at maximum cycle rate. The device is continously enabled for writing, i.e., $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ ≤ V_{IL}.
2. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = Vcc. Input levels are within 0.2 V of Vcc or ground. Clock is continuously running at maximum cycle rate.
3. $\overline{CE}$ must be ≥ Vcc – 0.2 V. All other inputs must be at either Vcc or ground level to ensure full powerdown. Clock must be running at least two cycles and stop at either Vcc or ground level.

Timing Characteristics

Table 3. Read Cycle

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of <2.4 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3 V (see Figure 9), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 8A).

Symbol	Parameter	Min	Max
tCKHCKH	Read Cycle Time	20	—
tCKHDOV	Clock Access Time	—	10
tCKHDOX	Output Active from Clock High	1.5	—
tCKHDOZ	Clock High to Q High Z ($\overline{OE}$ = V_{IH}) (See Figure 8B.)	—	6
tCKLCKH	Clock Low Pulse Width	7	—
tCKHCKL	Clock High Pulse Width	7	—
tADVCKH	Setup Time for AD	3	—
tCEVCKH	Setup Time for $\overline{CE}$	3	—
tOEVCKH	Setup Time for $\overline{OE}$	3	—
tWEVCKH	Setup Times for $\overline{WE}$, $\overline{BWH}$, $\overline{BWL}$	3	—
tCKHADX	Hold Time for AD	3	—
tCKHCEX	Hold Time for $\overline{CE}$	3	—
tCKHOEX	Hold Time for $\overline{OE}$	3	—
tCKHWEX	Hold Time for $\overline{WE}$	3	—

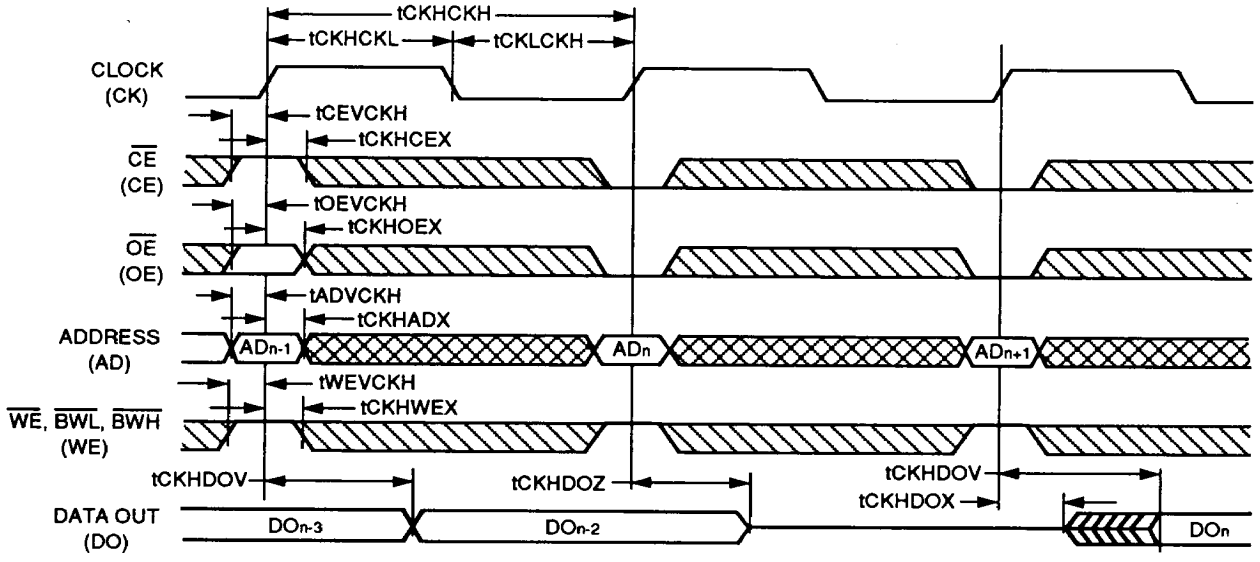
Timing Characteristics (continued)

Table 4. Write Cycle

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of <2.4 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3 V (see Figure 9), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 8A).

Symbol	Parameter	Min	Max
tCKHCKH	Write Cycle Time	20	—
tCKHDOZ	Clock High to Q High Z ($\overline{OE}$ = V_{IH}) (See Figure 8B.)	—	6
tCKLCKH	Clock Low Pulse Width	7	—
tCKHCKL	Clock High Pulse Width	7	—
tADVCKH	Setup Time for AD	3	—
tCEVCKH	Setup Time for $\overline{CE}$	3	—
tOEVCKH	Setup Time for $\overline{OE}$	3	—
tWEVCKH	Setup Times for $\overline{WE}$, $\overline{BWH}$, $\overline{BWL}$	3	—
tCKHADX	Hold Time for AD	3	—
tCKHCEX	Hold Time for $\overline{CE}$	3	—
tCKHDOX	Hold Time for $\overline{OE}$	3	—
tCKHWEX	Hold Time for $\overline{WE}$	3	—
tDIVCKH	Data-in Valid to Clock High	3	—
tCKHDIX	Data-in Hold Time	3	—
tCKHDOX	Output Active from Clock High	1.5	—
tCKHDOV	Clock High to Data-out Valid	—	10

Timing Diagrams



Notes:
When the $\overline{CE}$ is high, regardless of the $\overline{OE}$ level, the outputs 3-state.

The outputs Qn-3 and Qn-2 are from two previous cycles where $\overline{WE}$ is high, and $\overline{CE}$ and $\overline{OE}$ are low.

Figure 3. Read Cycle 1

Timing Characteristics (continued)

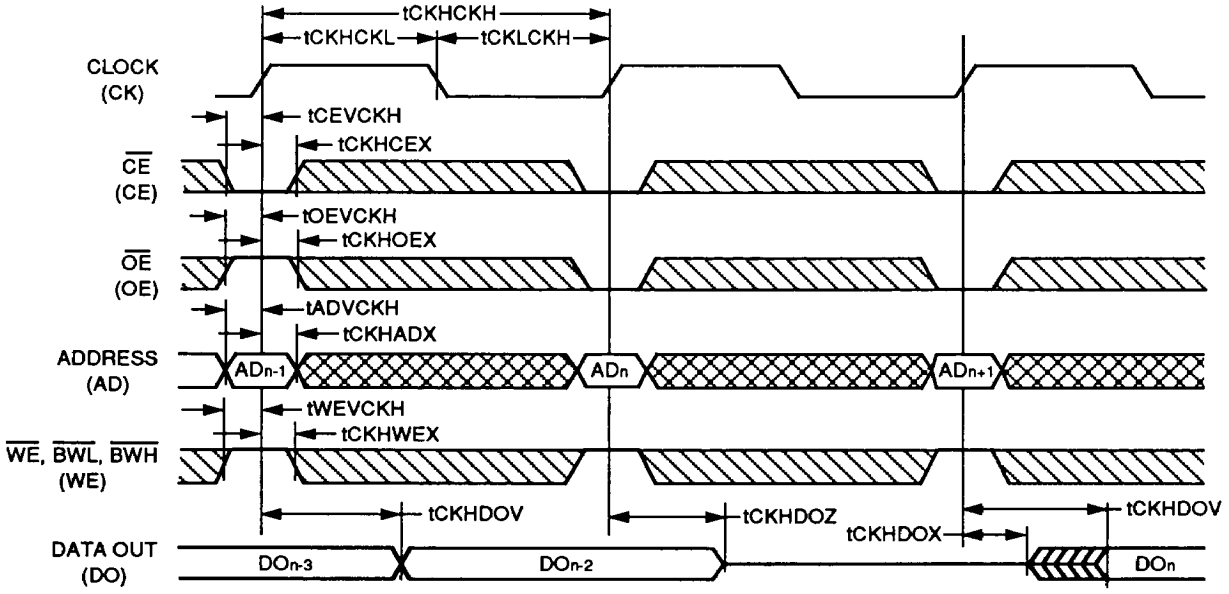


Figure 4. Read Cycle 2

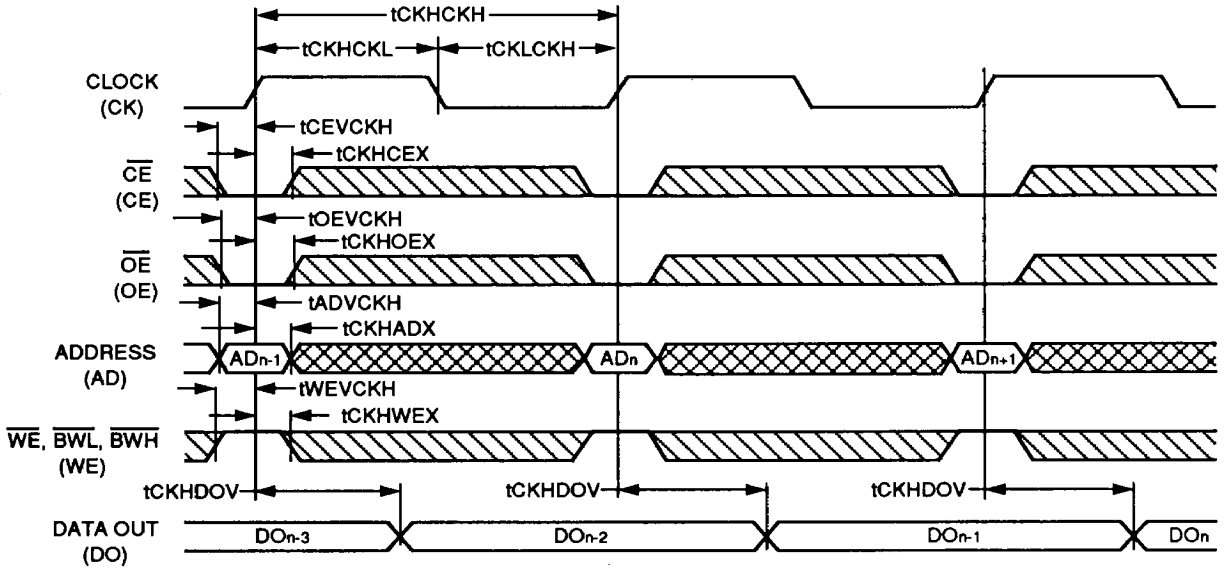
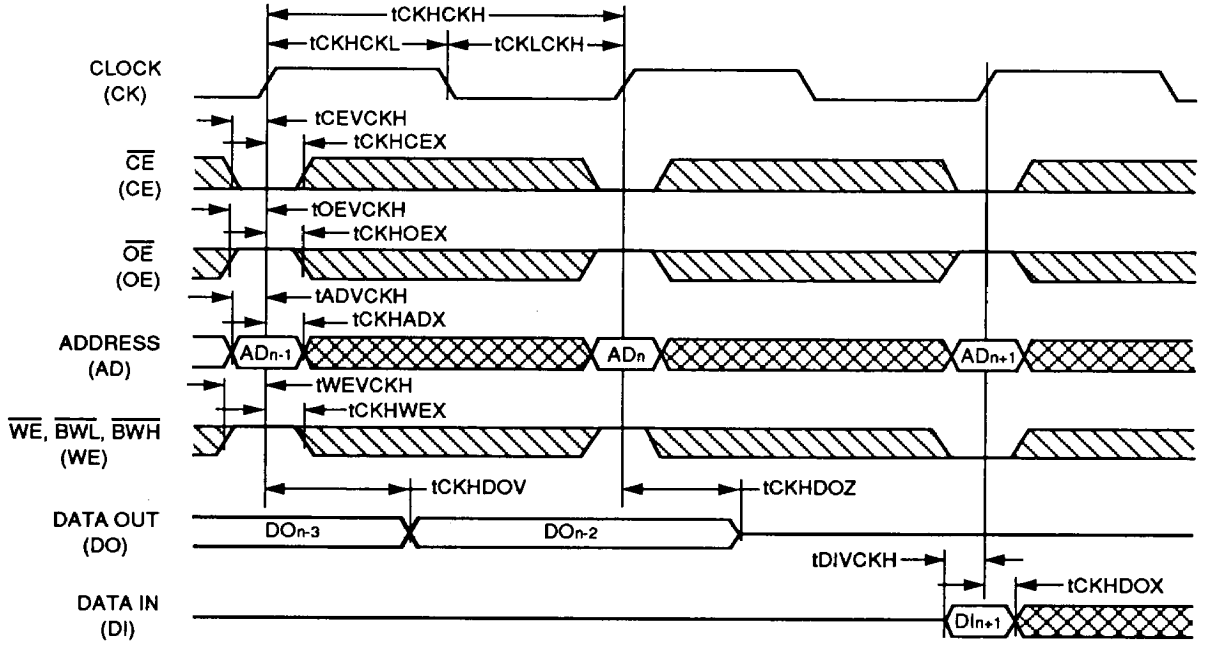


Figure 5. Read Cycle 3

Timing Characteristics (continued)



Notes:
Since the device has common I/O, the data out must be 3-stated before the data in can be applied. It is recommended that the data in is applied in the next cycle. $\overline{OE}$ must be latched in high in the previous cycle.

The outputs Qn-3 and Qn-2 are from two previous cycles where $\overline{WE}$ is high, $\overline{CE}$ and $\overline{OE}$ are low.

Figure 6. Write Cycle

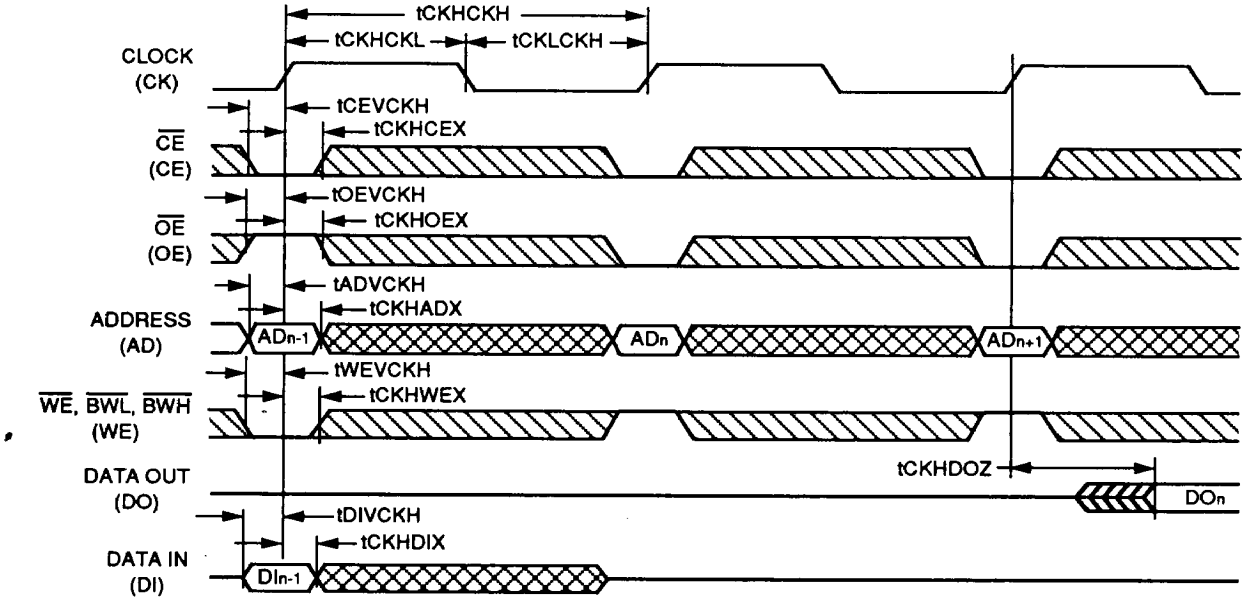


Figure 7. Write/Read Cycle

Timing Characteristics (continued)

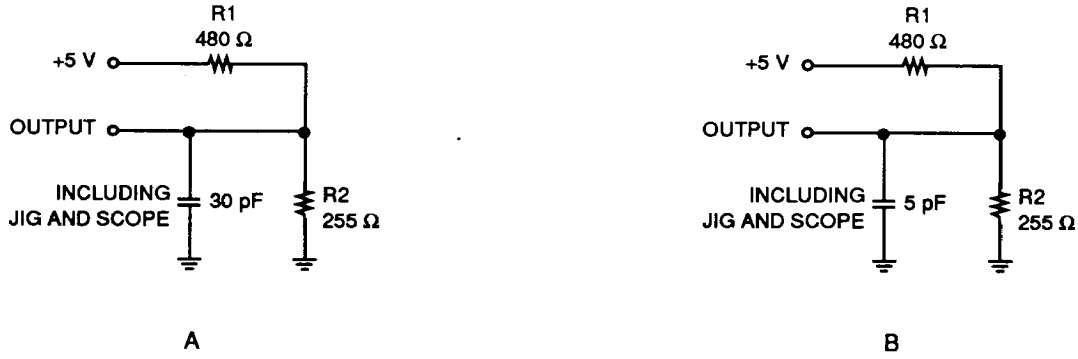


Figure 8. Test Loads

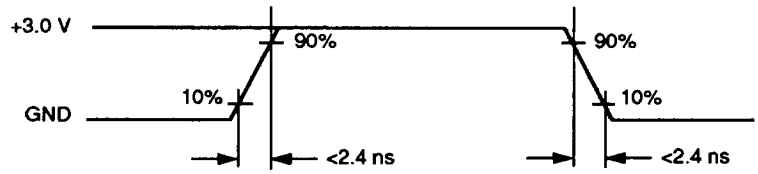
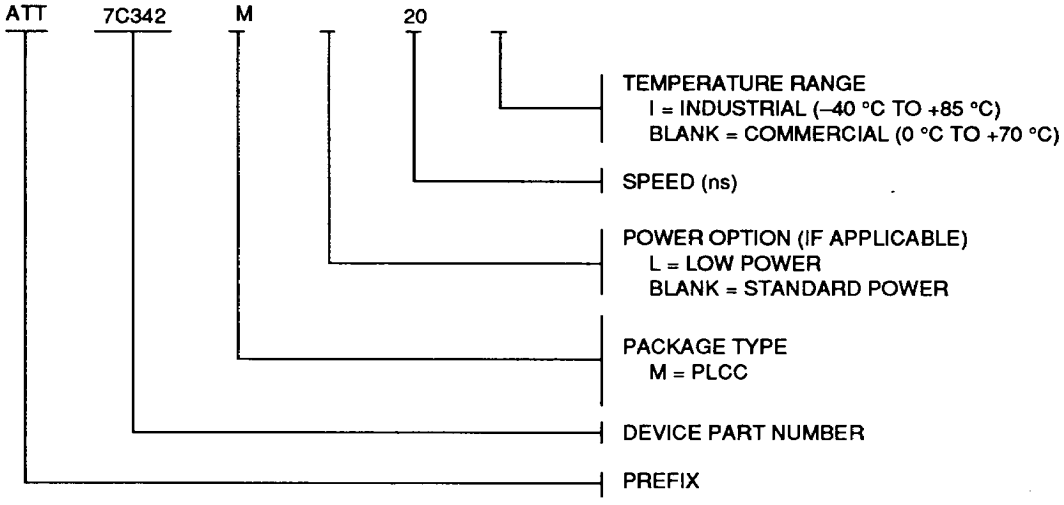


Figure 9. Transition Times

Ordering Information



Operating Range 0 °C to 70 °C

Package Style	Performance Speed	
	25 ns	20 ns
52-Pin PLCC	ATT7C342M–25	ATT7C342M–20

For additional information, contact your AT&T Account Manager or the following:
U.S.A.: AT&T Microelectronics, Dept. AL-520404200, 555 Union Boulevard, Allentown, PA 18103
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Tel. (03) 5371-2700, FAX (03) 5371-3556
SPAIN: AT&T Microelectronica de España, Poligono Industrial de Tres Cantos (Zona Oeste), 28770 Colmenar Viejo, Madrid, Spain
Tel. (34) 1-8071441, FAX (34) 1-8071420

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