

SONY**CXK581020SP/J** -35/45/55**131072-word × 8-bit High Speed CMOS Static RAM****Description**

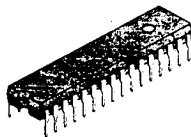
CXK581020SP/J are 131,072-word × 8-bit high speed CMOS static RAMs suitable for use in high speed and low power applications.

Organized as 131,072 words by 8 bits, it operates from a single 5V supply.

Features

- Fast access time : (Access time)
CXK581020SP/J-35 35ns (Max.)
CXK581020SP/J-45 45ns (Max.)
CXK581020SP/J-55 55ns (Max.)
- Low power operation : (Operation)
CXK581020SP/J-35, 45, 55 300mW (Typ, Cycle = Min.)
- Single +5V supply : +5V ± 10 %
- Fully static memory ... No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible : All inputs and outputs.
- Available in 32 pin 400-mil DIP and 400-mil SOJ

CXK581020SP
32 pin DIP (Plastic)



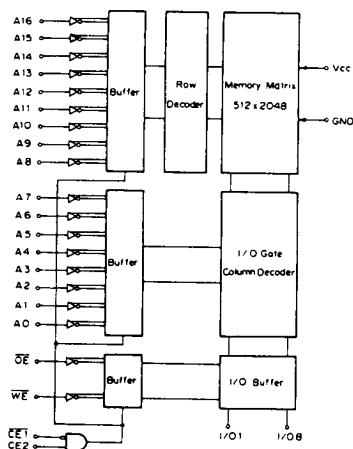
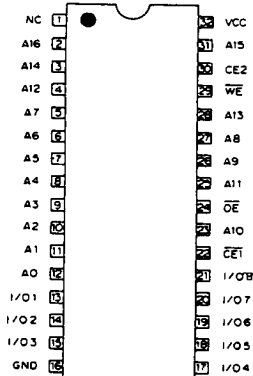
CXK581020J
32 pin SOJ (Plastic)

**Function**

131,072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration
(Top View)****Pin Description**

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V Power supply
GND	Ground
NC	No connection

E89612BOY - ST

Absolute Maximum Ratings

(Ta = 25 °C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* **Note)** V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V _{CC} current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC2}
L	H	L	H	Read	Data out	I _{CC2}
L	H	X	L	Write	Data in	I _{CC2}

Note) X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70 °C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* **Note)** V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics**DC and operating characteristics**(V_{CC} = 5V ± 10 %, GND = 0V, T_a = 0 to + 70 °C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	- 2	—	2	μA
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL}	- 2	—	2	μA
Operating power supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	—	—	mA
Average operating current	I _{CC2}	Cycle = Min., Duty = 100 %, I _{OUT} = 0mA	—	—	130	mA
Standby current	I _{SB1}	CE1 ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	0.01	2	mA
	I _{SB2}	CE1 = V _{IH} or CE2 = V _{IL} , Cycle = Min.	—	—	55	mA
Output high voltage	V _{OH}	I _{OH} = - 4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

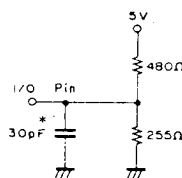
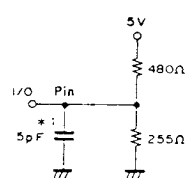
* **Note)** V_{CC} = 5V, T_a = 25 °C**I/O capacitance**(T_a = 25 °C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100 % tested.**AC characteristics**• **AC test conditions** (V_{CC} = 5V ± 10 %, T_a = 0 to + 70 °C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load	Fig. 1

Output Load (1)

Output Load (2)^{*2}* 1. C_L includes scope and jig capacitances.* 2. For t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{CHZ}, t_{OW}, t_{WHZ}**Fig. 1**

• Read cycle

Item	Symbol	-35		-45		-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	35	—	45	—	55	—	ns
Address access time	t _{AA}	—	35	—	45	—	55	ns
Chip enable access time ($\overline{\text{CE1}}$)	t _{CO1}	—	35	—	45	—	55	ns
Chip enable access time (CE2)	t _{CO2}	—	35	—	45	—	55	ns
Output enable to output valid	t _{OE}	—	20	—	25	—	30	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{\text{CE1}}$, CE2)	t _{LZ1} *, t _{LZ2} *	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{\text{CE1}}$, CE2)	t _{HZ1} *, t _{HZ2} *	0	15	0	20	0	25	ns
Chip disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	0	15	0	20	0	25	ns
Chip enable to power up time ($\overline{\text{CE1}}$, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip enable to power down time ($\overline{\text{CE1}}$, CE2)	t _{PD}	—	35	—	45	—	55	ns

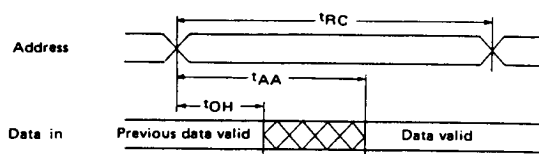
• Write cycle

Item	Symbol	-35		-45		-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t _{AW}	30	—	40	—	45	—	ns
Chip enable to end of write	t _{CW}	30	—	40	—	45	—	ns
Data to write time overlap	t _{DW}	18	—	20	—	25	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	30	—	35	—	40	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$, $\overline{\text{CE1}}$)	t _{WR1}	3	—	3	—	3	—	ns
Write recovery time (CE2)	t _{WR2}	5	—	5	—	5	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	15	0	15	0	15	ns

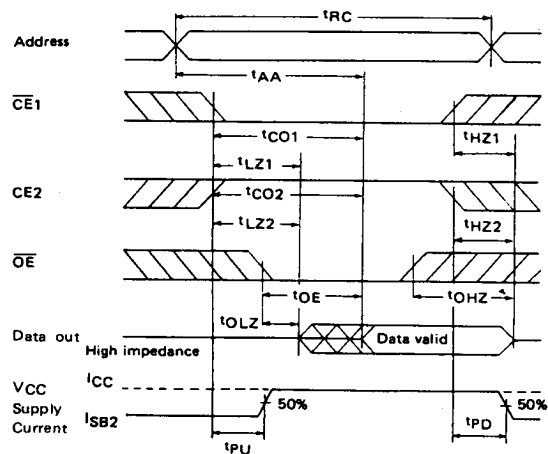
* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1 (2). This parameter is sampled and not 100% tested.

Timing Waveform

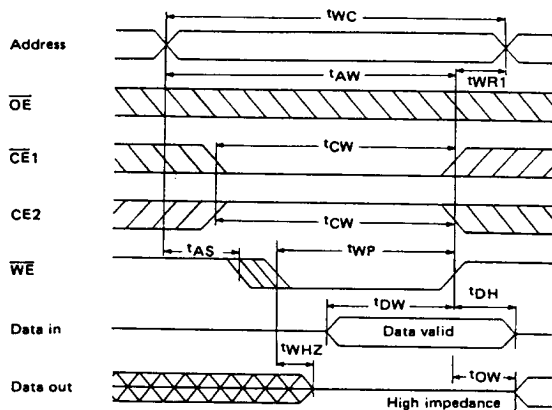
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



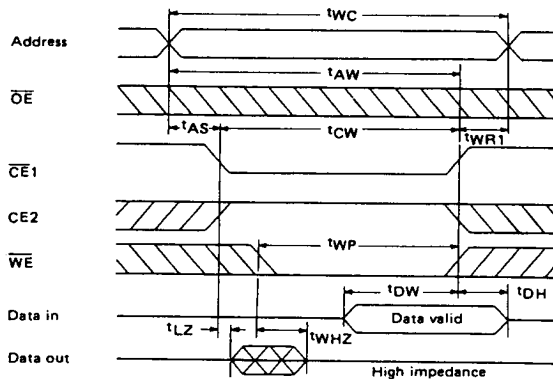
- Read cycle (2) : $\overline{WE} = V_{IH}$



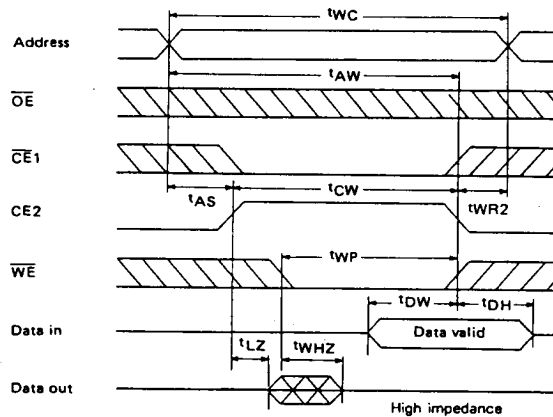
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{\text{CE1}}$ control



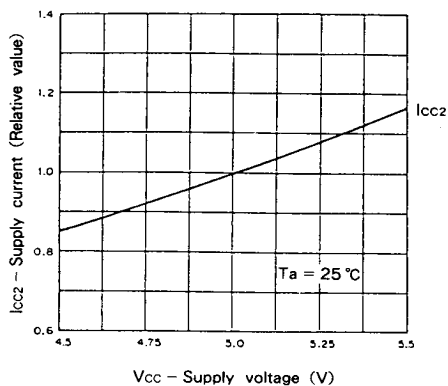
• Write cycle (3) : CE2 control



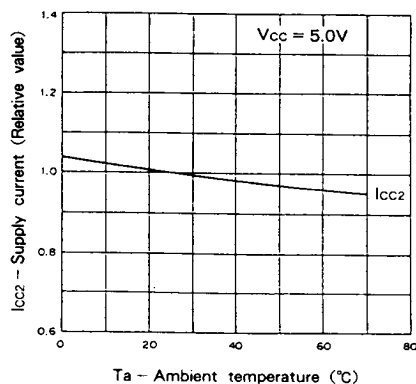
Note) During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Example of Representative Characteristics

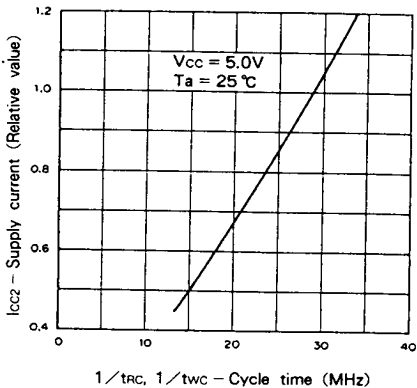
Supply current vs. Supply voltage



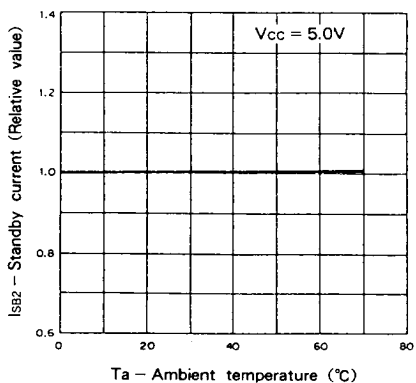
Supply current vs. Ambient temperature



Supply current vs. Cycle time

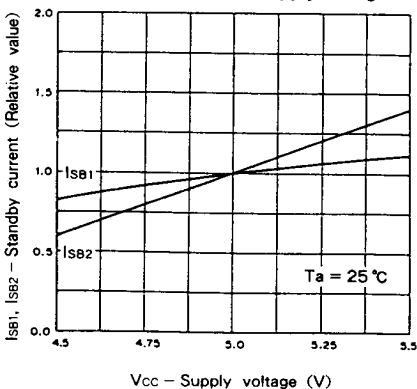


Standby current vs. Ambient temperature

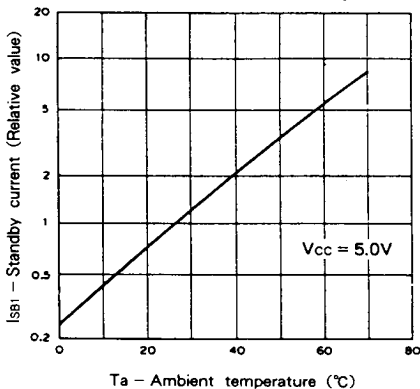


1/trc, 1/twc - Cycle time (MHz)

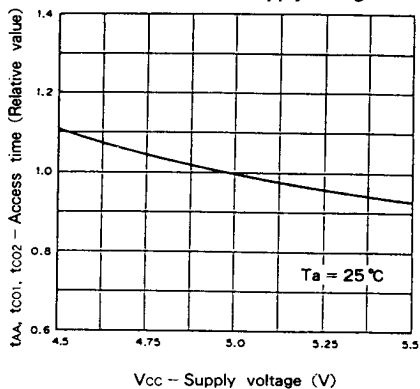
Standby current vs. Supply voltage



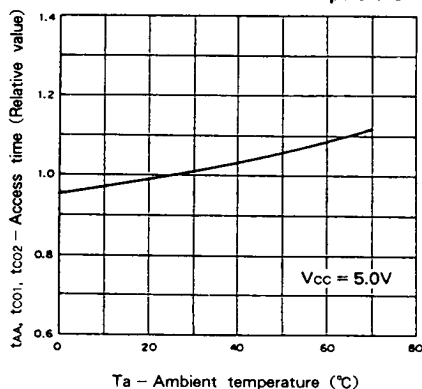
Standby current vs. Ambient temperature



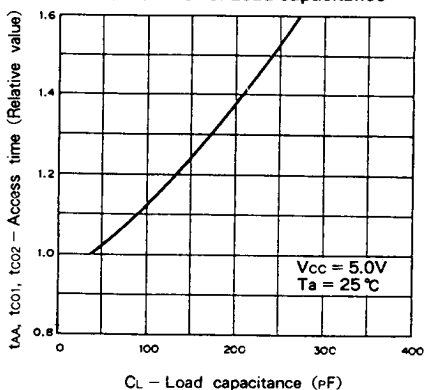
Access time vs. Supply voltage



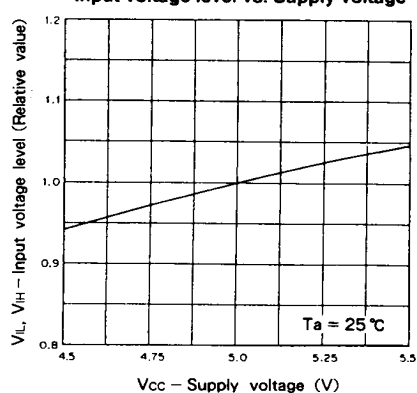
Access time vs. Ambient temperature



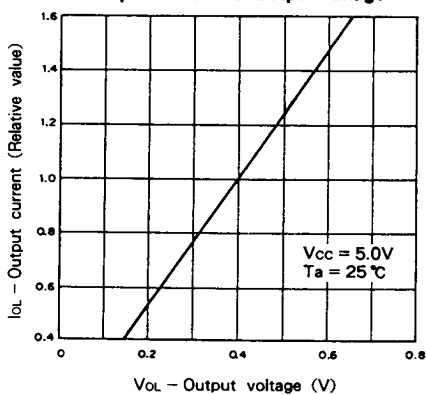
Access time vs. Load capacitance



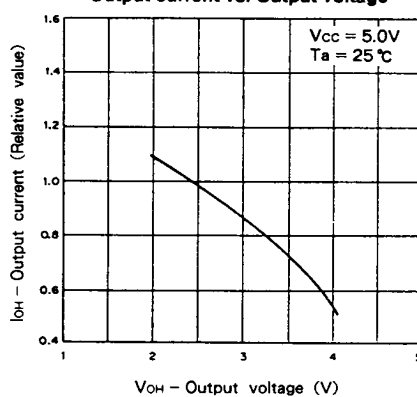
Input voltage level vs. Supply voltage



Output current vs. Output voltage

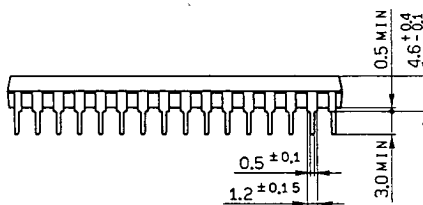
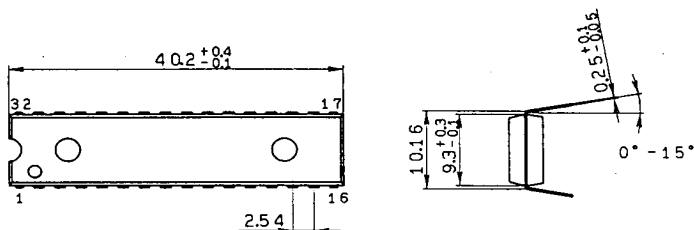


Output current vs. Output voltage



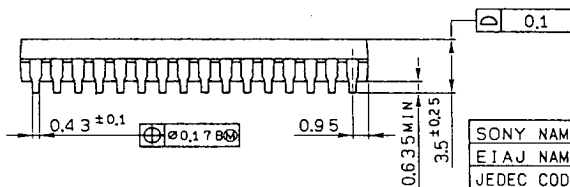
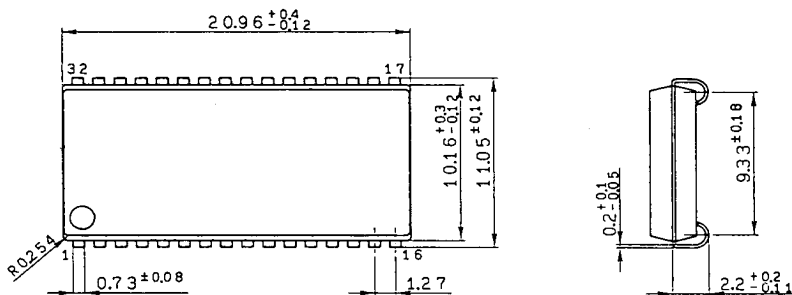
Package Outline Unit : mm

CXK581020SP 32 pin DIP (Plastic) 400mil 3.2g



SONY NAME	DIP-32P-02
EIAJ NAME	*DIP032-P-0400-A
JEDEC CODE	

CXK581020J 32 pin SOJ (Plastic) 400mil 1.3g



SONY NAME	SOJ-32P-01
EIAJ NAME	*SOJ032-P-0400-A
JEDEC CODE	