LH5316500

CMOS 16M (2M × 8 / 1M × 16) Mask-Programmable ROM

FEATURES

- 2,097,152 × 8 bit organization
  (Byte mode: $\overline{BYTE}$ = V_{IL})
  1,048,576 × 16 bit organization
  (Word mode: $\overline{BYTE}$ = V_{IH})
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 50 mA (MAX.)
  Standby: 100 µA (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP *
  44-pin, 600-mil SOP
  48-pin, 12 × 18 TSOP I
  64-pin, 14 × 20 mm^2 QFP

DESCRIPTION

The LH5316500 is a 16M-bit mask-programmable ROM organized as 2,097,152 × 8 bits (Byte mode) or 1,048,576 × 16 bits (Word mode) that can be selected by a $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

It provides high density and high speed access in a variety of packages including small and thin surface mount technology.

PIN CONNECTIONS

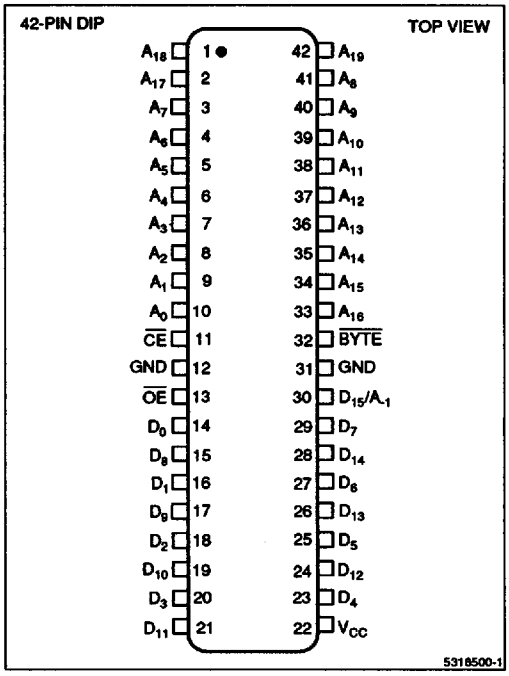

Figure 1. Pin Connections for DIP Package

* NOTE: For the 42-pin DIP, pin 30 becomes LSB address input (A_{-1}) when in byte mode, and data output (D_{15}) when in word mode.

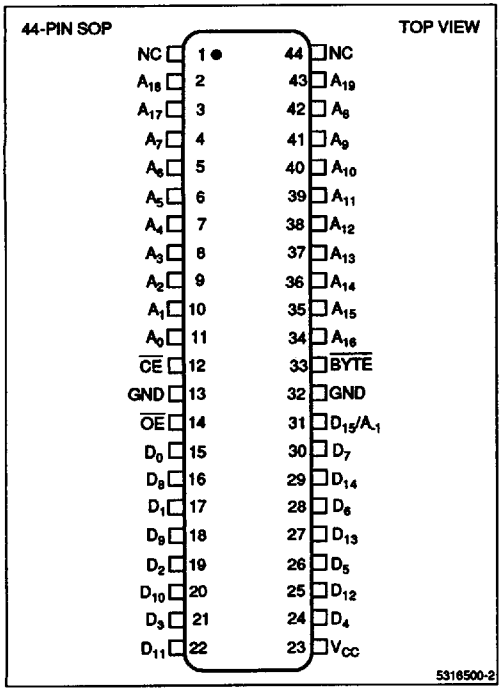

Figure 2. Pin Connections for SOP Package

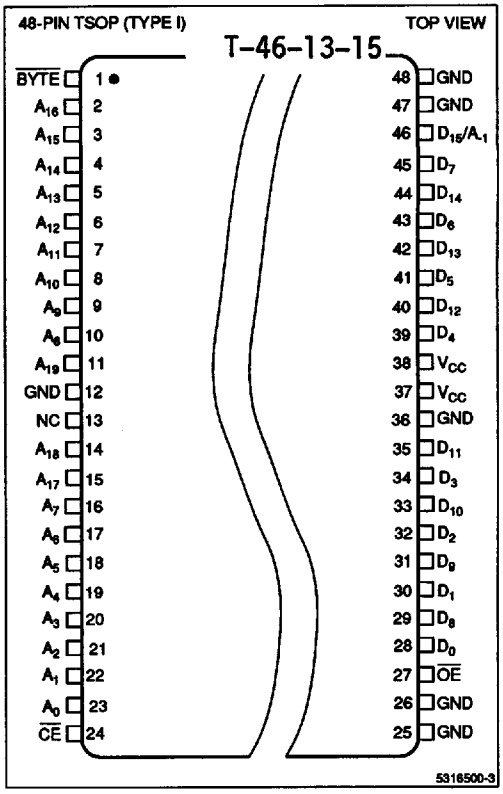

Figure 3. Pin Connections for TSOP Package (Type I)

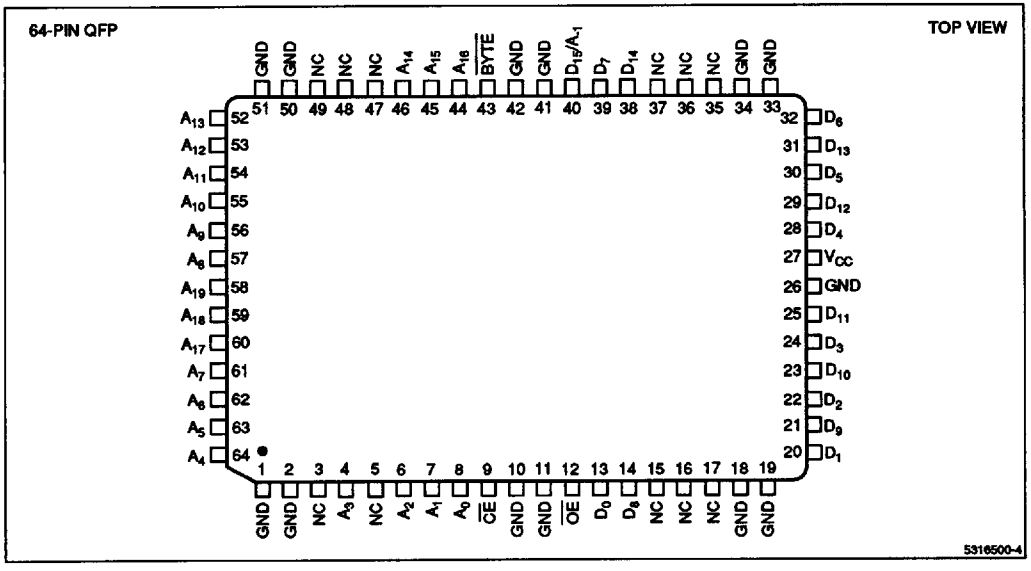

Figure 4. Pin Connections for QFP Package

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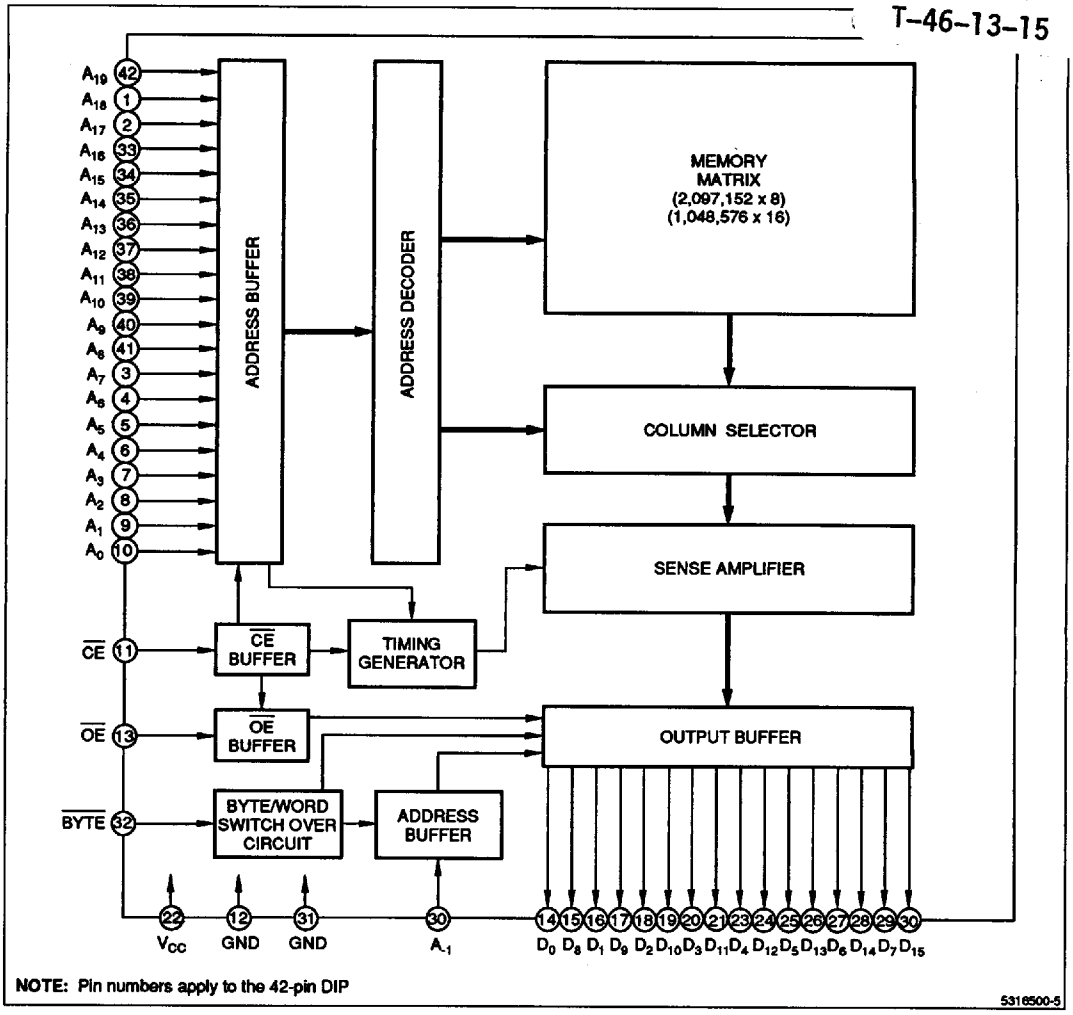

Figure 5. LH5316500 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_{19}	Address input
D_0 - D_{15}	Data output
$\overline{BYTE}$	8/16-bit (Byte/Word) mode switch input
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground
NC	No Connection

TRUTH TABLE

T-46-13-15

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		MODE	ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_7	D_8 - D_{16}		LSB	MSB	
H	X	X	X	High-Z	High-Z	High-Z	–	–	Standby
L	H	X	X	High-Z	High-Z		–	–	Operating
L	L	H	Inhibit	D_0 - D_7	D_8 - D_{15}	16-Bit	A_0	A_{19}	Operating
L	L	L	L	D_0 - D_7	High-Z	8-Bit	A_{-1}	A_{19}	Operating
L	L	L	H	D_8 - D_{15}	High-Z	8-Bit	A_{-1}	A_{19}	Operating

NOTE:
X = Don't Care; High-Z = High-Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "High" voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V, V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V, V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH} (Outputs open).
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL} (TTL level).

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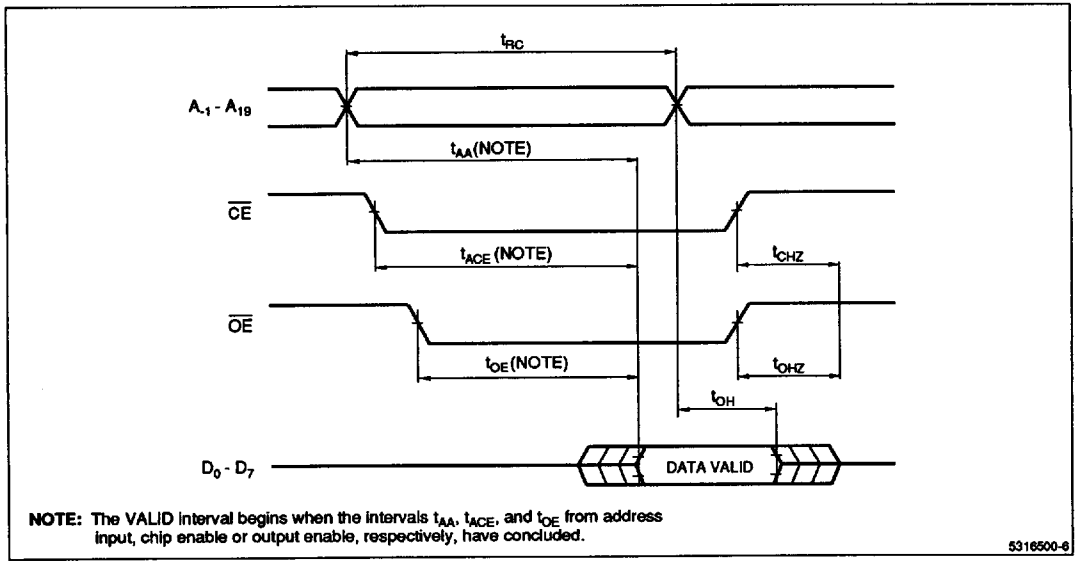
AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable access time	t_{ACE}		150	ns	
Output enable time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
Output floating time	t_{CHZ}		60	ns	1
	t_{OHZ}				

NOTE:
1. Determined by the time for the output to be opened, irrespective of output voltage.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V, 2.2 V
Output load condition	1TTL + 100 pF



NOTE: The VALID interval begins when the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively, have concluded.

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Figure 6. $\overline{BYTE}$ = V_{IL} in Byte Mode

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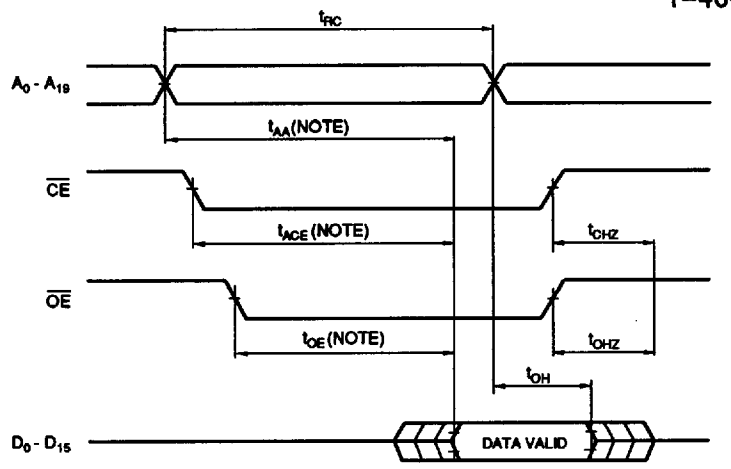

NOTE: The VALID interval begins when the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively, have concluded.

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Figure 7. $\overline{BYTE}$ = V_{IH} in Word Mode

ORDERING INFORMATION

LH5316500	X	-##
Device Type	Package	Speed

Speed: 15 150 Access Time (ns)

Package:
- D 42-pin, 600-mil DIP (DIP42-P-600)
- N 44-pin, 600-mil SOP (SOP44-P-600)
- M 64-pin, 14 x 20 mm² QFP (QFP64-P-1420)
- T 48-pin, 12 x 18 mm² TSOP (TSOP48-P-1218)

Device Type: CMOS 16M (2M x 8 OR 1M x 16) Mask Programmable ROM

Example: LH5316500D-15 (CMOS 16M (2M x 8) Mask-Programmable ROM, 150 ns, 42-pin, 600-mil DIP)

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