FEATURES

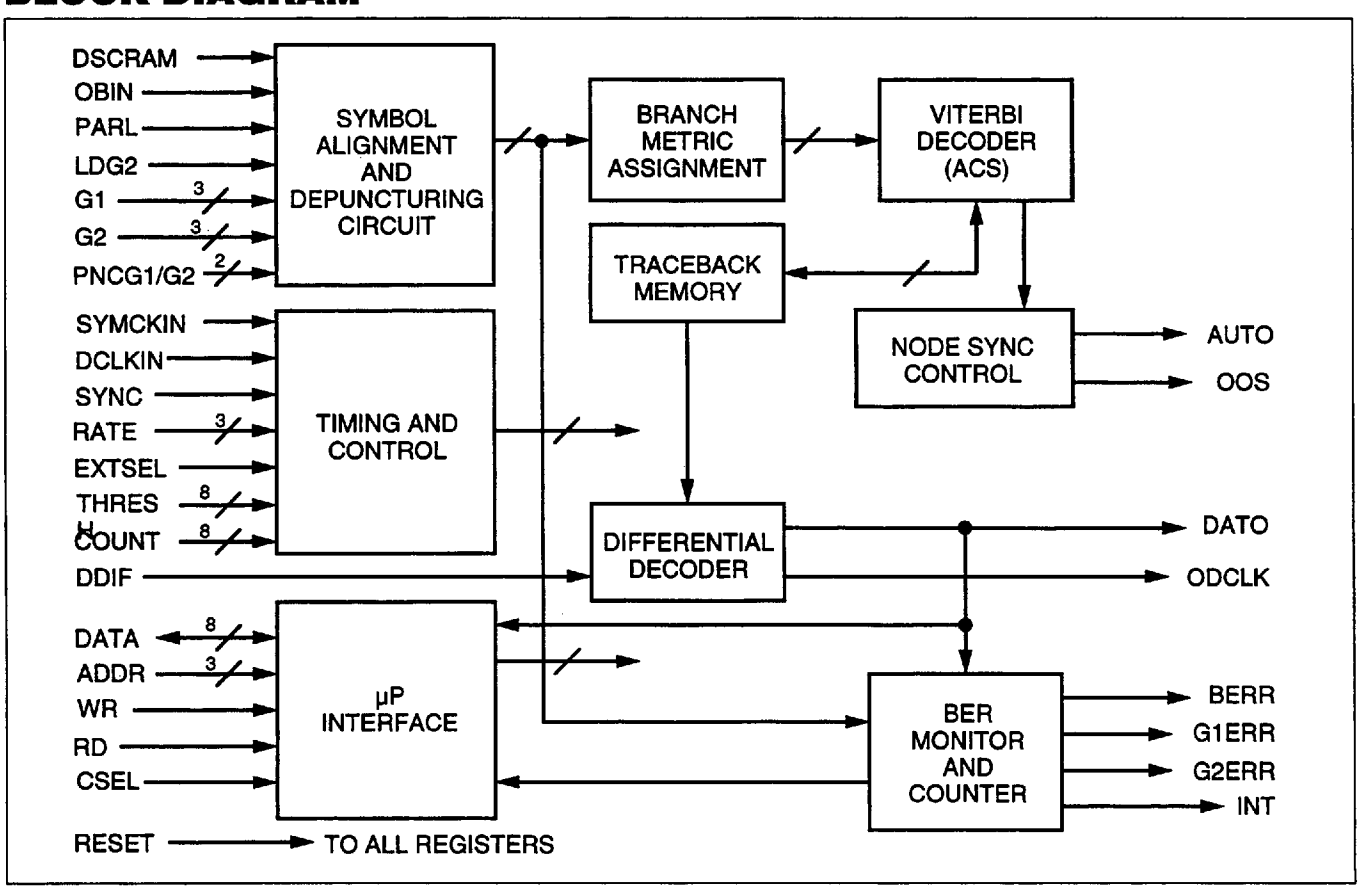
- **45 Mbps Operating Rate**
- **Constraint Length K = 7**
  $G_1 = 171_8$ $G_2 = 133_8$
- **Multiple Rates: Rate $^1/_2$ as well as Punctured codes at Rates $^2/_3$ through $^7/_8$**
- **Internal Depuncturing Capability at Rates $^2/_3$, $^3/_4$ and $^7/_8$**
- **Multiple Devices can be Multiplexed to Give Higher Data Rates**
- **Optimized Interface to Operate with BPSK and QPSK Demodulators**
- **Auto Node Sync Capability**
- **Differential Decoder**
- **"Invert G2" Descrambler**
- **Internal BER Monitor and BER Measurement Circuit**
- **5.2 dB Coding Gain @10^{-5} BER (R = $^1/_2$)**
- **100-pin PQFP Package**

FUNCTIONAL DESCRIPTION

Convolutional encoding and Viterbi decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. The STEL-2060 is a specialized product designed to perform this specific communications related function. At the encoder a stream of symbols is created which introduces a high degree of redundancy. This enables accurate decoding of the information despite a high symbol error rate resulting from an impaired communications link.

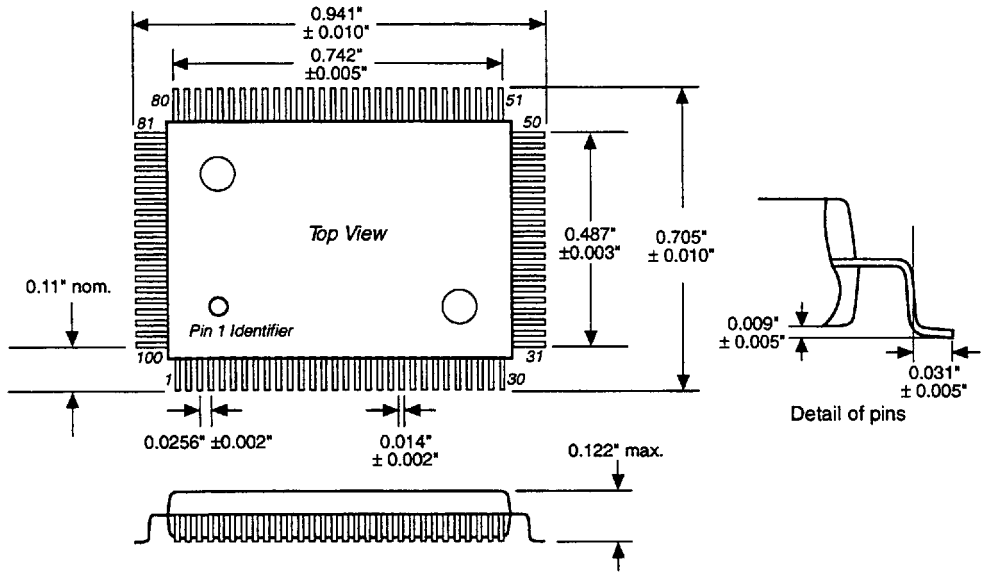
The STEL-2060 contains a K = 7 Viterbi Decoder. The data inputs can be in offset binary or offset signed-magnitude formats, with 3-bit soft decision. Auto node sync is provided for applications where symbol uncertainty can occur. Rate $^2/_3$, $^3/_4$, $^4/_5$, $^5/_6$, $^6/_7$ and $^7/_8$ punctured signals can be decoded, as well as non-punctured, Rate $^1/_2$, signals. The polynomials and puncturing patterns used are industry standards. Depuncturing logic is incorporated into the decoder to provide automatic depuncturing of received data at rates $^2/_3$, $^3/_4$ and $^7/_8$ when the puncturing patterns supported by the device are used. A BER monitor is also provided in the device, along with a circuit for computing the mean value of the BER over an extended period. These circuits operate with punctured codes as well as unpunctured. The STEL-2060 incorporates a descrambler for signals scrambled with the "Invert G2" algorithm. (With this method the G2 symbols are logically inverted at the encoder. This provides a very effective level of scrambling for the purpose of avoiding long strings of ones or zeroes in the transmitted signal using BPSK modulation.)

BLOCK DIAGRAM



PIN CONFIGURATION

Package: 100-pin PQFP
Thermal coefficient, θ_{ja} = 30° C/W



Notes: (1) Tolerances on pin spacing are not cumulative
(2) Dimensions shown are at seating plane
(3) I.C. denotes Internal Connection. This pin ***must*** be left unconnected. **Do not use for vias.**
(4) N.C. denotes No Connection. These pins can be used for vias.

PIN CONNECTIONS

1	V_{DD}	21	V_{SS}	41	V_{SS}	61	$DATA_0$	81	THR_0
2	N.C.	22	N.C.	42	V_{DD}	62	N.C.	82	THR_1
3	N.C.	23	PNCG1	43	PARL	63	INT	83	THR_2
4	$G1_0$	24	PNCG2	44	READ	64	N.C.	84	THR_3
5	$G1_1$	25	DSCRAM	45	V_{SS}	65	V_{SS}	85	THR_4
6	$G1_2$	26	SYNC	46	$ADDR_2$	66	ODCLK	86	THR_5
7	$G2_0$	27	LDG2	47	$ADDR_1$	67	N.C.	87	THR_6
8	$G2_1$	28	N.C.	48	$ADDR_0$	68	V_{SS}	88	THR_7
9	$G2_2$	29	N.C.	49	WRITE	69	DATO	89	EXTSEL
10	N.C.	30	V_{DD}	50	CSEL	70	N.C.	90	V_{SS}
11	OBIN	31	V_{DD}	51	V_{DD}	71	OOS	91	V_{SS}
12	N.C.	32	$COUNT_0$	52	V_{DD}	72	AUTO	92	V_{SS}
13	V_{SS}	33	$COUNT_1$	53	N.C.	73	N.C.	93	V_{DD}
14	SYMCKIN	34	$COUNT_2$	54	$DATA_7$	74	I.C.	94	V_{SS}
15	N.C.	35	$COUNT_3$	55	$DATA_6$	75	N.C.	95	DDIF
16	V_{SS}	36	$COUNT_4$	56	$DATA_5$	76	BERR	96	V_{SS}
17	DCLKIN	37	$COUNT_5$	57	$DATA_4$	77	G1ERR	97	$RATE_2$
18	N.C.	38	$COUNT_6$	58	$DATA_3$	78	G2ERR	98	$RATE_1$
19	V_{SS}	39	$COUNT_7$	59	$DATA_2$	79	V_{DD}	99	$RATE_0$
20	RESET	40	V_{DD}	60	$DATA_1$	80	V_{DD}	100	V_{DD}

INPUT SIGNALS

RESET

Reset. A logic low on this asynchronous input will completely reset all registers in the decoder to an initial condition within 20 nsec. Normal operation will commence after **RESET** goes high. This will not affect the values stored in the decision path memory but will reset the node sync state to the initial condition.

DCLKIN

Decoder clock input. It is the reference clock for all internal synchronous functions in the decoder when operating in the Internal Puncturing mode. It should nominally be a square wave with a maximum frequency of 45 MHz, corresponding to a decoded data rate of 45 Mbps. When operating at Rate $^1/_2$ and in the External Puncturing mode this clock will be generated internally from **SYMCKIN**, and **DCLKIN** should be connected to ground.

SYMCKIN

Symbol clock input. This is the reference clock for all internal synchronous functions in the symbol alignment and depuncturing circuits. It should nominally be a square wave with a maximum frequency of 90 MHz. Its frequency should be equal to $f_{DCLKIN}/2R$ in the parallel input mode (**PARL** = 1) and equal to f_{DCLKIN}/R in the sequential input mode (**PARL** = 0), where R is the decoding rate when using internal depuncturing. Please refer to the section on Punctured Mode Operation for more detailed information.

$G1_{2\text{-}0}$, $G2_{2\text{-}0}$

The $G1_{2\text{-}0}$ and $G2_{2\text{-}0}$ signals are the 3-bit soft decision input symbols to the decoder. They are presented to the decoder either sequentially or in parallel depending on the states of the **PARL** and $RATE_{2\text{-}0}$ inputs. In the parallel mode (**PARL** = 1) the symbols are clocked into the device on the rising edges of **SYMCKIN** when $RATE_{2\text{-}0} = 0$ (Rate $^1/_2$ and External Depuncturing) and on both edges of **SYMCKIN** when $RATE_{2\text{-}0} \neq 0$ (Internal Depuncturing). In the sequential mode (**PARL** = 0) in which the $G2_{2\text{-}0}$ inputs are not used, both the G1 and G2 symbols are loaded via the $G1_{2\text{-}0}$ pins. The G1 symbols are then latched in on the rising edges of **SYMCKIN** when **LDG2** is low and the G2 symbols are latched in on the rising edges of **SYMCKIN** when **LDG2** is high.

LDG2

When this signal is high during a rising edge of **SYMCKIN** the symbol loaded into the $G1_{2\text{-}0}$ pins will be G2. This function is only active when **PARL** is set low (sequential input mode) and $RATE_{2\text{-}0}$ is set to 000 (Rate $^1/_2$ operation or External Puncturing mode). If auto node sync is used, the **LDG2** signal can be derived by dividing the **SYMCKIN** signal by two. The auto node sync will then compensate for the phase ambiguity.

PARL

When this signal is high, the input symbols are accepted in parallel by the chip, using the $G1_{2\text{-}0}$ pins for the G1 symbols and the $G2_{2\text{-}0}$ pins for the G2 symbols. When it is set low, the inputs are accepted sequentially, using the $G1_{2\text{-}0}$ pins for both symbols. The sequential input is most suited for BPSK data, and the parallel input is most suited for QPSK data. The auto node sync sequence will operate on the assumption that the signal is BPSK modulated when **PARL** is set low and QPSK modulated when it is set high. Setting **PARL** low adds two cycles of **ODCLK** to the pipeline delay.

OBIN

The STEL-2060 can accept the soft-decision input data in either offset binary or offset signed-magnitude formats. When the **OBIN** input is set high, the format expected will be offset binary; when it is set low it will be offset signed-magnitude. The meanings of the 3-bit values for these two codes is shown in the following table:

OBIN = 1	OBIN = 0	Value
111	111	Most confident +
110	110	(Data = 1)
101	101	
100	100	Least confident +
011	000	Least confident –
010	001	
001	010	(Data = 0)
000	011	Most confident –

When using the STEL-2060 with hard-decision data, the symbols should be loaded into the $G1_2$ and $G2_2$ pins. The other symbol inputs should be set to a logic high level and **OBIN** should be set low.

$RATE_{2\text{-}0}$

These signals select the decoding rate for unpunctured operation (Rate $^1/_2$) and internally supported depuncturing patterns (Rates $^2/_3$, $^3/_4$ and $^7/_8$). These patterns are shown in the following table, where a 0 in the pattern indicates a punctured symbol:

$RATE_{2\text{-}0}$	Rate	Pattern
0 0 0	$^1/_2$	N.A.
0 0 1	$^2/_3$	G1: 10
		G2: 11
1 0 0	$^3/_4$	G1: 101
		G2: 110
0 1 0	$^7/_8$	G1: 1000101
		G2: 1111010

Other puncturing patterns can be implemented externally using the **PNCG1** and **PNCG2** inputs.

DDIF

When this input is set high, it causes the data out of the Viterbi decoder to be differentially decoded. This adds one cycle of **ODCLK** to the pipeline delay.

DSCRAM

When this input is set high, it causes the G2 symbols to be inverted before they enter the Viterbi decoder, thereby reversing the effect of the G2 inversion if an "Invert G2" scrambler is implemented at the encoder.

PNCG1, PNCG2

The **PNCG1** and **PNCG2** signals are used to control the STEL-2060 when operating in punctured modes not supported by the internal puncturing logic. In normal operation (Rate $^1/_2$ and when using internal puncturing) these pins should be set low. In the external depuncturing mode, the **PNCG1** signal must be set high to indicate that the G1 symbol is punctured and the **PNCG2** signal must be set high to indicate that the G2 symbol is punctured. A symbol will be depunctured when the **PNCG1** or **PNCG2** signals are high during the rising edge of **SYMCKIN** which latches the corresponding symbol in to the decoder. $\mathbf{RATE_{2\text{-}0}}$ should be set to 000 when operating in external depuncturing mode. Zero value metrics will be substituted internally for the actual metrics corresponding to the signals present on the $\mathbf{G1_{2\text{-}0}}$ and $\mathbf{G2_{2\text{-}0}}$ pins at that time. Internal depuncturing can be selected by the use of the **RATE** inputs.

SYNC

When the **SYNC** input is set high during the rising edge of **SYMCKIN** the internal symbol synchronization will be changed. When auto node sync is not desired this pin should be set low. It should be connected to the **AUTO** output to use the auto node sync capability of the STEL-2060. The state of this circuit will always be set to normal after a reset.

$\mathbf{COUNT_{7\text{-}0}}$

The 8-bit $\mathbf{COUNT_{7\text{-}0}}$ input defines the period (number of bits) used in the node synchronization circuit when **EXTSEL** is set high. The 8-bit number N is used to set up a period of (256N + 256) bits internally, where N is the value of $\mathbf{COUNT_{7\text{-}0}}$. An out-of-sync condition is declared (i.e., the output pin **OOS** is set high and **AUTO** pulses high) if the renormalization count exceeds the threshold value during a period of this number of bits.

$\mathbf{THR_{7\text{-}0}}$

The 8-bit $\mathbf{THR_{7\text{-}0}}$ input defines the threshold for node synchronization when **EXTSEL** is set high. The 8-bit number N is used to set up a threshold value of (8N + 6) internally, where N is the value of $\mathbf{THR_{7\text{-}0}}$. An out-of-sync condition is declared (i.e., the output pin **OOS** is set high and **AUTO** pulses high) if the renormalization count exceeds this threshold value.

EXTSEL

When the **EXTSEL** input is set high, the $\mathbf{COUNT_{7\text{-}0}}$ and $\mathbf{THR_{7\text{-}0}}$ information is derived from the $\mathbf{COUNT_{7\text{-}0}}$ and $\mathbf{THR_{7\text{-}0}}$ input pins. When it is set low, this information is derived from the data written into addresses 0 and 1.

OUTPUT SIGNALS

ODCLK

Output data clock. All outputs change on the rising edge of this clock. The falling edge of **ODCLK** can be used as a strobe for **DATO** output, which is guaranteed to be valid on this edge.

DATO

Decoded data output. This is the output of the Viterbi decoder. This signal changes on the rising edges of **ODCLK**. In Rate $^1/_2$ operation there will be a pipeline delay of 526 cycles of **ODCLK** from the $\mathbf{G1_{2\text{-}0}}/\mathbf{G2_{2\text{-}0}}$ inputs to the **DATO** output when **DDIF** is set low and **PARL** is set high. Setting **DDIF** high adds one cycle to this value and setting **PARL** low adds two cycles.

OOS

This output pin serves as a flag for the out-of-sync condition. When it goes high it signifies that the renormalization count in the internal node sync circuit has exceeded the threshold value set by the $\mathbf{THR_{7\text{-}0}}$ signal, declaring an out-of-sync condition. It will remain high until this condition ceases to exist. i.e., until the next time the threshold is not exceeded during a complete count period.

AUTO

This is the feedback signal from the internal node sync correction circuit. It will pulse high for one cycle of **DCLKIN** each time the renormalization count in the internal node sync circuit has exceeded the threshold value set by the $\mathbf{THR_{7\text{-}0}}$ signal and the out-of-sync condition is declared. It should be connected to the **SYNC** input when using the internal node sync facility.

BERR

The Bit Error output indicates that an error has been detected in either the G1 or G2 symbols corresponding to the current output bit.

G1ERR

The G1 Error output indicates that an error has been detected in the G1 symbol corresponding to the current output bit.

G2ERR

The G2 Error output indicates that an error has been detected in the G2 symbol corresponding to the current output bit.

Note: The **BERR**, **G1ERR** and **G2ERR** signals are in NRZ format, i.e., the signals will not return to zero between two consecutive errors. To generate pulsed outputs, the signals can be gated with the **ODCLK** signal.

MICROPROCESSOR INTERFACE

$\mathbf{DATA_{7\text{-}0}}$

All I/O and control functions can be accessed via the $\mathbf{DATA_{7\text{-}0}}$ bus with the associated control signals. The STEL-2060 is used as a memory or I/O mapped peripheral to the host processor.

$ADDR_{2-0}$

The 3-bit address bus is used to access the various I/O functions, as shown in the Memory Map table, below. Note that some addresses contain both Read and Write registers. These read and write mode registers are separate and contain different data.

WRITE

The **Write** input is used to write data to the microprocessor data bus. It is active low and is normally connected to the write line of the host processor.

READ

The **Read** input is used to read data from the microprocessor data bus. It is active low and is normally connected to the read line of the host processor.

CSEL

The Chip **Select** input can be used to selectively enable the microprocessor data bus. It is active low.

INT

The **Interrupt** output indicates when the Period Counter in the BER Monitor has completed a count period, and that a new value of **BERCT** is ready to be read from addresses 0_H and 1_H, when **INT** will go high for one symbol period.

INPUT (WRITE) FUNCTIONS

$COUNT_{7-0}$

The 8-bit $COUNT_{7-0}$ data defines the period (i.e., the number of bits) used in the node synchronization circuit. The 8-bit number N is used to set up a period of (256N + 256) internally, where N is the value of $COUNT_{7-0}$. If the renormalization count exceeds the threshold value during a period of this number of bits then an out-of-sync condition is declared (i.e., the output pin **OOS** is set high and **AUTO** pulses high). Reset value 00_H.

THR_{7-0}

The 8-bit THR_{7-0} data defines the threshold for node synchronization when **EXTSEL** is set low. The function is identical to that of the THR_{7-0} input signal. Reset value 00_H.

$BPER_{23-0}$

The 24-bit **BER Period** data is used to set the period (number of data bits) over which the mean BER is measured by the BER Monitor. The period used is 1000 times the value of $BPER_{23-0}$. Reset value $FFFFFF_H$.

Note: The BER Count function incorporated in the STEL-2060 uses a counter to count the number of thousands of bits received. When the value of this counter is **equal** to the value written into $BPER_{23-0}$ the number of errors counted is dumped into the $BERCT_{15-0}$ output register and can be read from read addresses $0\text{-}1_H$. Simultaneously, both the error and bit counters are reset and the process is restarted, and an interrupt (INT) is generated to indicate that the new value is ready to be read.

Since the default (reset) value of the $BPER_{23-0}$ register is FF FF FF_H a potential problem occurs if the desired value is not written into this register before the value of the counter has already incremented past this value. If this is not done the equality will not be detected until after the counter overflows and increments to the desired value once again. Even at the maximum rate of 45 Mbps this will take over 6 minutes and, at a more modest data rate, such as 1 Mbps, it will take over $4^1/2$ hours! In any case, the user can easily be misled into believing that the circuit is not operating correctly since the interrupts will not be generated as expected. It is therefore imperative that the $BPER_{23-0}$ value be written into the STEL-2060 as soon as possible after a reset to ensure that this condition does not take place. The maximum time allowable is just less than the desired interrupt period itself, since the counter begins counting right after the reset is released.

e.g., if the desired interrupt period is one second, the $BPER_{23-0}$ value must be written within one second of the reset. At a data rate of 1 Mbps the period would correspond to 10^6 bits and the correct $BPER_{23-0}$ value would be 10^3, or 00 03 $E8_H$.

If, for some reason, it is not possible to do this, a dummy value should first be written into the STEL-2060. This should be large enough so that, at the time of writing, the bit counter will not have exceeded the dummy value. In this way the first interrupt will be generated within a reasonable period of time and the dummy value can then be overwritten with the desired value. Again, care must be taken to ensure that the $BPER_{23-0}$ value written is greater than the instantaneous counter value, otherwise the same problem will occur.

e.g., in the above example, if it is not possible to write the $BPER_{23-0}$ value until 5 seconds after the reset, then a dummy $BPER_{23-0}$ value corresponding to >5 seconds, e.g., 6 seconds, or 00 17 70_H should first be written. The desired value of 00 03 $E8_H$ must then be written within one second of an interrupt generated by the STEL-2060, thereby ensuring that the counter has not exceeded the new value at that time.

OUTPUT (READ) FUNCTIONS

$BERCT_{15-0}$

The 16-bit **Bit Error Count** data represents the mean Bit Error Rate over the period determined by the BER Period data $BPER_{23-0}$. The actual BER is given by:

$$BER = \frac{8 \times BERCT_{15-0}}{1000 \times BPER_{23-0}}$$

The value will be updated each time the period counter completes its count. Completion is indicated by the **INT** output going high for one clock cycle. If the accumulator overflows during a measurement period its output will be caused to saturate at a value of $FFFF_H$.

MICROPROCESSOR INTERFACE MEMORY MAP

WRITE MODE REGISTERS

$ADDR_{2-0}$	$DATA_7$	$DATA_6$	$DATA_5$	$DATA_4$	$DATA_3$	$DATA_2$	$DATA_1$	$DATA_0$
0	$COUNT_7$	$COUNT_6$	$COUNT_5$	$COUNT_4$	$COUNT_3$	$COUNT_2$	$COUNT_1$	$COUNT_0$
1	THR_7	THR_6	THR_5	THR_4	THR_3	THR_2	THR_1	THR_0
2								
3	$BPER_7$	$BPER_6$	$BPER_5$	$BPER_4$	$BPER_3$	$BPER_2$	$BPER_1$	$BPER_0$
4	$BPER_{15}$	$BPER_{14}$	$BPER_{13}$	$BPER_{12}$	$BPER_{11}$	$BPER_{10}$	$BPER_9$	$BPER_8$
5	$BPER_{23}$	$BPER_{22}$	$BPER_{21}$	$BPER_{20}$	$BPER_{19}$	$BPER_{18}$	$BPER_{17}$	$BPER_{16}$

READ MODE REGISTERS

$ADDR_{2-0}$	$DATA_7$	$DATA_6$	$DATA_5$	$DATA_4$	$DATA_3$	$DATA_2$	$DATA_1$	$DATA_0$
0	$BERCT_7$	$BERCT_6$	$BERCT_5$	$BERCT_4$	$BERCT_3$	$BERCT_2$	$BERCT_1$	$BERCT_0$
1	$BERCT_{15}$	$BERCT_{14}$	$BERCT_{13}$	$BERCT_{12}$	$BERCT_{11}$	$BERCT_{10}$	$BERCT_9$	$BERCT_8$

PUNCTURED MODE OPERATION

CONCEPT OF PUNCTURING

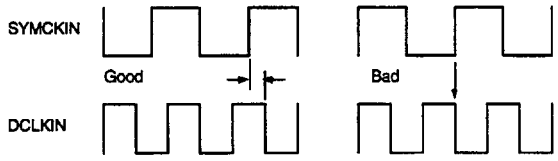
In punctured codes some of the symbols generated by the convolutional encoder are deleted, or punctured, from the transmitted sequence. For example, in a rate $^1/_2$ (unpunctured) sequence, four symbols are transmitted for every two data bits. If one symbol out of every group of four was punctured from the sequence then only three symbols would be transmitted for every two data bits. This would result in a rate $^2/_3$ code. The coding gain is significantly less than that for unpunctured operation, but this is the trade-off for the reduced bandwidth required to transmit the information. The STEL-2060 decoder is designed to operate with punctured codes as well as rate $^1/_2$ code. Two methods are provided for depuncturing the symbols. The external method can be used for all rates and patterns up to rate $^7/_8$ by indicating which symbols were punctured at the encoder (and then reinserted prior to decoding) with the **PNCG1** and **PNCG2** signals. When one of these signals is set high the input data at the corresponding symbol input is ignored, and the internally generated metric for the symbol pair (G1 and G2) assigns a zero weight to the punctured symbol in the pair. This is done because the Viterbi decoder has no way of knowing what the punctured symbol should have been. The recommended puncturing sequences for the various $^{(N-1)}/_N$ rates of punctured operation are shown in the tables. The portions shown in boldface are the basic sequences, which are then repeated. The use of the **PNCG1** and **PNCG2** signals for rate $^3/_4$ is shown in the External Puncturing timing diagrams. The sequence for rate $^3/_4$ is G1 G2 P G2 G1 P, and the punctured symbols are marked with asterisks in the timing diagrams.

USING INTERNAL DEPUNCTURING

The internal depuncturing method supports Rates $^2/_3$, $^3/_4$ and $^7/_8$ using the puncturing sequences specified in the tables, and the node sync process will automatically find the correct places to reinsert the punctured symbols. The puncturing sequences used for the rates supported are shown in the tables, along with the speeds of the two input clocks, **SYMCKIN** and **DCLKIN**. The portions shown in boldface are the basic sequences, which are then repeated. The symbol sequence for rate $^2/_3$ is shown in the Internal Puncturing timing diagrams. The sequence is G1 G2 P G2; only G1 symbols are punctured in this particular sequence. The **SYMCKIN** and **DCLKIN** clocks are used to clock in the symbols and to clock out the data bits. The speeds of these two clocks vary according to the modes and rate in use. When operating in the External Depuncturing modes the **DCLKIN** signal is not used and the **SYMCKIN** speed will be equal to the data rate (D) in the parallel mode (**PARL** = 1) and be equal to twice the data rate (2D) in the sequential mode (**PARL** = 0). In the Internal Depuncturing modes, however, **DCLKIN** is used and the speed of **SYMCKIN** will be as shown in the tables.

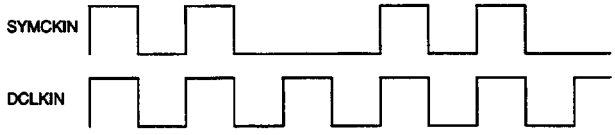
The depuncturing circuit in the STEL-2060 takes symbols synchronized to the SYMCKIN signal and depunctures them, i.e., inserts dummy symbols into the signal stream at the appropriate positions. To do this the circuit handles the symbols as a group of up to four pairs, depending on the code rate. This circuit operates at the SYMCKIN rate and, at this point, the group of depunctured symbols is transferred into another set of registers clocked with DCLKIN. There is an internal timing requirement that the falling edge of DCLKIN

must follow the rising edge of SYMCKIN by a minimum of 8 nsec. at this instant, otherwise the handover will not occur correctly. This occurs once every 4 cycles of DCLKIN at rate $^{7}/_{8}$, every 2 cycles at rate $^{3}/_{4}$ and every 3 cycles at rate $^{2}/_{3}$, the number of cycles of SYMCKIN depending on whether the parallel or sequential input mode is used, as well as the code rate. Two examples of clock phasing for rate $^{3}/_{4}$ parallel operation are shown below.

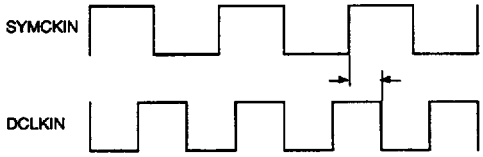


In the first example the falling edges of DCLKIN never coincide with the rising edges of SYMCKIN. Thus the timing violation will never occur provided that the delay from the non-coincident rising edges of SYMCKIN to the following falling edge of DCLKIN (shown by the arrows) exceeds 8 nsec. In the second case the falling edge of DCLKIN coincides with the rising edge of SYMCKIN once every two cycles of DCLKIN, resulting in a 50% probability that this may be the point at which the handover occurs, creating the problem discussed above.

There are several ways to satisfy the timing requirement, depending on the code rate. One effective way which works at all rates is to generate SYMCKIN from DCLKIN by puncturing the clock to reduce its frequency while keeping all the edges synchronized; this will require the use of a small FIFO to buffer the input symbols to cope with the punctured clock. The rate $^{3}/_{4}$ timing is shown below as an example.

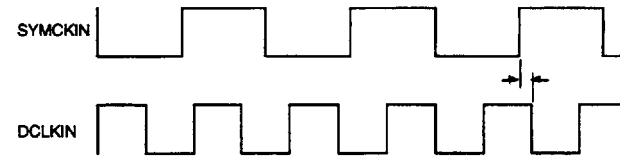


For rate $^{3}/_{4}$ operation it is possible to generate the two clocks with a mutual phase relationship that can exclude the timing violation, as was shown in the first figure. As previously stated, provided the two clocks can be generated as shown in the first example, where only the **rising** edges of DCLKIN coincide with the edges of SYMCKIN, the timing violation will never occur provided that the delay from the non-coincident rising edges of SYMCKIN to the following falling edge of DCLKIN (shown by the arrows) exceeds 8 nsec. In the example shown this will be true at data rates up to 30 Mbps. Care must be taken to ensure that jitter between the clocks is kept low enough to avoid the timing violation condition. A similar condition exists for rate $^{2}/_{3}$ operation, as shown below.



Here, the timing is such that the falling edges of DCLKIN only coincide with falling edges of SYMCKIN, never with rising edges. In this case the timing violation never occurs at any speed, since the non-coincident falling edges of DCLKIN will trail the rising edges of SYMCKIN by approximately 8 nsec. at a speed of 45 Mbps. Again, the same caveat regarding jitter must be observed. However, the symbol signal setup and hold requirements, shown in page 11 of the data sheet make it necessary for SYMCKIN to have a minimum low time of 12 nsec. to satisfy these requirements, so that it is not possible for this signal to be a square wave above 40 MHz for this reason. Since the method for eliminating the clock timing violation presented here relies on the use of square waves (50% mark-space ratio), it cannot be used above 40 MHz because of the setup and hold time requirements.

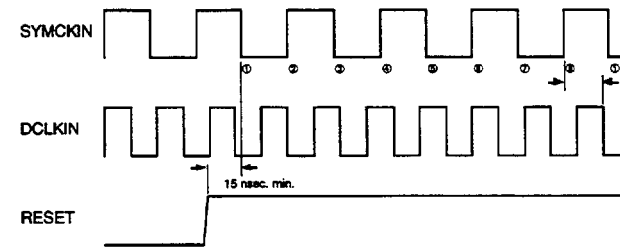
Again, a similar condition exists for rate $^{7}/_{8}$ operation, as shown below.



However, in this case the timing violation will begin to occur at speeds over 15 Mbps, so that this method of solving the timing problem is less useful for rate $^{7}/_{8}$ operation.

Note that for sequential mode operation (PARL = 0) the frequency of the SYMCKIN signal will be doubled in every case. This presents a problem with the synchronized clock method presented here since it will not be possible to generate the necessary waveforms with the correct mutual phasing guaranteed because of the phase ambiguity of the SYMCKIN signal itself relative to the internal handover process. In this case it will be necessary to use either the punctured clock approach or the synchronized reset approach.

The third method, which, while having the disadvantage that it is susceptible to loss of sync from disturbances, is easier to implement than clock puncturing and provides a lot more margin than simple clock phase synchronization. It consists of a synchronized reset generator used in conjunction with clock phase synchronization. This is shown below for rate $^{7}/_{8}$.



This ensures that the STEL-2060 starts up during the optimum phase of the SYMCKIN/DCLKIN repetition cycle, i.e., the phase with the maximum separation between the rising edge of SYMCKIN and the next falling edge of DCLKIN; the

decoder will then continue to operate correctly provided that nothing occurs to upset this cycle. This method exploits the fact that not all falling edges of DCLKIN have a timing sensitivity relative to the rising edges of SYMCKIN, as was discussed earlier. For example, in rate $^{7}/_{8}$ operation only every fourth falling edge of DCLKIN is critical, starting with the fourth one after the reset is released. By timing the rising edge of the reset at a point in the cycle where there is good separation between the rising edge of SYMCKIN and the following falling edge of DCLKIN the same situation will occur again every four cycles of DCLKIN, which is precisely where the timing sensitivity occurs, as shown in the figure. This method ensures good timing margins for stable operation at all data rates up to 40 Mbps, this limit again being set by the symbol setup and hold time requirements and need to use square waves for the clocks.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: *Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability.*

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–65 to +150	°C
T_a	Operating Temperature (Ambient)	–40 to +85	°C
V_{DDmax}	Max. voltage between V_{DD} and V_{SS}	+7 to –0.7	volts
$V_{I/O(max)}$	Max. voltage on any input or output pin	V_{DD} + 0.3	volts
$V_{I/O(min)}$	Min. voltage on any input or output pin	V_{SS} – 0.3	volts

RECOMMENDED OPERATING CONDITIONS

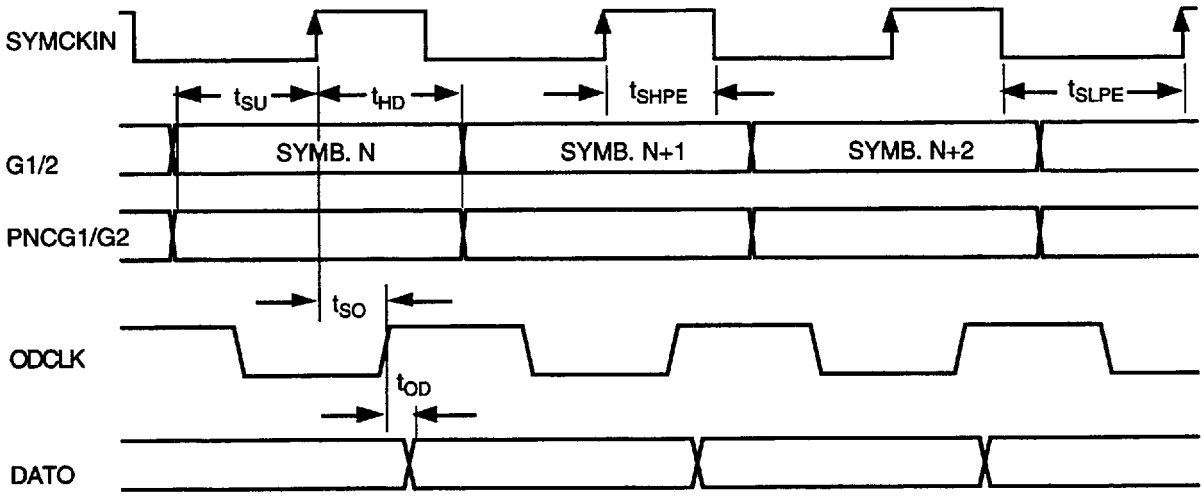
Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 10%	volts
T_a	Operating Temperature (Ambient)	0 to +70	°C

D.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 ± 5% volts, T_a = 0° to 70° C)

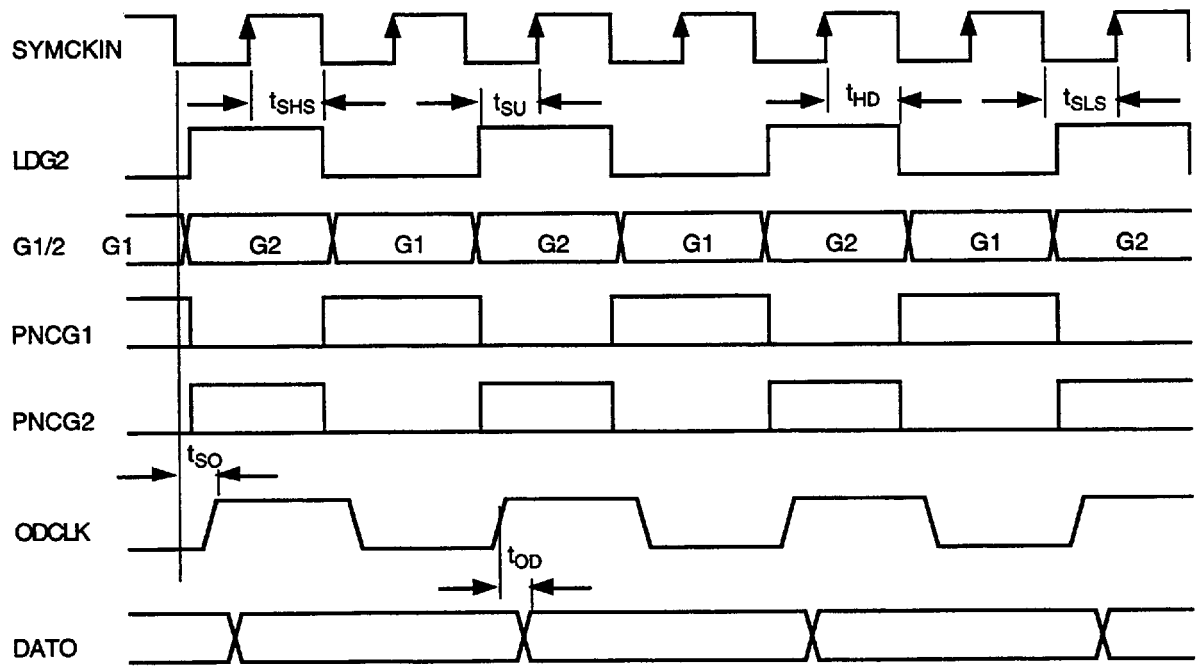
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational		8		mA/Mbps	@ 45 Mbps (f_{DATA})
$V_{IH(min)}$	Min. High Level Input Voltage	2.0			volts	Guaranteed Logic '1'
$V_{IL(max)}$	Max. Low Level Input Voltage			0.8	volts	Guaranteed Logic '0'
$V_{OH(min)}$	Min. High Level Output Voltage	2.4			volts	I_O = –4.0 mA
$V_{OL(max)}$	Max. Low Level Output Voltage			0.4	volts	I_O = +4.0 mA
$I_{IH(max)}$	Max. High Level Input Current			10	µA	V_{IN} = +5.0 volts
$I_{IL(max)}$	Max. Low Level Input Current			–10	µA	V_{IN} = 0 volts

TIMING. RATE 1/2 AND EXTERNAL DEPUNCTURING

(a) PARALLEL INPUT MODE (PARL = 1)



(b) SEQUENTIAL INPUT MODE (PARL = 0)



A.C. CHARACTERISTICS (Operating Conditions: V_{DD} = 5.0 ±5% volts, T_a = 0° to 70° C)

Symbol	Parameter	Min.	Max.	Units	Conditions
f_{DAT}	Data speed, Parallel input mode (**PARL** = 1), all rates when **not** using Internal Depuncturing		45	Mbps	**PARL** = 1 **and** $\mathbf{RATE_{2-0}}$ = 0
f_{DAT}	Data speed, Sequential input mode (**PARL** = 0), Rate 1/2 and all rates and modes **when** using Internal Depuncturing		45	Mbps	**PARL** = 0 **or** $\mathbf{RATE_{2-0}} \neq 0$
t_{SU}	**G1, G2, PNCG1** or **PCNG2, LDG2** to **SYMCKIN** Setup	3		nsecs.	**PARL** = 0 **or**
t_{HD}	**G1, G2, PNCG1** or **PCNG2, LDG2** to **SYMCKIN** Hold	5		nsecs.	$\mathbf{RATE_{2-0}}$ = 0
t_{SUI}	**G1, G2, PNCG1** or **PCNG2, LDG2** to **SYMCKIN** Setup	6		nsecs.	**PARL** = 1 **and**
t_{HDI}	**G1, G2, PNCG1** or **PCNG2, LDG2** to **SYMCKIN** Hold	6		nsecs.	$\mathbf{RATE_{2-0}} \neq 0$
t_{SHPE}, t_{SLPE}	**SYMCKIN** Pulse width (high or low), Parallel input mode, all rates when **not** using Internal Depuncturing	10		nsecs.	**PARL** = 1 **and** $\mathbf{RATE_{2-0}}$ = 0
t_{SHPI}, t_{SLPI}	**SYMCKIN** Pulse width (high or low), Parallel input mode, all rates **when** using Internal Depuncturing	12		nsecs.	**PARL** = 1 **and** $\mathbf{RATE_{2-0}} \neq 0$
t_{SHS}, t_{SLS}	**SYMCKIN** Pulse width (high or low), Serial input mode	6		nsecs.	**PARL** = 0
t_{SO}	**SYMCKIN** to **ODCLK** stable delay ($\mathbf{RATE_{2-0}}$ = 000)	3	8	nsecs.	
t_{DO}	**DCLKIN** to **ODCLK** stable delay ($\mathbf{RATE_{2-0}} \neq 000$)	3	8	nsecs.	Load = 15 pF
t_{OD}	**ODCLK** to output stable delay, all other outputs	1	3	nsecs.	Load = 15 pF

PUNCTURED SYMBOL SEQUENCES

1. RATE 1/2 AND EXTERNAL DEPUNCTURING - SEQUENTIAL INPUTS (PARL = 0)

Rate	Symbol sequence (suffix is symbol number in sequence, all at $G1_{2-0}$ input)	SYMCKIN	DCLKIN
1/2	$G1_1$ $G2_1$ $G1_2$ $G2_2$ $G1_3$ $G2_3$ (Not Punctured)	2 D	0
2/3	$G1_1$ $G2_1$ P_2 $G2_2$ $G1_3$ $G2_3$ P_4 $G2_4$ $G1_5$ $G2_5$ P_6 $G2_6$	2 D	0
3/4	$G1_1$ $G2_1$ P_2 $G2_2$ $G1_3$ P_3 $G1_4$ $G2_4$ P_5 $G2_5$ $G1_6$ P_6 $G1_7$ $G2_7$	2 D	0
4/5	$G1_1$ $G2_1$ P_2 $G2_2$ P_3 $G2_3$ P_4 $G2_4$ $G1_5$ $G2_5$ P_6 P_6 $G2_7$ P_7	2 D	0
5/6	$G1_1$ $G2_1$ P_2 $G2_2$ $G1_3$ P_3 P_4 $G2_4$ $G1_5$ P_5 $G1_6$ $G2_6$ P_7 $G2_7$	2 D	0
6/7	$G1_1$ $G2_1$ P_2 $G2_2$ P_3 $G2_3$ $G1_4$ P_4 P_5 $G2_5$ $G1_6$ P_6 $G1_7$ $G2_7$	2 D	0
7/8	$G1_1$ $G2_1$ P_2 $G2_2$ P_3 $G2_3$ P_4 $G2_4$ $G1_5$ P_5 P_6 $G2_6$ $G1_7$ P_7	2 D	0

2. RATE 1/2 AND EXTERNAL DEPUNCTURING - PARALLEL INPUTS (PARL = 1)

Rate	Input	Symbol sequence (suffix is symbol number in sequence)	SYMCKIN	DCLKIN
1/2	$G1_{2-0}$	$G1_1$ $G1_2$ $G1_3$ $G1_4$ $G1_5$ $G1_6$ (Not Punctured)	D	0
	$G2_{2-0}$	$G2_1$ $G2_2$ $G2_3$ $G2_4$ $G2_5$ $G2_6$		
2/3	$G1_{2-0}$	$G1_1$ P_2 $G1_3$ P_4 $G1_5$ P_6 $G1_7$ P_8 $G1_9$ P_{10}	D	0
	$G2_{2-0}$	$G2_1$ $G2_2$ $G2_3$ $G2_4$ $G2_5$ $G2_6$ $G2_7$ $G2_8$ $G2_9$ $G2_{10}$		
3/4	$G1_{2-0}$	$G1_1$ P_2 $G1_3$ $G1_4$ P_5 $G1_6$ $G1_7$ P_8 $G1_9$ $G1_{10}$	D	0
	$G2_{2-0}$	$G2_1$ $G2_2$ P_3 $G2_4$ $G2_5$ P_6 $G2_7$ $G2_8$ P_9 $G2_{10}$		
4/5	$G1_{2-0}$	$G1_1$ P_2 P_3 P_4 $G1_5$ P_6 P_7 P_8 $G1_9$ P_{10}	D	0
	$G2_{2-0}$	$G2_1$ $G2_2$ $G2_3$ $G2_4$ $G2_5$ $G2_6$ $G2_7$ $G2_8$ $G2_9$ $G2_{10}$		
5/6	$G1_{2-0}$	$G1_1$ P_2 $G1_3$ P_4 $G1_5$ $G1_6$ P_7 $G1_8$ P_9 $G1_{10}$	D	0
	$G2_{2-0}$	$G2_1$ $G2_2$ P_3 $G2_4$ P_5 $G2_6$ $G2_7$ P_8 $G2_9$ P_{10}		
6/7	$G1_{2-0}$	$G1_1$ P_2 P_3 $G1_4$ P_5 $G1_6$ $G1_7$ P_8 P_9 $G1_{10}$	D	0
	$G2_{2-0}$	$G2_1$ $G2_2$ $G2_3$ P_4 $G2_5$ P_6 $G1_7$ $G2_8$ P_9 $G2_{10}$		
7/8	$G1_{2-0}$	$G1_1$ P_2 P_3 P_4 $G1_5$ P_6 $G1_7$ $G1_8$ P_9 P_{10}	D	0
	$G2_{2-0}$	$G2_1$ $G2_2$ $G2_3$ $G2_4$ P_5 $G2_6$ P_7 $G2_8$ $G2_9$ $G2_{10}$		

3. INTERNAL DEPUNCTURING - SEQUENTIAL INPUTS (PARL = 0)

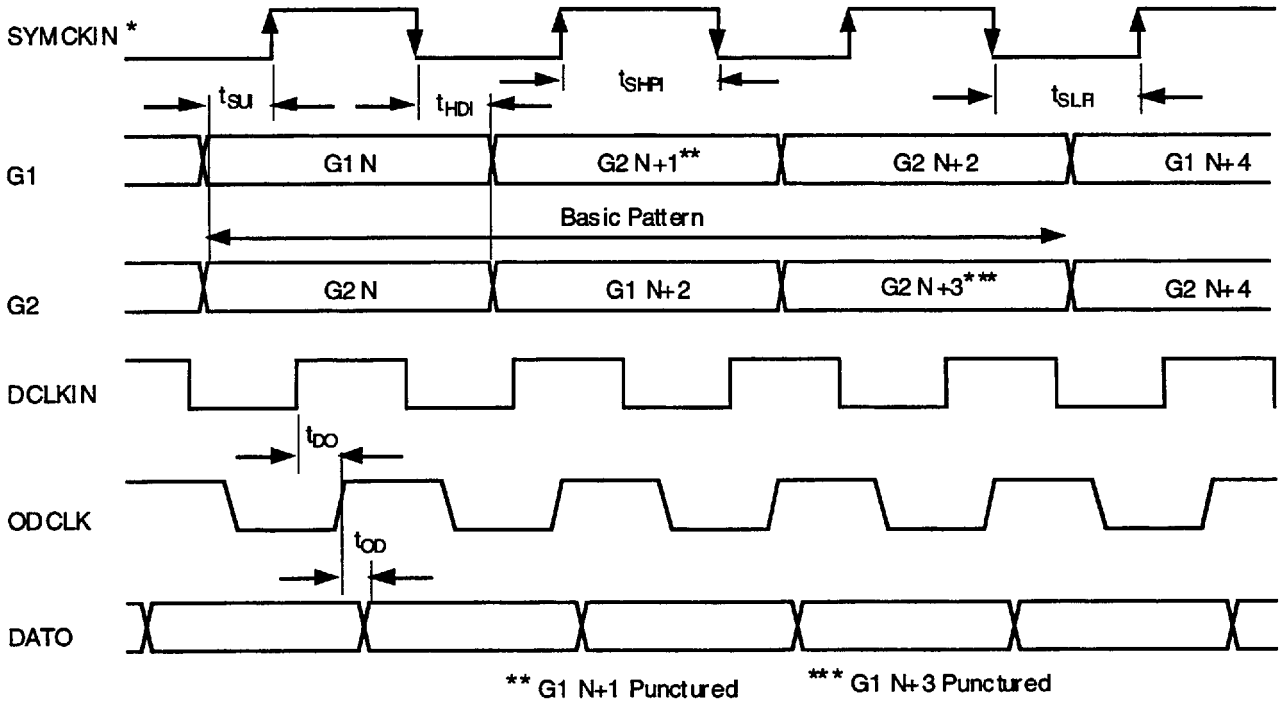
Rate	Symbol sequence (suffix is symbol number in sequence, all at $G1_{2-0}$ input)	SYMCKIN	DCLKIN
1/2	$G1_1$ $G2_1$ $G1_2$ $G2_2$ $G1_3$ $G2_3$ $G1_4$ $G2_4$ $G1_5$ (Not Punctured)	2 D	0
2/3	$G1_1$ $G2_1$ $G2_2$ $G1_3$ $G2_3$ $G2_4$ $G1_5$ $G2_5$ $G2_6$ $G1_7$ $G2_7$ $G2_8$	3/2 D	D
3/4	$G1_1$ $G2_1$ $G2_2$ $G1_3$ $G1_4$ $G2_4$ $G2_5$ $G1_6$ $G1_7$ $G2_7$ $G2_8$ $G1_9$	4/3 D	D
7/8	$G1_1$ $G2_1$ $G2_2$ $G2_3$ $G2_4$ $G1_5$ $G2_6$ $G1_7$ $G1_8$ $G2_8$ $G2_9$ $G2_{10}$	8/7 D	D

4. INTERNAL DEPUNCTURING - PARALLEL INPUTS (PARL = 1)

Rate	Input	Symbol sequence (suffix is symbol number in sequence)	SYMCKIN	DCLKIN
1/2	$G1_{2-0}$	$G1_1$ $G1_2$ $G1_3$ $G1_4$ $G1_5$ $G1_6$ $G1_7$ (Not Punctured)	D	0
	$G2_{2-0}$	$G2_1$ $G2_2$ $G2_3$ $G2_4$ $G2_5$ $G2_6$ $G2_7$		
2/3	$G1_{2-0}$	$G1_1$ $G2_2$ $G2_3$ $G1_5$ $G2_6$ $G2_7$ $G1_9$ $G2_{10}$ $G2_{11}$	3/4 D	D
	$G2_{2-0}$	$G2_1$ $G1_3$ $G2_4$ $G2_5$ $G1_7$ $G2_8$ $G2_9$ $G1_{11}$ $G2_{12}$		
3/4	$G1_{2-0}$	$G1_1$ $G2_2$ $G1_4$ $G2_5$ $G1_7$ $G2_8$ $G1_{10}$ $G2_{11}$ $G1_{13}$ $G2_{14}$	2/3 D	D
	$G2_{2-0}$	$G2_1$ $G1_3$ $G2_4$ $G1_6$ $G2_7$ $G1_9$ $G2_{10}$ $G1_{12}$ $G2_{13}$ $G1_{15}$		
7/8	$G1_{2-0}$	$G1_1$ $G2_2$ $G2_4$ $G2_6$ $G1_8$ $G2_9$ $G2_{11}$ $G1_{13}$ $G1_{15}$ $G2_{16}$	4/7 D	D
	$G2_{2-0}$	$G2_1$ $G2_3$ $G1_5$ $G1_7$ $G2_8$ $G2_{10}$ $G1_{12}$ $G2_{14}$ $G2_{15}$ $G1_{17}$		

INTERNAL DEPUNCTURING TIMING. RATE 2/3 SHOWN

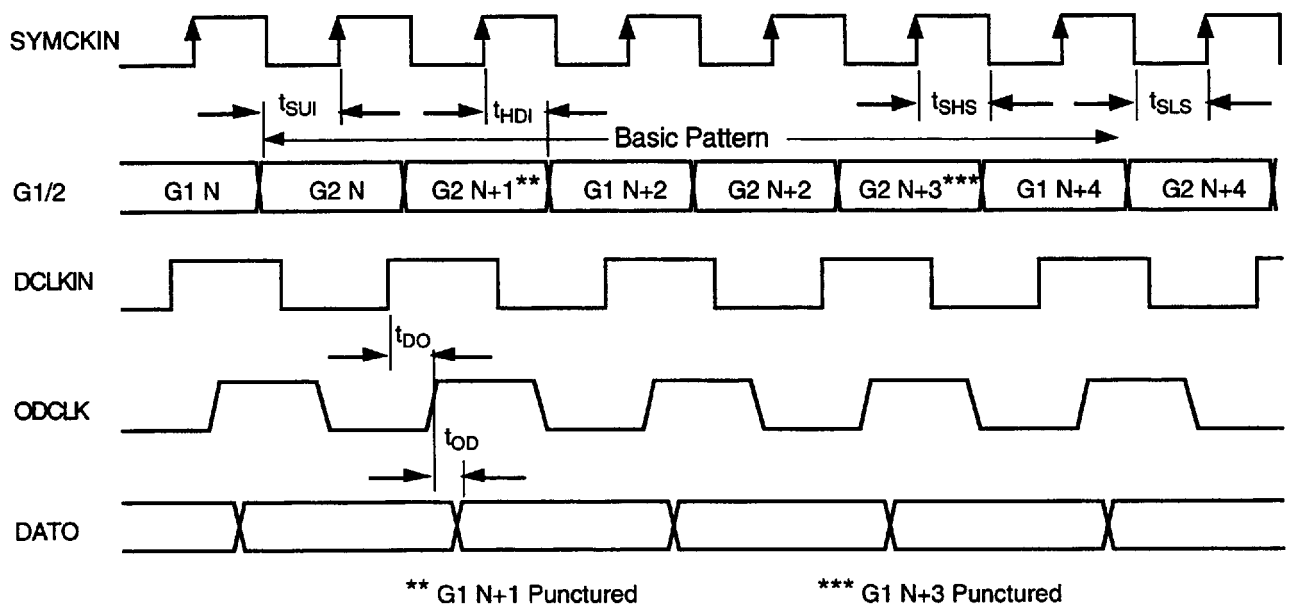
(a) PARALLEL INPUT MODE (PARL = 1)



** G1 N+1 Punctured *** G1 N+3 Punctured

* Within each symbol period, rising edge of SYMCLKIN must precede falling edge, as shown

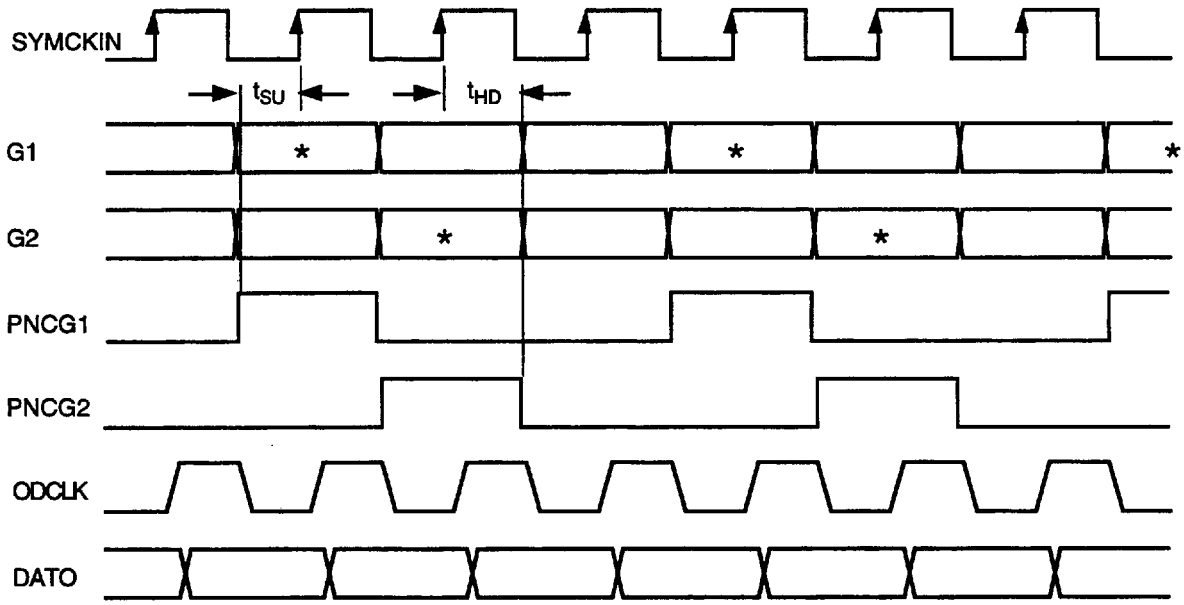
(b) SEQUENTIAL INPUT MODE (PARL = 0)



** G1 N+1 Punctured *** G1 N+3 Punctured

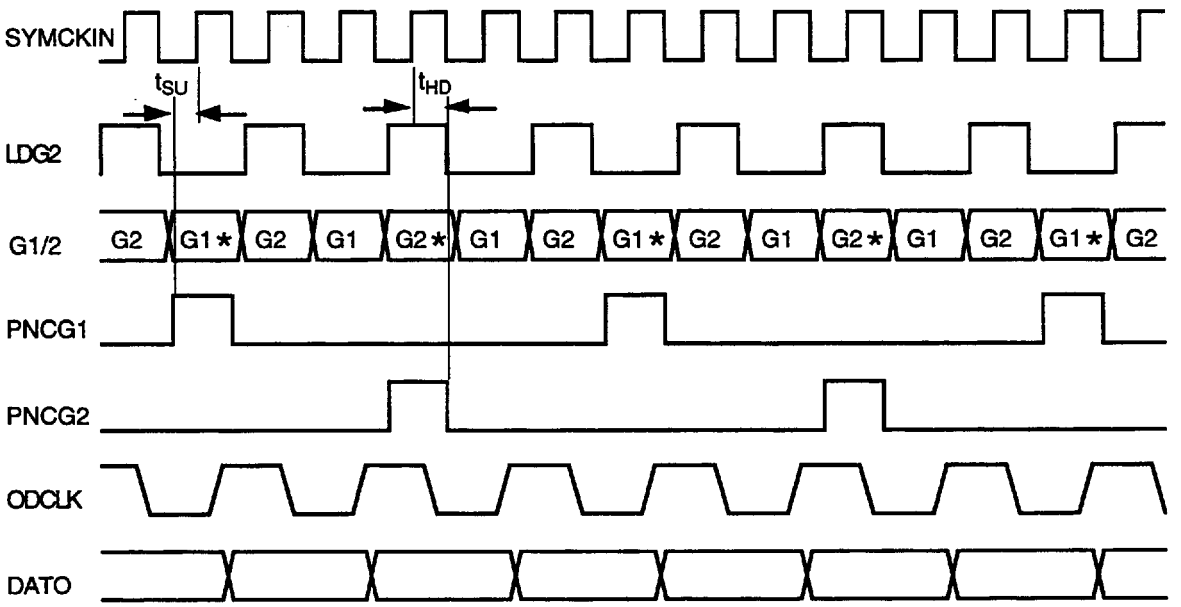
EXTERNAL DEPUNCTURING TIMING. RATE 3/4 SHOWN

(a) PARALLEL INPUT MODE (PARL = 1)



* Indicates Punctured Symbols

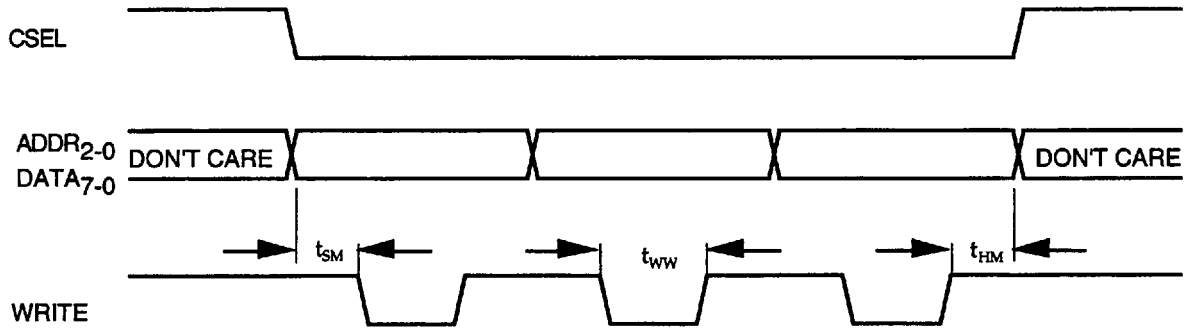
(b) SEQUENTIAL INPUT MODE (PARL = 0)



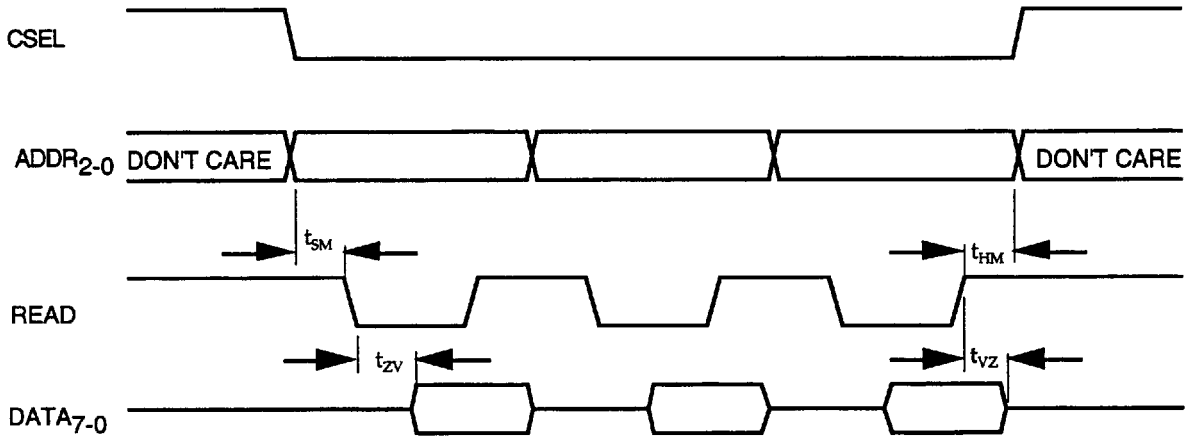
* Indicates Punctured Symbols

MICROPROCESSOR INTERFACE TIMING

1. WRITE MODE



2. READ MODE



A.C. CHARACTERISTICS

(Operating Conditions: V_{DD} = 5.0 ±5% volts, T_a = 0° to 70° C)

Symbol	Parameter	Min.	Max.	Units
t_{SM}	**CSEL**, **ADDR**$_{2-0}$ or **DATA**$_{7-0}$ to **WRITE** or **READ** Setup	10		nsecs.
t_{HM}	**CSEL**, **ADDR**$_{2-0}$ or **DATA**$_{7-0}$ to **WRITE** or **READ** Hold	5		nsecs.
t_{WW}	**WRITE** Pulse width	5		nsecs.
t_{ZV}	**READ** (low) to **DATA**$_{7-0}$ Valid		10	nsecs.
t_{VZ}	**READ** (high) to **DATA**$_{7-0}$ High-Impedance		10	nsecs.

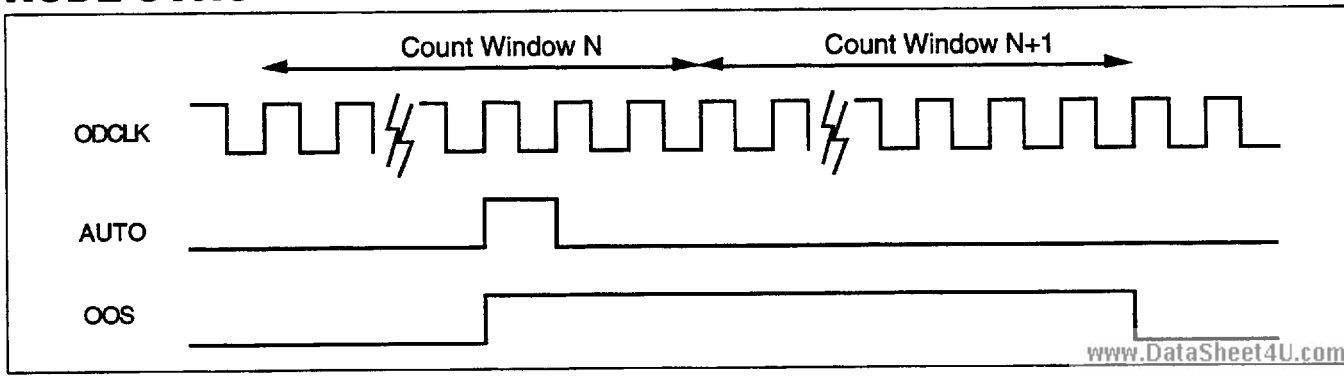
NODE SYNCHRONIZATION

In a communication system using Viterbi decoding the decoder will only operate correctly when the symbols G1 and G2 are loaded into the decoder in the correct order. Identifying which symbol is G1 and which one is G2 is referred to as node synchronization. The STEL-2060 contains a circuit designed to carry out the node synchronization function automatically. It uses the internally generated metrics of the received sequence to do this. These constantly changing parameters are periodically renormalized to keep them within bounds. If renormalization occurs too frequently it is a good indication that the system is not converging, most likely due to lack of node synchronization. The renormalization rate at which the system will decide to change the node sync is determined by the threshold parameter. This is an 8-bit number which is set by the $\mathbf{THR}_{7\text{-}0}$ inputs. When the renormalization count exceeds this value, the **OOS** output will go high and the **AUTO** output will pulse high for one clock cycle, as shown during Count Window N in the timing diagram below. The counter is reset after a number of bits determined by the number set by the $\mathbf{COUNT}_{7\text{-}0}$ inputs, so that the threshold must be exceeded somewhere in that period for resynchronization to take place. **OOS** will be reset if the counter then counts through an entire window and the threshold is not exceeded, as shown during Count Window N + 1 in the timing diagram below. The most suitable threshold setting will depend on the value of E_b/N_0, the coding rate, and the signal level at the G1 and G2 inputs. For full scale inputs, i.e., the peak signal values almost saturate the digital inputs, suitable starting values for the threshold will be 1% for Rate $^1/_2$, 0.5% for Rates $^2/_3$ to $^6/_7$, and 0.1% for Rate $^7/_8$. e.g., for Rate $^1/_2$, if the number of bits over which the measure is made is set to 512 ($\mathbf{COUNT}_{7\text{-}0} = 01_H$) the threshold should be set to 5. Setting $\mathbf{THR}_{7\text{-}0} = 0$ gives a value of 6, which is adequately close. More reliable results will be obtained by counting over a longer period to improve the averaging process, but this increases the time taken to make a decision and hence to acquire node sync. Thus, starting with a low count period and then increasing it (and adjusting the threshold accordingly to maintain a value of 1%) when **OOS** goes low will result in a faster acquisition of correct node sync with a lower probability of accidental loss of node sync once correct sync has been achieved. To use the internal node sync the **AUTO** output must be connected to the **SYNC** input. The synchronization sequence depends on the setting of the **PARL** input. When **PARL** is set low it is assumed that the data was modulated using BPSK, and when it is set high it is assumed that the data was modulated using QPSK. The appropriate synchronization sequences will be invoked, as shown in the node sync sequence tables. Note that the pipeline delay through the device will be affected by the node sync state. If multiple devices are used in parallel to achieve higher data rates, it is necessary for the all devices to have the same node sync state to equalize their pipeline delays. It will be necessary to reset the devices together to achieve this state

When internal depuncturing is used, additional node sync states exist because of the uncertainty of the current symbol position in the puncture sequence. In this case the node sync circuit will also search through the sequence by adding delays in the depuncturing process to precess through the sequence. In the sequential input mode (**PARL** = 0) this is simply an extension of the node sync process, since the alternate state is achieved by delaying the symbols. In the parallel input mode, however, this is different from the "invert G2 and swap" process, and in this sync sequence "invert G2 and swap" precedes the delay addition, so that the system goes through both the initial and alternate states for each delay addition tried. This is shown for the Rate $^2/_3$ case. In each case the symbols are read into the depuncturing circuit in groups of three (in the BPSK mode) or six (in the QPSK mode) and attempts are made to reinsert the punctured symbol in all of the possible insertion positions. The positions of the punctured symbols in the sequences are shown by the asterisks (*). The resulting groups of four or eight symbols are then decoded in pairs, resulting in two decoded bits in the BPSK mode and four bits in the QPSK mode. For higher rates the sequences will be extensions of this procedure.

When external depuncturing is used, the determination of which symbols were punctured, and need to be reinserted into the symbol sequence, is part of the node sync process. This is because the acquisition of correct node sync cannot be completed until the punctured symbols are reinserted correctly. The **AUTO** and **OOS** outputs of the STEL-2060 can be used as indicators of the operation of the internal node sync process; **OOS** will remain high as long as node sync has not been achieved and **AUTO** will pulse each time a new node sync state is being tried. Since there are only two possible internal node sync states, alternate pulses on the **AUTO** output can be used as an indication that the depuncturing is incorrect and a new depuncturing sequence should be tried externally.

NODE SYNC TIMING



NODE SYNC SEQUENCES

1. RATE 1/2

PARL	Input	Initial State	Alternate State
0	G1	$G1_n$ $G2_n$	$G2_n$ $G1_{n+1}$
	G2	N.A.	N.A.
1	G1	$G1_n$	$\overline{G2_n}$
	G2	$G2_n$	$G1_n$

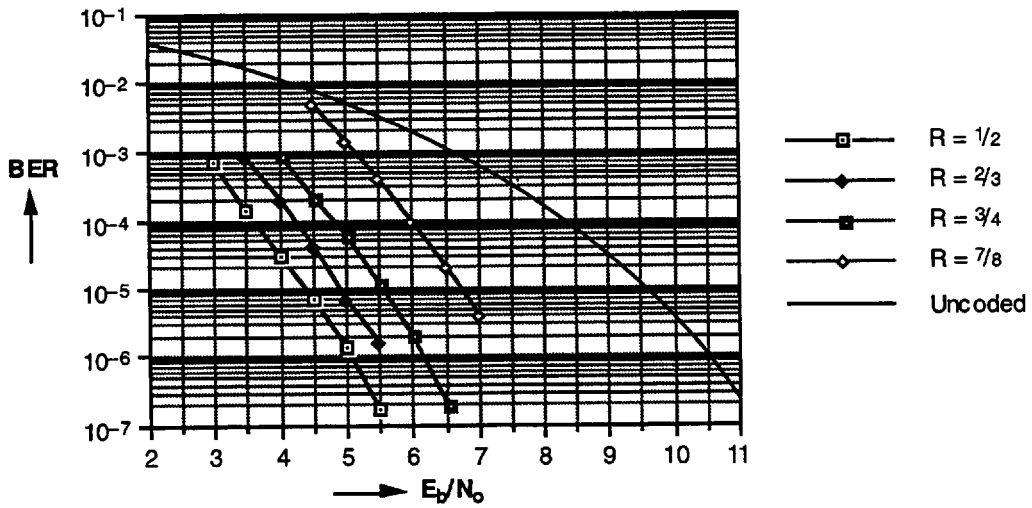
2. RATE 2/3, PARL = 0 (BPSK MODE)

Input	Initial State	Alternate States	
		1	2
G1	$G1_n$ $G2_n{}^*$ $G2_{n+1}$ (No delay)	$G2_n{}^*$ $G2_{n+1}$ $G1_{n+2}$ (One symbol delay)	$G2_{n+1}$ $G1_{n+2}$ $G2_{n+2}{}^*$ (Two symbol delay)

3. RATE 2/3, PARL = 1 (QPSK MODE)

Input	Initial State	Alternate States				
		1	2	3	4	5
G1	$G1_n$ $G2_{n+1}$ $G2_{n+2}{}^*$	$G2_n{}^*$ $G1_{n+2}$ $G2_{n+3}$	$G2_n{}^*$ $G1_{n+2}$ $G2_{n+3}$	$G2_{n+1}$ $G2_{n+2}{}^*$ $G1_{n+4}$	$^*G2_{n+1}$ $G2_{n+2}{}^*G1_{n+4}$	$G1_{n+2}$ $G2_{n+3}$ $G2_{n+4}{}^*$
G2	$G2_n{}^*$ $G1_{n+2}$ $G2_{n+3}$	$\overline{G1_n}$ $\overline{G2_{n+1}}$ $\overline{G2_{n+2}{}^*}$	$G2_{n+1}$ $G2_{n+2}{}^*$ $G1_{n+4}$	$\overline{G2_n{}^*}$ $\overline{G1_{n+2}}$ $\overline{G2_{n+3}}$	$G1_{n+2}$ $G2_{n+3}$ $G2_{n+4}$	$\overline{G2_{n+1}}$ $\overline{G2_{n+2}{}^*}G1_{n+4}$
	(No Invert/Swap No delay)	(Invert/Swap No delay)	(No Invert/Swap One symb. delay)	(Invert/Swap One symb. delay)	(No Invert/Swap Two symb. delay)	(Invert/Swap Two symb. delay)

BER PERFORMANCE



The coding gain obtained by the use of Convolutional coding and Viterbi decoding is extremely dependent on many parameters. Not surprisingly, the code rate is a primary factor, but so are the bit error rate (BER) and amplitude of the input signal. The BER affects the coding gain because the error correction capability of the Viterbi decoder is dependent on the statistics of the errors, specifically the clustering of errors. As the BER of the input signal increases, so does the clustering, causing a reduction in the error correcting capability of the device, along with the coding gain. The signal amplitude is important because of the weighting given to the signal amplitude as an indication of the likelihood of an error in a given symbol pair.

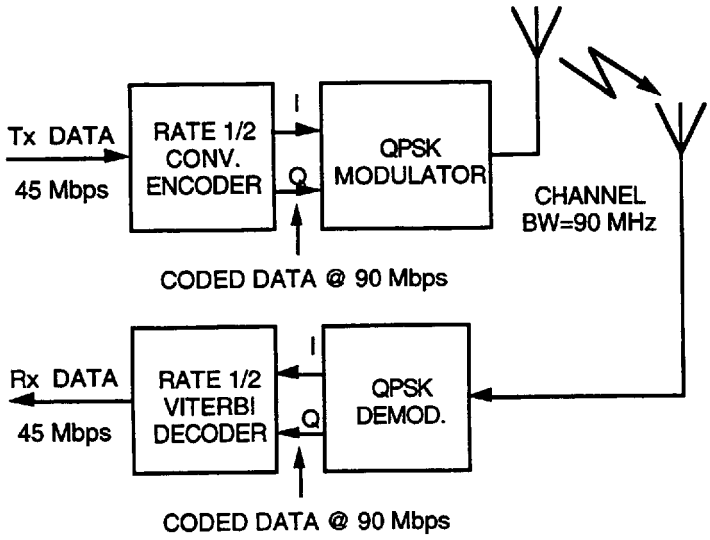
Consequently it is important to maintain the signal amplitude at an optimum level in order to maximize the performance. The performance curves shown above were measured using a digital link simulator with the signal level set at one half of full scale; i.e., the signal amplitude without noise ranged from 101 to 001 in signed magnitude format, or 101 to 010 in offset binary format. The coding gain under these conditions is about 0.2 dB less than that under optimum signal level conditions. The performance of the STEL-2060 is shown here for unpunctured operation (Rate 1/2) as well as punctured operation at the rates for which internal depuncturing is supported (Rates 2/3, 3/4 and 7/8). The error rate for uncoded data is shown for comparison.

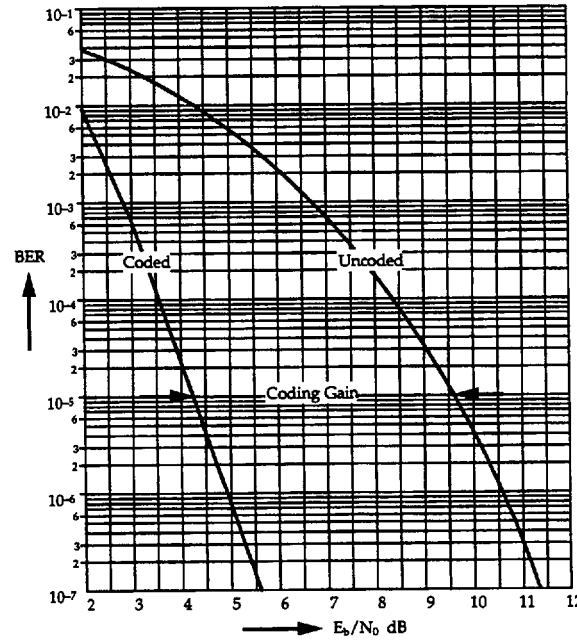
APPLICATION INFORMATION

The STEL-2060 can be used in a variety of different environments. One example of a system using a convolutional encoder with the STEL-2060 Viterbi decoder is illustrated here. The STEL-2060 cannot be used as a common decoder in multi-channel applications because of the memory incorporated on the chip which is dedicated to a single channel.

The system modulates a data stream of rate 45 Mbps using binary PSK (BPSK) or quaternary PSK (QPSK). To be able to use convolutional coding, the system must either have available the additional bandwidth needed to transmit symbols at a higher rate or must be able to make use of higher levels of modulation. e.g., by changing from BPSK to QPSK modulation, the data can be encoded at Rate $^1/_2$ without requiring any additional bandwidth. The performance improvement that can be expected is shown in the graph below.

The STEL-2060 is designed to accept symbols synchronously. **SYMCKIN** is supplied by the user to clock in the symbols. The maximum data rate is 45 Mbps, using a **SYMCKIN** frequency of 45 MHz (when **PARL** is set high) or 90 MHz (when **PARL** is set low) at rate $^1/_2$, corresponding to 90 MSymbols per sec.





QPSK Communication System Using Convolutional Encoding and Viterbi Decoding. Rate = $^1/_2$

FOR FURTHER INFORMATION
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