GigaBit Logic

Addendum # 1

GaAs IC Data Book & Designer's Guide - May 1988

SUMMARY OF CHANGES

Part #/Databook Section	Description of Changes	Databook Page	Addendum Page
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	New values for ISS, IEE, and Pd in DC Characteristics Table	1-39	
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68 I/O drawing	Title - Leaded Chip Carrier	10-5	5
Sales Offices Listing	Phone number for Centaur Corp. - Irvine office	10-7	5

Important Notices

The content of this addendum modifies GigaBit's *GaAs IC Data Book & Designer's Guide*, May 1988.

GigaBit Logic reserves the right to make changes in its devices or device specifications without notice.

GigaBit Logic warrants performance of its IC products to current specifications in accordance with GigaBit's standard warranty terms and conditions.

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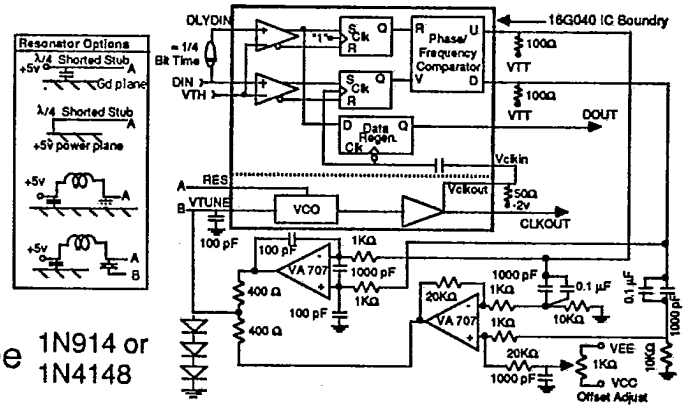
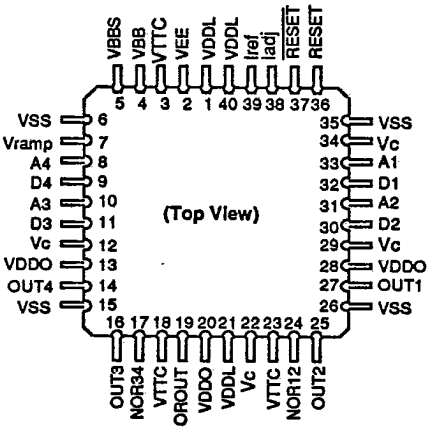
ITEM	DATABOOK PAGE #	DESCRIPTION
Three 1N914 or 1N4148		
16G060	3-42	Pinout changes. The correct pinout diagram is shown below.
GaAs IC Reliability & Quality Assurance Handbook	9-36	In the Activation Energy Results section, the median life at junction temperature of 225°C is 2,420 Hours instead of 4,240 Hours. At 175°C junction temperature, the median life is 94,758 Hours instead of 124,758 Hours.
68 I/O Package	10-5	The 68 pin package drawing is of a leaded chip carrier.
Sales Offices Listing	10-7	The phone number of the Centaur Corporation office in Irvine, California is: (714) 261-2123

Pin #	Was	Is
3	Vc	VTTC
22	VTTC	Vc
23	Vc	VTTC



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16G060
ADVANCE

Time Delay Generator
2 To 20 ns Programmable Delay/1 ps Resolution

DISTINCTIVE CAPABILITIES

- Voltage-programmable edge delay and pulsewidth
- Single-ended D inputs select true or inverted output
- ECL and 10G PicoLogic compatible I/O
- Temperature and voltage compensated using VBB threshold reference input
- On-chip VBBS (-1.2V) reference voltage supply
- GHz switching rate between programmed timing sets
- Wire-OR output capability
- Available in C- leaded or leadless chip carrier or dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- Clock system deskew
- Precision pulse generation
- Time Delay Vernier
- HS timeset formatter

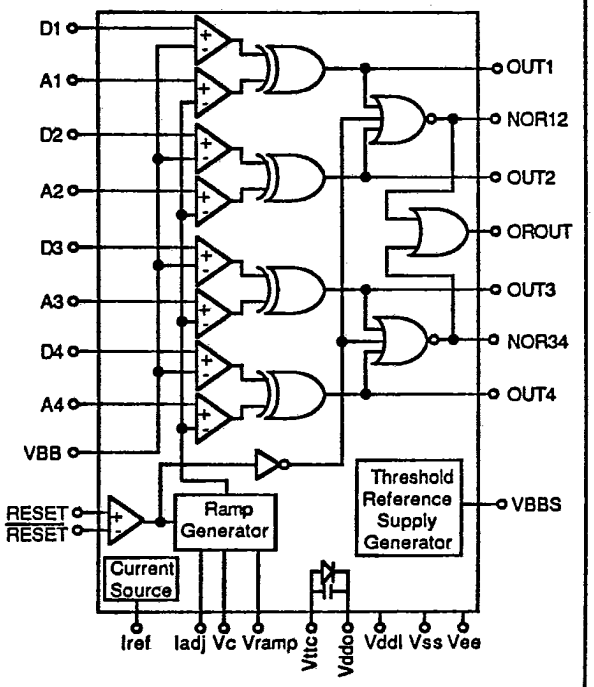
FUNCTIONAL DESCRIPTION

The 16G060 is an ECL or 10G PicoLogic compatible high resolution time delay generator. Because of its sensitive differential amplifier and linear ramp generator circuitry, the 16G060 can produce voltage ramp-based time delays with picosecond resolution over nanosecond ranges. The outputs can be inverted under control of the D (digital) inputs. Outputs OUTn are pulse outputs equal to the Reset input pulse width but with the leading edge delayed by the amount of delay programmed. The two NOR outputs provide pulses with both leading and trailing edge delay programmability. The OR output can provide up to two pulses with independent delay programmability of all leading and trailing edges. The device features a nominal -1.2V GaAs/ECL threshold reference supply voltage output on pin VBBS. Output transition times are typically 150ps.

The 16G060 features a reference level current source output (Iref) which when connected to the ramp generator adjust input (Iadj) configures an 8 to 10 ns total ramp delay. Shorter or longer delays can be programmed by externally setting the current into Iadj using a resistor to ground (Vddl).

The 16G060 is fabricated using GigaBit's high volume, production proven GaAs MESFET process technology.

BLOCK DIAGRAM



16G060 ORDERING INFORMATION

Package Type	Part Number
C-Leaded chip carrier	16G060-2C
Leadless chip carrier	16G060-2L
Unpackaged dice	16G060-2X

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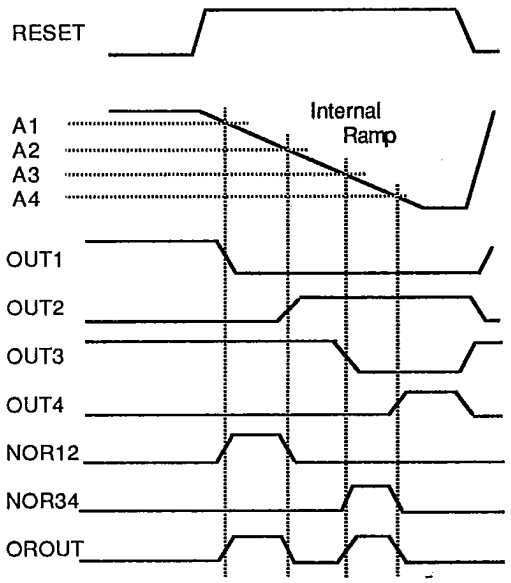
GigaBit Logic 16G060

FUNCTIONAL DESCRIPTION (cont.)



The diagram above shows one possible timing setup for the 16G060. The analog inputs A1 thru A4 are configured with DC voltages such that A1>A2>A3>A4 and the digital inputs D1 thru D4 are set to provide delayed falling edges (D = '1') or rising edges (D = '0'). (In this case D1 = D3 = '1' and D2 = D4 = '0'.) The delayed edge outputs OUT1 thru OUT4 behave as shown. The NOR12 output is a pulse with rising edge determined by A1 and falling edge determined by A2. The NOR34 output is a pulse similarly determined by A3 and A4. The OROUT output is simply the logical OR of NOR12 and NOR34.

By changing the logical states of D1 thru D4 , other combinations of true and inverted edge delay outputs can be generated. The pulse outputs can be made to produce or not produce pulses. This leads to the very useful ability to use the OROUT output or an external wire-OR of OUT1 -4 to produce different pulse or edge delays between firings of the ramp. For a total ramp time setting (using Iadj) of 2 ns, the cycle rate of the device would be once every 2.75 ns (0.75 ns required for ramp reset). This means that preset timings could be switched at a 360 MHz rate

PIN DESCRIPTIONS

D1 to D4	Data inputs
A1 to A4	Analog voltage delay programming inputs
OUT1 - 4	Delayed edge outputs
NOR12	Pulse output controlled by D1,A1,D2,A2
NOR34	Pulse output controlled by D3,A3,D4,A4
OROUT	NOR12 + NOR34
RESET, $\overline{\text{RESET}}$	Differential ramp reset/start control
Iadj	Ramp-rate control current input
Iref	Current source output for ramp-rate control
VDDO	Output driver ground (0V)
VDDL	Internal logic ground (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
Vramp	-7.0V supply to the ramp generator
VTTC	VDDO internal decoupling capacitor return. VTTC is brought into the 16G060 package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the16G060 die. VTTC is typically equal to VTT (nominally -2.0V).
Vc	-2.0V supply to ramp generator and analog input termination voltage.
VBB	Threshold reference level input. Provided to allow direct tracking of the driving logic family's output threshold voltage. Connect to VBBS when the 16G060 is driven from PicoLogic. When driving from ECL or other GaAs families, connect to that family's threshold voltage. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference voltage output. Nominally equal to -1.2V with a 40Ω source impedance. Connect to VBB when interfacing with PicoLogic. ΔVBBS/ΔTemp. = 0.6mV/°C, ΔVBBS/ΔVSS = 200mV/V.

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Functional Description (continued)

The detailed operation of the 16G060 is described by the following tables:

For outputs OUT1 thru OUT4,

Dn	OUTn
0	An
1	

Edges are defined by Input An

For output NOR12 , (assuming A1 > A2),

D1	D2	NOR12
0	0	A1 A2
0	1	(Low)
1	0	
1	1	

Reset High Pulsewidth

Output NOR34 is similar, (assuming A3 > A4),

D3	D4	NOR34
0	0	A3 A4
0	1	(Low)
1	0	
1	1	

Reset High Pulsewidth

For output OROUT, (assuming A1 > A2 > A3 > A4), a variety of output waveforms can be produced, many of which will be the same as one or the other of the NOR outputs. This results from setting one of the NOR outputs to 'Low' with the (0,1) D-input combination so that OROUT is determined by the other NOR output, or from masking one NOR waveform with the

Additional output waveforms are shown below.

D1	D2	D3	D4	OROUT
0	1	x	x	NOR34
x	0	0	0	NOR34
x	x	0	1	NOR12
1	1	1	x	NOR12
0	0	1	0	A1 A2 A3 A4
0	0	1	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	

Reset High Pulsewidth

By setting the analog voltage inputs A1 thru A4 to desired levels and switching the D1 thru D4 inputs between ramp cycles, useful combinations of timing waveforms can be generated at high speed. For example:

D1	D2	D3	D4	OROUT
0	0	0	1	A1 A2=A3 A4
1	0	0	1	
0	1	1	0	
0	1	0	0	

Reset High Pulsewidth

Since D1 thru D4 can be operated at GHz speeds, a sequence of timing changes can be executed at a maximum speed determined by the ramp cycle rate used, rather than by the speed of the DAC's used to provide analog inputs A1 thru A4.

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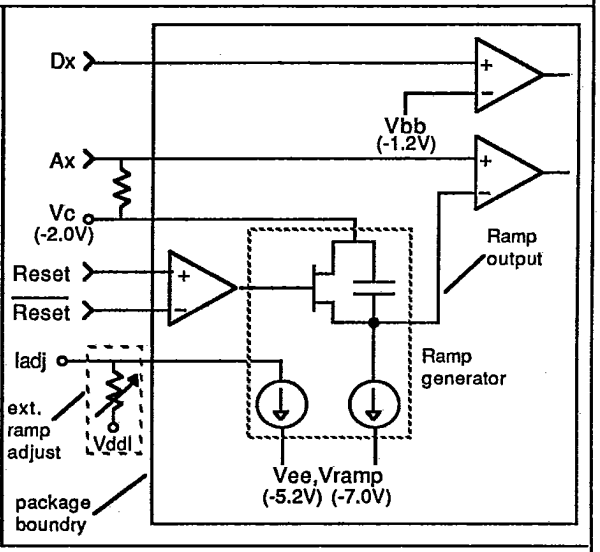
GigaBit Logic 16G060

16G060 APPLICATIONS INFORMATION

The diagram to the right shows more detail of the ramp generator circuit. Note that the proper termination point for the analog inputs is the Vc pin in order to minimize the effect of any Vc supply noise on the switching threshold of the ramp voltage comparator.

The total ramp period is adjustable from approximately 2 to 20 ns via application of between 1 and 5 mA into the Iadj pin. This current can be provided using a resistor to Vddl (Gnd) in the range of from 3500Ω to 700Ω. The Iref current output of approximately 3 mA provides for a total ramp period of about 4 to 5 ns when Iref is strapped to the Iadj input.

It is also possible to operate the 16G060 with Vramp = Vee = -5.2V. In this case, the total ramp delay is reduced to approximately 3 to 4 ns and the Iadj input will have no adjustment control.



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ABSOLUTE MAXIMUM RATINGS

(Beyond which useful life may be impaired) (Note 1)

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATING	NOTES
TSTOR	Storage Temperature	- 65 °C to + 150 °C	
TJ	Junction Temperature	- 55 °C to + 150 °C	
TC	Case Temperature Under Bias	- 55 °C to + 125 °C	2
VDDO	Output Driver Supply Voltage	VSS to + 1.0 V	
VSS	Supply Voltage	- 4.0 V to + 0.5 V	
VEE	Supply Voltage	-7.0 V to VSS + 0.5 V	
VRAMP	Supply Voltage	-7.5 V to VSS + 0.5 V	
VIND	Voltage Applied to Digital Inputs, Continuous (Vss = -3.4V, Vee = -5.2V, Vramp = -7.0V)	- 4.0 V to + 0.5 V	
VINA	Voltage Applied to Analog Inputs, Continuous (Vss = -3.4V, Vee = -5.2V, Vramp = -7.0V)	-5.7 V to -1.5 V	
VADJ	Voltage Applied to Iadj Input	-5.7 V to -1.5 V	
IIN	Current Into Any Input; Continuous	- 0.5 mA to 1.0 mA	
VOUT	Voltage Applied to Any Output	-4.0V to +7.0 V	3
IOUT	Current From Any Output; Continuous	-100 mA	
PD	Power Dissipation Per Output POUT = (VDDO-VOUT) x IOUT	100 mW	
VBB	Threshold Reference Input Voltage	-4.0V to +0.5V	
IBB	Input current (from interfacing family)	-0.5mA to +1.0mA	
VTTC	VDDO Internal Decoupling Cap. Return	-6.0 V to VDDO	
VTT	Load Termination Supply	-6.0 V to VDDO + 6.0 V	

Notes:
1. All voltages specified with VDDL defined as ground. Positive curent is defined as current into the device. Power supply sequencing is not necessary, but since the VEE supply is used to bias off the normally-on depletion mode FETs, sustained (>5 secs.) application of VSS in the absence of VEE may result in excessive power dissipation and damage to the device.
2. TC is measured at case top. 3. Subject to IOUT and PD limitations.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TC	Case OperatingTemperature		25		℃	
VDDL	Logic Supply Voltage		Gnd		V	1
VDDO	Output Driver Supply Voltage	-0.8	Gnd	1.0	V	
VC	Ramp Supply Voltage	-2.2	-2.0	-1.8	V	
VSS	Supply Voltage	- 3.5	- 3.4	- 3.3	V	
VEE	Supply Voltage	- 5.5	- 5.2	- 5.1	V	
VRAMP	Ramp Supply Voltage	- 7.5	- 7.0	- 6.5	V	
VTTC	VDDO Internal Decoupling Return	VSS	VTT	VDDO	V	2
VTT	Load Termination Supply Voltage	VSS	- 2.0	- 2.0	V	2
RLOAD	Output Termination Load Resistance	25	50	100	Ω	

Notes: 1. Tcase measured at case top. User attention to appropriate device thermal management is recommeded. See GigaBit Application Note 3, "Thermal Management of PicoLogic and NanoRam GaAs Digital IC Families" for a complete discussion of device thermal management. Heatsinks are available from GigaBit. See page 8, notes 6 and 7.
2. The RLOAD and VTT combination used is subject to maximum output current and power restrictions.

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GigaBit Logic

16G060

DC CHARACTERISTICS (Notes 1,2)

VSS = -3.5V to -3.3V, VEE =-5.2V, Vramp = -7.0V, Vc = -2.0V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	16G060 Minimum	16G060 Typical	16G060 Maximum	Units	Test Conditions	Notes
VOH	Output Voltage High	- 0.8	-0.4	-0.3	V		
VOL	Output Voltage Low	- 2.0	-1.9	- 1.8	V		
IOH	Output Current High		-70	-60	mA	VOH = -0.8V	3
VIH	Input Voltage High	- 1.0		VDDL	V		6
VIL	Input Voltage Low	VSS		- 1.6	V		6
IIN	Input Current	-500		500	uA	VIN = -1.0V to -1.6V	6
VAin	A1 -A 4 Input Voltage	- 4.0		- 2.4	V		
Iref	Ref. Current Output		2.0		mA		
VBBS	Thresh. Ref. Voltage		-1.2		V		4
Iadj	Ramp Rate Control	1.0	2.0	5.0	mA		
Ic	Vc Supply Current		20		mA		
Iramp	Vramp Supply Current		20		mA		
ISS	Power Supply Current		200		mA		
IEE	Power Supply Current		50		mA		
PD	Power Dissipation		1000		mW		5

Notes:

1. These characteristics are applicable from DC to 500 MHz.
2. Test conditions unless otherwise indicated: VBB = -1.3V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to -2.0V.
3. IOH is the available source follower output current at VOH = -0.8V.
4. Nominally equal to -1.2V with a 40Ω source impedance. The range of VBBS at 25°C is -1.05V to -1.3V. ΔVBBS/ΔTemp. = +0.6mV/°C; ΔVBBS/ΔVSS = +0.2mV/mV.
5. Measured at nominal supply voltages and 50% output duty cycle. Excludes VDDO output source follower power (typically 15 mW per loaded output) .
6. Digital inputs only (Reset, Reset, D1, D2, D3, D4).

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE =-5.2V, Vramp = -7.0V, Vc = -2.0V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER		Tc = +25°C MIN	TYP	MAX		UNITS	NOTES
tr, tf	Output rise/fall times			125	175		ps	2
tpwr	Reset pulse width		750	600			ps	
tdr	Reset delay			150			ps	
tdrs	Ramp start delay			150			ps	3
tdo1	Output delay (OUTn)		400	500	600		ps	
tdo2	Output delay (OR/NOR)		400	450	550		ps	
Linearity	Analog voltage to delay time linearity			1.0			%	
Δe	Edge placement accuracy			Tbd			ps	

NOTES:

1. Test conditions unless otherwise indicated: VBB = -1.2V, VTT = -2.0V, VTTC = VTT, RLOAD = 50Ω to VTT, VIH = -0.7V, VIL = -1.7V, VOH ≥ -0.7V, VOL ≤ -1.7V, VAin = -2.7V to -3.7V. Input signal rise and fall times ≤ 200 ps.
2. Rise and fall times are measured at the 20% and 80% points of the transition from Vol max to Voh min.
3. Measured with A input at -2.4V.

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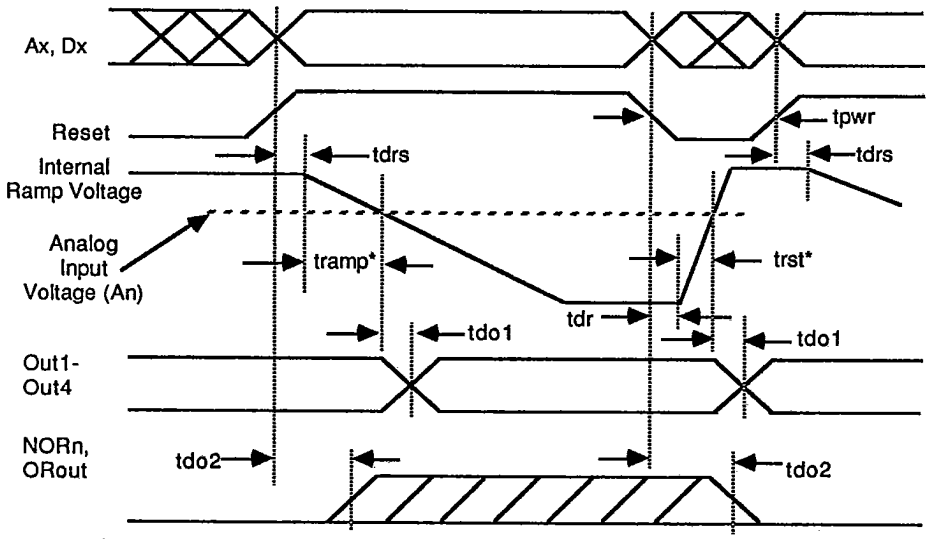
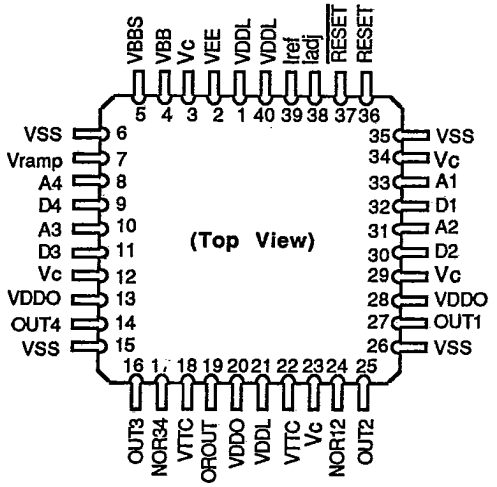
GBL GigaBit Logic **16G060**

SWITCHING WAVEFORMS



* tramp and trst are delays determined by the ramp rate and analog input voltage set by the user.

PIN FUNCTION DRAWING - PACKAGE TYPES "L" AND "C"



NOTES: Pin 1 is marked for orientation.

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