

# Am2167

## 16,384x1 Static RAM

### DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 35 ns maximum
- Automatic power down when deselected
- Low power dissipation
  - Am2167: 660 mW active, 110 mW power down
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL-compatible interface levels
- No power-on current surge

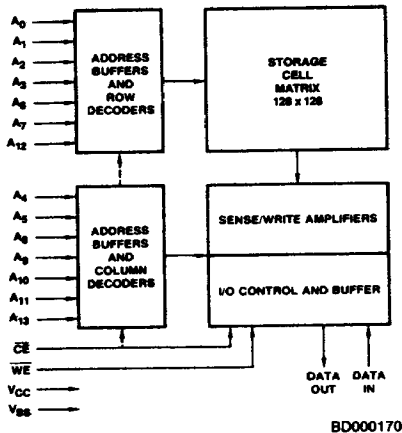
### GENERAL DESCRIPTION

The Am2167 is a high-performance, 16,384-bit, static, read/write, random-access memory. It is organized as 16,384 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to six standard Schottky TTL loads or up to seven standard TTL loads.

Only a single +5-volt power supply is required. When deselected ( $\overline{CE} \geq V_{IH}$ ), the Am2167 automatically enters a power-down mode which reduces power dissipation by 80%.

Data In and Data Out use separate pins and are the same polarity allowing them to be connected together for operation in a common data bus environment. Data Out is a three-state output allowing similar devices to be wire-OR'd together.

### BLOCK DIAGRAM

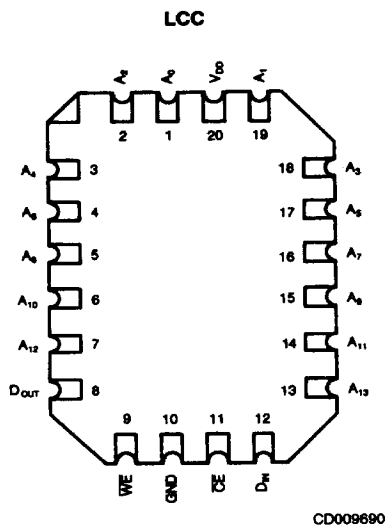
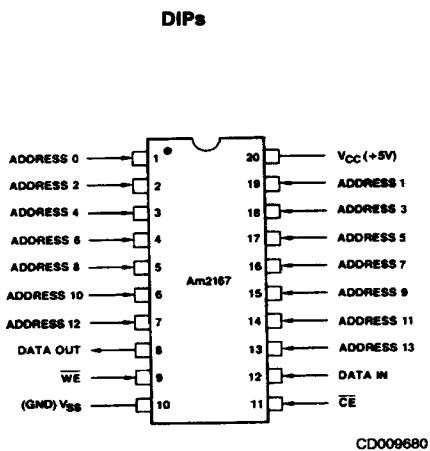


### PRODUCT SELECTOR GUIDE

Part Number	Am2167-35	Am2167-45	Am2167-55	Am2167-70
Maximum Access Time (ns)	35	45	55	70
Maximum Active Current (mA)	120	120 (160 mil)	120 (160 mil)	120 (160 mil)
Maximum Standby Current (mA)	20	20 (30 mil)	20 (30 mil)	20 (30 mil)
Full Military Operating Range Version	No	Yes	Yes	Yes

## CONNECTION DIAGRAMS

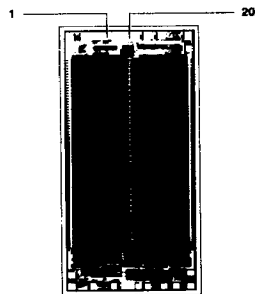
### Top View



Note: Pin 1 is marked for orientation.

## METALLIZATION AND PAD LAYOUT

Address Designators	
External	Internal
A <sub>0</sub>	A <sub>1</sub>
A <sub>1</sub>	A <sub>6</sub>
A <sub>2</sub>	A <sub>2</sub>
A <sub>3</sub>	A <sub>5</sub>
A <sub>4</sub>	A <sub>3</sub>
A <sub>5</sub>	A <sub>0</sub>
A <sub>6</sub>	A <sub>4</sub>
A <sub>7</sub>	A <sub>13</sub>
A <sub>8</sub>	A <sub>10</sub>
A <sub>9</sub>	A <sub>6</sub>
A <sub>10</sub>	A <sub>11</sub>
A <sub>11</sub>	A <sub>9</sub>
A <sub>12</sub>	A <sub>12</sub>
A <sub>13</sub>	A <sub>7</sub>



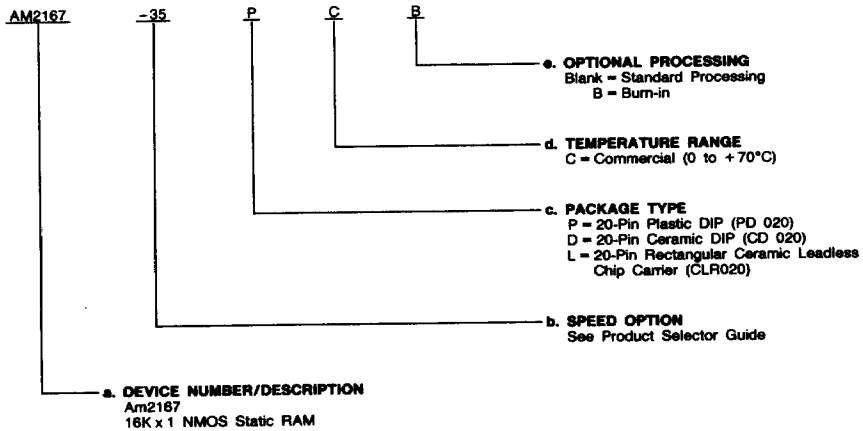
Die Size: 0.121" x 0.249"

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM2167-35	PC, PCB, DC, DCB, LC, LCB
AM2167-45	PD, PCB, DC, DCB
AM2167-55	
AM2167-70	

#### Valid Combinations

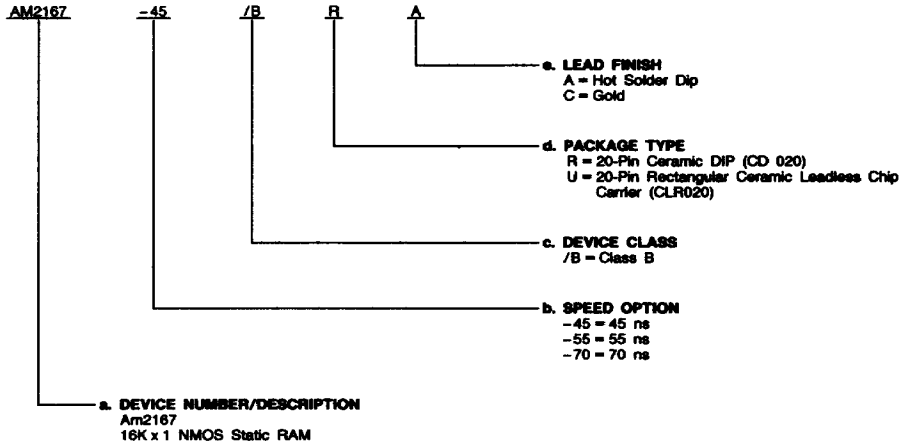
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM2167-45	/BRA, /BUA
AM2167-55	
AM2167-70	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

#### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

#### **A<sub>0</sub> - A<sub>13</sub> Address (Inputs)**

The address input lines select the RAM location to be read or written.

#### **CE Chip Enable (Input, Active LOW)**

The Chip Enable selects the memory device.

#### **WE Write Enable (Input, Active LOW)**

When Write Enable is LOW and Chip Enable is also LOW, data is written into the location specified on the address pins.

#### **D<sub>IN</sub> Data (Input)**

This pin issued for entering data during write operation.

#### **D<sub>OUT</sub> Data (Output, Three State)**

This pin is three state during write operation. It becomes active when CE is LOW and WE is HIGH.

#### **V<sub>CC</sub> Power Supply**

#### **V<sub>SS</sub> Ground**

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
Signal Voltages with Respect to Ground .....	-3.5 V to +7.0 V
Power Dissipation .....	1.2 W
DC Output Current .....	50 mA

Maximum ratings are to be for system design reference, parameters given may not be 100% tested by AMD.

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES (Note 4)

Commercial (C) Devices	Ambient Temperature (T <sub>A</sub> ) .....	0 to +70°C
	Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V
Military (M) Devices	Ambient Temperature (T <sub>A</sub> ) .....	-55 to +125°C
	Supply Voltage (V <sub>CC</sub> ) .....	+4.5 to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted) (Note 4)

Parameter Symbol	Parameter Description	Test Conditions	Am2167-35		Am2167-45, Am2167-55, Am2167-70		Unit
			Min.	Max.	Min.	Max.	
I <sub>OH</sub>	Output HIGH Current	V <sub>OH</sub> = 2.4 V	V <sub>CC</sub> = 4.5 V		-4	-4	mA
I <sub>OL</sub>	Output LOW Current	V <sub>OL</sub> = 0.4 V	COM'L		16	16	mA
			MIL		12	12	
			2.2	6.0	2.2	6.0	
V <sub>IH</sub>	Input HIGH Voltage		-2.5	0.8	-2.5	0.8	V
V <sub>IL</sub>	Input LOW Voltage		-10	10	-10	10	μA
I <sub>Ix</sub>	Input Load Current	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-50	50	-50	50	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled	5		5		pF
C <sub>I</sub>	Input Capacitance	Test Frequency = 1.0 MHz	6		6		pF
C <sub>O</sub>	Output Capacitance	T <sub>A</sub> = 25°C, All pins at 0 V, V <sub>CC</sub> = 5 V (Note 9)					
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	Max V <sub>CC</sub> , CE ≤ V <sub>IL</sub> Output Open	COM'L		120	120	mA
			MIL		N/A	160	
			20	20	20	30	
I <sub>SB</sub>	Automatic $\overline{CE}$ Power Down Current	MAX V <sub>CC</sub> , (CE ≥ V <sub>IH</sub> ) (Note 3)	COM'L		20	20	mA
			MIL		N/A	30	

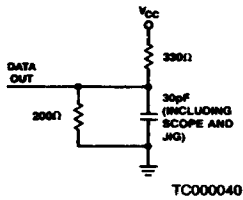
- Notes: 1. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance. Output timing reference is 1.5 V.
2. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull-up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required to keep the device deselected during V<sub>CC</sub> power up. Otherwise I<sub>SB</sub> will exceed values given.
4. For test and correlation purposes, ambient temperature is defined as the "Instant-on" case temperature.
5. The device must be selected during the previous cycle. Otherwise t<sub>AA</sub> and t<sub>RC</sub> are equivalent to t<sub>ACS</sub>.
6. Transition is measured ±500 mV from steady state voltage with load specified in Figure 2 for t<sub>HZ</sub>, t<sub>LZ</sub>, t<sub>OW</sub> and t<sub>WZ</sub>.
7.  $\overline{WE}$  is HIGH for read cycle.
8. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
9. Parameter not 100% tested. Guaranteed by characterization.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (Note 1) (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

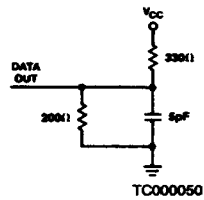
No.	Parameter Symbol	Parameter Description	Am2167-35		Am2167-45		Am2167-55		Am2167-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>											
1	$t_{RC}$	Address Valid to Address Do Not Care Time (Read Cycle Time) (Note 5)	30		40		50		70		ns
2	$t_{AA}$	Address Valid to Data Out Valid Delay (Address Access Time) (Note 5)		30		40		50		70	ns
3	$t_{ACS}$	Chip Enable LOW to Data Out Valid (Chip Enable Access Time)		35		45		55		70	ns
4	$t_{LZ}$	Chip Enable LOW to Data Out On (Notes 6, 9)	5		5		5		5		ns
5	$t_{HZ}$	Chip Enable HIGH to Data Out Off (Notes 6, 9)	0	20	0	25	0	30	0	40	ns
6	$t_{OH}$	Output hold time from address change	COM'L	3	3	3	3	3	3	3	ns
			MIL	1	1	1	1	1	1	1	ns
7	$t_{PD}$	Chip Enable HIGH to Power Down Delay (Note 9)		25		30		30		55	ns
8	$t_{PU}$	Chip Enable LOW to Power Up Delay (Note 9)	0		0		0		0		ns
<b>WRITE CYCLE</b>											
9	$t_{WC}$	Address Valid to Address Do Not Care (Write Cycle Time)	30		40		50		70		ns
10	$t_{WP}$	Write Enable LOW to Write Enable HIGH (Note 2)	20		20		25		40		ns
11	$t_{WR}$	Write Enable HIGH to Address	0		0		0		0		ns
12	$t_{WZ}$	Write Enable LOW to Output in HIGH Z (Notes 6 & 9)	0	20	0	20	0	25	0	35	ns
13	$t_{DW}$	Data In Valid to Write Enable HIGH	15		15		20		30		ns
14	$t_{DH}$	Data Hold Time	5		5		5		5		ns
15	$t_{AS1}$	Address Valid to Write Enable LOW (WE Controlled Write)	5		5		5		5		ns
	$t_{AS2}$	Address Valid to Write Enable LOW (CE Controlled Write)	0		0		0		0		ns
16	$t_{CW}$	Chip Enable LOW to Write Enable HIGH (Note 2)	30		40		50		55		ns
17	$t_{OW}$	Write Enable HIGH to Output in LOW Z (Notes 6 & 9)	0		0		0		0		ns
18	$t_{AW}$	Address Valid to End of Write	30		40		50		70		ns

Notes: See notes following DC Characteristics table.

**SWITCHING TEST CIRCUITS**



**A. Output Load**



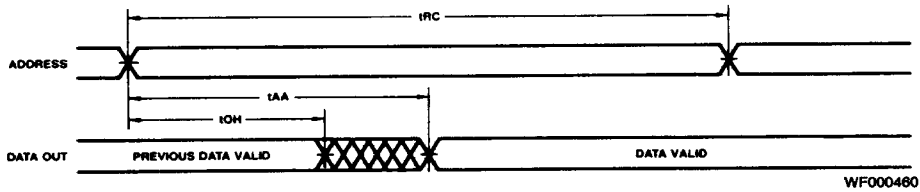
**B. Output Load for  $t_{HZ}$ ,  $t_{LZ}$ ,  $t_{OW}$ ,  $t_{WZ}$**

# SWITCHING WAVEFORMS

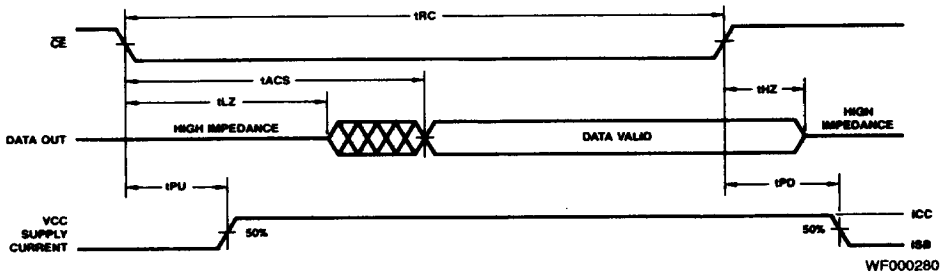
## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



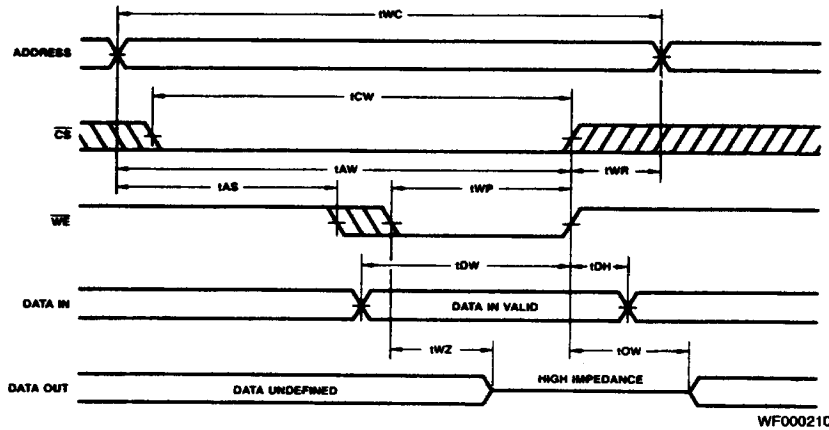
Read Cycle No. 1 (Notes 5, 7)



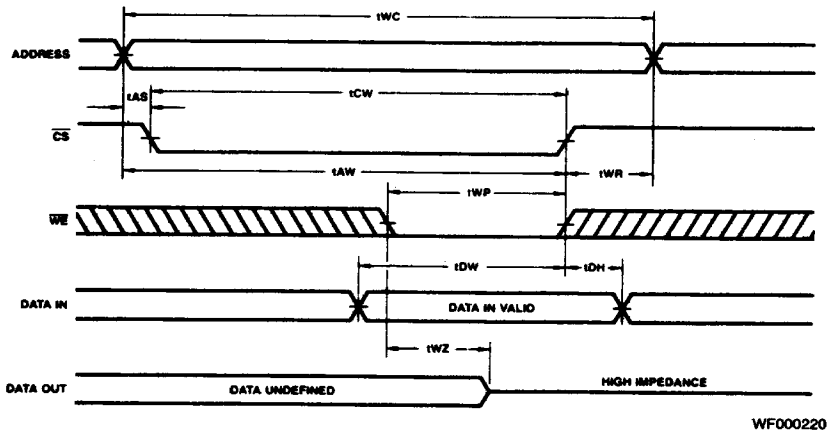
Read Cycle No. 2 (Notes 7, 8)

Notes: See notes following DC Characteristics table.

**SWITCHING WAVEFORMS (Cont'd.)**



**Write Cycle No. 1 ( $\overline{WE}$  Controlled)**



**Write Cycle No. 2 ( $\overline{CE}$  Controlled)**

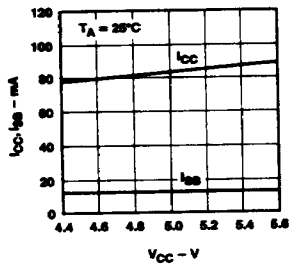
Note: If  $\overline{CE}$  goes high simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

4



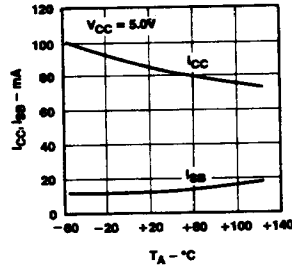
## TYPICAL PERFORMANCE CURVES

**Supply Current versus Supply Voltage**



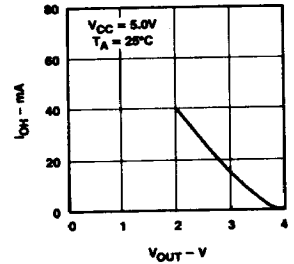
OP000940

**Supply Current versus Ambient Temperature**



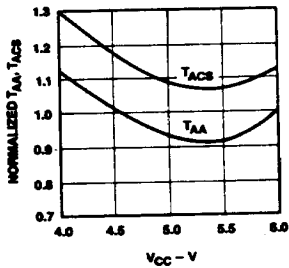
OP000950

**Output Source Current versus Output Voltage**



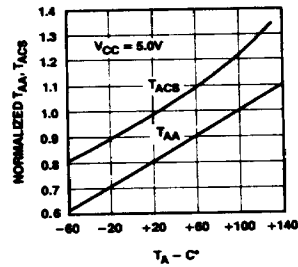
OP000960

**Normalized Access Time versus Supply Voltage**



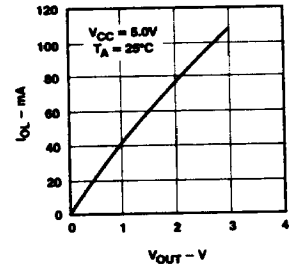
OP000970

**Normalized Access Time versus Ambient Temperature**



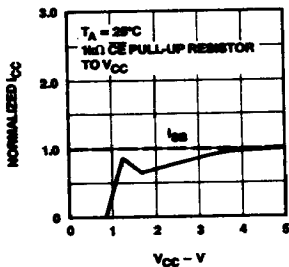
OP000980

**Output Sink Current versus Output Voltage**



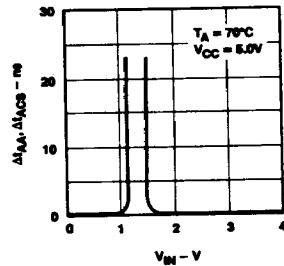
OP000990

**Typical Power-On Current versus Power Supply**



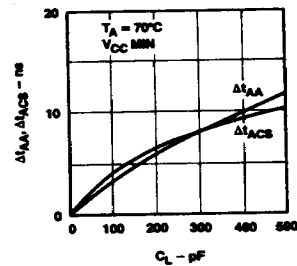
OP001000

**Access Time Change versus Input Voltage**



OP001010

**Access Time Change versus Output Loading**



OP001020