National Semiconductor

DM9318 Priority Encoders

General Description

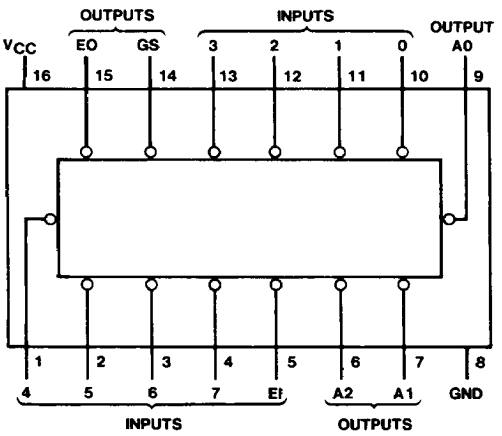
These TTL encoders feature priority decoding of the input data to ensure that only the highest-order data line is encoded. All inputs are buffered to represent one normalized Series 54/74 load. The DM9318 and DM8318 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

Features

- Pin for pin with popular DM54148/74148
- Encodes 8 data lines to 3-line binary (octal)
- Applications include:
  - N-bit encoding
  - Code converters and generators
- Typical data delay 10 ns
- Typical power dissipation 190 mW

Connection Diagram

Dual-In-Line Package



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Order Number DM9318J, DM9318N or DM9318W
See NS Package Number J16A, N16E or W16A

Function Table

Inputs									Outputs				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High Logic Level, L = Low Logic Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	0 Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	0 Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	MIL	−35		−85	mA
			COM	−35		−85	
I_{CC1}	Supply Current Condition 1	V_{CC} = Max, (Note 3)			35	55	mA
I_{CC2}	Supply Current Condition 2	V_{CC} = Max, (Note 4)			40	60	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC1} is measured with all inputs and outputs open.

Note 4: I_{CC2} is measured with inputs 7 and EI grounded and outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to ABCD In Phase		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to ABCD In Phase		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to ABCD Out of Phase		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to ABCD Out of Phase		19	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to E0 Out of Phase		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to E0 Out of Phase		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to GS In Phase		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to GS In Phase		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	EI to A0, 1, 2 In Phase		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	EI to A0, 1, 2 In Phase		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	EI to GS In Phase		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	EI to GS In Phase		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	EI to E0 In Phase		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	EI to E0 In Phase		26	ns

Logic Diagram

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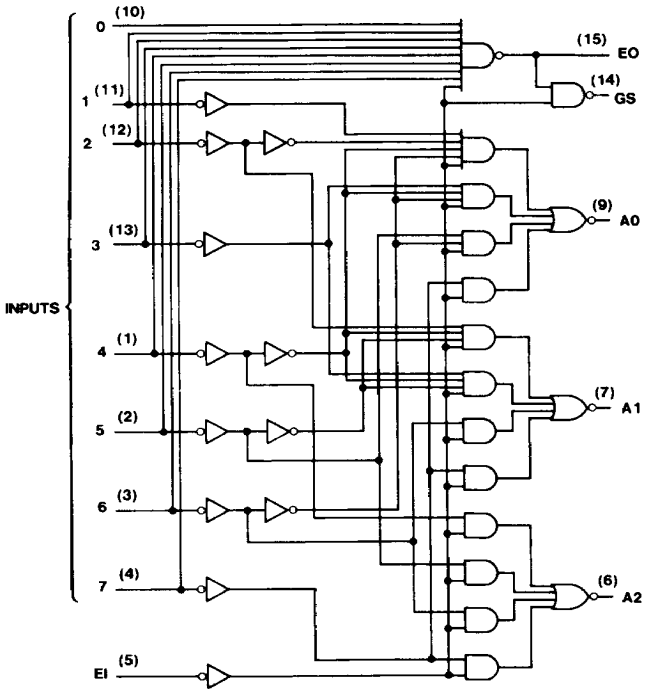

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