National Semiconductor

ADVANCE INFORMATION
March 1990

FLX™1000 CMOS FLEXCELL Gate Arrays

General Description

National Semiconductor presents its FLX 1000-Series 0.8 micron CMOS gate arrays. Fabricated with National's advanced dual-layer metal, one-layer poly M2CMOS III technology, this very high speed family features a 1.0 micron drawn geometry with a 0.8 micron effective channel length.

The 0.8 micron family of gate arrays offers complexities from 21,000 to 252,000 raw gates with utilization factor greater than 40%. Up to 64 Kbits static RAM or up to 192 Kbits ROM can be implemented on the largest gate array with the NSC proprietary module generator software. The speed combined with very high gate count and large memory modules in the FLX1000 family make it well suited for achieving system-on-silicon integration. The family offers boundary scan pads fully conformed to the IEEE P1149.1 standard for design for testability.

Features

- Two-layer metal, one-layer poly interconnect for high performance and flexibility
- Latch-up immune state-of-the-art 0.8μ Leffective (1.0μ drawn) programmable silicon-gate M2CMOS III technology
- Ultra-high performance: 500 ps typical gate delays (2-input) NAND, 2 loads, 5.0V, 25°C ambient)
- Core macros fully compatible with the 0.8 micron CMOS standard cell family
- High ESD protection ≥ 2000V
- Complexity up to 252,000 raw gates
- A total of 444 selectable signal/power pads which may be used as an Input, Output, bidirectional IO, Power or Ground Pad
- Standard and high drive versions of macro cells
- TTL Output Drivers capable of driving up to 48 mA with selectable slew rates in a single I/O location
- Output Drivers capable of driving transmission line with characteristic impedance as low as 25Ω in a single I/O location
- Input and I/Os: TTL, CMOS, Schmitt Trigger
- Oscillator macros up to 75 MHz
- Power-On-Reset macro
- LSSD latches and scan path flip-flops to facilitate testability
- Boundary scan pads conforming to the IEEE P1149.1 standard (JTAG)
- Auto place-and-route at greater than 40% utilization
- Several options of standard production packages
- Fully integrated design automation system
- Separate Power Ring for Core and I/Os to minimize noise
- Module generated high density static single and dual port RAMs or high speed single, dual and multi-port RAM
- High speed high density RAM module generator
  t_{cyc} = 30 ns @ 8K x 8 (worst case*)
  t_{acc} = 20 ns @ 8K x 8 (worst case*)
  8K x 8 consumes 45% of FLX1250
- Module generated high density ROM

Product Configurations

Device	Gate Complexity	Estimated Usable Gates	Available IO Pads	
			Wirebond	TAB
FLX1021	21000	12000	84	108
FLX1038	38000	20000	124	156
FLX1056	56000	28000	152	196
FLX1080	80000	40000	188	240
FLX1120	122000	57000	232	300
FLX1160	160000	72000	268	348
FLX1200	207000	90000	308	400
FLX1250	252000	108000	340	444

*Worst case process, V_{DD} = 4.5V, T_{junc} = +100°C

RRD-B20M30/Printed in U. S. A.

Sample Core Macros

Function	Macro Name	Gate Equiv
GATES		
2-Input NAND Gate (1X)	nd2	1
2-Input NAND Gate, Dual (1X)	nd2d	1.5
3-Input NAND Gate (1X)	nd3	1.5
4-Input NAND Gate (1X)	nd4	1.5
2-Input NOR Gate (1X)	nr2	1
3-Input NOR Gate (1X)	nr3	1.5
4-Input NOR Gate (1X)	nr4	1.5
2-Input Exclusive-OR (2X)	xo202	3
2-Input Exclusive-NOR (2X)	xn202	3
2-Input AND Gate (1X)	an2	1.5
3-Input AND Gate (1X)	an3	2
2-Input OR Gate (2X)	or202	1.5
3-Input OR Gate (1X)	or3	2
BUFFERS		
Inverter (1X)	iv1	0.6
Inverter (2X)	iv102	0.6
Inverter (4X)	iv104	1.5
Driver (8X)	dr108	3.5
Driver (13X)	dr113	6
Driver, TRI-STATE (8X)	drt208	6
LATCHES		
D-Latch with Enableb (2X)	ld202	3.5
D-Latch with Resetb, set, Enable, (2X)	ldrs102	5
FLIP-FLOPS		
D Flip-Flop (2X)	fd102	6
D Flip-Flop with Set-Bar and Reset-Bar (2X)	fdrs102	7
MULTIPLEXERS AND DEMULTIPLEXERS		
2 to 1 Multiplexer (2X)	mx202a	2.5
4 to 1 Multiplexer (3X)	mx403a	6

Sample I/O Buffers

CMOS Inputs					
Non-Inverting			Inverting*		
2x	8x	15x	2x	8x	11x
ic01	ic02	ic03	ic51	ic52	ic53

TTL Inputs					
Non-Inverting			Inverting*		
2x	8x	15x	2x	8x	11x
it01	it02	it03	it51	it52	it53

CMOS Schmitt-Trigger					
Non-Inverting			Inverting*		
2x	8x	15x	2x	8x	11x
is01	is02	is03	is51	is52	is53

TTL Schmitt-Trigger					
Non-Inverting			Inverting*		
2x	8x	15x	2x	8x	11x
il01	il02	il03	il51	il52	il53

Non-Inverting Output Drivers (TTL/CMOS Compatible)		
Characteristic	Output Current Source/Sink (mA)	Macro Name
Optimized for TTL Loads	5/7 21/29	ot25 ot23
Balance CMOS Output 25Ω 50Ω	 33/29 16/14	 oz61 oz63

*Conforming to the IEEE P1149.1 (JTAG) standard, inverting inputs are configured as a non-inverting input driving an inverter. The inverting input is a hardware macro located in the I/O cell.

DC Characteristics

Specified at V_{DD} = 5V ± 10%, V_{SS} = Ground, Over All Temperature Ranges (Unless Otherwise Specified)

Symbol	Parameter	Conditions	V_{DD}	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Notes 1, 5)						
	CMOS Level		4.5V			0.3 V_{DD}	V
	TTL Level (Low Power)		4.5V			0.8	V
	TTL Level (High Speed)		4.5V			0.8	V
V_{IH}	High Level Input Voltage (Notes 1, 5)						
	CMOS Level		5.5V	0.7 V_{DD}			V
	TTL Level (Low Power)		5.5V	2.0			V
	TTL Level (High Speed)		5.5V	2.25			V
V_{t+}	CMOS Positive Going Threshold		4.5V	3.2			
	Voltage-Schmitt Trigger (Notes 1, 5)		5.5V			3.9	V
V_{t-}	CMOS Negative Going Threshold		4.5V	1.0			
	Voltage-Schmitt Trigger (Notes 1, 5)		5.5V			1.4	V
V_H	CMOS Hysteresis Voltage-Schmitt Trigger (Notes 1, 5)			1.0	1.6		V
V_{t+}	TTL Positive Going Threshold		4.75V	1.2			
	Voltage-Schmitt Trigger (Notes 1, 5)		5.25V			2.0	V
V_{t-}	TTL Negative Going Threshold		4.75V	0.7			
	Voltage-Schmitt Trigger (Notes 1, 5)		5.25V			1.5	V
V_H	TTL Hysteresis Voltage-Schmitt Trigger (Notes 1, 5)			0.45	0.5		V
I_{IL}	Low Level Input Current	V_{IN} = V_{SS}					
	Without Pull-Up Resistor		5.5V	−10			μA
	With Weak Pull-Up Resistor		5.5V	−150	−40		μA
	With Strong Pull-Up Resistor		5.5V	−3000	−1000		μA
I_{IH}	High Level Input Current	V_{IN} = 5.5V					
	Without Pull-Up Resistor		5.5V			10	μA
	With Weak Pull-Down Resistor		5.5V		40	150	μA
	With Strong Pull-Down Resistor		5.5V		1000	3000	μA

DC Characteristics

Specified at V_{DD} = 5V ± 10%, V_{SS} = Ground, Over All Temperature Ranges (Unless Otherwise Specified) (Continued)

Symbol	Parameter	Conditions	V_{DD}	Min	Typ	Max	Units
V_{OL}	Low Voltage Output	$V_{IN} = V_{IL}$ or V_{IH}					
		I_{OL} = 20 μA	4.5V			0.1	V
	ot25	I_{OL} = 7 mA	4.5V			0.4	V
	ot23	I_{OL} = 29 mA	4.5V			0.5	V
	oz63	I_{OL} = 14 mA	4.5V			0.5	V
	oz61	I_{OL} = 29 mA	4.5V			0.5	V
V_{OH}	High Voltage Output	$V_{IN} = V_{IL}$ or V_{IH}					
		I_{OH} = −20 μA	4.5V	V_{DD} − 0.1			V
	ot25	I_{OH} = 5 mA	4.5V	3.7			V
	ot23	I_{OH} = 21 mA	4.5V	3.7			V
	oz63	I_{OH} = 16 mA	4.5V	3.7			V
	oz61	I_{OH} = 33 mA	4.5V	3.7			V
I_{OZL}	Low Level TRI-STATE Output Current (Notes 2, 3)	$V_O = V_{SS}$ V_{IN} (en) = V_{IL} or V_{IH}	5.5V	−20			μA
I_{OZH}	High Level TRI-STATE Output Current (Notes 2, 3)	V_O = 5.5V V_{IN}(en) = V_{IL} or V_{IH}	5.5V			20	μA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{SS}$ or V_{DD}	User Design Dependent				
C_{IN}	Input Capacitance (Note 4)					20	pF
C_{OUT}	Output Capacitance (Note 4)					20	pF

Note 1: This test cannot be performed unless a hook-up to a special output is defined.

Note 2: I_{OZ} specifications are for output buffers without pull up or down resistors.

Note 3: Specification limits for I/Os with both TRI-STATE outputs and pull up or down resistors will be the sum of the individual leakages.

Note 4: C_{IN} and C_{OUT} specifications are guaranteed by design. This parameter is tested only for device qualification.

Note 5: This parameter can only be guaranteed if a combination path is defined. Not to be functionally tested.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	−0.3V to +6.0V
Input Voltage (V_I)	−0.3V to V_{DD} + 0.3V
DC Input Current (I_I)	±200 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions

DC Supply Voltage (V_{DD})	4.5V to 5.5V
Operating Ambient Temperature Range (T_A)	
Commercial	0°C to +70°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C

Typical Propagation Delays of Selected Macros (V_{DD} = 5.0V, T_{amb} = 25°C)

Macro	Function	0 pF Delay (ns)		ΔDelay/0.2 pF* (ns)	
		LH	HL	LH	HL
LOGIC GATES					
nd2	2-Input NAND	0.24	0.15	0.17	0.18
nr2	2-Input NOR	0.24	0.28	0.34	0.10
iv1	Inverter	0.18	0.18	0.12	0.12
xo202	2-Input XOR (2X)	0.60	0.58	0.09	0.06
FLIP-FLOPS/LATCHES					
fdrs102	D-FF with Resetb and Setb (2X)				
	CLK to Q	1.70	1.54	0.10	0.06
	CLK to QB	1.13	1.27	0.09	0.06
	RB to Q		0.68		0.07
	SB to Q	1.21		0.10	
ldrs102	D-Latch with Resetb, Set, Enable (2X)				
	D to Q	1.01	1.53	0.10	0.07
	D to QB	1.93	1.43	0.10	0.06
	E to Q	1.36	1.65	0.10	0.07
	E to QB	2.05	1.86	0.10	0.06
	RB to Q		0.97		0.10
	S to Q	0.46		0.10	
MUX					
mx403a	4 to 1 Multiplexer (3X)				
	A to Y	0.76	1.04	0.06	0.04
	B to Y	0.76	1.04	0.06	0.04
	C to Y	0.74	1.02	0.06	0.04
	D to Y	0.74	1.03	0.06	0.04
	S0 to Y	1.17	1.43	0.03	0.04
	S1 to Y	0.68	0.64	0.06	0.04
mx202a	2 to 1 Multiplexer (2X)				
	A to Y	0.60	0.61	0.06	0.06
	B to Y	0.60	0.61	0.06	0.06
	S to Y	0.60	0.54	0.09	0.06

Note: All Delay times are in ns. Conditions are: V_{DD} = 5.0V with Input Pulse Trise = Tfall = 2.0 ns, measured from 10% to 90% point, Ambient Temperature = 25°C, Typical Process.

*This is the estimated capacitive load for a fanout of 2. Actual value after placement and routing could differ.

Typical Propagation Delays of Selected Macros (V_{DD} = 5.0V, T_{amb} = 25°C) (Continued)

Macro	Function	0 pF (ns)		ΔDelay/pF* (ns)	
		LH	HL	LH	HL
INPUT BUFFERS					
ic01	CMOS Non-Inverting Input (2X)	0.34	0.47	0.44	0.31
it01	TTL Non-Inverting Input (2X)	0.71	0.61	0.44	0.39

Macro	Function		Output Load Capacitance			
			15 pF	50 pF	100 pF	200 pF
OUTPUT BUFFERS						
ot25	TTL Output Buffer (Note 1)	t_{PLH} t_{PHL}	1.62 1.81	2.60 3.62	3.92 6.19	6.55 11.31
ot23	TTL Output Buffer (Note 1)	t_{PLH} t_{PHL}	1.69 1.55	2.23 2.36	2.82 3.38	3.78 5.32
oz61	25Ω Balance CMOS Output (Note 2)	t_{PLH} t_{PHL}	1.77 1.70	2.43 2.37	3.12 3.11	4.28 4.41
oz63	50Ω Balance CMOS Output (Note 2)	t_{PLH} t_{PHL}	1.80 1.70	2.68 2.65	3.77 3.90	5.88 6.38

*This is the estimated capacitive load for 10 standard input load + 2 mm interconnect metal.

Note 1: For TTL loads, the times are measured from 50% point of V_{IN} to V_{OUT} = 1.3V.

Note 2: For CMOS loads, the times are measured from 50% point of V_{IN} to 50% point of V_{OUT}.

Derating Factors

To determine propagation delay under other conditions, use the derating factors summarized in Table I and Table II.

Tpd = Ttyp * Kderating * K process

TABLE I. Derating Factor for Voltage and Temperature

T_{JUNC} / V_{DD}	−40°C	0°C	25°C	85°C	100°C	125°C	150°C
4.5V	0.91	1.02	1.09	1.24	1.27	1.34	1.39
4.75V	0.87	0.97	1.05	1.19	1.21	1.29	1.33
5.0V	0.83	0.93	1.00	1.14	1.16	1.23	1.27
5.25V	0.80	0.90	0.97	1.10	1.12	1.19	1.23
5.5V	0.77	0.87	0.93	1.06	1.08	1.14	1.18

TABLE II. Derating Factor for Process Variation

Process	Best	Typ	Worst
Kprocess	0.66	1.00	1.42

Flexcell Package Availability Chart

Package Type	Leads	Pins	Code	•FLX1021	•FLX1038	•FLX1056	•FLX1080	•FLX1120	•FLX1160	•FLX1200	•FLX1250
Ceramic DIP	SB	28	D1	A	A						
Side Braze	SB	40	D3	A	A						
(D)	SB	48	D5	A	A	A					
Plastic DIP		28	N1	A	A						
(N)		40	N3	A	A						
		48	N5	A	A	A					
Ceramic	NL	44	E2	A	A						
Leadless	NL	68	E4	A	A	A	A	A			
Chip Carrier	NL	84	E5	A	A	A	A	A			
(LCC)											
Ceramic	JB	44	E1	P	P						
Leaded	JB	68	E19		P	P					
Chip Carrier	JB	84	E20		P	P					
(LDCC)											
Plastic Leaded	JB	44	V2	A	A	A					
Chip Carrier	JB	52	V3	A	A	A					
(PLCC)	JB	68	V4	A	A	A	A				
	JB	84	V5	A	A	A	A	A			
CQFP (JEDEC)	GW	132	EL8		P	P	P				
PQFP (JEDEC)	GW	132	VF8	A	A	A	A	A			
Ceramic Quad	GW	80	EA	E	E	E					
Flat Pack	GW	100	EB	E	E	E					
(CQFP) EIAJ	GW	120	EC		P	A	A				
	GW	144	ED		P	A	A				
	GW	160	EE			E	A	A			
	GW	208	EG				E	P	A	P	P
Plastic Quad	GW	80	VF4	A	A	A					
Flat Pack	GW	100	VF7	A	A	A					
(PQFP) EIAJ	GW	120	VF2		A	A	A				
	GW	144	VF6			A	A				
	GW	160	VF3			A	A	P	P	P	P
	GW	208	VL				A	P	A	P	P
Ceramic Pin	10x10	68	U0	A	A	A	A				
Grid Array	11x11	68	U1	A	A	A	A				
(CPGA)	10x10	84	U2	A	A	A	A	A			
	11x11	84	U3	P	A	A	A				
	13x13	124	U6		A	A	P	A	A		
	15x15	144	U11		A	A	A	A			
	15x15	180	U9			P	A	A			
	15x15	224	U12					P	A		
Plastic	13x13	124	NU6		P	A	A	P	A	P	
Pin Grid	15x15	144	NU11				A	A			
Array											
(PPGA)											

SB = Side Braze
NL = No Leads
JB = J Bend

GW = Gull Wing
FP = Flat Pack

A = Approved for booking business
P = Planned for future release, call factory before booking
E = Engineering only

I/O Buffers

Each I/O cell on the perimeter of the array can be configured as input, output, bidirectional, TRI-STATE, or power and ground. The boundary-scan circuit conforming to the IEEE P1149.1 (JTAG) standard can be implemented in the I/O cell.

All input, output and bidirectional IO buffers are protected against latchup and static discharge to a specification of 200 mA and 2000V.

Input Buffers

Input Buffers are available with CMOS-, TTL- (high speed or low power), CMOS-Schmitt-Trigger, TTL-Schmitt-Trigger. All input buffers have optional strong, weak pull-up or strong, weak pull-down resistors.

Output Buffers

Output buffers are available with standard and controlled slew rate, TRI-STATE, and open-drain or open-source configurations, up to 48 mA drives capability in a single I/O location. High speed output driver are capable of driving transmission lines with characteristic impedance as low as 25Ω in one I/O pad. All output buffers are tri-statable for boundary scan testing.

Bidirectional Buffers

Bidirectional buffers are provided by combining any available input buffer with any available TRI-STATE output buffer in a single IO cell by the user during the schematic capture. Hence, a large variety of Bidirectional buffers can be generated in the FLX1000 family.

CORE Flexcells

The core of the FLX1000 Series is composed of columns of n- and p-diffusion separated by the routing channels for the poly interconnection. The macro cell is configured from the poly layer over the two adjacent n- and p-diffusion columns. Since the poly layer is programmable, very dense single-, dual-, and multi-port RAM and ROM can be implemented in any configuration.

Benefits of the Flexcell

Programmable poly layer greatly increases density and flexibility. Gate utilizations of 50% to 70% are achievable. Future products with a third metal layer will achieve even higher utilization. High performance and high density counters, register files, adder, multiplier and memory (single-, dual-, multi-port RAM or ROM) can be generated. Fewer contacts and vias in cells and interconnect increase the reliability.

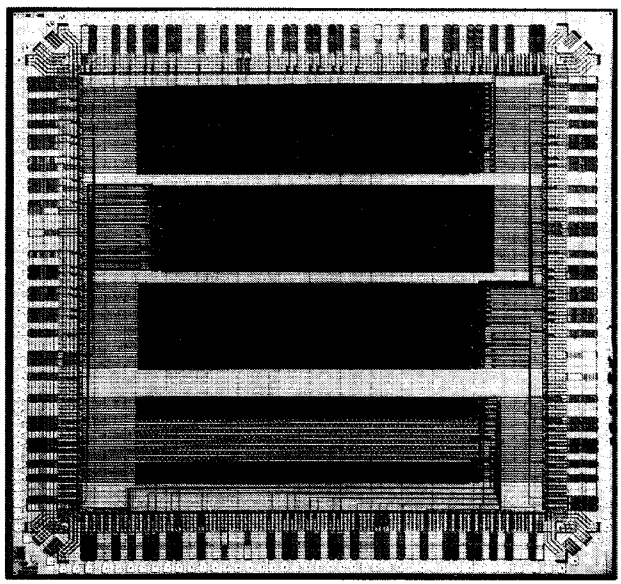

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FIGURE 1. FLX1080 Flexcell Gate Array

Design Automation Support

National Semiconductor's FLX1000 family libraries are planned for the following CAD systems:

- National's DA4 system
- Mentor
- Viewlogic

The open architecture of the National's Design Automation System allows the transfer of the design from the user's workstation to the National's system through the EDIF backplane. National uses the EDIF standard for netlists and symbols when receiving and transmitting data between CAE tools. A rule based framework with modular design packages satisfies the different needs of the designers. Schematic capture, followed by Electrical Rules Checking, Critical Path Analysis, and simulation can be done on the designer's workstation. The Placement and Routing software package gives the designer access to automatic place and route, and allows designer's interactive intervention.

A Hardware description language model (Verilog XL™ HDL model) can be used for functional verification. Then, Synopsis Design Compiler™ can be run to synthesize and optimize the design. This gate-level result can be resimulated to confirm functionality and evaluate circuit timing. The verification in the behavioral language combined with the synthesis tools cuts the design cycle time while increasing the design efficiency.

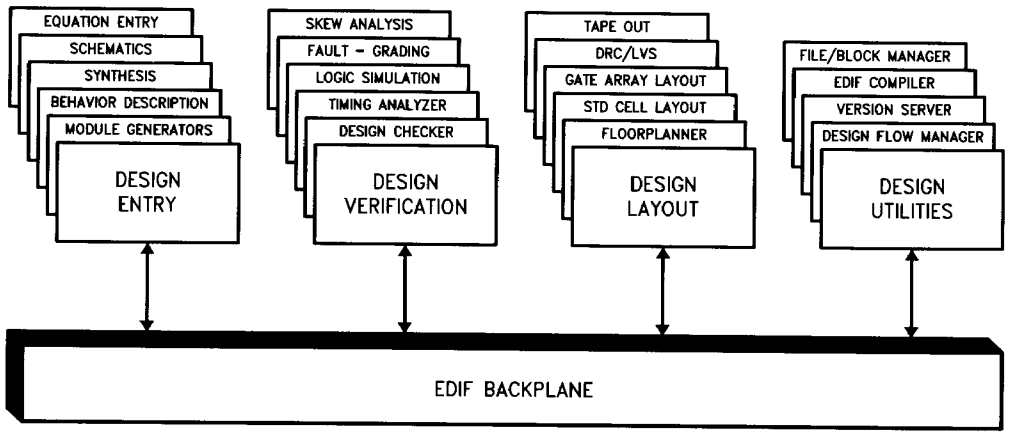

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FIGURE 2. Open Architecture through EDIF

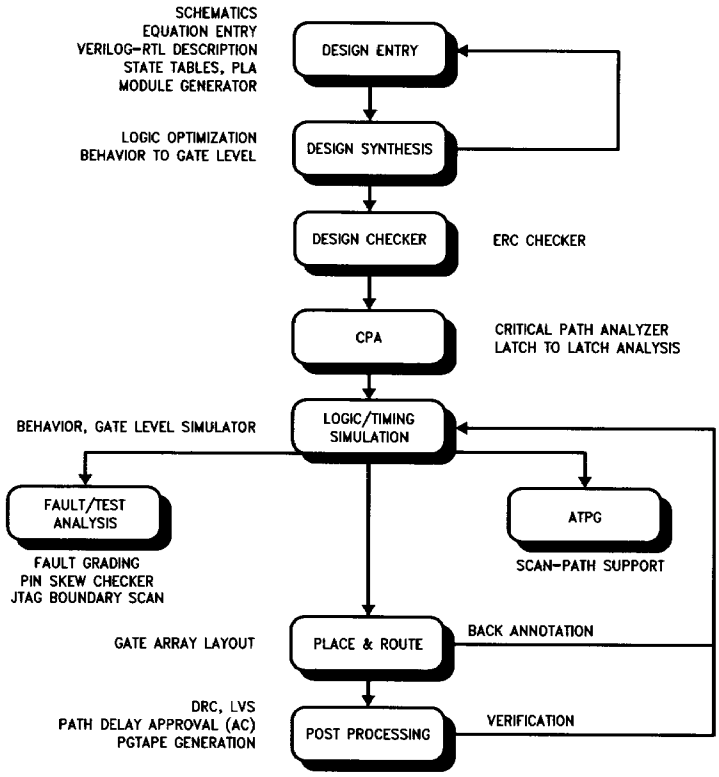

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FIGURE 3. Flexcell/DA4 Design Flow

ASIC Design Centers

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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