

# **PM8610**

## **SBI Bus Serializer (SBS) Telecom Standard Product**

### **Data Sheet**

**Preliminary**

**Issue 3: May, 2001**

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# 1 Features

- The PM8610 SBI336 Bus Serializer (SBS) is a:
  - Scalable Bandwidth Interconnect (SBI) converter and Time Division Multiplexer (TDM) SBI switch.
  - Quad byte-wide 19.44 MHz SBI bus to 777.6 MHz serial SBI336S converter.
  - Byte-wide 77.76 MHz SBI336 bus to 777.6 MHz serial SBI336S converter.
  - DS0, NxDS0, T1, E1, TVT1.5, TVT2, DS3 and E3 granular quad SBI to serial SBI336S switch. Supports subrate link switching with the restriction that subrate links must be symmetric in both the transmit and receive directions.
  - DS0, NxDS0, T1, E1, TVT1.5, TVT2, DS3 and E3 granular SBI336 to serial SBI336S switch. Supports subrate link switching with the restriction that subrate links must be symmetric in both the transmit and receive directions.

Note: The byte-wide 77.76 MHz SBI336 bus interface can be used instead of the serial SBI336S interface. All converter and switch capabilities can be used with the byte-wide SBI interface.

- VT channelized TelecomBus to TelecomBus converter and TDM switch. This requires the telecombus J1 byte to be in a fixed location corresponding to a value of 0 or 522 that is immediately following the C1 octets.
- Quad byte-wide 19.44 MHz TelecomBus to serial 777.6 MHz TelecomBus converter.
- Byte-wide 77.76 MHz TelecomBus to serial 777.6 MHz TelecomBus converter.
- VT1.5, VT2, STS-1 quad 19.44 MHz TelecomBus to serial TelecomBus switch.
- VT1.5, VT2, STS-1 77.76 MHz TelecomBus to serial TelecomBus switch.

Note: The byte-wide 77.76 MHz TelecomBus interface can be used instead of the serial TelecomBus interface. All converter and switch capabilities can be used with the byte-wide TelecomBus interface.

- Can be used with the Narrowband Switch Elements, NSE-20G to implement a DS0 granularity SBI Memory:Space:Memory switch scalable to 20 Gbit/s and the NSE-8G to implement a switch scalable to 8 Gbit/s. In TelecomBus mode, can implement a 20 Gbit/s VT1.5/VT2 granularity Memory:Space:Memory switch.
- Integrates two independent DS0 granularity Memory Switches. One switch is placed between the incoming 77.76 MHz byte wide SBI336 bus (or quad multiplexed 19.44 MHz SBI buses) and the transmit working and protect Serial SBI336S link (or the 77.76 MHz byte wide transmit SBI336 bus). The transmit working and protect links transmit the same data. The other switch is placed between the receive working or protect Serial SBI336S link (or the 77.76 MHz byte wide receive SBI336 bus) and the outgoing 77.76 MHz byte wide SBI336 bus (or quad multiplexed 19.44 MHz SBI buses).
- Provides 125  $\mu$ S nominal latency in DS0 mode. Channel Associated Signaling (CAS) latency through the SBS in DS0 mode is two T1 multiframes (6 mS) or two E1 multiframes (4 mS).
- Provides less than 16  $\mu$ S nominal latency in TelecomBus mode or SBI mode without DS0 level switching.

- Permits any receive or incoming byte from an input port to be mapped to any outgoing or transmit byte, respectively, on the associated output port through the Memory switch.
- Supports redundant working and protect serial SBI336S links in support of a redundant Memory:Space:Memory switch with the NSE.
- Encodes and decodes byte wide SBI and SBI336 bus control signals for all SBI supported link types and clock modes for transport over the serial SBI336S interface.
- Encodes data from the incoming SBI bus or TelecomBus stream to a working and protect 777.6 Mbit/s LVDS serial links with 8B/10B-based encoding.
- Decodes data from a working and protect 777.6 MHz LVDS serial links with 8B/10B-based encoding to the outgoing SBI bus or TelecomBus stream.
- In SBI mode, switches Channel Associated Signaling bits (CAS) with all DS0 data.
- Uses 8B/10B-based line coding protocol on the serial links to provide transition density guarantee and DC balance and to offer a greater control character vocabulary than the standard 8B/10B protocol.
- Provides optional pseudo-random bit sequence (PRBS) generation for each outgoing LVDS serial data link for off-line link verification. PRBS can be inserted with STS-1 granularity.
- Provides PRBS detection for each incoming LVDS serial link for off-line link verification. PRBS is verified with STS-1 granularity.
- Provides pins to coordinate updating of the connection map of the time-slot interchange blocks in the local device, peer SBS devices and companion NSE switch device.
- Can communicate with the NSE switch device over an in-band communications channel in the LVDS links. This channel includes mechanisms for central control and configuration.
- Derives all internal timing from a single 77.76 MHz system clock and a system frame pulse.
- Implemented in 1.8 V/3.3 V 0.18  $\mu$ m CMOS and packaged in a 352 ball 27 mm x 27 mm UBGA package.
- Consumes low power at 1.4 W.

## **2 Applications**

- T1/E1 SONET/SDH Cross-connects
- T1/E1 SONET/SDH Add-Drop Multiplexers
- OC-48 Multiservice Access Multiplexers
- Channelized OC-12/OC-48 Any Service Any Port Switches
- Serial Backplane Board Interconnect
- Shelf to Shelf Cabled Serial Interconnect
- Voice Gateways

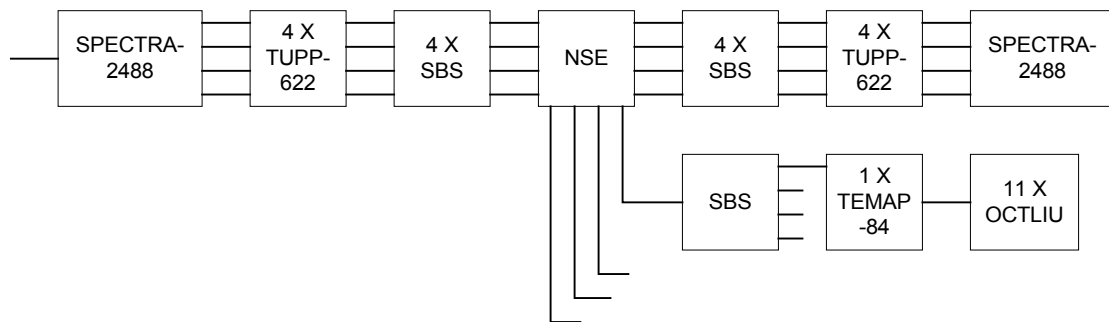
### 3 References

1. IEEE 802.3, "Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications", Section 36.2, 1998.
2. A.X. Widmer and P.A. Franaszek, "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code," IBM Journal of Research and Development, Vol. 27, No 5, September 1983, pp 440-451.
3. U.S. Patent No. 4,486,739, P.A. Franaszek and A.X. Widmer, "Byte Oriented DC Balanced (0,4) 8B/10B Partitioned Block Transmission Code," December 4, 1984.
4. Telcordia - SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 2, Revision 2, January 1999.
5. ITU, Recommendation G.707 - "Digital Transmission Systems – Terminal equipments - General", March 1996.
6. ITU, Rec Recommendation O.151 – "Error Performance Measuring Equipment Operating at the Primary Rate and Above", October 1992.

## 4 Application Examples

Figure 1 and Figure 2 show a PM8610 SBI336 Bus Serializer (SBS) connected to a TelecomBus to implement a T1 or E1 Add/Drop function. When connected to a TelecomBus, the SBS and the PM8620 or PM8621 Narrowband Switching Element (NSE) implements a T1/E1 Memory:Space:Memory switch. The SBS requires all path pointer justifications to be translated into tributary pointer movements so that J1 is fixed to the location following C1 or H3. In both examples, J1 alignment is performed with the TUPP-622. Switching within the SBS and NSE is done using Transparent Virtual Tributary, TVT, mapping across the serial SBI336S LVDS links.

**Figure 1 OC-48 T1/E1 ADM (Individually Drop/Add any T1/E1 in STS-48)**



**Figure 2 OC-48 T1/E1 ADM (Drop/Add up to STS-48 at STS-1 Granularity)**

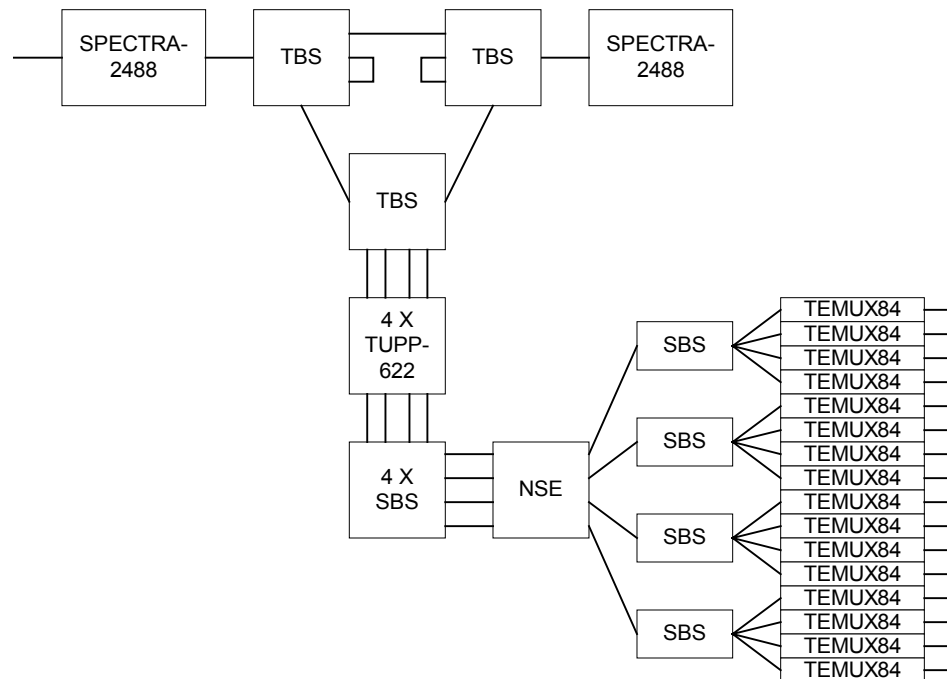
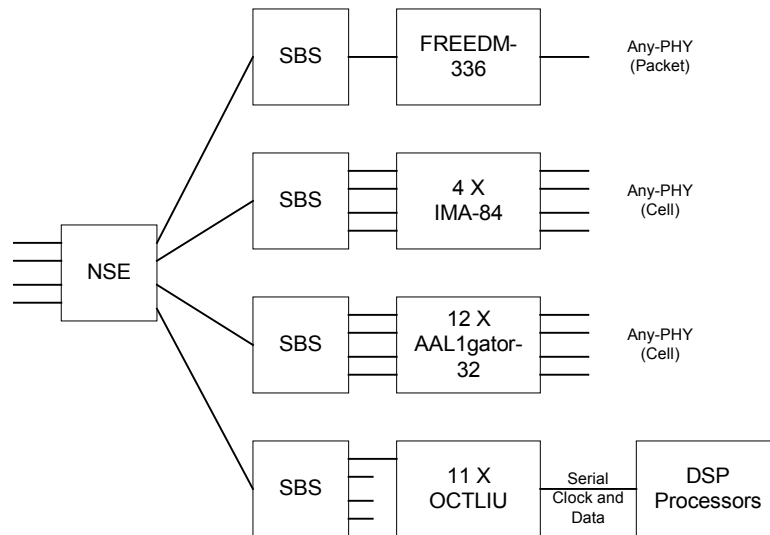
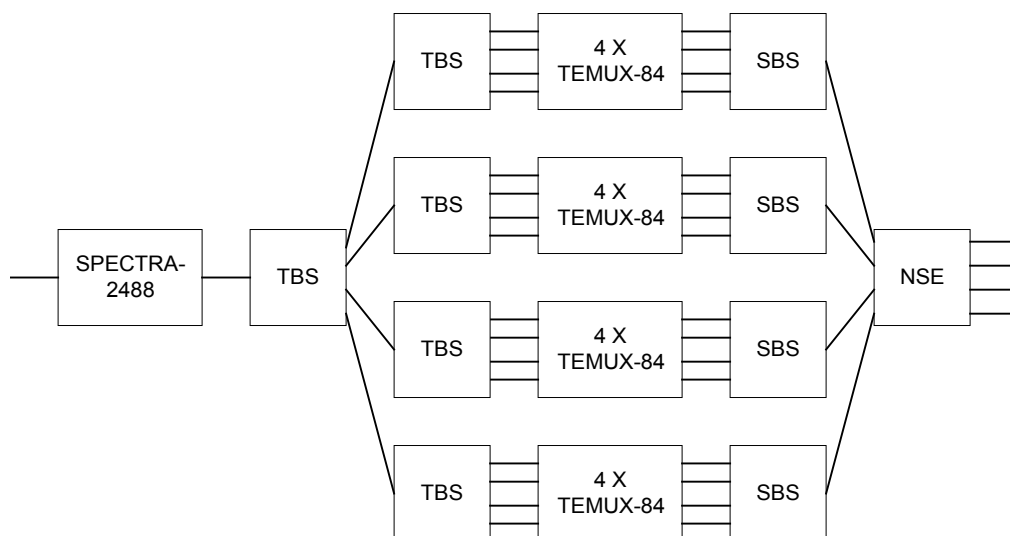


Figure 3 and Figure 4 show examples of the SBS used to implement high density T1/E1 Channelized Physical Interface cards and NxDS0 Multiservice access cards using SBS and NSE devices. DS0, NxDS0, T1, E1, Transparent VTs, E3, DS3 and sub-rate links can be switched between the Physical Layer and Layer 2 devices using SBS and NSE devices.

**Figure 3 Any-Service-Any-Port NxDS0 TDM Access Solution**

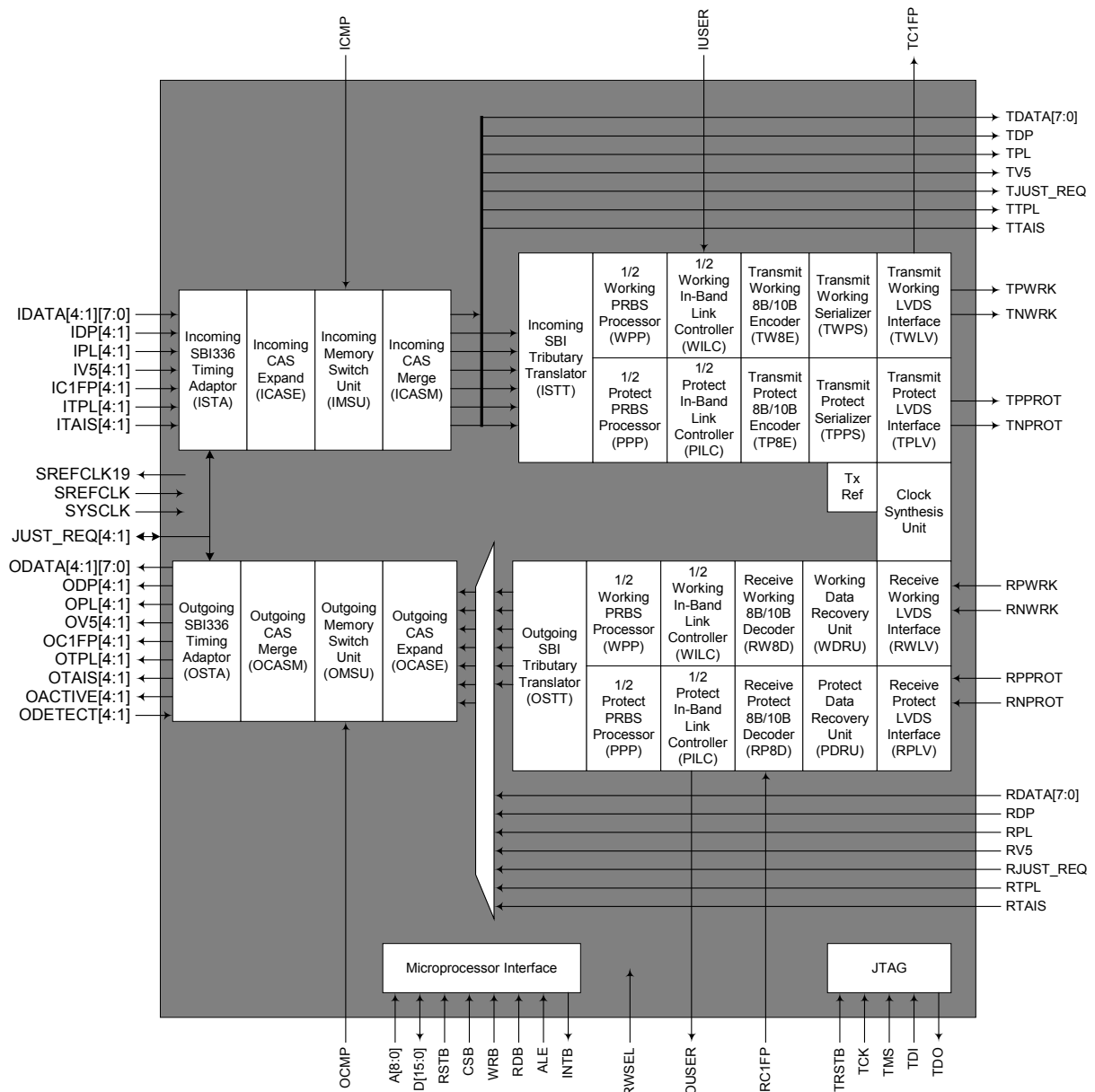


**Figure 4 Any-Service-Any-Port T1/E1 Channelized PHY Card**

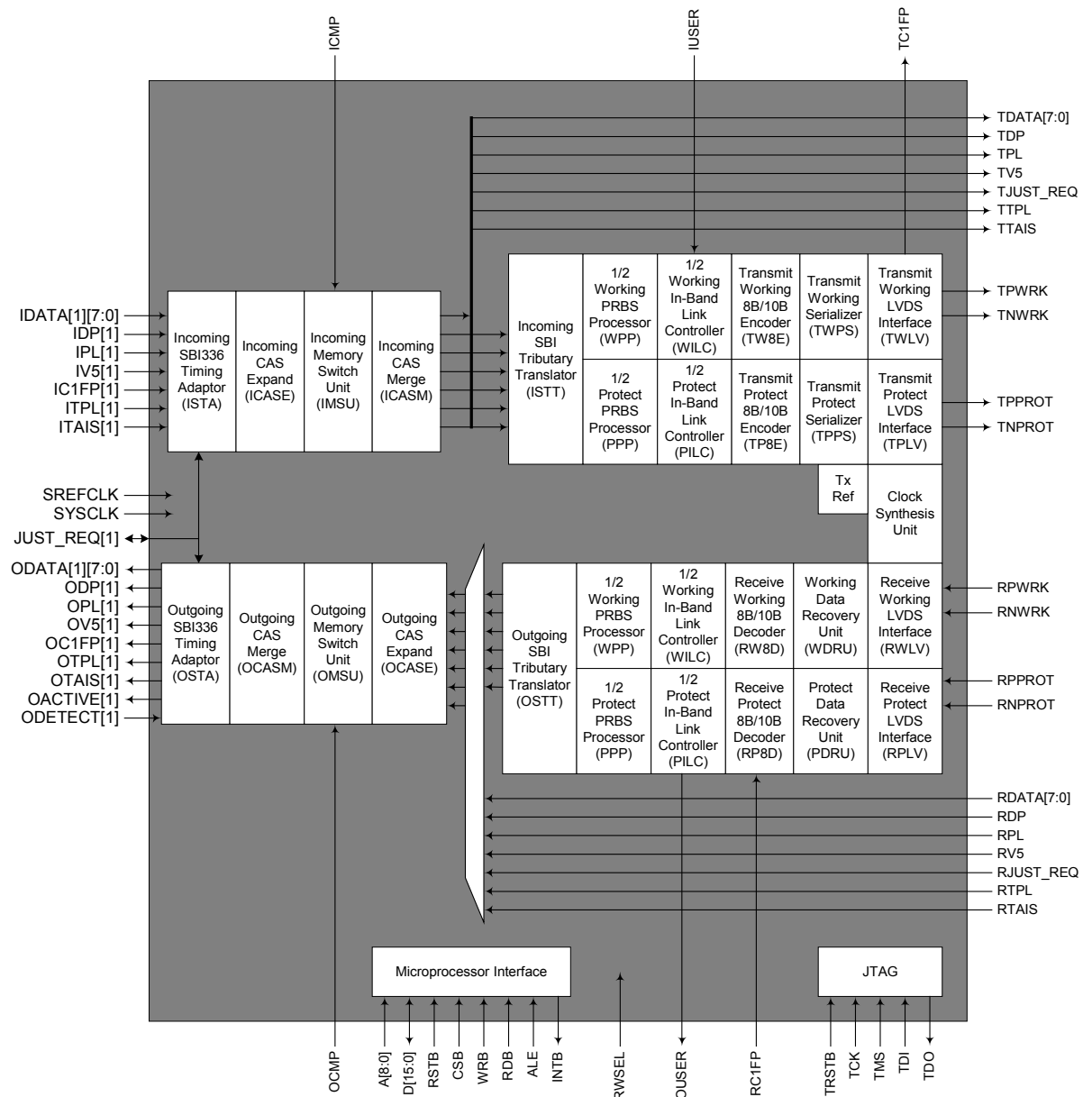


## 5 Block Diagram

Figure 5 Quad 19 MHz SBI Bus/TelecomBus SBS Block Diagram



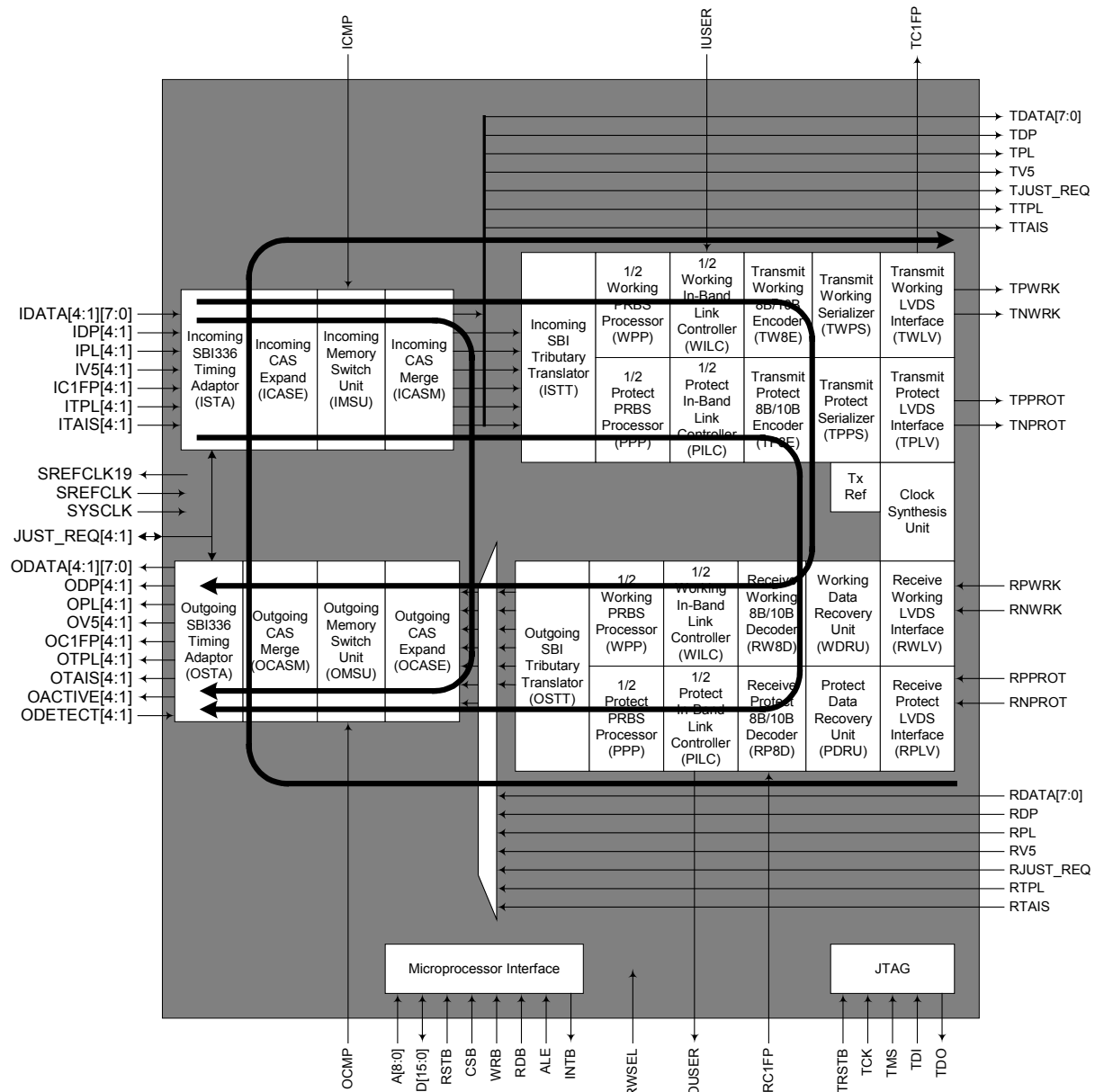
**Figure 6 77 MHz SBI Bus/TelecomBus SBS Block Diagram**





## 6 Loopback Configurations

Figure 7 Loopback Block Diagram



## 7 Description

The PM8610 SBI336 Bus Serializer (SBS) is a monolithic integrated circuit that implements conversion between a byte-serial 19.44 MHz SBI bus or 77.76 MHz SBI336 bus and a redundant 777.6 Mbit/s bit-serial 8B/10B-base SBI336S bus.

In TelecomBus mode, the SBS implements conversion between any 19.44 MHz TelecomBus or 77.76 MHz TelecomBus format and a redundant 777.6 Mbit/s bit-serial 8B/10B-base serial TelecomBus format. In line with the bus conversion is a DS0 granular switch allowing any input DS0 to be output on any output DS0. The redundant 777.6 Mbit/s serial interfaces can be disabled and a byte-wide SBI336 bus can be enabled in its place with all the DS0 level switching capabilities.

The SBS can be used to connect and switch high density T1/E1 framer devices supporting an SBI bus with link layer devices supporting an SBI bus over a serial backplane. Placing a PM8620 or PM8621 Narrowband Switch Element (NSE) between the framer and link layer devices allows up to 20 Gbit/s NxDS0 switches to be constructed.

In the ingress direction, the SBS connects an incoming SBI stream to a pair of redundant serial SBI336S LVDS links through a DS0 memory switch. The incoming SBI bus can be either a single 77.76 MHz SBI bus (SBI336) or four 19.44 MHz SBI buses (SBI). In TelecomBus mode an incoming 77.76 MHz TelecomBus or four 19.44 MHz TelecomBuses that have the J1 path fixed and all high order pointer justifications converted to tributary pointer justifications can be switched through a VT granular switch to a pair of redundant serial LVDS TelecomBus format links. The incoming data is encoded into an extended set of 8B/10B characters and transferred onto two redundant 777.6 Mbit/s serial LVDS links. SBI or TelecomBus frame boundaries, pointer justification events and master timing controls are marked by 8B/10B control characters. Incoming SPEs may be optionally overwritten with the locally generated  $X^{23} + X^{18} + 1$  pseudo-random bit sequence (PRBS) pattern for diagnosis of downstream equipment. The PRBS processor is configurable to handle any combination of SPEs and can be inserted independently into either of the redundant LVDS links. A DS0 memory switch provides arbitrary mapping of streams on the incoming SBI bus stream(s) to the working and protect LVDS links. In TelecomBus mode, a VT1.5/VT2 memory switch provides arbitrary mapping of tributaries on the incoming TelecomBus stream(s) to the working and protect LVDS links. Multi-cast is supported.

In the egress direction, the SBS connects two independent 777.6 Mbit/s serial LVDS links to an outgoing SBI Bus. Each link contains a constituent SBI336S stream. Bytes on the links are carried as 8B/10B characters. The SBS decodes the characters into data and control signals for a single 77.76 MHz SBI336 bus or four 19.44 MHz SBI buses. Alternatively the SBS decodes two independent 777.6 Mbit/s TelecomBus formatted serial LVDS links characters into a single 77.76 MHz or quad 19.44 MHz TelecomBuses. A PRBS processor is provided to monitor the decoded payload for the  $X^{23} + X^{18} + 1$  pattern in each SPE. The PRBS processor is configurable to handle any combination of SPEs in the serial LVDS link. Data on the outgoing SBI bus stream(s) may be sourced from either of the LVDS links.

An In-band signaling link over the serial LVDS links allows this device to be controlled by a companion switching device, a Narrowband Switching Element, PM8620 NSE-20G. This link can be used as communication link between a central processor and the local microprocessor.

Three loopbacks are provided on the SBS. The outgoing-to-incoming loopback allows data entering the SBS on the receive interface to be looped back from the output of the OCASM to the input of the ICASE and then returned to the transmit interface. The transmit 8B/10B-to-receive 8B/10B loopback allows data entering on the incoming bus to be looped back from the output of the TW8E and TP8E to the input of the RW8D and RP8D, respectively. Only the data looped back on the active link (working or protect) will make it back to the outgoing bus. The transmit to receive loopback allows data entering on the incoming bus to be looped back from the output of the ICASM to the input of the OCASE and then returned to the outgoing bus.

## 8 Pin Diagram

The SBS is packaged in a 352-pin UBGA package having a body size of 27 mm by 27 mm and a ball pitch of 1 mm.

**Figure 8 Pin Diagram**

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
A	VSS	VSS	TC1FP	NC	NC	TDATA[7][1]	ODATA[1][1]	ITPL	ITAIS	ODATA[1][3]	ODATA[1][5]	ODATA[1][7]	VSS	VSS	OPL[1]	RJUST_REQ	RDATA[2]	NC	RDP	RTAIS	NC	DVDDI	JUST_REQ[2]	NC	VSS	VSS	A	
B	VSS	DVDDO	VSS	TDATA[0]	TDATA[2]	TDATA[4]	ODP[1]	ODATA[1][2]	NC	ODETECT[1]	NC	NC	OTAIS[1]	OTPL[1]	NC	RDATA[1]	RDATA[4]	RDATA[7]	RTPL	OTAIS[2]	OCMP	OACTIVE[2]	SREFCLK19	VSS	DVDDO	VSS	B	
C	VSS	VSS	DVDDO	NC	NC	NC	TDATA[5]	ODATA[1][0]	ITDP	TV5	DVDDI	ODATA[1][6]	NC	OV5[1]	OC1FP[1]	RDATA[3]	RDATA[6]	RV5	OTPL[2]	ICMP	ODETECT[2]	SREFCLK	NC	DVDDO	VSS	ODATA[1][9]	C	
D	VSS	VSS	AVDH	DVDDO	TJUST_REQ	TDATA[1]	TDATA[3]	TDATA[6]	DVDDO	ITPL	OACTIVE[1]	ODATA[1][4]	NC	DVDDO	RDATA[0]	RDATA[5]	RPL	NC	DVDDO	NC	SYSCLK	NC	DVDDO	NC	ODATA[1][10]	NC	D	
E	VSS	NC	AVDH	NC	<b>352 UBGA BOTTOM VIEW</b>																		NC	ODATA[1][11]	ODATA[1][14]	ODATA[1][17]	ODATA[1][19]	E
F	RESK	RES	NC	NC																			ODATA[1][3]	ODATA[1][5]	NC	ITPL[1]	F	
G	VSS	NC	NC	NC																			ODATA[1][6]	ODP[1]	OV5[1]	PL[1]	G	
H	TNPROT	TNPROT	NC	NC																			DVDDO	IC1FP[1]	ITAIS[1]	ODATA[2][0]	H	
J	VSS	NC	NC	AVDH																			NC	DVDDI	ODATA[2][1]	ODATA[2][3]	J	
K	TPWRK	TNWRK	NC	NC																			NC	ODATA[2][2]	ODATA[2][5]	ODATA[2][7]	K	
L	VSS	NC	NC	NC																			ODATA[2][4]	ODATA[2][6]	ODP[2]	OV5[2]	L	
M	RPWRK	RNWRK	ATB0	ATB1																			OPL[2]	OC1FP[2]	ITDO	NC	M	
N	RPPROT	RNPROT	NC	AVDL																			DVDDO	NTB	NC	VSS	N	
P	AVDL	AVDL	NC	CSU_AVDH																			TRSTB	TMS	TCK	VSS	P	
R	ITPL[4]	ITAIS[4]	AVDL	IV5[4]	ODATA[3][2]	ODATA[3][0]	ODETECT[3]	TDI	R																			
T	VSS	PL[4]	IC1FP[4]	AVDH	ODATA[3][7]	ODATA[3][5]	ODATA[3][3]	ODATA[3][1]	T																			
U	ODATA[4][6]	ODATA[4][7]	DVDDI	ODP[4]	NC	ODP[3]	ODATA[3][6]	ODATA[3][4]	U																			
V	VSS	ODATA[4][3]	ODATA[4][4]	ODATA[4][5]	DVDDO	OTPL[3]	OPL[3]	OACTIVE[3]	V																			
W	ITAIS[2]	ODATA[4][0]	ODATA[4][2]	ODATA[4][1]	NC	OC1FP[3]	OV5[3]	NC	W																			
Y	VSS	IC1FP[2]	ITPL[2]	AVDH	ODATA[3][1]	A[0]	JUST_REQ[1]	OTAIS[3]	Y																			
AA	WRB	RDB	DVDDI	ALE	A[2]	A[1]	JUST_REQ[3]	USER2	AA																			
AB	VSS	CSB	AVDH	DVDDO	NC	A[3]	NC	ODATA[3][5]	AB																			
AC	VSS	VSS	AVDH	DVDDO	RSTB	JUST_REQ[4]	OTPL[4]	DVDDO	NC	ODATA[4][6]	ODATA[4][2]	USER2	DVDDO	NC	ODATA[2][4]	ITAIS[3]	DVDDO	D[5]	ODATA[3][4]	A[7]	DVDDO	NC	A[4]	DVDDI	AC			
AD	VSS	VSS	DVDDO	RWSEL	ODETECT[4]	OV5[4]	NC	D[14]	ODATA[4][7]	NC	ODATA[4][0]	D[12]	D[9]	PL[2]	ODATA[2][6]	ODATA[2][1]	D[7]	ITPL[3]	ODP[3]	D[4]	ODATA[3][3]	D[1]	A[6]	DVDDO	VSS	A[5]	AD	
AE	VSS	DVDDO	VSS	OACTIVE[4]	OTAIS[4]	ODP[4]	D[15]	NC	ODATA[4][4]	ODATA[4][1]	NC	D[11]	NC	IV5[2]	ODATA[2][7]	ODATA[2][3]	ODATA[2][0]	DVDDI	IC1FP[3]	ODATA[3][7]	ODATA[3][6]	ODATA[3][2]	ODATA[3][0]	VSS	DVDDO	VSS	AE	
AF	VSS	VSS	RC1FP	OC1FP[4]	OPL[4]	NC	DVDDI	ODATA[4][5]	ODATA[4][3]	NC	D[13]	D[10]	VSS	VSS	ODP[2]	ODATA[2][5]	ODATA[2][2]	NC	IV5[3]	PL[3]	D[6]	ODATA[3][5]	D[3]	A[8]	VSS	VSS	AF	
	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		

## 9 Pin Description

Pin Name	Type	Pin No.	Function
<b>Receive Serial Data Interface (5 Signals)</b>			
RPWRK RNWRK	Analog LVDS Input	M26 M25	<p><b>Receive Working Serial Data.</b> In SBI336 mode, the differential receive working serial data link (RPWRK/RNWRK) carries the receive 77.76 MHz SBI336 data from an upstream working source, in bit serial format, SBI336S.</p> <p>In TelecomBus mode, RPWRK/RNWRK carries the receive 77.76 MHz TelecomBus from an upstream working source, in bit serial format.</p> <p>Data on RPWRK/RNWRK is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is expected first and the bit 'j' is expected last.</p> <p>RPWRK/RNWRK are nominally 777.6 Mbit/s data streams.</p>
RPPROT RNPROT	Analog LVDS Input	N26 N25	<p><b>Receive Protect Serial Data.</b> In SBI336 mode, the differential receive protect serial data link (RPPROT/RNPROT) carries the receive 77.76 MHz SBI336 data from an upstream protect source, in bit serial format, SBI336S.</p> <p>In TelecomBus mode, RPPROT/RNPROT carries the receive 77.76 MHz TelecomBus from an upstream protection source, in bit serial format.</p> <p>Data on RPPROT/RNPROT is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is expected first and the bit 'j' is expected last.</p> <p>RPPROT/RNPROT are nominally 777.6 Mbit/s data streams.</p>

Pin Name	Type	Pin No.	Function
RC1FP	Input	AF24	<p><b>Receive Serial Frame Pulse.</b> The receive serial SBI336S frame pulse signal (RC1FP) provides system timing of the receive serial interface. When using the receive parallel interface, this signal indicates the first C1 byte on the bus.</p> <p><u>Using the Receive Serial Interface:</u></p> <p>When using the receive serial interface, RC1FP is set high once every multiframe (4 frames for SBI without CAS, 48 frames for SBI with CAS, and 4 frames for TelecomBus), or multiple thereof. The RC1FP_DLY[13:0] bits (register 007H) are used to align the C1 frame boundary 8B/10B character on the receive serial interface (RPWRK/RNWRK and RPPROT/RNPROT) with RC1FP.</p> <p><u>Using the Receive Parallel Interface:</u></p> <p>In SBI mode, this signal also indicates multiframe alignment which occurs every 4 frames, therefore this signal is pulsed every fourth C1 octet to produce a 2KHz multiframe signal. The frame pulse does not need to be repeated every 2KHz as the SBS will flywheel in its absence.</p> <p>When using the SBI bus in synchronous mode the RC1FP signal can be used to indicate T1 and E1 multiframe alignment by pulsing on 48 SBI frame boundaries. This must be done if CAS is to be switched along with the data.</p> <p>In TelecomBus mode, this signal may also be pulsed to indicate the J1 byte position and the byte following J1. The J1 byte position must be locked to an offset of either 0 or 522. The byte following J1 is used to indicate multiframe alignment and should only pulse once every 4 frames marking the frame with the V1s.</p> <p>RC1FP is sampled on the rising edge of SYSCLK.</p>
<b>Receive SBI336 Interface (14 Signals)</b>			
RDATA[7] RDATA[6] RDATA[5] RDATA[4] RDATA[3] RDATA[2] RDATA[1] RDATA[0]	Input	B9 C10 D11 B10 C11 A10 B11 D12	<p><b>Receive Data (RDATA[7:0]).</b> This is the receive SBI336 data bus when configured for SBI336 byte-wide interface instead of the Serial SBI336S interface. When in TelecomBus mode this is the data bus for 77.76 MHz TelecomBus. The receive data bus is a time division multiplexed bus which transports tributaries by assigning them to fixed octets within the SBI or TelecomBus structure.</p> <p>In SBI336 mode, multiple devices can drive this bus at uniquely assigned tributary columns within the SBI336 bus structure.</p> <p>RDATA[7:0] is sampled on the rising edge of SYSCLK.</p> <p>RDATA[7:0] have integral pull-up resistors.</p>
RDP	Input	A8	<p><b>Receive Data Parity (RDP).</b> This is the receive data bus parity when configured for the Receive byte-wide interface. This signal carries the even or odd parity for the receive bus signals. In SBI336 mode, the parity calculation encompasses the RDATA[7:0], RPL and RV5 signals. In TelecomBus mode, the parity calculation encompasses the RDATA[7:0] and optionally the RC1FP and RPL signals.</p> <p>Multiple devices can drive this signal at uniquely assigned tributary columns within the fixed structure. This parity signal is intended to detect multiple sources in the column assignment.</p> <p>RDP is sampled on the rising edge of SYSCLK.</p> <p>RDP has an integral pull-up resistor.</p>

Pin Name	Type	Pin No.	Function
RPL	Input	D10	<p><b>Receive Payload (RPL).</b> This receive SBI336 data bus payload signal indicates valid tributary payload data when configured for the receive SBI336 byte-wide interface. In TelecomBus mode this signal indicates valid path payload.</p> <p><u>In SBI336 mode:</u></p> <p>This active high signal indicates valid data within the SBI336 structure. This signal is high during all octets making up a tributary which includes all octets shaded grey in the framing format tables. This signal goes high during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI336 bus structure. This signal goes low during the octet following the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI336 bus structure. For fractional rate links this signal indicates that the current octet is carrying valid data when high.</p> <p>Multiple SBI336 devices can drive this signal at uniquely assigned tributary columns within the SBI336 bus structure.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal distinguishes between transport overhead bytes and synchronous payload bytes. RPL is set high to mark each payload byte on RDATA[7:0] and is set low to mark each transport overhead byte on RDATA[7:0].</p> <p>RPL is sampled on the rising edge of SYSCLK.</p> <p>RPL has an integral pull-up resistor.</p>
RV5	Input	C9	<p><b>Receive Payload Indicator (RV5).</b> This is the receive payload indicator that locates the floating payload on the SBI336 or TelecomBus when configured for the receive byte-wide interface.</p> <p><u>In SBI336 mode:</u></p> <p>This active high signal locates the position of the floating payloads for each tributary within the SBI336 structure. Timing differences between the port timing and the SBI336 bus timing are indicated by adjustments of this payload indicator relative to the fixed SBI336 structure. All movements indicated by this signal must be accompanied by appropriate adjustments in the RPL signal.</p> <p>Multiple devices can drive this signal at uniquely assigned tributary columns within the SBI336 structure.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal identifies tributary payload frame boundaries on the receive parallel data bus. RV5 is set high to mark the V5 bytes on the bus.</p> <p>RV5 is sampled on the rising edge of SYSCLK.</p> <p>RV5 has an integral pull-up resistor.</p>

Pin Name	Type	Pin No.	Function
RTPL	Input	B8	<p><b>Receive Tributary Payload (RTPL).</b> This signal indicates valid tributary payload data when configured for the receive byte-wide TelecomBus interface.</p> <p>RTPL is set high during valid VC11 and VC12 bytes. RTPL is set low for all transport overhead bytes, high order path overhead bytes, fixed stuff column bytes and tributary transport overhead bytes (V1,V2,V3,V4).</p> <p>RTPL is ignored when configured for SBI336 mode.</p> <p>RTPL is sampled on the rising edge of SYSCLK.</p> <p>RTPL has an integral pull-up resistor.</p>
RTAIS	Input	A7	<p><b>Receive Tributary AIS Indicator (RTAIS).</b> This signal indicates tributaries in low order path AIS state when configured for the receive byte-wide TelecomBus interface.</p> <p>RTAIS is set high when the tributary on the receive bus is in AIS state and is set low when the tributary is out of AIS state.</p> <p>RTAIS is ignored when configured for SBI336 mode.</p> <p>RTAIS is sampled on the rising edge of SYSCLK.</p> <p>RTAIS has an integral pull-up resistor.</p>
RJUST_REQ	Input	A11	<p><b>Receive Justification Request (RJUST_REQ).</b> This is the receive side justification request when configured for SBI336 byte-wide interface instead of the Serial SBI336S interface and when connecting to a PHY device. This signal is not used when connecting to a SBI336 link layer device nor when in TelecomBus mode.</p> <p>The SBI336 Bus Justification Request signal, RJUST_REQ, is used to speed up, slow down or maintain the minimal rate of a slave timed SBI device.</p> <p>This active high signal indicates negative timing adjustments on the SBI336 bus when asserted high during the V3 or H3 octet, depending on the tributary type. In response to this the slave timed SBI336 device should send an extra byte in the V3 or H3 octet of the next frame along with a valid payload signal indicating a negative justification.</p> <p>This signal indicates positive timing adjustments on the SBI336 bus when asserted high during the octet following the V3 or H3 octet, depending on the tributary type. The slave timed SBI336 device should respond to this by not sending an octet during the V3 or H3 octet of the next frame along with a valid payload signal indicating a positive justification.</p> <p>For fractional rate links this signal is asserted high during any available information byte to indicate to the slave timed SBI336 device that the timing master device is able to accept another byte of data. For every byte that this signal is asserted high the slave device is expected to send a valid byte of data.</p>
RJUST_REQ (continued)			<p>All timing adjustments from the slave timed device in response to the justification request must still set the payload and payload indicators appropriately for timing adjustments.</p> <p>RJUST_REQ is sampled on the rising edge of SYSCLK.</p> <p>RJUST_REQ has an integral pull-up resistor.</p>



Pin Name	Type	Pin No.	Function
<b>Outgoing SBI Bus (68 Signals)</b>			
OC1FP[4] OC1FP[3] OC1FP[2] OC1FP[1]	Output	AF23 W3 M3 C12	<p><b>Outgoing C1 Frame Pulse (OC1FP[4:1]).</b> This signal indicates the first C1 octet on the outgoing SBI or TelecomBus.</p> <p><u>In SBI/SBI336 mode:</u></p> <p>This signal also indicates multiframe alignment which occurs every 4 frames, therefore this signal is pulsed every fourth C1 octet to produce a 2KHz multiframe signal.</p> <p>When using the SBI bus in synchronous mode the OC1FP signal indicates T1 and E1 signaling multiframe alignment by pulsing on 48 SBI frame boundaries. This must be done if CAS is to be switched along with the data.</p> <p>For both 19.44 MHz SBI and 77.76 MHz SBI336 buses, only OC1FP[1] will indicate the C1 byte position and OC1FP[4:2] are held low.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal may also be pulsed to indicate the J1 byte position and the byte following J1. The J1 byte position is locked to an offset of either 0 or 522. The byte following J1 is used to indicate multiframe alignment and is only pulsed once every 4 frames marking the frame with the V1s.</p> <p>For a 77.76 MHz TelecomBus, only OC1FP[1] is used and OC1FP[4:2] are held low. For a 19.44 MHz TelecomBus, OC1FP[4:1] are all generated with the same C1 frame alignment. OC1FP[4:1] is updated on the rising edge of SREFCLK.</p>

Pin Name	Type	Pin No.	Function		
ODATA[4][7] ODATA[4][6] ODATA[4][5] ODATA[4][4] ODATA[4][3] ODATA[4][2] ODATA[4][1] ODATA[4][0]	Tristate Output	AD18 AC17 AF19 AE18 AF18 AC16 AE17 AD16	<p><b>Outgoing Data (ODATA[4:1][7:0]).</b> The Outgoing Data buses, ODATA[4:1][7:0], are separate time division multiplexed buses which transport tributaries by assigning them to fixed octets within the SBI or TelecomBus structure.</p> <p>In 19.44 MHz SBI mode, The SBS can drive this bus at uniquely assigned tributary columns within the SBI bus structure.</p> <p>ODATA[1][7:0] can be either a 19.44 MHz SBI or TelecomBus when combined with ODATA[4:2][7:0] or can be used as a standalone 77.76 MHz SBI336 or TelecomBus.</p> <p>ODATA[4:2][7:0] are held tri-state when configured for 77.76 MHz operation.</p> <p>ODATA[4:1][7:0] are updated on the rising edge of SREFCLK.</p>		
ODATA[3][7] ODATA[3][6] ODATA[3][5] ODATA[3][4] ODATA[3][3] ODATA[3][2] ODATA[3][1] ODATA[3][0]		T4 U2 T3 U1 T2 R4 T1 R3			
ODATA[2][7] ODATA[2][6] ODATA[2][5] ODATA[2][4] ODATA[2][3] ODATA[2][2] ODATA[2][1] ODATA[2][0]		K1 L3 K2 L4 J1 K3 J2 H1			
ODATA[1][7] ODATA[1][6] ODATA[1][5] ODATA[1][4] ODATA[1][3] ODATA[1][2] ODATA[1][1] ODATA[1][0]		A15 C15 A16 D15 A17 B19 A20 C19			
ODP[4] ODP[3] ODP[2] ODP[1]		Tristate Output		AE21 U3 L2 B20	<p><b>Outgoing Bus Data Parity (ODP[4:1]).</b> The outgoing data parity signals carry the even or odd parity for the corresponding outgoing buses. In SBI/SBI336 modes, the parity calculation for ODP[x] encompasses the ODATA[x][7:0], OPL[x] and OV5[x] signals. In TelecomBus mode, the parity calculation encompasses the ODATA[x][7:0] and optionally the OC1FP[x] and OPL[x] signals.</p> <p>In 19.44 MHz SBI mode, The SBS can drive this bus at uniquely assigned tributary columns within the SBI bus structure. This parity signal is intended to detect conflicts in the tributary assignment.</p> <p>ODP[1] can be part of either a 19.44 MHz SBI or TelecomBus when combined with ODP[4:2] or can be used as part of a standalone 77.76 MHz SBI336 or TelecomBus.</p> <p>ODP[4:2] are held tri-state when configured for 77.76 MHz operation.</p> <p>ODP is updated on the rising edge of SREFCLK.</p>

Pin Name	Type	Pin No.	Function
OPL[4] OPL[3] OPL[2] OPL[1]	Tristate Output	AF22 V2 M4 A12	<p><b>Outgoing Bus Payload (OPL[4:1]).</b> The outgoing payload signal, OPL[x], indicates valid tributary data within each of the corresponding SBI buses. In TelecomBus mode, this signal indicates valid path payload.</p> <p><u>In SBI/SBI336 mode:</u></p> <p>This active high signal is asserted during all octets making up a tributary which includes all octets shaded grey in the framing format tables. This signal goes high during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI bus structure. This signal goes low during the octet after the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI bus structure. For fractional rate links this signal indicates that the current octet is carrying valid data when high.</p> <p>In 19.44 MHz SBI mode, the SBS can drive this signal at uniquely assigned tributary columns within the SBI bus structure.</p> <p>In locked TVT mode, this signal must be driven in the same manner as for floating TVTs.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal distinguishes between transport overhead bytes and synchronous payload bytes. OPL[x] is set high to mark each payload byte on ODATA[x][7:0] and is set low to mark each transport overhead byte.</p>
OPL[4] OPL[3] OPL[2] OPL[1] (continued)			<p>OPL[1] can be part of either a 19.44 MHz SBI or TelecomBus when combined with OPL[4:2] or can be used as part of a standalone 77.76 MHz SBI336 or TelecomBus.</p> <p>OPL[4:2] are held tri-state when configured for 77.76 MHz operation.</p> <p>OPL[x] is updated on the rising edge of SREFCLK.</p>

Pin Name	Type	Pin No.	Function
OV5[4] OV5[3] OV5[2] OV5[1]	Tristate Output	AD21 W2 L1 C13	<p><b>Outgoing Bus Payload Indicator (OV5[4:1]).</b> The active high signal, OV5[x], locates the position of the floating payload for each tributary within each of the corresponding outgoing SBI/SBI336 or TelecomBuses.</p> <p><u>In SBI/SBI336 mode:</u></p> <p>This active high signal locates the position of the floating payloads for each tributary within the SBS/SBI336 structure. Timing differences between the port timing and the bus timing are indicated by adjustments of this payload indicator relative to the fixed bus structure. All movements indicated by this signal must be accompanied by appropriate adjustments in the OPL[x] signal.</p> <p>In 19.44 MHz SBI mode, the SBS can drive this signal at uniquely assigned tributary columns within the SBI bus structure.</p> <p>In locked TVT mode or fractional rate link mode this signal may be driven but must be ignored by the receiving device.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal identifies tributary payload frame boundaries on the corresponding outgoing data bus. OV5[x] is set high to mark the V5 bytes on the bus.</p> <p>OV5[1] can be part of either a 19.44 MHz SBI or TelecomBus when combined with OV5[4:2] or can be used as part of a standalone 77.76 MHz SBI336 or TelecomBus.</p> <p>OV5[4:2] are held tri-state when configured for 77.76 MHz operation.</p> <p>OV5[x] is updated on the rising edge of SREFCLK.</p>
JUST_REQ[4] JUST_REQ[3] JUST_REQ[2] JUST_REQ[1]	Bidir	AC21 AA2 A4 Y2	<p><b>Shared Bus Justification Request (JUST_REQ[4:1]).</b> The SBI Bus Justification Request signal, JUST_REQ[x], is used to speed up, slow down or maintain the minimal rate of a slave timed SBI device.</p> <p>When the SBS is configured to be connected to a physical layer device, JUST_REQ[4:1] is an input. In SBI mode, JUST_REQ[4:1] is aligned to OC1FP[1] and the Outgoing bus. In SBI336 mode, JUST_REQ[1] is aligned to the IC1FP[1] and Incoming Bus.</p> <p>When the SBS is configured to be connected to a link layer device, JUST_REQ[4:1] is an output. In SBI mode, JUST_REQ[4:1] is aligned to IC1FP[1] and the Incoming bus. In SBI336 mode, JUST_REQ[1] is aligned to OC1FP[1] and the Outgoing bus.</p> <p>This active high signal, JUST_REQ[x], indicates negative timing adjustments on the corresponding SBI bus when asserted high during the V3 or H3 octet, depending on the tributary type. In response to this the slave timed SBI device should send an extra byte in the V3 or H3 octet of the next frame along with a valid payload signal indicating a negative justification.</p> <p>This signal indicates positive timing adjustments on the corresponding SBI bus when asserted high during the octet following the V3 or H3 octet, depending on the tributary type. The slave timed SBI device should respond to this by not sending an octet during the V3 or H3 octet of the next frame along with a valid payload signal indicating a positive justification.</p>

Pin Name	Type	Pin No.	Function
JUST_REQ[4] JUST_REQ[3] JUST_REQ[2] JUST_REQ[1] (continued)			<p>For fractional rate links this signal is asserted high during any available information byte to indicate to the slave timed SBI device that the timing master device is able to accept another byte of data. For every byte that this signal is asserted high the slave device is expected to send a valid byte of data.</p> <p>All timing adjustments from the slave timed device in response to the justification request must still set the payload and payload indicators appropriately for timing adjustments.</p> <p>JUST_REQ[1] can be part of either a 19.44 MHz SBI bus when combined with JUST_REQ[4:2] or can be used as part of a standalone 77.76 MHz SBI336 bus.</p> <p>JUST_REQ[4:1] is configured as an input in TelecomBus mode and is ignored.</p> <p>JUST_REQ[4:1] is asserted and sampled on the rising edge of SREFCLK.</p>
OACTIVE[4] OACTIVE[3] OACTIVE[2] OACTIVE[1]	Output	AE23 V1 B5 D16	<p><b>Outgoing Bus Active Indicator (OACTIVE[4:1]).</b> The active high Outgoing SBI Bus Active Indicator signal, OACTIVE[x], is asserted high during all octets when driving data and control signals, ODATA[x][7:0], ODP[x], OPL[x] and OV5[x], onto the bus.</p> <p>All other SBI devices driving the bus listen to this signal to detect multiple sources driving the bus which can occur due to configuration problems.</p> <p>OACTIVE[4:1] is only valid when the SBS is configured for a 19.44 MHz SBI bus. In all other modes, OACTIVE[4:1] is held low.</p> <p>OACTIVE[x] is updated on the rising edge of SREFCLK.</p>
ODETECT[4] ODETECT[3] ODETECT[2] ODETECT[1]	Input	AD22 R2 C6 B17	<p><b>Outgoing Bus Active Detector (ODETECT[4:1]).</b> This input listens to the OR of all other SBI device ACTIVE signals.</p> <p>When another device is driving OACTIVE[x] high and this device detects ODETECT[x] is high from that other device it signals a collision and tristates the bus to minimize or eliminate contention. Tristating is only done with the 19.44 MHz SBI buses.</p> <p>The AND of OACTIVE[x] and ODETECT[x] is sampled on the rising edge of SREFCLK to indicate that a collision occurred and can be used to indicate contention to management procedures.</p> <p>ODETECT[4:1] is only valid when the SBS is configured for a 19.44 MHz SBI bus. In all other modes, ODETECT[4:1] is ignored.</p> <p>ODETECT[4:1] have integral pull-up resistors.</p>
OTPL[4] OTPL[3] OTPL[2] OTPL[1]	Tristate Output	AC20 V3 C8 B13	<p><b>Outgoing Tributary Payload (OTPL[4:1]).</b> This signal is used to indicate tributary payload when configured for TelecomBus and is held low when configured for SBI or SBI336 buses.</p> <p>OTPL[x] is set high during valid VC11 and VC12 bytes of the corresponding Outgoing bus. OTPL[x] is set low for all transport overhead bytes, high order path overhead bytes, fixed stuff column bytes and tributary transport overhead bytes (V1,V2,V3,V4).</p> <p>OTPL[1] can be part of either a 19.44 MHz TelecomBus when combined with OTPL[4:2] or can be used as part of a standalone 77.76 MHz TelecomBus.</p> <p>OTPL[4:2] are held tri-state when configured for 77.76 MHz operation.</p> <p>OTPL[x] is updated on the rising edge of SREFCLK.</p>

Pin Name	Type	Pin No.	Function
OTAIS[4] OTAIS[3] OTAIS[2] OTAIS[1]	Tristate Output	AE22 Y1 B7 B14	<p><b>Outgoing Tributary Alarm Indication Signal (OTAIS[4:1]).</b> This signal indicates tributaries in low order path AIS state for the corresponding Outgoing TelecomBus and is held low when configured for SBI or SBI336 buses.</p> <p>OTAIS[x] is set high when the tributary on the corresponding Outgoing bus is in AIS state and is set low when the tributary is out of AIS state.</p> <p>OTAIS[1] can be part of either a 19.44 MHz TelecomBus when combined with OTAIS[4:2] or can be used as part of a standalone 77.76 MHz TelecomBus.</p> <p>OTAIS[4:2] are held tri-state when configured for 77.76 MHz operation.</p> <p>OTAIS[x] is updated on the rising edge of SREFCLK.</p>
<b>Incoming SBI Bus (56 Signals)</b>			
IC1FP[4] IC1FP[3] IC1FP[2] IC1FP[1]	Input	T24 AE8 Y25 H3	<p><b>Incoming C1 Frame Pulse (IC1FP[4:1]).</b> This signal indicates the first C1 octet on the incoming SBI or TelecomBus.</p> <p><u>In SBI/SBI336 mode:</u></p> <p>This signal also indicates multiframe alignment which occurs every 4 frames, therefore this signal is pulsed every fourth C1 octet to produce a 2KHz multiframe signal. The frame pulse does not need to be repeated every 2KHz as the SBS will flywheel in its absence.</p> <p>When using the SBI bus in synchronous mode the IC1FP signal can be used to indicate T1 and E1 multiframe alignment by pulsing on 48 SBI frame boundaries. This must be done if CAS is to be switched along with the data.</p> <p>For both 19.44 MHz SBI and 77.76 MHz SBI336 buses, only IC1FP[1] is used and IC1FP[4:2] are ignored.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal may also be pulsed to indicate the J1 byte position and the byte following J1. The J1 byte position must be locked to an offset of either 0 or 522. The byte following J1 is used to indicate multiframe alignment and should only pulse once every 4 frames marking the frame with the V1s.</p>
IC1FP[4] IC1FP[3] IC1FP[2] IC1FP[1] (continued)			<p>IC1FP[1] can be part of either a 19.44 MHz TelecomBus when combined with IC1FP[4:2] or can be used as part of a standalone 77.76 MHz TelecomBus. When using a 19.44 MHz TelecomBus, all 4 C1 positions must be aligned and the four signals, IC1FP[4:1], are logically OR'ed together internally.</p> <p>IC1FP[4:1] is sampled on the rising edge of SREFCLK.</p> <p>IC1FP[4:2] have integral pull-up resistors.</p>

Pin Name	Type	Pin No.	Function
IDATA[4][7] IDATA[4][6] IDATA[4][5] IDATA[4][4] IDATA[4][3] IDATA[4][2] IDATA[4][1] IDATA[4][0]  IDATA[3][7] IDATA[3][6] IDATA[3][5] IDATA[3][4] IDATA[3][3] IDATA[3][2] IDATA[3][1] IDATA[3][0]  IDATA[2][7] IDATA[2][6] IDATA[2][5] IDATA[2][4] IDATA[2][3] IDATA[2][2] IDATA[2][1] IDATA[2][0]  IDATA[1][7] IDATA[1][6] IDATA[1][5] IDATA[1][4] IDATA[1][3] IDATA[1][2] IDATA[1][1] IDATA[1][0]	Input	U25 U26 V23 V24 V25 W24 W23 W25  AE7 AE6 AF5 AC7 AD6 AE5 Y4 AB1  AE12 AD12 AF11 AC12 AE11 AF10 AD11 AE10  E1 G4 F3 E2 F4 E3 D2 C1	<p><b>Incoming Bus Data (IDATA[4:1][7:0]).</b> The Incoming data buses, IDATA[4:1][7:0], are separate time division multiplexed buses which transports tributaries by assigning them to fixed octets within the SBI or TelecomBus structure.</p> <p>Multiple SBI/SBI336 devices can drive this bus at uniquely assigned tributary columns within the SBI/SBI336 bus structure.</p> <p>IDATA[1][7:0] can be either a 19.44 MHz SBI or TelecomBus when combined with IDATA[4:2][7:0] or can be used as a standalone 77.76 MHz SBI336 or TelecomBus.</p> <p>IDATA[4:1][7:0] is sampled on the rising edge of SREFCLK.</p> <p>IDATA[4:2][7:0] have integral pull-up resistors.</p>
IDP[4] IDP[3] IDP[2] IDP[1]	Input	U23 AD8 AF12 G3	<p><b>Incoming Bus Data Parity (IDP[4:1]).</b> The Incoming data parity signals carry the even or odd parity for the corresponding Incoming buses. In SBI/SBI336 modes, the parity calculation encompasses the IDATA[x][7:0], IPL[x] and IV5[x] signals. In TelecomBus mode, the parity calculation encompasses the IDATA[x][7:0] and optionally the IC1FP[x] and IPL[x] signals.</p> <p>Multiple SBI/SBI336 devices can drive this signal at uniquely assigned tributary columns within the SBI/SBI336 bus structure. This parity signal is intended to detect multiple sources in the column assignment.</p> <p>IDP[1] can be part of either a 19.44 MHz SBI or TelecomBus when combined with IDP[4:2] or can be used as part of a standalone 77.76 MHz SBI336 or TelecomBus.</p> <p>IDP[x] is sampled on the rising edge of SREFCLK.</p> <p>IDP[4:2] have integral pull-up resistors.</p>

Pin Name	Type	Pin No.	Function
IPL[4] IPL[3] IPL[2] IPL[1]	Input	T25 AF7 AD13 G1	<p><b>Incoming Bus Payload (IPL[4:1]).</b> The Incoming Payload signal, IPL[4:1], indicates valid tributary data within each of the corresponding SBI buses. In TelecomBus mode, this signal indicates valid path payload.</p> <p><u>In SBI/SBI336 mode:</u></p> <p>This active high signal is asserted during all octets making up a tributary which includes all octets shaded grey in the framing format tables. This signal goes high during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI/SBI336 structure. This signal goes low during the octet following the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI/SBI336 structure. For fractional rate links this signal indicates that the current octet is carrying valid data when high.</p> <p>Multiple SBI/SBI336 devices can drive this signal at uniquely assigned tributary columns within the SBI/SBI336 structure.</p> <p>For locked TVTs, this signal must be driven in the same manner as for floating TVTs.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal distinguishes between transport overhead bytes and the synchronous payload bytes. IPL[x] is set high to mark each payload byte on IDATA[x][7:0] and is set low to mark each transport overhead byte..</p> <p>IPL[1] can be part of either a 19.44 MHz SBI or TelecomBus when combined with IPL[4:2] or can be used as part of a standalone 77.76 MHz SBI336 or TelecomBus.</p> <p>IPL[x] is sampled on the rising edge of SREFCLK.</p> <p>IPL[4:2] have integral pull-up resistors.</p>



Pin Name	Type	Pin No.	Function
IV5[4] IV5[3] IV5[2] IV5[1]	Input	R23 AF8 AE13 G2	<p><b>Incoming Bus Payload Indicator (IV5[4:1]).</b> This signal locates the position of the floating payload for each tributary within each of the incoming SBI/SBI336 or TelecomBuses.</p> <p><u>In SBI/SBI336 mode:</u></p> <p>This active high signal locates the position of the floating payloads for each tributary within the SBI/SBI336 structure. Timing differences between the port timing and the bus timing are indicated by adjustments of this payload indicator relative to the fixed bus structure. All movements indicated by this signal must be accompanied by appropriate adjustments in the IPL[x] signal.</p> <p>Multiple SBI/SBI336 devices can drive this signal at uniquely assigned tributary columns within the SBI/SBI336 structure.</p> <p>For locked TVTs, this signal must either be driven in the same manner as for floating TVTs or held low.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal identifies tributary payload frame boundaries on the corresponding incoming data bus. IV5[x] is set high to mark the V5 bytes on the bus.</p> <p>IV5[1] can be part of either a 19.44 MHz SBI or TelecomBus when combined with IV5[4:2] or can be used as part of a standalone 77.76 MHz SBI336 or TelecomBus.</p> <p>IV5[x] is sampled on the rising edge of SREFCLK.</p> <p>IV5[4:2] have integral pull-up resistors.</p>
ITPL[4] ITPL[3] ITPL[2] ITPL[1]	Input	R26 AD9 Y24 F1	<p><b>Incoming Tributary Payload (ITPL[4:1]).</b> This signal is used to indicate tributary payload when configured for TelecomBus and is unused when configured for SBI or SBI336 buses.</p> <p>ITPL[x] is set high during valid VC11 and VC12 bytes of the corresponding Incoming bus. ITPL[x] is set low for all transport overhead bytes, high order path overhead bytes, fixed stuff column bytes and tributary transport overhead bytes (V1,V2,V3,V4).</p> <p>ITPL[1] can be part of either a 19.44 MHz TelecomBus when combined with ITPL[4:2] or can be used as part of a standalone 77.76 MHz TelecomBus.</p> <p>ITPL[x] is sampled on the rising edge of SREFCLK.</p> <p>ITPL[4:2] have integral pull-up resistors.</p>
ITAIS[4] ITAIS[3] ITAIS[2] ITAIS[1]	Input	R25 AC10 W26 H2	<p><b>Incoming Tributary Alarm Indication Signal (ITAIS[4:1]).</b> This signal indicates tributaries in low order path AIS state for the corresponding Incoming TelecomBus and is unused when configured for SBI or SBI336 buses.</p> <p>ITAIS[x] is set high when the tributary on the corresponding Incoming bus is in AIS state and is set low when the tributary is out of AIS state.</p> <p>ITAIS[1] can be part of either a 19.44 MHz TelecomBus when combined with ITAIS[4:2] or can be used as part of a standalone 77.76 MHz TelecomBus.</p> <p>ITAIS[x] is sampled on the rising edge of SREFCLK.</p> <p>ITAIS[4:2] have integral pull-up resistors.</p>

Pin Name	Type	Pin No.	Function
<b>Transmit Serial Data Interface (4 Signals)</b>			
TPWRK TNWRK	Analog LVDS Output	K26 K25	<p><b>Transmit Working Serial Data.</b> In SBI336 mode, the differential transmit working serial data link (TPWRK/TNWRK) carries a transmit 77.76 MHz SBI336 data stream to a downstream working sink, in bit serial format, SBI336S.</p> <p>In TelecomBus mode, TPWRK/TNWRK carries the transmit 77.76 MHz TelecomBus data stream to a downstream working sink, in bit serial format.</p> <p>Data on TPWRK/TNWRK is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last.</p> <p>TPWRK/TNWRK are nominally 777.6 Mbit/s data streams.</p>
TPPROT TNPROT	Analog LVDS Output	H25 H26	<p><b>Transmit Protect Serial Data.</b> In SBI336 mode, the differential transmit protect serial data link (TPPROT/TNPROT) carries a transmit 77.76 MHz SBI336 data stream to a downstream protect sink, in bit serial format, SBI336S.</p> <p>In TelecomBus mode, TPPROT/TNPROT carries the transmit 77.76 MHz TelecomBus data stream to a downstream protection sink, in bit serial format.</p> <p>Data on TPPROT/TNPROT is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit 'a' is transmitted first and the bit 'j' is transmitted last.</p> <p>TPPROT/TNPROT are nominally 777.6 Mbit/s data streams.</p>
<b>Transmit SBI336 Interface (15 Signals)</b>			
TC1FP	Output	A24	<p><b>Transmit Serial SBI Frame Pulse.</b> The transmit serial SBI frame pulse signal (TC1FP) provides system timing of the transmit serial interface. When using the transmit parallel interface, this signal indicated the first C1 octet on the transmit SBI336 or TelecomBus.</p> <p><u>Using the Transmit Serial Interface:</u></p> <p>TC1FP is set high to indicate that the C1 frame boundary 8B/10B character has been serialized out on the transmit working serial data link (TPWRK/TNWRK) and the transmit protection serial data link (TPPROT/ TNPROT). TC1FP is output every 4 frame for SBI mode without CAS and for TelecomBus mode. TC1FP is output every 48 frames for SBI mode with CAS.</p> <p><u>Using the Transmit Parallel Interface:</u></p> <p>In SBI/SBI336 mode, this signal also indicates multiframe alignment which occurs every 4 frames, therefore this signal is pulsed every fourth C1 octet to produce a 2KHz multiframe signal.</p> <p>When using the SBI bus in synchronous mode the TC1FP signal indicates T1 and E1 signaling multiframe alignment by pulsing on 48 SBI frame boundaries. This must be done if CAS is to be switched along with the data.</p> <p>In TelecomBus mode, this signal may also be pulsed to indicate the J1 byte position and the byte following J1. The J1 byte position is locked to an offset of either 0 or 522. The byte following J1 is used to indicate multiframe alignment and is only pulsed once every 4 frames marking the frame with the V1s.</p> <p>TC1FP is updated on the rising edge of SYSCLK.</p>

Pin Name	Type	Pin No.	Function
TDATA[7] TDATA[6] TDATA[5] TDATA[4] TDATA[3] TDATA[2] TDATA[1] TDATA[0]	Output	A21 D19 C20 B21 D20 B22 D21 B23	<b>Transmit Data (TDATA[7:0]).</b> This is the transmit data bus when configured for the Transmit byte-wide interface. The transmit data bus is a time division multiplexed bus which transports tributaries by assigning them to fixed octets within the 77.76 MHz SBI336 or TelecomBus structure.  TDATA[7:0] is updated on the rising edge of SYSCLK.
TDP	Output	C18	<b>Transmit Data Parity (TDP).</b> This is the transmit data bus parity when configured for the Transmit byte-wide interface. This signal carries the even or odd parity for the transmit bus signals. In SBI336 mode, the parity calculation encompasses the TDATA[7:0], TPL and TV5 signals. In TelecomBus mode, the parity calculation encompasses the TDATA[7:0] and optionally the TC1FP and TPL signals.  TDP is updated on the rising edge of SYSCLK.
TPL	Output	D17	<b>Transmit Payload (TPL).</b> The transmit SBI336 data bus payload signal indicates valid tributary payload data when configured for the transmit SBI336 byte-wide interface. In TelecomBus mode this signal indicates valid path payload.  <u>In SBI336 mode:</u>  This active high signal indicates valid data within the SBI336 structure. This signal is high during all octets making up a tributary which includes all octets shaded grey in the framing format tables. This signal goes high during the V3 or H3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed SBI336 structure. This signal goes low during the octet following the V3 or H3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed SBI336 structure. For fractional rate links this signal indicates that the current octet is carrying valid data when high.  <u>In TelecomBus mode:</u>  This signal distinguishes between transport overhead bytes and synchronous payload bytes. TPL is set high to mark each payload byte on TDATA[7:0] and is set low to mark each transport overhead byte on TDATA[7:0].  TPL is updated on the rising edge of SYSCLK.

Pin Name	Type	Pin No.	Function
TV5	Output	C17	<p><b>Transmit Payload Indicator (TV5).</b> The transmit payload indicator (TV5) locates the floating payload on the SBI336 or TelecomBus when configured for the transmit byte-wide interface.</p> <p><u>In SBI336 mode:</u></p> <p>This active high signal locates the position of the floating payloads for each tributary within the SBI336 structure. Timing differences between the port timing and the SBI336 bus timing are indicated by adjustments of this payload indicator relative to the fixed SBI336 structure. All movements indicated by this signal must be accompanied by appropriate adjustments in the TPL signal.</p> <p><u>In TelecomBus mode:</u></p> <p>This signal identifies tributary payload frame boundaries on the transmit parallel data bus. TV5 is set high to mark the V5 bytes on the bus.</p> <p>TV5 is updated on the rising edge of SYSCLK.</p>
TTPL	Output	A19	<p><b>Transmit Tributary Payload (TTPL).</b> This signal indicates valid tributary payload data when configured for transmit byte-wide TelecomBus interface.</p> <p>TTPL is set high during valid VC11 and VC12 bytes. TTPL is set low for all transport overhead bytes, high order path overhead bytes, fixes stuff column bytes and tributary transport overhead bytes (V1,V2,V3,V4).</p> <p>TTPL is held low in SBI336 mode.</p> <p>TTPL is updated on the rising edge of SYSCLK.</p>
TTAIS	Output	A18	<p><b>Transmit Tributary AIS Indicator (TAIS).</b> This signal indicates tributaries in low order path AIS state when configured for the transmit byte-wide TelecomBus interface.</p> <p>TTAIS is set high when the tributary on the transmit bus is in AIS state and is set low when the tributary is out of AIS state.</p> <p>TTAIS is held low in SBI336 mode</p> <p>TTAIS is updated on the rising edge of SYSCLK.</p>

Pin Name	Type	Pin No.	Function
TJUST_REQ	Output	D22	<p><b>Transmit Justification Request (TJUST_REQ).</b> This is the transmit side justification request when configured for SBI336 byte-wide interface instead of the Serial SBI336S interface and when connecting to a link layer device. This signal is held low when connecting to a SBI336 physical layer device or when in TelecomBus mode.</p> <p>The SBI336 Bus Justification Request signal, TJUST_REQ, is used to speed up, slow down or maintain the minimal rate of a slave timed SBI336 device.</p> <p>This active high signal indicates negative timing adjustments on the SBI336 bus when asserted high during the V3 or H3 octet, depending on the tributary type. In response to this the slave timed SBI336 device should send an extra byte in the V3 or H3 octet of the next receive frame along with a valid payload signal indicating a negative justification.</p> <p>This signal indicates positive timing adjustments on the SBI336 bus when asserted high during the octet following the V3 or H3 octet, depending on the tributary type. The slave timed SBI336 device should respond to this by not sending an octet during the V3 or H3 octet of the next receive frame along with a valid payload signal indicating a positive justification.</p> <p>For fractional rate links this signal is asserted high during any available information byte to indicate to the slave timed SBI336 device that the timing master device is able to accept another byte of data. For every byte that this signal is asserted high the slave device is expected to send a valid byte of data.</p>
TJUST_REQ (continued)			<p>All timing adjustments from the slave timed device in response to the justification request must still set the payload and payload indicators appropriately for timing adjustments.</p> <p>TJUST_REQ is updated on the rising edge of SYSCLK.</p>
<b>Microprocessor Interface (30 Signals)</b>			
CSB	Input	AB25	<p><b>Chip Select Bar.</b> The active low chip select signal (CSB) controls microprocessor access to registers in the SBS device. CSB is set low during SBS Microprocessor Interface Port register accesses. CSB is set high to disable microprocessor accesses.</p> <p>If CSB is not required (i.e. register accesses controlled using RDB and WRB signals only), CSB should be connected to an inverted version of the RSTB input.</p>
RDB	Input	AA25	<p><b>Read Enable Bar.</b> The active low read enable bar signal (RDB) controls microprocessor read accesses to registers in the SBS device. RDB is set low and CSB is also set low during SBS Microprocessor Interface Port register read accesses. The SBS drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.</p>
WRB	Input	AA26	<p><b>Write Enable Bar.</b> The active low write enable bar signal (WRB) controls microprocessor write accesses to registers in the SBS device. WRB is set low and CSB is also set low during SBS Microprocessor Interface Port register write accesses. The contents of D[15:0] are clocked into the addressed register on the rising edge of WRB while CSB is low.</p>

Pin Name	Type	Pin No.	Function
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	AE20 AD19 AF16 AD15 AE15 AF15 AD14 AC11 AD10 AF6 AC8 AD7 AF4 AC6 AD5 AE4	<b>Microprocessor Data Bus.</b> The bi-directional data bus, D[15:0] is used during SBS Microprocessor Interface Port register reads and write accesses. D[15] is the most significant bit of the data words and D[0] is the least significant bit.
A[8]/TRS A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	AF3 AC5 AD4 AD1 AC2 AB3 AA4 AA3 Y3	<b>Microprocessor Address Bus.</b> The microprocessor address bus (A[8:0]) selects specific Microprocessor Interface Port registers during SBS register accesses.  A[8] is also the Test Register Select (TRS) address pin and selects between normal and test mode register accesses. TRS is set high during test mode register accesses, and is set low during normal mode register accesses.
ALE	Input	AA23	<b>Address Latch Enable.</b> The address latch enable signal (ALE) is active high and latches the address bus (A[11:0]) when it is set low. The internal address latches are transparent when ALE is set high. ALE allows the SBS to interface to a multiplexed address/data bus. ALE has an integral pull up resistor.
INTB	Open Drain Output	N3	<b>Interrupt Request Bar.</b> The active low interrupt enable signal (INTB) output goes low when an SBS interrupt source is active and that source is unmasked. INTB returns high when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.
<b>General Function (9 Signals)</b>			
SYSCLK	Input	D6	<b>SBI System Clock.</b> The 77 MHz SBI reference clock signal, SYSCLK, is the master clock for the SBS device. SYSCLK is a 77.76 MHz clock, with a nominal 50% duty cycle. RC1FP, RDATA[7:0], RDP, RPL, RV5, RTPL, RTAIS and RJUST_REQ are sampled on the rising edge of SYSCLK. TC1FP, TDATA[7:0], TDP, TPL, TV5, TTPL, TAIS and TJUST_REQ are updated on the rising edge of SYSCLK.
SREFCLK19	Output	B4	<b>19.44 MHz SBI Reference Clock.</b> The 19.44 MHz SBI reference clock signal, SREFCLK19, is a reference for 19.44 MHz SBI bus and TelecomBus interfaces. SREFCLK19 is a 19.44 MHz clock, with a nominal 50% duty cycle and is generated from the 77.76 MHz SYSCLK.  When the incoming and outgoing buses are running at 19.44 MHz, this signal should be tied to SREFCLK.

Pin Name	Type	Pin No.	Function
SREFCLK	Input	C5	<p><b>SBI Reference Clock.</b> The SBI reference clock, SREFCLK, is a reference for the incoming and outgoing SBI bus and TelecomBus interfaces. SREFCLK is either a 77.76 MHz clock with a nominal 50% duty cycle or a 19.44 MHz clock with a nominal 50% duty cycle. IC1FP, IDATA[4:1][7:0], IDP[4:1], IPL[4:1], IV5[4:1], ITPL[4:1], ITAIS[4:1] and JUST_REQ[4:1] are sampled on the rising edge of SREFCLK. OC1FP, ODATA[4:1][7:0], ODP[4:1], OPL[4:1], OV5[4:1], OTPL[4:1], OTAIS[4:1] and JUST_REQ[4:1] are updated on the rising edge of SYSCLK.</p> <p>When the incoming and outgoing buses are running at 77.76 MHz, this signal should be tied to SYSCLK.</p> <p>When the incoming and outgoing buses are running at 19.44 MHz, this signal should be tied to SREFCLK19.</p>
ICMP	Input	C7	<p><b>Incoming Connection Memory Page.</b> The incoming connection memory page select signal, ICMP, controls the selection of the connection memory page in the Incoming Memory Switch Unit, IMSU. When ICMP is set high, connection memory page 1 is selected. When ICMP is set low, connection memory page 0 is selected.</p> <p>The byte location during which ICMP is sampled is dependant on the mode of operation.</p> <p><u>4-Frame SBI/SBI336 mode:</u></p> <p>ICMP is sampled at the C1 byte position of the incoming bus on the first frame of the 4-frame multiframe (marked by IC1FP[1]). Changes to the connection memory page selection is synchronized to the frame boundary (A1 byte position) of the next four frame multiframe.</p> <p><u>48-Frame SBI/SBI336 mode:</u></p> <p>ICMP is sampled at the C1 byte position of the incoming bus on the first frame of the 48-frame multiframe (marked by IC1FP[1]). Changes to the connection memory page selection is synchronized to the frame boundary (A1 byte position) of the next 48-frame multiframe.</p> <p><u>TelecomBus mode:</u></p> <p>ICMP is sampled at the C1 byte position of every frame on the incoming bus (marked by IC1FP[4:1]). Changes to the connection memory page selection are synchronized to the frame boundary (A1 byte position) of the next frame.</p> <p>ICMP is sampled on the rising edge of SREFCLK.</p>

Pin Name	Type	Pin No.	Function
OCMP	Input	B6	<p><b>Outgoing Connection Memory Page.</b> The outgoing connection memory page select signal, OCMP, controls the selection of the connection memory page in the Outgoing Memory Switch Unit, OMSU. When OCMP is set high, connection memory page 1 is selected. When OCMP is set low, connection memory page 0 is selected.</p> <p>The byte location during which OCMP is sampled is dependant on the mode of operation.</p> <p><u>4-Frame SBI/SBI336 mode:</u> OCMP is sampled at the C1 byte position of the receive bus on the first frame of the 4-frame multiframe (marked by RC1FP). Changes to the connection memory page selection is synchronized to the frame boundary (A1 byte position) of the next four frame multiframe.</p> <p><u>48-Frame SBI/SBI336 mode:</u> OCMP is sampled at the C1 byte position of the receive bus on the first frame of the 48-frame multiframe (marked by RC1FP). Changes to the connection memory page selection is synchronized to the frame boundary (A1 byte position) of the next 48-frame multiframe.</p> <p><u>TelecomBus mode:</u> OCMP is sampled at the C1 byte position of every frame on the receive bus (marked by RC1FP). Changes to the connection memory page selection are synchronized to the frame boundary (A1 byte position) of the next frame. OCMP is sampled on the rising edge of SYSCLK.</p>
RWSEL	Input	AD23	<p><b>Receive Working Serial Data Select.</b> The receive working serial data select signal, RWSEL, selects between sourcing outgoing data, ODATA[4:1][7:0], from the receive working serial data link, RPWRK/RNWRK, or the receive protect serial data link, RPPROT/RNPROT. When RWSEL is set high, the working serial bus is selected. When RWSEL is set low, the protect serial bus is selected. RWSEL is sampled at the C1 byte location as defined by the receive serial interface frame pulse signal, RC1FP. Changes to the selection of the working and protect serial streams are synchronized to the SBI frame boundary of the next frame. RWSEL is sampled on the rising edge of SYSCLK.</p>
IUSER2	Input	AC15	<p><b>Input In-band Link User Signal.</b> The input in-band link user signal, IUSER2, provides external control over one of the bits in the in-band link. The USER[2] bit in the header of the in-band signaling channel of both the working and protection serial links will reflect the state of this input. IUSER2 an asynchronous signal and is internally synchronized to SYSCLK.</p>
OUSER2	Output	AA1	<p><b>Output In-Band Link User Signal.</b> The output in-band link user signal, OUSER2, reflects the state of the USER[2] bit in the header of the in-band signaling channel of either the working or the protection serial link, whichever is active. OUSER2 is an asynchronous output.</p>



Pin Name	Type	Pin No.	Function
RSTB	Input	AC22	<b>Reset Enable Bar.</b> The active low reset signal, RSTB, provides an asynchronous SBS reset. RSTB is a Schmitt triggered input with an integral pull-up resistor.
<b>JTAG Interface (5 Signals)</b>			
TCK	Input	P2	<b>Test Clock.</b> The JTAG test clock signal, TCK, provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	P3	<b>Test Mode Select.</b> The JTAG test mode select signal, TMS, controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	R1	<b>Test Data Input.</b> The JTAG test data input signal, TDI, carries test data into the SBS via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Tristate	M2	<b>Test Data Output.</b> The JTAG test data output signal, TDO, carries test data out of the SBS via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Input	P4	<b>Test Reset Bar.</b> The active low JTAG test reset signal, TRSTB, provides an asynchronous SBS test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor.  Note that when TRSTB is not being used, it must be connected to the RSTB input.
<b>Analog Reference Resistors (2 Signals)</b>			
RES	Analog	F25	<b>Reference Resistor Connection (RES).</b> An off-chip 3.16kΩ ±1% resistor is connected between this positive resistor reference pin and a Kelvin ground pin, RESK. An on-chip negative feedback path will force the 0.8 V VREF onto RES, therefore forcing 252uA of current to flow through the resistor.
RESK	Analog	F26	<b>Reference Resistor Connection (RESK).</b> An off-chip 3.16 kΩ ±1% resistor is connected between the positive resistor reference pin, RESK, and this Kelvin ground pin. An on-chip negative feedback path will force the 0.8 VREF onto RESK, therefore forcing 252 uA of current to flow through the resistor.
<b>Analog Test Bus (2 Signals)</b>			
ATB0	Analog	M24	<b>Analog test pin (ATB0).</b> This pin is used for PMC validation and testing.
ATB1	Analog	M23	<b>Analog test pin (ATB1).</b> This pin is used for PMC validation and testing.

Pin Name	Type	Pin No.	Function
<b>Analog High Voltage Power (8 Signals)</b>			
CSU_AVDH	Power	P23	<b>CSU Analog Power (CSU_AVDH).</b> This pin should be connected to a well-decoupled +3.3V DC supply.
AVDH[6] AVDH[5] AVDH[4] AVDH[3] AVDH[2] AVDH[1] AVDH[0]	Power	Y23 T23 J23 D24 E24 AB24 AC24	<b>Analog Power (AVDH[6:0]).</b> These pins should be connected to a well-decoupled +3.3 V DC supply.
<b>Analog Low Voltage Power (4 Signals)</b>			
AVDL[3] AVDL[2] AVDL[1] AVDL[0]	Power	N23 P25 P26 R24	<b>Analog Power (AVDL[3:0]).</b> This pin should be connected to a well-decoupled +1.8V DC supply. Each AVDL pin requires individual filtering.
<b>Digital Core Power (8 Signals)</b>			
DVDDI[7] DVDDI[6] DVDDI[5] DVDDI[4] DVDDI[3] DVDDI[2] DVDDI[1] DVDDI[0]	Power	U24 AA24 AF20 AE9 AC1 J3 A5 C16	<b>Digital Core Power (DVDDI[7:0]).</b> The digital core power pins should be connected to a well-decoupled +1.8 V DC supply.
<b>Digital I/O Power (22 Signals)</b>			
DVDDO[21] DVDDO[20] DVDDO[19] DVDDO[18] DVDDO[17] DVDDO[16] DVDDO[15] DVDDO[14] DVDDO[13] DVDDO[12] DVDDO[11] DVDDO[10] DVDDO[9] DVDDO[8] DVDDO[7] DVDDO[6] DVDDO[5] DVDDO[4] DVDDO[3] DVDDO[2] DVDDO[1] DVDDO[0]	Power	AB23 D23 C24 B25 D18 D13 D8 D4 C3 B2 H4 N4 V4 AC4 AD3 AE2 AC9 AC14 AC19 AC23 AD24 AE25	<b>Digital I/O Power (DVDDO[21:0]).</b> The digital I/O power pins should be connected to a well-decoupled +3.3 V DC supply.

Pin Name	Type	Pin No.	Function
<b>Ground (40 Signals)</b>			
VSS[39] VSS[38] VSS[37] VSS[36] VSS[35] VSS[34] VSS[33] VSS[32] VSS[31] VSS[30] VSS[29] VSS[28] VSS[27] VSS[26] VSS[25] VSS[24] VSS[23] VSS[22] VSS[21] VSS[20] VSS[19] VSS[18] VSS[17] VSS[16] VSS[15] VSS[14] VSS[13] VSS[12] VSS[11] VSS[10] VSS[9] VSS[8] VSS[7] VSS[6]	Ground	A26 B26 C25 A25 B24 A14 A13 B3 A2 A1 B1 C2 N1 P1 AD2 AE1 AF1 AF2 AE3 AF13 AF14 AE24 AF25 AF26 AE26 AD25 AD26 AC25 AC26 AB26 Y26 V26 T26 L26	<b>Ground (VSS[39:0]).</b> The ground pins, VSS[39:0], should be connected to GND.
VSS[5] VSS[4] VSS[3] VSS[2] VSS[1] VSS[0]	Ground	J26 G26 E26 D26 D25 C26	

Pin Name	Type	Pin No.	Function
<b>No Connect (60 signals)</b>			
NC[59:25]	No Connect	A23 A22 A9 A6 A3 B18 B16 B15 B12 C23 C22 C21 C14 C4 D14 D9 D7 D5 D3 D1 E25 E23 E4 F24 F23 F2 G25 G24 G23 H24 H23 J25 J24 J4 K24	The No Connect pins must be left floating.

Pin Name	Type	Pin No.	Function
NC[24:0]	No Connect	K23 K4 L25 L24 L23 M1 N24 N2 P24 U4 W4 W1 AB4 AB2 AC18 AC13 AC3 AD20 AD17 AE19 AE16 AE14 AF21 AF17 AF9	

**Notes on Pin Description:**

1. All SBS inputs and bi-directionals except the LVDS links present minimum capacitive loading and operate at TTL (V<sub>dd</sub> reference) logic levels.
2. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.
3. All SBS outputs have 8 mA drive capability.
4. The DVDDI and AVDL power pins are not internally connected to each other. Failure to connect these pins externally may cause malfunction or damage to the SBS.
5. The AVDH, CSU\_AVDH and DVDDO power pins are not internally connected to each other. Failure to connect these pins externally may cause malfunction or damage to the SBS.
6. The DVDDI, DVDDO, AVDH, CSU\_AVDH and AVDL power pins all share a common ground.
7. To prevent damage to the SBS and to ensure proper operation, power must be applied simultaneously to all 3.3 V power pins followed by power to all the 1.8 V power pins followed by input pins driven by signals.
8. To prevent damage to the SBS, power must first be removed from input pins. Then power may be removed from all the 1.8 V power supply pins. Only then, should power be simultaneously removed from all the 3.3 V power pins.

## 10 Functional Description

### 10.1 SBI Bus Data Formats

The 19.44 MHz Scalable Bandwidth Interconnect (SBI™) bus is a multi-point to multi-point bus. Since each SBS SBI interface handles the full SBI bus capacity, it will be more common for a single SBS to talk to multiple devices over the SBI bus, but there is nothing in the SBS that would prevent the SBS from sharing an SBI bus with other SBI devices.

#### 10.1.1 SBI Multiplexing Structure

The SBI structure uses a locked SONET/SDH structure fixing the position of the TU-3 relative to the STS-3/STM-1. The SBI is also of fixed frequency and alignment as determined by the reference clock (SREFCLK19) and frame indicator signal (IC1FP). Frequency deviations are compensated by adjusting the location of the T1/E1/DS3/E3/TVT1.5/TVT2 channels using floating tributaries as determined by the V5 indicator and payload signals (IV5[x] and IPL[x]). TVTs also allow for synchronous operation where SONET/SDH tributary pointers are carried within the SBI structure in place of the V5 indicator and payload signals (IV5[x] and IPL[x]). Fractional links use as many bytes as required within a given synchronous payload envelope (SPE) using the payload signals to indicate bytes carrying valid data.

Table 1 shows the bus structure for carrying T1, E1, TVT1.5, TVT2, DS3, E3 and Fractional tributaries in a SDH STM-1 like format. Up to 84 T1s, 63 E1s, 84 TVT1.5s, 63 TVT2s, 3 DS3s, 3 E3s or 3 Fractional rate links are carried within the octets labeled SPE1, SPE2 and SPE3 in columns 16-270. All other octets are unused and are of fixed position. The frame signal (IC1FP) occurs during the octet labeled C1 in Row 1 column 7.

The multiplexed links are separated into three SPEs: SPE1, SPE2 and SPE3. Each envelope carries up to 28 T1s, 21 E1, 28 TVT1.5s, 21 TVT2s, a DS3, an E3 or a Fractional link. SPE1 carries the T1s numbered 1,1 through 1,28, E1s numbered 1,1 through 1,21, DS3 number 1,1, E3 number 1,1 or Fractional link 1,1. SPE2 carries T1s numbered 2,1 through 2,28, E1s numbered 2,1 through 2,21, DS3 number 2,1, E3 number 2,1 or Fractional link 2,1. SPE3 carries T1s numbered 3,1 through 3,28, E1s numbered 3,1 through 3,21, DS3 number 3,1, E3 number 3,1 or Fractional link 3,1. TVT1.5s are numbered the same as T1 tributaries and TVT2s are numbered the same as E1 tributaries.

**Table 1 Structure for Carrying Multiplexed Links**

		SBI Column														
		1	6	7	8	15	16	17	18	19	268	269	270			
Row	1	-	...	-	C1	-	...	-	SPE1	SPE2	SPE3	SPE1	...	SPE1	SPE2	SPE3
	2	-	...	-	-	-	...	-	SPE1	SPE2	SPE3	SPE1	...	SPE1	SPE2	SPE3
	9	-	-	-	-	-	-	-	SPE1	SPE2	SPE3	SPE1	-	SPE1	SPE2	SPE3
		1	2	3	3	5	6	6	6	7	90	90	90			
		SPE Column														

The mapping for each link type are rigidly defined. However, the mix of links transported across the bus at any one time is flexible. Each SPE, comprising 85 columns numbered 6 through 90, operates independently allowing a mix of T1s, E1s, TVT1.5s, TVT2s, DS3s, E3s or Fractional links. For example, SPE1 could transport a single DS3, SPE2 could transport a single E3 and SPE3 could transport either 28 T1s or 21 E1s. Each SPE is restricted to carrying a single tributary type. SBI columns 16-18 are unused for T1, E1, TVT1.5 and TVT2 tributaries.

**Tributary Numbering**

The tributary numbering convention for T1 and E1 uses the SPE number followed by the tributary number within that SPE. These are numbered sequentially. Table 2 and Table 3 show the T1 and E1 column numbering and relates the tributary number to the SPE column numbers and overall SBI column structure. Numbering for DS3 or E3 follows the same naming convention even though there is only one DS3 or E3 per SPE. TVT1.5s and TVT2s follow the same numbering conventions as T1 and E1 tributaries respectively. SBI columns 16-18 are unused for T1, E1, TVT1.5 and TVT2 tributaries.

**Table 2 T1/TVT1.5 Tributary Column Numbering**

T1#	SPE1 Column	SPE2 Column	SPE3 Column	SBI Column
1,1	7,35,63			19,103,187
2,1		7,35,63		20,104,188
3,1			7,35,63	21,105,189
1,2	8,36,64			22,106,190
2,2		8,36,64		23,107,191
...				
1,28	34,62,90			100,184,268
2,28		34,62,90		101,185,269
3,28			34,62,90	102,186,270

**Table 3 E1/TVT2 Tributary Column Numbering**

E1#	SPE1 Column	SPE2 Column	SPE3 Column	SBI Column
1,1	7,28,49,70			19,82,145,208
2,1		7,28,49,70		20,83,146,209
3,1			7,28,49,70	21,84,147,210
1,2	8,29,50,71			22,85,148,211
2,2		8,29,50,71		23,86,149,212
...				
1,21	27,48,69,90			79,142,205,268
2,21		27,48,69,90		80,143,206,269
3,21			27,48,69,90	81,144,207,270

**10.1.2 SBI Timing Master Modes**

The SBI is a synchronous bus that is timed to a reference 19.44 MHz clock and a 2 KHz frame pulse (8 KHz is easily derived from the 2 KHz and 19.44 MHz clock). All sources and sinks of data on this bus are timed to the reference clock and frame pulse.

The data format on the data bus allows for compensating between clock differences on the PHY, SBI and Link Layer devices. This is achieved by floating data structures within the SBI format.

Timing is communicated across the SBI bus by floating data structures within the bus. Payload indicator signals in the SBI control the position of the floating data structure and, therefore, the timing. When sources are running faster than the SBI, the floating payload structure is advanced by an octet by passing an extra octet in the V3 octet locations (H3 octet for DS3 and E3 mappings). When the source is slower than the SBI, the floating payload is retarded by leaving the octet after the V3 or H3 octet unused. Both these rate adjustments are indicated by the SBI control signals.

On the Drop Bus, all timing is sourced from the PHY and is passed onto the Link Layer device by the arrival rate of data over the SBI.

On the Add Bus, timing can be controlled by either the PHY or the Link Layer device by controlling the payload and by making justification requests. When the Link Layer device is the timing master the PHY device gets its transmit timing information from the arrival rate of data across the SBI. When the PHY device is the timing master it signals the Link Layer device to speed up or slow down with justification request signals. The PHY timing master indicates a speedup request to the Link Layer by asserting the justification request signal high during the V3 or H3 octet. When this is detected by the Link Layer it will advance the channel by inserting data in the next V3 or H3 octet as described above. The PHY timing master indicates a slowdown request to the Link Layer by asserting the justification request signal high during the octet after the V3 or H3 octet. When detected by the Link Layer it will retard the channel by leaving the octet following the next V3 or H3 octet unused. Both advance and retard rate adjustments take place in the frame or multi-frame following the justification request.



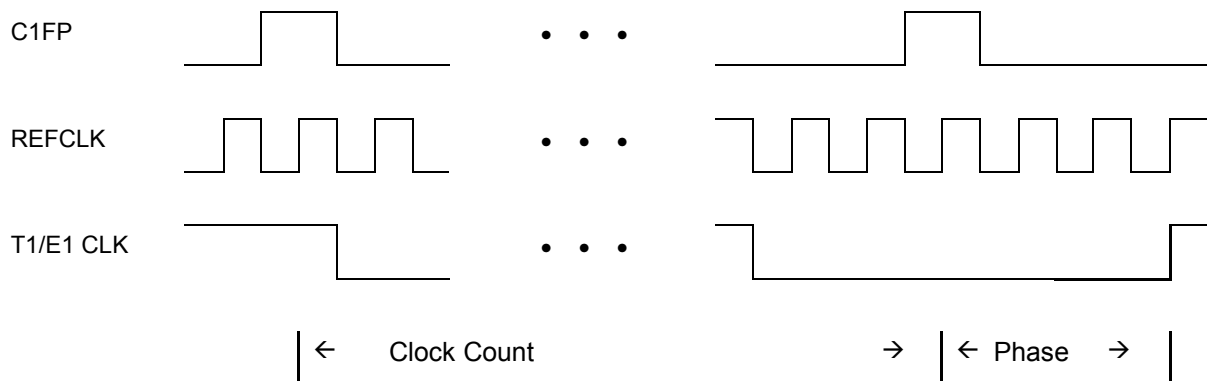
The SBI bus supports a synchronous SBI mode for T1 and E1 links. In this mode, the DS0s or timeslots within the T1 or E1 tributaries are fixed to the locations shown in the T1 and E1 mappings. Effectively synchronous mode locks the V5 in the octet following the V1 octet and does not allow the tributaries to float relative to SREFCLK19.

### 10.1.3 SBI Link Rate Information

The SBI bus provides a method for carrying link rate information. This is optional on a per channel basis. Two methods are specified, one for T1 and E1 channels and the second for DS3 and E3 channels. Link rate information is not available for TVTs. These methods use the reference 19.44 MHz SBI clock and the IC1FP frame synchronization signal to measure channel clock ticks and clock phase for transport across the bus.

The T1 and E1 method allows for a count of the number of T1 or E1 rising clock edges between two IC1FP frame pulses. This count is encoded in ClkRate[1:0] to indicate that the nominal number of clocks, one more than nominal or one less than nominal should be generated during the IC1FP period. This method also counts the number of 19.44 MHz clock rising edges after sampling IC1FP high to the next rising edge of the T1 or E1 clock, giving the ability to control the phase of the generated clock. The link rate information passed across the SBI bus via the V4 octet and is shown in Table 4. Table 5 shows the encoding of the clock count, ClkRate[1:0], passed in the link rate octet.

**Table 4 T1/E1 Link Rate Information**



Link Rate Octet	Bit #	7	6	5:4	3:0
T1/E1 Format		ALM	0	ClkRate[1:0]	Phase[3:0]

**Table 5 T1/E1 Clock Rate Encoding**

ClkRate[1:0]	T1 Clocks / 2KHz	E1 Clocks / 2 KHz
"00" – Nominal	772	1024
"01" – Fast	773	1025
"1x" – Slow	771	1023

The DS3 and E3 method for transferring link rate information across the SBI passes the encoded count of DS3/E3 clocks between C1FP pulses in the same method used for T1/E1 tributaries, but does not pass any phase information. The other difference from T1/E1 link rate is that ClkRate[1:0] indicates whether the nominal number of clocks are generated or if four fewer or four extra clocks are generated during the C1FP period. The format of the DS3/E3 link rate octet is shown in Table 6. This is passed across the SBI via the Linkrate octet which follows the H3 octet in the column, see Table 12 and Table 15. Table 7 shows the encoding of the clock count, ClkRate[1:0], passed in the link rate octet.

**Table 6 DS3/E3 Link Rate Information**

Link Rate Octet	Bit #	7	6	5:4	3:0
DS3/E3 Format		ALM	0	ClkRate[1:0]	Unused

**Table 7 DS3/E3 Clock Rate Encoding**

ClkRate[1:0]	DS3 Clocks / 2KHz	E3 Clocks / 2 KHz
"00" – Nominal	22368	17184
"01" – Fast	22372	17188
"1x" – Slow	22364	17180

### 10.1.4 Alarms

A method is provided for transferring alarm conditions across the SBI bus. This is optional on a per tributary basis and is valid for T1, E1, DS3, E3 tributaries but not valid for transparent VTs or Fractional links.

Table 4 and Table 6 show the alarm indication bit (ALM) as bit 7 of the Link Rate Octet. Devices that do not support alarm indications should set this bit to 0. When not enabled, the value of this bit must be ignored by the receiving device.

The presence of an alarm condition is indicated by the ALM bit set high in the Link Rate Octet. The absence of an alarm condition is indicated by the ALM bit set low in the Link Rate Octet. The ALM bit is transparent to the SBS.

### 10.1.5 T1 Tributary Mapping

Table 8 shows the format for mapping 84 T1s within the SPE octets. The DS0s and framing bits within each T1 are easily located within this mapping for channelized T1 applications. It is acceptable for the framing bit to not carry a valid framing bit on the Add Bus since the Physical Layer device will provide this information. Unframed T1s use the exact same format for mapping 84 T1s into the SBI except that the T1 tributaries need not align with the frame bit and DS0 locations. The V1, V2 and V4 octets are not used to carry T1 data and are either reserved or used for control across the interface. When enabled, the V4 octet is the Link Rate octet of Tables 1 and 3. It carries alarm and clock phase information across the SBI bus. The V1 and V2 octets are unused and should be ignored by devices listening to the SBI bus. The V5 and R octets do not carry any information and are fixed to a zero value. The V3 octet carries a T1 data octet but only during rate adjustments as indicated by the V5 indicator signals, IV5 and OV5, and payload signals, IPL and OPL. The PPSSSSFR octets carry channel associated signaling (CAS) bits and the T1 framing overhead. The DS0 octets are the 24 DS0 channels making up the T1 link.

The V1, V2, V3 and V4 octets are fixed to the locations shown. All the other octets, shown shaded for T1#1,1, float within the allocated columns maintaining the same order and moving a maximum of one octet per 2 KHz multi-frame. The position of the floating T1 is identified via the V5 Indicator signals, IV5 and OV5, which locate the V5 octet. When the T1 tributary rate is faster than the SBI nominal T1 tributary rate, the T1 tributary is shifted ahead by one octet which is compensated by sending an extra octet in the V3 location. When the T1 tributary rate is slower than the nominal SBI tributary rate the T1 tributary is shifted by one octet which is compensated by inserting a stuff octet in the octet immediately following the V3 octet and delaying the octet that was originally in that position.

**Table 8 T1 Framing Format**

ROW #	COL #	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28
	1-18	19	20-102	103	104-186	187	188-270
1	Unused	V1	V1	V5	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V2	V2	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V3	V3	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-
9	Unused	DS0#22	-	DS0#23	-	DS0#24	-
1	Unused	V4	V4	R	-	PPSSSSFR	-
2	Unused	DS0#1	-	DS0#2	-	DS0#3	-
3	Unused	DS0#4	-	DS0#5	-	DS0#6	-
4	Unused	DS0#7	-	DS0#8	-	DS0#9	-
5	Unused	DS0#10	-	DS0#11	-	DS0#12	-
6	Unused	DS0#13	-	DS0#14	-	DS0#15	-
7	Unused	DS0#16	-	DS0#17	-	DS0#18	-
8	Unused	DS0#19	-	DS0#20	-	DS0#21	-

COL #	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28	T1#1,1	T1#2,1-3,28
<b>ROW #</b> 1-18	<b>19</b>	<b>20-102</b>	<b>103</b>	<b>104-186</b>	<b>187</b>	<b>188-270</b>
9 Unused	DS0#22	-	DS0#23	-	DS0#24	-

The P<sub>1</sub>P<sub>0</sub>S<sub>1</sub>S<sub>2</sub>S<sub>3</sub>S<sub>4</sub>FR octet carries T1 framing in the F bit and channel associated signaling in the P<sub>1</sub>P<sub>0</sub> and S<sub>1</sub>S<sub>2</sub>S<sub>3</sub>S<sub>4</sub> bits. CAS is optional. The R bit is reserved and is set to 0. The P<sub>1</sub>P<sub>0</sub> bits are used to indicate the phase of the channel associated signaling and the S<sub>1</sub>S<sub>2</sub>S<sub>3</sub>S<sub>4</sub> bits are the channel associated signaling bits for the 24 DS0 channels in the T1. Table 9 shows the channel associated signaling bit mapping and how the phase bits locate the sixteen state CAS mapping as well as T1 frame alignment for super frame and extended superframe formats. When using four state CAS then the signaling bits are A1-A24, B1-B24, A1-B24, B1-B24 in place of are A1-A24, B1-B24, C1-C24, D1-D24. When using 2 state CAS there are only A1-A24 signaling bits.

**Table 9 T1 Channel Associated Signaling bits**

				SF	ESF	
S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	F	F	P <sub>1</sub> P <sub>0</sub>
A1	A2	A3	A4	F1	M1	00
A5	A6	A7	A8	S1	C1	00
A9	A10	A11	A12	F2	M2	00
A13	A14	A15	A16	S2	F1	00
A17	A18	A19	A20	F3	M3	00
A21	A22	A23	A24	S3	C2	00
B1	B2	B3	B4	F4	M4	01
B5	B6	B7	B8	S4	F2	01
B9	B10	B11	B12	F5	M5	01
B13	B14	B15	B16	S5	C3	01
B17	B18	B19	B20	F6	M6	01
B21	B22	B23	B24	S6	F3	01
C1	C2	C3	C4	F1	M7	10
C5	C6	C7	C8	S1	C4	10
C9	C10	C11	C12	F2	M8	10
C13	C14	C15	C16	S2	F4	10
C17	C18	C19	C20	F3	M9	10
C21	C22	C23	C24	S3	C5	10
D1	D2	D3	D4	F4	M10	11
D5	D6	D7	D8	S4	F5	11
D9	D10	D11	D12	F5	M11	11
D13	D14	D15	D16	S5	C6	11
D17	D18	D19	D20	F6	M12	11
D21	D22	D23	D24	S6	F6	11

T1 tributary asynchronous timing is compensated via the V3 octet as described in section 10.1.2. T1 tributary link rate adjustments are optionally passed across the SBI via the V4 octet as described in section 10.1.3. T1 tributary alarm conditions are optionally passed across the SBI bus via the link rate octet in the V4 location as described in Section 10.1.3 and 10.1.4.

The SBI bus allows for a synchronous T1 mode of operation. In this mode the T1 tributary mapping is fixed to that shown in Table 8 and rate justifications are not possible using the V3 octet. The clock rate information within the link rate octet in the V4 location is not used in synchronous mode.

### **10.1.6 E1 Tributary Mapping**

Table 10 shows the format for mapping 63 E1s within the SPE octets. The timeslots and framing bits within each E1 are easily located within this mapping for channelized E1 applications. It is acceptable for the framing bits to not carry valid framing information on the Add Bus since the physical layer device will provide this information. Unframed E1s use the exact same format for mapping 63 E1s into the SBI except that the E1 tributaries need not align with the timeslot locations associated with channelized E1 applications. The V1, V2 and V4 octets are not used to carry E1 data and are either reserved used for control information across the interface. When enabled, the V4 octet carries clock phase information across the SBI. The V1 and V2 octets are unused and should be ignored by devices listening to the SBI bus. The V5 and R octets do not carry any information and are fixed to a zero value. The V3 octet carries an E1 data octet but only during rate adjustments as indicated by the V5 indicator signals, IV5 and OV5, and payload signals, IPL and OPL. The PP octets carry channel associated signaling phase information and E1 frame alignment. TS#0 through TS#31 make up the E1 channel.

The V1, V2, V3 and V4 octets are fixed to the locations shown. All the other octets, shown shaded for E1#1,1, float within the allocated columns maintaining the same order and moving a maximum of one octet per 2 KHz multi-frame. The position of the floating E1 is identified via the V5 Indicator signals, IV5 and OV5, which locate the V5 octet. When the E1 tributary rate is faster than the E1 tributary nominal rate, the E1 tributary is shifted ahead by one octet which is compensated by sending an extra octet in the V3 location. When the E1 tributary rate is slower than the nominal rate the E1 tributary is shifted by one octet which is compensated by inserting a stuff octet in the octet immediately following the V3 octet and delaying the octet that was originally in that position.

**Table 10 E1 Framing Format**

ROW #	COL #	E1#1,1	#2,1-	E1#1,1	#2,1-	E1#1,1	#2,1-	E1#1,1	#2,1-
	1-18	19	20-81	82	83-144	145	146-207	208	209-270
1	Unused	V1	V1	V5	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-
1	Unused	V2	V2	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-
1	Unused	V3	V3	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-
9	Unused	TS#29	-	TS#30	-	TS#31	-	R	-
1	Unused	V4	V4	R	-	PP	-	TS#0	-
2	Unused	TS#1	-	TS#2	-	TS#3	-	TS#4	-
3	Unused	TS#5	-	TS#6	-	TS#7	-	TS#8	-
4	Unused	TS#9	-	TS#10	-	TS#11	-	TS#12	-
5	Unused	TS#13	-	TS#14	-	TS#15	-	TS#16	-
6	Unused	TS#17	-	TS#18	-	TS#19	-	TS#20	-
7	Unused	TS#21	-	TS#22	-	TS#23	-	TS#24	-
8	Unused	TS#25	-	TS#26	-	TS#27	-	TS#28	-

	<b>COL #</b>	<b>E1#1,1</b>	<b>#2,1-</b>	<b>E1#1,1</b>	<b>#2,1-</b>	<b>E1#1,1</b>	<b>#2,1-</b>	<b>E1#1,1</b>	<b>#2,1-</b>
<b>ROW #</b>	<b>1-18</b>	<b>19</b>	<b>20-81</b>	<b>82</b>	<b>83-144</b>	<b>145</b>	<b>146-207</b>	<b>208</b>	<b>209-270</b>
<b>9</b>	Unused	TS#29	-	TS#30	-	TS#31	-	R	-

When using CAS TS#16 carries the ABCD signaling bits and the timeslots 17 through 31 are renumbered 16 through 30. The PP octet is 0h for all frames except for the frame which carries the CAS for timeslots 15/30 at which time the PP octet is C0h. The first octet of the CAS multi-frame, RRRRRRRR, is reserved and should be ignored by the receiver when CAS signaling is enabled. Table 11 shows the format of timeslot 16 when carrying channel associated signaling.

**Table 11 E1 Channel Associated Signaling bits**

<b>TS#16[7:4]</b>	<b>TS#16[3:0]</b>	<b>PP</b>
RRRR	RRRR	00
ABCD1	ABCD16	00
ABCD2	ABCD17	00
ABCD3	ABCD18	00
ABCD4	ABCD19	00
ABCD5	ABCD20	00
ABCD6	ABCD21	00
ABCD7	ABCD22	00
ABCD8	ABCD23	00
ABCD9	ABCD24	00
ABCD10	ABCD25	00
ABCD11	ABCD26	00
ABCD12	ABCD27	00
ABCD13	ABCD28	00
ABCD14	ABCD29	00
ABCD15	ABCD30	C0

E1 tributary asynchronous timing is compensated via the V3 octet as described in section 10.1.2. E1 tributary link rate adjustments are optionally passed across the SBI via the V4 octet as described in section 10.1.3. E1 tributary alarm conditions are optionally passed across the SBI bus via the link rate octet in the V4 location as described in Sections 10.1.3 and 10.1.4.

The SBI bus allows for a synchronous E1 mode of operation. In this mode, the E1 tributary mapping is fixed to that shown in Table 10 and rate justifications are not possible using the V3 octet. The clock rate information within the link rate octet in the V4 location is not used in synchronous mode.



### 10.1.7 DS3 Tributary Mapping

Table 12 shows a DS3 tributary mapped within the first synchronous payload envelope, SPE1. The V5 indicator pulse identifies the V5 octet. The DS3 framing format does not follow an 8KHz frame period so the floating DS3 multi-frame located by the V5 indicator, shown in heavy border grey region in Table 12, will jump around relative to the H1 frame on every pass. In fact the V5 indicator will often be asserted twice per H1 frame, as is shown by the second V5 octet in Table 12. The V5 indicator and payload signals indicate negative and positive rate adjustments which are carried out by either putting a data byte in the H3 octet or leaving empty the octet after the H3 octet.

**Table 12 DS3 Framing Format**

	SPE COL #		DS3 1	DS3 2-56	DS3 57	DS3 58-84	DS3 Col 85
ROW	SBI COL# 1,4,7,10	13	16	...	184	...	268
1	Unused	H1	V5	DS3	DS3	DS3	DS3
2	Unused	H2	DS3	DS3	DS3	DS3	DS3
3	Unused	H3	DS3	DS3	DS3	DS3	DS3
4	Unused	Linkrate	DS3	DS3	DS3	DS3	DS3
5	Unused	Unused	DS3	DS3	DS3	DS3	DS3
6	Unused	Unused	DS3	DS3	DS3	DS3	DS3
7	Unused	Unused	DS3	DS3	DS3	DS3	DS3
8	Unused	Unused	DS3	DS3	V5	DS3	DS3
9	Unused	Unused	DS3	DS3	DS3	DS3	DS3

Because the DS3 tributary rate is less than the rate of the grey region, padding octets are interleaved with the DS3 tributary to make up the difference in rate. Interleaved with every DS3 multi-frame are 35 stuff octets, one of which is the V5 octet. These 35 stuff octets are spread evenly across seven DS3 subframes. Each DS3 subframe is eight blocks of 85 bits. The 85 bits making up a DS3 block are padded out to be 11 octets. Table 13 shows the DS3 block 11 octet format where R indicates a stuff bit, F indicates a DS3 framing bit and I indicates DS3 information bits. Table 14 shows the DS3 multi-frame format that is packed into the grey region of Table 12. In this table V5 indicates the V5 octet which is also a stuff octet, R indicates a stuff octet and B indicates the 11 octet DS3 block. Each row in Table 14 is a DS3 multi-frame. The DS3 multi-frame stuffing format is identical for 5 multi-frames and then an extra stuff octet after the V5 octet is added every sixth frame.

**Table 13 DS3 Block Format**

Octet #	1	2	3	4	5	6	7	8	9	10	11
Data	RRRFVIII	8*1	8*1	8*1	8*1	8*1	8*1	8*1	8*1	8*1	8*1

**Table 14 DS3 Multi-frame Stuffing Format**

V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	4*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B
V5	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B	5*R	8*B

DS3 asynchronous timing is compensated via the H3 octet as described in section 10.1.2. DS3 link rate adjustments are optionally passed across the SBI via the Linkrate octet as described in section 10.1.3. DS3 alarm conditions are optionally passed across the SBI bus via the Linkrate octet as described in section 10.1.3 and 10.1.4.

**10.1.8 E3 Tributary Mapping**

Table 15 shows a E3 tributary mapped within the first synchronous payload envelope SPE1. The V5 indicator pulse identifies the V5 octet. The E3 framing format does not follow an 8KHz frame period so the floating frame located by the V5 indicator and shown in grey in Table 15, will jump around relative to the H1 frame on every pass. In fact the V5 indicator will be asserted two or three times per H1 frame, as is shown by the second and third V5 octet in Table 15. The V5 indicator and payload signals indicate negative and positive rate adjustments which are carried out by either putting a data byte in the H3 octet or leaving empty the octet after the H3 octet.

**Table 15 E3 Framing Format**

	SPE COL #		E3 1	E3 2-18	E3 19	E3 20-38	E3 39	E3 40-84	E3 85
ROW	SBI COL# 1,4,7,10	13	16	...	70	...	130	...	268
1	Unused	H1	V5	E3	E3	E3	E3	E3	E3
2	Unused	H2	E3	E3	E3	E3	E3	E3	E3
3	Unused	H3	E3	E3	E3	E3	E3	E3	E3
4	Unused	Linkrate	E3	E3	V5	E3	E3	E3	E3
5	Unused	Unused	E3	E3	E3	E3	E3	E3	E3
6	Unused	Unused	E3	E3	E3	E3	E3	E3	E3
7	Unused	Unused	E3	E3	E3	E3	V5	E3	E3
8	Unused	Unused	E3	E3	E3	E3	E3	E3	E3
9	Unused	Unused	E3	E3	E3	E3	E3	E3	E3

Because the E3 tributary rate is less than the rate of the grey region, padding octets are interleaved with the E3 tributary to make up the difference in rate. Interleaved with every E3 frame is an alternating pattern of 81 and 82 stuff octets, one of which is the V5 octet. These 81 or 82 stuff octets are spread evenly across the E3 frame. Each E3 subframe is 48 octet which is further broken into 4 equal blocks of 12 octets each. Table 16 shows the alternating E3 frame stuffing format that is packed into the grey region of Table 15. Note that there are 6 stuff octets after the V5 octet in one frame and 5 stuff octets after the V5 octet in the next frame. In this table V5 indicates the V5 octet which is also a stuff octet, R indicates a stuff octet, D indicates an E3 data octet, FAS indicates the first byte of the 10 bit E3 Frame Alignment Signal.

**Table 16 E3 Frame Stuffing Format**

V5	6*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
V5	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D
	5*R	FAS	11*D	5*R	12*D	5*R	12*D	5*R	12*D

E3 asynchronous timing is compensated via the H3 octet as described in Section 10.1.2. E3 link rate adjustments are optionally passed across the SBI via the Linkrate octet as described in section 10.1.3. E3 alarm conditions are optionally passed across the SBI bus via the Linkrate octet as described in section 10.1.3 and 10.1.4.

### 10.1.9 Transparent VT1.5/TU11 Mapping

VT1.5 and TU11 virtual tributaries, TVT1.5s, are transported across the SBI bus in a similar manner to the T1 tributary mapping. Table 17 shows the transparent structure where “I” is used to indicate information bytes. There are two options when carrying virtual tributaries on the SBI bus, the primary difference being how the floating V5 payload is located.

The first option is locked TVT mode which carries the entire VT1.5/TU11 virtual tributary indicated by the shaded region in Table 17. Locked is used to indicate that the location of the V1,V2 pointer is locked. The virtual tributary must have a valid V1,V2 pointer to locate the V5 payload. In this mode the V5 indicator and payload signals, IV5, OV5, IPL and OPL, may be generated but must be ignored by the receiving device. In locked mode timing is always sourced by the transmitting side, therefore justification requests are not used and the JUST\_REQ signal is ignored. Other than the V1 and V2 octets which must carry valid pointers, all octets can carry data in any format. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 17.

The second option is floating TVT mode which carries the payload comprised of the V5 and I octets within the shaded region of Table 17. In this mode the V1,V2 pointers are still in a fixed location and may be valid but are ignored by the receiving device. The V5 indicator and payload signals, IV5, OV5, IPL and OPL, must be valid and are used to locate the floating payload. The justification request signal can be used to control the timing on the add bus. The V3 octets are used to accommodate justification requests. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 17.

**Table 17 Transparent VT1.5/TU11 Format**

ROW #	COL #	VT1.5#1,1	#2,1-3,28	VT1.5#1,1	#2,1-3,28	VT1.5#1,1	#2,1-3,28
	1-18	19	20-102	103	104-186	187	188-270
1	Unused	V1	V1	V5	-		-
2	Unused		-		-		-
3	Unused		-		-		-
4	Unused		-		-		-
5	Unused		-		-		-
6	Unused		-		-		-
7	Unused		-		-		-
8	Unused		-		-		-
9	Unused		-		-		-
1	Unused	V2	V2		-		-
2	Unused		-		-		-
3	Unused		-		-		-
4	Unused		-		-		-
5	Unused		-		-		-
6	Unused		-		-		-
7	Unused		-		-		-
8	Unused		-		-		-
9	Unused		-		-		-
1	Unused	V3	V3		-		-
2	Unused		-		-		-
3	Unused		-		-		-
4	Unused		-		-		-
5	Unused		-		-		-
6	Unused		-		-		-
7	Unused		-		-		-
8	Unused		-		-		-
9	Unused		-		-		-
1	Unused	V4	V4		-		-
2	Unused		-		-		-
3	Unused		-		-		-

COL #	VT1.5#1,1	#2,1-3,28	VT1.5#1,1	#2,1-3,28	VT1.5#1,1	#2,1-3,28
<b>1-18</b>	<b>19</b>	<b>20-102</b>	<b>103</b>	<b>104-186</b>	<b>187</b>	<b>188-270</b>
4	Unused		-		-	
5	Unused		-		-	
6	Unused		-		-	
7	Unused		-		-	
8	Unused		-		-	
9	Unused		-		-	

**10.1.10 Transparent VT2/TU12 Mapping**

VT2 and TU12 virtual tributaries, TVT2s, are transported across the SBI bus in a similar manner to the E1 tributary mapping. Table 18 shows the transparent structure where “I” is used to indicate information bytes. There are two options when carrying virtual tributaries on the SBI bus, the primary difference being how the floating V5 payload is located.

The first option is locked TVT mode, which carries the entire VT2/TU12 virtual tributary indicated by the shaded region in Table 18. Locked is used to indicate that the location of the V1,V2 pointer is locked. The virtual tributary must have a valid V1,V2 pointer to locate the V5 payload. In this mode the V5 indicator and payload signals, IV5, OV5, IPL and OPL, are optionally generated but must be ignored by the receiving device. In locked mode timing is always sourced by the transmitting side, therefore justification requests are not used and the JUST\_REQ signal is ignored. Other than the V1 and V2 octets which are carrying valid pointers, all octets can carry data in any format. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 18.

The second option is floating TVT mode, which carries the payload comprised of the V5 and I octets within the shaded region of Table 18. In this mode the V1,V2 pointers are still in a fixed location and may be valid but are ignored by the receiving device. The V5 indicator and payload signals, IV5, OV5, IPL and OPL, must be valid and are used to locate the floating payload. The justification request signal can be used to control the timing on the add bus. The V3 octet is used to accommodate justification requests. The location of the V1,V2,V3 and V4 octets is fixed to the locations shown in Table 18.

**Table 18 Transparent VT2/TU12 Format**

COL #	E1#1,1	#2,1-3,28	E1#1,1	#2,1-3,28	E1#1,1	#2,1-3,28	E1#1,1	#2,1-3,28
<b>1-18</b>	<b>19</b>	<b>20-81</b>	<b>82</b>	<b>83-144</b>	<b>145</b>	<b>146-207</b>	<b>208</b>	<b>209-270</b>
1	Unuse	V1	V1	V5	-		-	
2	Unuse		-		-		-	
3	Unuse		-		-		-	
4	Unuse		-		-		-	
5	Unuse		-		-		-	
6	Unuse		-		-		-	
7	Unuse		-		-		-	

	COL #	E1#1,1	#2,1- 208	E1#1,1	#2,1- 208	E1#1,1	#2,1- 208	E1#1,1	#2,1- 208
ROW #	1-18	19	20-81	82	83-144	145	146-207	208	209-270
8	Unuse		-		-		-		-
9	Unuse		-		-		-		-
1	Unuse	V2	V2		-		-		-
2	Unuse		-		-		-		-
3	Unuse		-		-		-		-
4	Unuse		-		-		-		-
5	Unuse		-		-		-		-
6	Unuse		-		-		-		-
7	Unuse		-		-		-		-
8	Unuse		-		-		-		-
9	Unuse		-		-		-		-
1	Unuse	V3	V3		-		-		-
2	Unuse		-		-		-		-
3	Unuse		-		-		-		-
4	Unuse		-		-		-		-
5	Unuse		-		-		-		-
6	Unuse		-		-		-		-
7	Unuse		-		-		-		-
8	Unuse		-		-		-		-
9	Unuse		-		-		-		-
1	Unuse	V4	V4		-		-		-
2	Unuse		-		-		-		-
3	Unuse		-		-		-		-
4	Unuse		-		-		-		-
5	Unuse		-		-		-		-
6	Unuse		-		-		-		-
7	Unuse		-		-		-		-
8	Unuse		-		-		-		-
9	Unuse		-		-		-		-

### 10.1.11 Fractional Rate Tributary Mapping

The Fractional Rate SBI mapping is intended for support of data services over fractional DS3 or similar links. A fractional rate link is mapped into any SPE octet as defined in Table 1. Table 19 shows all the available information (I) octets useable for carrying a Fractional rate link mapped to a single SPE. There are no V1 to V5 bytes nor frame alignment signals in a fractional rate link. The Add bus and Drop bus payload signals, IPL and OPL, indicate when a fractional rate information byte contains valid data or is empty. The fractional rate link Add bus can have the timing master be either the PHY or the Link Layer device. When the PHY is the timing master the JUST\_REQ signal from the PHY communicates the transmit rate to the Link Layer device. The JUST\_REQ signal is asserted during any of the available fractional rate link octets to indicate that the PHY can accept another byte of data. For every byte that is marked with the JUST\_REQ signal the Link Layer device should respond with a valid byte to the PHY within a short time. The PHY accepts data from the Link Layer device whenever it sees valid data as indicated by the IPL or OPL signal, whether it is timing master or slave.

**Table 19 Fractional Rate Format**

	<b>SPE COL #</b>	<b>Fractional 1</b>	<b>Fractional 2-84</b>	<b>Fractional Col 85</b>
ROW	SBI COL# 1,4,7,10,13	16	...	268
1	Unused			
2	Unused			
3	Unused			
4	Unused			
5	Unused			
6	Unused			
7	Unused			
8	Unused			
9	Unused			

### 10.1.12 SBI336 Bus Format

The 77.76 MHz SBI336 bus is exactly four interleaved 19.44 MHz SBI buses. There are some slight differences between the two formats to accommodate the increased clock rate. The differences are:

The JUST\_REQ signal is referenced to the Drop bus C1FP alignment rather than the common Add/Drop C1FP alignment of the SBI bus. This aids 77.76 MHz bus timing by allowing buffering and retiming logic to be put between SBI336 devices. This change also aids construction of larger SBI cross connect systems using smaller buffers between devices by controlling the C1 frame alignment independently in each direction.

### 10.1.13 SBI336 Multiplexing Structure

**Table 20 Structure for Carrying Multiplexed Links in SBI336**

		SBI Column																		
		1	24	25	26	60	61	62	63	64	65	66	67	68	1078	1079	1080			
Row	1	-	...	-	C1	-	...	-	1,SPE1	2,SPE1	3,SPE1	4,SPE1	1,SPE2	2,SPE2	3,SPE2	4,SPE2	...	2,SPE3	3,SPE3	4,SPE3
2	-	...	-	-	-	...	-	1,SPE1	2,SPE1	3,SPE1	4,SPE1	1,SPE2	2,SPE2	3,SPE2	4,SPE2	...	2,SPE3	3,SPE3	4,SPE3	
⋮																				
9	-	-	-	-	-	-	1,SPE1	2,SPE1	3,SPE1	4,SPE1	1,SPE2	2,SPE2	3,SPE2	4,SPE2	...	2,SPE3	3,SPE3	4,SPE3		
		1	2	3	3	5	6	6	6	6	6	6	6	6	6	6	90	90	90	
		SPE Column																		

Table 20 shows how 12 SPEs are multiplexed into a 77.76 MHz SBI336 bus. The structure is exactly the same as byte interleaving four 19.44 MHz SBI buses. 1,SPE1 identifies SPE1 from the first SBI equivalent bus, 2,SPE1 identifies SPE1 from the second SBI equivalent bus, and so on. All tributary mapping formats are exactly the same as for the 19.44 MHz SBI bus with the only difference that there are four times the number of tributaries. Tributary numbering appends the equivalent SBI number to the original SBI numbering. For example, the first T1 in a SBI bus would be numbered T1 #1,1 whereas the first T1 in a SBI336 bus would be numbered T1 #1,1,1. Likewise the second T1 in a SBI bus would be T1 #2,1 whereas the second T1 in a SBI336 bus would be T1 #2,1,1.

## 10.2 Incoming SBI336 Timing Adapter

The Incoming SBI336 Timing Adapter, ISTA, provides a multiplexing function of four incoming 19.44 MHz SBI or TelecomBuses into a 77.76 MHz SBI336 or TelecomBus. This involves simple column muxing of the four incoming SBI or TelecomBuses. The timing adapter block also provides a transparent mode when the incoming interface is already in SBI336 or 77.76 MHz TelecomBus format.

When the SBS is connected to an 19.44 MHz SBI physical layer device, the justification request signal, JUST\_REQ, is an input to the SBS and is aligned to the outgoing bus. This block re-aligns the justification request signal from the outgoing frame alignment, marked by OC1FP, to the internal incoming SBI336 frame alignment. When the SBS is connected to a 19.44 MHz SBI link layer device or any 77.76 MHz SBI336 device, no re-alignment of the justification request is required by this block.



## 10.3 CAS Expanders

The Channel Associated Signaling Expander blocks, ICASE and OCASE, pull the CAS information from the SBI336 formatted bus on a tributary basis so that it can be switched through the memory switch with the DS0 data. For tributaries enabled for DS0 switching the Channel Associated Signaling bits (CAS bits) are double buffered on a signaling multiframe boundary and repeated along side the tributary data for the duration of the multiframe. This function is enabled on a per tributary basis and can be used for T1 and E1 tributaries simultaneously across SBI SPEs. This block adds one T1 multiframe (24 frames) or one E1 multiframe (16 frames) of latency to the CAS bits.

## 10.4 Memory Switch Units

The Memory Switch Unit blocks, IMSU and OMSU, provide DS0 or column switching of the SBI336 or 77.76 MHz TelecomBus. Any input byte (or column) can be switched to any output byte (or column). Four bits of Channel Associated Signaling (CAS) and three or four bits of control information are switched along with the data byte. In SBI336 mode, the control signals are PL, V5 and JUST\_REQ. In TelecomBus mode, the control signals are PL, TPL, V5 and TAIS.

In DS0 switch mode, the data entering the MSU is stored in two alternating pages of memory. Each page contains one complete frame (9720 bytes) of data. One of these alternating pages is currently filling while the other is currently full. Data exiting the MSU is extracted from the currently full page. As a consequence, the MSU imposes a nominal switching latency of 1 frame (125us). The selection of bytes to fill each output port requires a switching connection memory. Control is required for each of the 9720 bytes in the output SBI336 frame. Complete specification of an output byte requires 14 bits to specify which of the 9720 input bytes to use. Dual copies of this control memory are required to provide hitless frame boundary switchover.

In column switch mode, the same switching principle described above is used, but less memory is required. Data entering the MSU is stored in two alternating pages of memory. Each page contains one row (1080 bytes) of data. In this mode, the nominal latency is 1 row if a frame (<15 us). The switching connection memory for the output port requires control for each of the 1080 columns in the frame. Complete specification of an output column requires 11 bits to specify which of the 1080 input columns to use. Dual copies of this control memory are required to provide hitless frame boundary switchover.

Each MSU can be independently bypassed for reduced latency or debugging purposes.

### 10.4.1 Data Buffer

The Data Buffer block contains a double buffer structure for each frame consisting of a data byte, 4-bits of Channel Associated Signaling information and 4 bits of control information necessary for identifying valid data and timing.

## 10.4.2 Connection Memory

The Connection Memory sub-block contains two pages of mapping configuration, page 0 and page 1. One page is designated the active page and the other the stand-by page. Selection between which page is to be active and which is to be stand-by is controlled by the ICMP signal (for the IMSU) and OCMP signal (for the OMSU). The Connection Memory sub-block samples the value on the ICMP signal at the C1 byte position as defined by the incoming frame pulse signal, IC1FP. The Connection Memory sub-block samples the value on the OCMP signal at the C1 byte position as defined by the receive serial interface frame pulse signal, RC1FP. Swaps between the active/standby status of the two pages are synchronized to the first A1 byte of the next frame or multiframe. This arrangement allows all devices in a cross-connect system to be updated in a coordinated fashion. Consequently, DS0 streams or tributaries not being assigned new positions are unaffected by page swaps.

The CMP input signals can be overridden by register configuration or by the SBI336S inband link channel.

## 10.5 CAS Merging

The Channel Associated Signaling Merge blocks, ICASM and OCASM, insert the CAS signaling information into the SBI bus on a tributary basis. CAS signaling channels within the SBI bus are constructed out of the available CAS bits for T1 and E1 SBI tributaries that are enabled for CAS signaling. The resulting CAS signaling channel replaces the octets of the SBI bus where the new CAS signaling is to be inserted. This block adds one T1 multiframe (24 frames) or one E1 multiframe (16 frames) of latency to the CAS bits.

## 10.6 Incoming SBI336 Tributary Translator

The Incoming SBI336 Tributary Translator block, ISTT, translates all SBI336 timing and Channel Associated Signaling information for all tributaries into SBI336S format. The output from this block is a 77.76 MHz SBI336 stream with all tributaries and control signals encoded into an internal format that closely resembles the serial SBI336S format.

This block translates all tributary types into a form that is easy for the 8B/10B encoder to handle in a more generic form. A control RAM keeps the current configuration for each of the incoming SBI bus tributaries so that it can perform the translation function.

Common to all tributaries is identification of the first C1 byte. There are unique mappings of the 8B/10B codes for the supported SBI and SBI336 bus link types: Asynchronous T1/E1, Synchronous (locked) T1/E1, Transparent VT1.5/VT2, DS3/E3 and Fractional rate links. Much of the identification and mapping of a link into serial SBI format is based on the C1 frame pulse and a tributaries location relative to that C1 pulse. In addition to the C1FP identification this block identifies multiframe alignment, valid payload, pointer movements for floating tributaries and timing control for encoding into the 8B/10B serial SBI format.

This block is transparent in TelecomBus mode.

## 10.7 PRBS Processors

The Working and Protection PRBS Processor blocks, WPP and PPP, provides in-service and off-line PRBS generation and detection for diagnostics of the equipment downstream of the two LVDS links. Each PRBS Processor has the capacity to source and monitor PRBS data for the associated Working or Protection Serial SBI336S stream with a granularity of unchannelized SBI SPEs of TelecomBus STS-1s.

### 10.7.1 PRBS Generator

The PRBS generator sub-block optionally overwrites the data originating from the incoming data streams, IDATA[4:1][7:0]. When enabled, the PRBS generator sub-block inserts synchronous payload envelope, SPE bytes into the serial transmit links. The inserted data is derived from an internal linear feedback shift register (LFSR) with a polynomial of  $X^{23} + X^{18} + 1$ .

### 10.7.2 PRBS Detector

The PRBS detector sub-block monitors the synchronous payload envelope, SPE, bytes in the incoming data stream. The incoming data is compared against the expected value derived from an internal linear feedback shift register (LFSR) with a polynomial of  $X^{23} + X^{18} + 1$ . If the incoming data fails to match the expected value for three consecutive bytes, the PRBS detector sub-block will enter out-of-synchronization (OOS) state. The LFSR will be re-initialized using the incoming data bytes. The new LFSR seed is confirmed by comparison with subsequent incoming data bytes. The PRBS detector sub-block will exit the OOS state when the incoming data matches the LFSR output for three consecutive bytes. The PRBS detector sub-block will remain in the OOS state and re-load the LFSR if confirmation failed. The PRBS sub-block counts PRBS byte errors and optionally generates interrupts when it enters and exits the OOS state.

## 10.8 Transmit 8B/10B Encoders

The Transmit 8B/10B Encoder blocks, TW8E and TP8E, construct an 8B/10B character stream from an incoming translated SBI336 bus or TelecomBus carrying an STS-12/STM-4 equivalent stream.

In SBI mode, these blocks encode the SBI336S stream as shown in Table 21. When configured for Synchronous mode for DS0 switching, the 8B/10B encoder transmits CAS signaling multiframe alignment across the SBI336S interface by generating a C1FP character every 48 frame times. When not configured for DS0 switching the C1FP character is sent every 4 frames.

### 10.8.1 SBI336S 8B/10B Character Encoding

Table 21 shows the mapping of SBI336S bus control bytes and signals into 8B/10B control characters. The linkrate octet in location V4, V1 and V2, the in-band programming channel, the V3 octet when it contains data are all carried as data. Justification requests for master timing are carried in the V5 character so there are three V5 characters used, nominal, negative timing adjustment request, positive timing adjustment request.

**Table 21 SBI336S Character Encoding**

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
Common to All Link Types			
K28.5	001111 1010	110000 0101	IC1FP='b1 C1FP frame and multiframe alignment
K23.7-	111010 1000	-	Overhead Bytes (columns 1-60 or 1-72 except for C1 and in-band programming channel), V3 or H3 byte except during negative justification, byte after V3 or H3 byte during positive justification, unused bytes in fraction rate links
Asynchronous T1/E1 Links			
K27.7-	110110 1000	-	V5 byte, no justification request
K28.7-	001111 1000	-	V5 byte, negative justification request
K29.7-	101110 1000	-	V5 byte, positive justification request
Synchronous T1/E1 Links			
K27.7-	110110 1000	-	V5 byte
Asynchronous DS3/E3 Links			
K27.7-	110110 1000	-	V5 byte, no justification request
K28.7-	001111 1000	-	V5 byte, negative justification request*
K29.7-	101110 1000	-	V5 byte, positive justification request*
Fractional Rate Links			
K28.7-	001111 1000	-	V5 byte, send one extra byte request**
K29.7-	101110 1000	-	V5 byte, send one less byte request**
Floating Transparent Virtual Tributaries			
K27.7-	110110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b0
K27.7+	-	001001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b1
K28.7-	001111 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b0
K28.7+	-	110000 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b1
K29.7-	101110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b0

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
K29.7+	-	010001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b1
K30.7-	011110 1000	-	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b0
K30.7+	-	100001 0111	V5 byte IV5=1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b1

**Notes**

- Note there can be multiple V5s per SBI frame when in DS3 or E3 mode but only one justification can occur per SBI frame. Positive and negative justification request through V5 required by the SBI336S interface should be limited to one per frame.
- Note fractional rate links are symmetric in the transmit and receive direction over SBI336S. When using clock slave mode with a fractional rate link the clock master makes single byte adjustments to the slaves rate once per frame.

### 10.8.2 Serial TelecomBus 8B/10B Character Encoding

Table 22 shows the mapping of TelecomBus control bytes and signals into 8B/10B control characters. When the TelecomBus control signals conflict each other, the 8B/10B control characters are generated according to the sequence of the table, with the characters at the top of the table taking precedence over those lower in the table.

**Table 22 Serial TelecomBus Character Encoding**

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
High Order Path Termination (HPT) Mode			
K28.5	001111 1010	110000 0101	IC1FP='b1 IPL='b0 C1FP frame and multiframe alignment
K28.0-	001111 0100	-	IPL='b0 High-order path H3 byte position, no negative justification event.
K28.0+	-	110000 1011	IPL='b0 High-order path PSO byte position, positive justification event.
K28.6	001111 0110	110000 1001	IC1FP='b1, IPL='b1 High-order path frame alignment (J1).
Low Order Path Termination (LPT) Mode			
K28.4+	-	110000 1101	IT AIS='b1

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
			Low-order path AIS.
K27.7-	110110 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b0  Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K27.7+	-	001001 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b00, IDATA[5] = REI = 'b1  Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K28.7-	001111 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b0  Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K28.7+	-	110000 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b01, IDATA[5] = REI = 'b1  Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K29.7-	101110 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b0  Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K29.7+	-	010001 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b10, IDATA[5] = REI = 'b1  Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K30.7-	011110 1000	-	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b0  Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K30.7+	-	100001 0111	IV5='b1, IDATA[0,4] = ERDI[1:0] = 'b11, IDATA[5] = REI = 'b1  Low order path frame alignment. ERDI and REI are encoded in the V5 byte.
K23.7-	111010 1000	000101 0111	ITPL='b0  Non low-order path payload bytes.

## **10.9 Transmit Serializer**

The Transmit Serializer blocks, TWPS and TPPS, convert 8B/10B characters to bit-serial format. The Transmit Working Serializer, TWPS, generates a serial stream for the working transmit LVDS link, TPWRK/TNWRK. The Transmit Protect Serializer, TPPS, generates a serial stream for the protect transmit LVDS link, TPPROT/TNPROT.

## **10.10 LVDS Transmitters**

The LVDS Transmitters, TWLV and TPLV, convert 8B/10B encoded digital bit-serial streams to LVDS signaling levels. The Transmit Working LVDS Interface, TWLV, drives the working transmit LVDS links, TPWRK/TNWRK. The Transmit Protect LVDS Interface block, TPLV, drives the protect transmit LVDS link, TPPROT/TNPROT.

## **10.11 Clock Synthesis Unit**

The Clock Synthesis Unit, CSU, block generates the 777.6 MHz clock for the transmit and receive LVDS links.

## **10.12 Transmit Reference Generator**

The Transmit Voltage Reference Generator block generates bias voltages and currents for the LVDS Transmitters.

## **10.13 LVDS Receivers**

The LVDS Receivers, RWLV and RPLV, convert LVDS signaling levels to 8B/10B encoded digital bit-serial. The Receive Working LVDS Interface block, RWLV, connects to the working receive LVDS links, RPWRK/RNWRK. The Receive Protect LVDS Interface block, RPLV, connects to the protect receive LVDS link RPPROT/RNPROT.

## **10.14 Data Recovery Units**

The Data Recovery Units, WDRU and PDRU, monitor the receive LVDS link for transitions to determine the extent of bit cycles on the link. It then adjusts its internal timing to sample the link in the middle of the data “eye”. WDRU retrieves data from the working receive LVDS link, RPWRK/RNWRK. PDRU processes the protect receive LVDS link, RPPROT/RNPROT.

The DRU block also converts the serial stream into 10-bit words. The words are constructed from ten consecutive received bits without regard to 8B/10B character boundaries.

## 10.15 Receive 8B/10B Decoders

The Receive 8B/10B serial SBI336S Bus decoders, RW8D and RP8D, frame to the receive stream to find 8B/10B character boundaries. It also contains a FIFO to bridge between the timing domain of the receive LVDS links and the system clock timing domain. The RW8D block performs framing and elastic store functions on data retrieved from the working receive LVDS link, RPWRK/RNWRK. The RP8D block processes data on the protect receive LVDS link, RPPROT/RNPROT.

### 10.15.1 FIFO Buffer

The FIFO buffer sub-block provides isolation between the timing domain of the associated receive LVDS link and that of the system clock, SYSCLK. The FIFO also provides a retiming function to allow individual links in a multi-SBS system to have varying interconnect delay. This eases timing distribution and synchronization in large systems. Data with arbitrary alignment to 8B/10B characters are written into a 10-bit by 24-word deep FIFO at the link clock rate. Data is read from the FIFO at every SYSCLK cycle.

### 10.15.2 Serial SBI336S and TelecomBus Alignment

The alignment functionality performed by each receiver can be broken down into two parts, character alignment and frame alignment. Character alignment finds the 8B/10B character boundary in the arbitrarily aligned incoming data. Frame alignment finds SBI336S or TelecomBus frame and multiframe boundaries within the Serial link.

The character and frame alignment are expected to be robust enough for operation over a cabled interconnect.

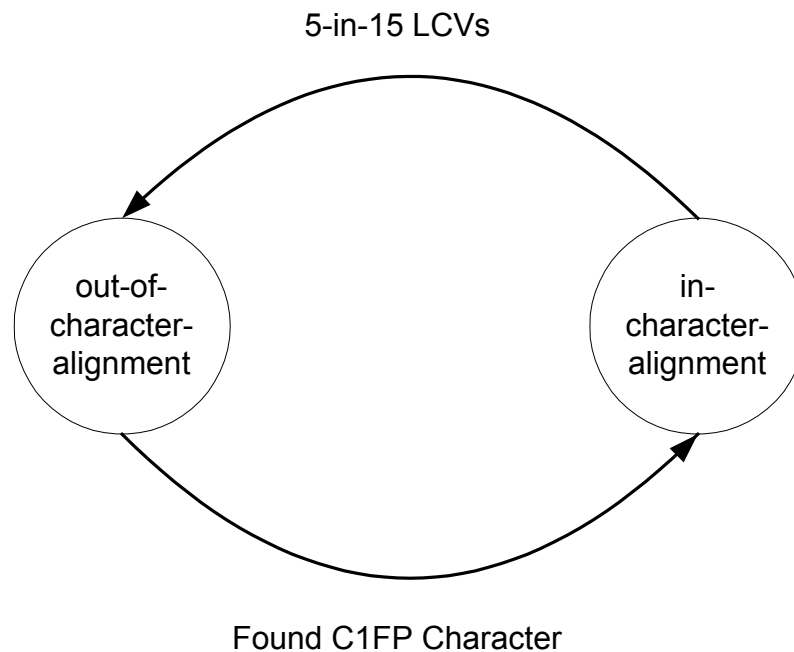
### 10.15.3 Character Alignment Block

Character alignment locates character boundaries in the incoming 8B/10B data stream. The character alignment algorithm may be in one of two states, in-character-alignment state and out-of-character-alignment state. The two states of the character alignment algorithm is shown in Figure 9.

When the character alignment state machine is in the out-of-character-alignment state, it maintains the current alignment, while searching for a C1FP character. If it finds the C1FP character it will re-align to the C1FP character and move to the in-character-alignment state. The C1FP character is found by searching for the 8B/10B C1FP character, K28.5+ or K28.5-, simultaneously in ten possible bit locations. While in the in-character-alignment state, the state machine monitors LCVs. If 5 or more LCVs are detected within a 15 character window the character alignment state machine transitions to out-of-character-alignment state. The special characters listed in Table 21 and Table 22 are ignored for LCV purposes. Upon return to in-character-alignment state the LCV count is cleared.



**Figure 9 Character Alignment State Machine**



#### 10.15.4 Frame Alignment

Frame alignment locates SBI or TelecomBus frame and multiframe boundaries in the incoming 8B/10B data stream. The frame alignment state machine may be in one of two states, in-frame-alignment state and out-of-frame-alignment state. Each SBI336S frame is 125uS in duration.

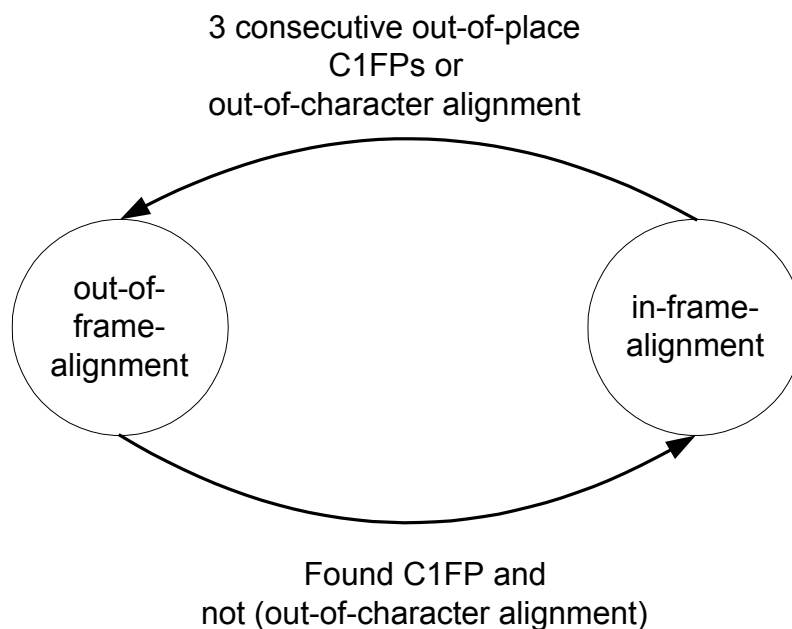
In SBI mode: Encoded over the SBI336S frame alignment is SBI336S multiframe alignment which is every four SBI336S frames or 500uS. When carrying DS0 traffic in synchronous mode, signaling multiframe alignment is also necessary and is also encoded over SBI336S alignment. Signaling multiframe alignment is every 24 frames for T1 links and every 16 frames for E1 links, therefore signaling multiframe alignment covering both T1 and E1 multiframe alignment is every 48 SBI336S frames or 6ms. Therefore C1FP characters are sent every four or every 48 frames.

In TelecomBus mode: Encoded over the serial link is the tributary multiframe alignment which is every 4 frames or 500uS. Multiframe alignment is required so that a downstream device can extract the T1 or E1 data from the tributary. The multiframe information is preserved by only sending out C1FP characters every four frames.

The frame alignment state machine establishes frame alignment over the link and is based on the frame and not the multiframe alignments. When the frame alignment state machine is in the out-of-frame-alignment state, it maintains the current alignment, while searching for a C1FP character. When it finds the C1FP character the state machine transitions to the in-frame-alignment state. While in the in-frame-alignment state the state machine monitors out-of-place C1FP characters. Out-of-place C1FP characters are identified by maintaining a frame counter based on the C1FP character. The counter is initialized by the C1FP character when in the out-of-character-alignment state, and is unaffected in the in-character-alignment state. If 3 consecutive C1FPs have been found that do not agree with the expected location as defined by the frame counter, the state will change to out-of-frame-alignment state.

The frame alignment state machine is also sensitive to character alignment. When the character alignment state machine is in the out-of-character-alignment state, the frame alignment state machine is forced out-of-alignment, and is held in that state until the character alignment state machine transitions to the in-character alignment state.

**Figure 10 Frame Alignment State Machine**



**10.15.5 SBI336S Multiframe Alignment**

SBI336S multiframe alignment is communicated across the link by controlling the frequency of the C1FP character. The most frequent transmission of the C1FP character is every four SBI336S frame times. This is the SBI336S multiframe and is used when there are no synchronous tributaries requiring signalling multiframe alignment on the SBI336S bus. When there are synchronous tributaries on the SBI336S bus the C1FP character is transmitted every 48 frame times. This is the CAS signaling multiframe and is the lowest common multiple of the 24 frame T1 multiframe and the 16 frame E1 multiframe.

The SBI336S multiframe and signaling multiframe alignment is based a free running multiframe counter that is reset with each C1FP character received. Under normal operating conditions each received C1FP character will coincide with the free running multiframe counter. SBI336S multiframe alignment is always required, SBI336S signaling multiframe alignment is optional and only required when synchronous tributaries are supported with DS0 level switching.

## **10.16 Outgoing SBI336S Tributary Translator**

The Outgoing SBI Tributary Translator block, OSTT, processes all timing information and Channel Associated Signaling information for the tributaries on the outgoing SBI Bus or buses. Input to this block is a 77 MHz SBI stream with all tributaries encoded in an internal format that closely resembles the serial SBI format.

This block is transparent in TelecomBus mode.

### **10.16.1 Outgoing SBI336S Translation**

This block translates the generic internal SBI format to the external SBI format. A control RAM keeps the current configuration of the outgoing SBI bus(es) and the tributaries carried so that it can perform the translation function.

Common to all tributaries is identification of the first C1 byte. There are unique mappings of the 8B/10B codes for the supported SBI bus link types: Asynchronous T1/E1, Synchronous (locked) T1/E1, Transparent VT1.5/VT2, DS3/E3 and Fractional rate links. Much of the identification and mapping of a link from serial SBI format is based on the OC1FP frame pulse and a tributaries location relative to that C1 reference. In addition to the OC1FP identification this block identifies multiframe alignment, valid payload, pointer movements for floating tributaries and timing control for decoding from the 8B/10B serial SBI format.

## **10.17 Outgoing SBI336 Timing Adapter**

The Outgoing SBI336 Timing Adapter, OSTA, provides a demultiplexing from a 77.76 MHz SBI336 or TelecomBus to four outgoing 19.44 MHz SBI or TelecomBuses. The outgoing timing adapter block also provides a transparent mode when the outgoing interface is already in 77.76 MHz SBI336 or TelecomBus format.

When the SBS is connected to a 19.44 MHz SBI link layer device the justification request signal, JUST\_REQ, is an output from the SBS and is aligned to the incoming bus. This block re-aligns the internal justification request signal from the internal outgoing SBI336 frame alignment to the incoming SBI frame alignment, marked by IC1FP. When the SBS is connected to a 19.44 MHz SBI physical layer device or any 77.76 MHz SBI336 device, no re-alignment of the justification request is required by this block.

## 10.18 In-band Link Controller

In order to permit centralized control of distributed NSE/SBS fabrics from the NSE microprocessor interface (for applications in which NSEs are located on fabric cards, and SBSs are located on multiple line cards), an in-band signaling channel is provided between the NSE and the SBS over the Serial interface. Each NSE can control up to 32 SBSs which are attached by the LVDS links. The NSE-SBS in-band channel is full duplex, but the NSE has active control of the link.

The SBS contains two independent In-Band Link Controllers. One ILC is connected to the Working Transmit Serial LVDS Link and the other is connected to the Protection Transmit Serial LVDS Link.

The in-band channel is carried in the first 36 columns of four rows of the SBI or TelecomBus structure, rows 3, 6, 7 and 8. The overall in-band channel capacity is thus  $36 \times 4 \times 64 \text{kb/s} = 9.216 \text{Mb/s}$ . Each 36 bytes per row allocated to the in-band signaling channel is its own in-band message between the end points. Four bytes of each 36 byte inband message are reserved for end-to-end control information and error protection, leaving  $8.192 \text{Mb/s}$  available for user data transfer between the end points.

The data transferred between the end points has no fixed format, effectively providing a clear channel for packet transfer between the attached microprocessors at each of the LVDS link terminating devices. Using the microprocessor interface, the user is able to send and receive any packet up to 32 bytes in length. The first two bytes of each 36 byte message contains a header and the last two bytes of the message is a CRC-16 which detects errors in the message.

This in-band channel is expected to be used almost entirely to carry out switching control changes in the SBSs. To configure a DS0 in an SBS device most often requires a local microprocessor to write to one memory location consisting of a 16-bit address and a 16-bit data. Using this as a baseline and assuming an efficient use of the in-band channel bandwidth we can set a maximum of  $(32 \text{bytes/row} \times 4 \text{ rows/frame} \times 8000 \text{ frames/sec} / 4 \text{ bytes/write})$  256,000 DS0 configurations per second.

Considering that configuring a T1 when switching DS0s requires 27 DS0 writes indicates that the in-band signaling channel bandwidth sets maximum limit of over 9000 T1 configurations per second. In real life these limits will not be achieved but this shows that the in-band link should not be the bottleneck. In TelecomBus mode this same configuration will require only 3 writes per T1 link.

In N+1 protected architectures it is likely that full configuration of a port card will be necessary during the switchover. This would require the entire connection memory be reconfigured. Assuming connections for overhead bytes are also reconfigured, the fastest that a complete reconfiguration can take place is  $9720 \text{ register writes}$  which equates to  $(9720 \text{ writes} \times 4 \text{ bytes/write} / (32 \text{ bytes/row} \times 4 \text{ rows/frame} \times 8000 \text{ frames/second}))$  38 milliseconds. It is also possible that the spare card could hold all the connection configurations for all the port cards it is protecting locally, for even faster switch over.

### 10.18.1 In-Band Signaling Channel Fixed Overhead

The In-Band Link Controller block generates and terminates two bytes of fixed header and a CRC-16 per every 36 byte in-band message. The two byte header provides control and status between devices at the ends of the LVDS link. The CRC-16 is calculated over the entire 34 byte in-band message and provides the terminating end the ability to detect errors in the in-band message. The format of the in-band message and header bytes is shown in Figure 11 and Figure 12.

**Figure 11 In-Band Signaling Channel Message Format**

1 byte	1 byte	32 bytes	2 bytes
Header1	Header2	Free Format Information	CRC-16

**Figure 12 In-Band Signaling Channel Header Format**

Header1							
Bit 7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit 0
Valid	Link[1:0]		Page[1:0]		User[2:0]		

Header2							
Bit 7	Bit 6	Bit 5	Bit4	Bit3	Bit2	Bit1	Bit 0
Aux[7:0]							

**Table 23 In-band Message Header Fields**

Field Name	Received by SBS	Transmitted by SBS
Valid	Message slot contains a valid message(1) or is empty(0). If empty this message will not be put into Rx Message FIFO (other header information processed as usual)	Message slot contains a valid message(1) or is empty(0). The header and CRC bytes are transmitted regardless of the state of this bit.
Link[1:0]#	Each bit indicates which Link to use, working(0) or Protect(1). Other algorithms are possible in indicate Working or Protect over these 2 bits.	Each bit shows current Link in use, working(0) or Protect(1). Other algorithms are possible in indicate Working or Protect over these 2 bits.  These bits are transmitted immediately.
Page[1:0]#	Each bit indicates which configuration page to use, page (1) or page (0) for the corresponding MSU. Page[1] controls the IMSU configuration page and Page[0] controls the OMSU configuration page.	Each bit shows current control page in use, page (1) or page (0) for the corresponding MSU. Page[1] indicates the IMSU configuration page and Page[0] indicates the OMSU configuration page  Only transmitted from the beginning of the first message of the frame
User[2:0]#	User defined bits which may be read through the microprocessor interface. User[2] is also output from the SBS on the OUSER2 pin.	User defined bits. User[2] is sourced from the IUSER2 input to the SBS. User[1:0] are sourced from an internal register.

		Transmitted immediately.
Aux[7:0]#	User defined auxiliary register indication.	User defined auxiliary register indication. Transmitted immediately.

#Change in these bits (received side) will not be processed if the received message CRC-16 indicates an error.

Interrupts can be generated when CRC errors are detected or the USER or LINK bits change state. There is no inherent flow control provided by the In-Band Link Controller. The attached microprocessor is able to provide flow control via interrupts when the in-band message fifo overflows and via the USER bits in the header.

As each message arrives, the CRC-16 and valid bit is checked; if the valid bit is not set the message is discarded, if it fails the CRC check it is flagged as being in error and an interrupt is generated if enabled. If the CRC-16 is OK, regardless of the valid bit, the Page Link, User and Aux bits are passed on immediately. If the fifo erroneously overflows, an interrupt is generated.

## 10.19 Microprocessor Interface

The Microprocessor Interface block provides normal and test mode registers, and logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance testability of the SBS.

Address	Register
000H	SBS Master Reset
001H	SBS Master Configuration
002H	SBS Revision/Part Number
003H	SBS Part Number/Manufacturer ID
004H	SBS Master Bypass
005H	SBS Master SPE Control #1
006H	SBS Master SPE Control #2
007H	SBS Receive Synchronization Delay
008H	SBS In-Band Link User Bits
009H	SBS Receive Configuration
00AH	SBS Transmit Configuration
00BH	SBS Transmit J1 Configuration
00CH	SBS Transmit V1 Configuration
00DH	SBS Transmit H1-H2 Pointer Value
00EH	SBS Transmit Alternate H1-H2 Pointer Value
00FH	SBS Transmit H1-H2 Pointer Selection
010H	SBS Master Interrupt Source
011H	SBS Interrupt Register
012H	SBS Interrupt Enable Register
013H	SBS Loopback Configuration

<b>Address</b>	<b>Register</b>
014H	SBS Master Clock Monitor #1, Accumulation Trigger
015H	SBS Master Clock Monitor #2
016H	SBS Master Interrupt Enable Register
017H	SBS Free User Register
020H	ISTA Incoming Parity Configuration
021H	ISTA Incoming Parity Status
022H	ISTA TelecomBus Configuration
023H	ISTA Reserved
024H – 027H	Reserved
028H	IMSU Configuration
029H	IMSU Interrupt Status and Memory Page Update
02AH	IMSU Indirect Time Switch Address
02BH	IMSU Indirect Time Switch Data
02CH – 02FH	Reserved
030H	ICASM CAS Enable Indirect Address
031H	ICASM CAS Enable Indirect Control
032H	ICASM CAS Enable Indirect Data
033H	ICASM Reserved
034H – 037H	Reserved
038H	ISTT Control RAM Indirect Access Address Register
039H	ISTT Control RAM Indirect Access Control Register
03AH	ISTT Control RAM Indirect Access Data Register
03BH	Reserved
03CH – 03FH	Reserved
040H	OSTT Control RAM Indirect Access Address Register
041H	OSTT Control RAM Indirect Access Control Register
042H	OSTT Control RAM Indirect Access Data Register
043H	Reserved
044H – 047H	Reserved
048H	OMSU Configuration
049H	OMSU Interrupt Status and Memory Page Update
04AH	OMSU Indirect Time Switch Address
04BH	OMSU Indirect Time Switch Data
04CH – 04FH	Reserved
050H	OCASM Indirect Address
051H	OCASM Indirect Control
052H	OCASM Indirect Data
053H	OCASM Reserved
054H – 05FH	Reserved
060H	OSTA Outgoing Configuration and Parity

<b>Address</b>	<b>Register</b>
061H	OSTA Outgoing J1 Configuration
062H	OSTA Outgoing V1 Configuration
063H	OSTA H1-H2 Pointer Value
064H	OSTA Alternate H1-H2 Pointer Value
065H	OSTA H1-H2 Pointer Selection
066H	OSTA Output Enable Indirect Access Address
067H	OSTA Output Enable Indirect Access Control
068H	OSTA Output Enable Indirect Access Data
069H – 06FH	OSTA Reserved
070H	WPP Indirect Address
071H	WPP Indirect Data
072H	WPP Generator Payload Configuration
073H	WPP Monitor Payload Configuration
074H	WPP Monitor Byte Error Interrupt Status
075H	WPP Monitor Byte Error Interrupt Enable
076H	Reserved
077H	Reserved
078H	Reserved
079H	WPP Monitor Synchronization Interrupt Status
07AH	WPP Monitor Synchronization Interrupt Enable
07BH	WPP Monitor Synchronization State
07CH	WPP Performance Counters Transfer Trigger
07DH – 07FH	WPP Reserved
080H	PPP Indirect Address
081H	PPP Indirect Data
082H	PPP Generator Payload Configuration
083H	PPP Monitor Payload Configuration
084H	PPP Monitor Byte Error Interrupt Status
085H	PPP Monitor Byte Error Interrupt Enable
086H	Reserved
087H	Reserved
088H	Reserved
089H	PPP Monitor Synchronization Interrupt Status
08AH	PPP Monitor Synchronization Interrupt Enable
08BH	PPP Monitor Synchronization State
08CH	PPP Performance Counters Transfer Trigger
08DH – 08FH	PPP Reserved
090H	WILC Transmit Message FIFO Data High
091H	WILC Transmit Message FIFO Data Low
092H	WILC Reserved



<b>Address</b>	<b>Register</b>
093H	WILC Transmit Control
094H	WILC Reserved
095H	WILC Transmit Status and FIFO Synch
096H	WILC Receive Message FIFO Data High
097H	WILC Receive Message FIFO Data Low
098H	WILC Reserved
099H	WILC Receive Control
09AH	WILC Receive Auxiliary
09BH	WILC Receive Status and FIFO Synch
09CH	WILC Reserved
09DH	WILC Interrupt Enable and Control
09EH	WILC Reserved
09FH	WILC Interrupt Reason
0A0H	PILC Transmit Message FIFO Data High
0A1H	PILC Transmit Message FIFO Data Low
0A2H	PILC Reserved
0A3H	PILC Transmit Control
0A4H	PILC Reserved
0A5H	PILC Transmit Status and FIFO Synch
0A6H	PILC Receive Message FIFO Data High
0A7H	PILC Receive Message FIFO Data Low
0A8H	PILC Reserved
0A9H	PILC Receive Control
0AAH	PILC Receive Auxiliary
0ABH	PILC Receive Status and FIFO Synch
0ACH	PILC Reserved
0ADH	PILC Interrupt Enable and Control
0AEH	PILC Reserved
0AFH	PILC Interrupt Reason
0B0H	TW8E Control and Status
0B1H	TW8E Interrupt Status
0B2H	TW8E Time-slot Configuration #1
0B3H	TW8E Time-slot Configuration #2
0B4H	TW8E Test Pattern
0B5H	TW8E Analog Control
0B6H – 0B7H	TW8E Reserved
0B8H	TP8E Control and Status
0B9H	TP8E Interrupt Status
0BAH	TP8E Time-slot Configuration #1
0BBH	TP8E Time-slot Configuration #2

<b>Address</b>	<b>Register</b>
0BCH	TP8E Test Pattern
0BDH	TP8E Analog Control
0BEH – 0BFH	TP8E Reserved
0C0H	RW8D Control and Status
0C1H	RW8D Interrupt Status
0C2H	RW8D Line Code Violation Count
0C3H	RW8D Analog Control #1
0C4H – 0C7H	RW8D Reserved
0C8H	RP8D Control and Status
0C9H	RP8D Interrupt Status
0CAH	RP8D Line Code Violation Count
0CBH	RP8D Analog Control
0CCH – 0CFH	RP8D Reserved
0D0H	CSTR Control
0D1H	CSTR Interrupt Enable and Status
0D2H	CSTR Interrupt Indication
0D3H	CSTR Reserved
0D4H – 0DFH	Reserved
0E0H	REFDLL Configuration
0E1H	REFDLL Reserved
0E2H	REFDLL Reserved
0E3H	REFDLL Control Status
0E4H – 0E7H	Reserved
0E8H	SYSDLL Configuration
0E9H	SYSDLL Reserved
0EAH	SYSDLL Reserved
0EBH	SYSDLL Control Status
0ECH – 0FFH	Reserved
100H	SBS Master Test
101H – 1FFH	Reserved for Test

**Note**

1. For all register accesses, CSB must be set low.

## 11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the SBS. Normal mode registers (as opposed to test mode registers) are selected when A[8] is set low.

### **Notes on Normal Mode Register Bits:**

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.
2. All configuration bits that can be written into can also be read back. This allows the processor controlling the TSB to determine the programming state of the block.
3. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.
4. Writing into read-only normal mode register bit locations does not affect SBS operation unless otherwise noted.

**Register 000H: SBS Master Reset**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ARESET	0
Bit 0	R/W	DRESET	0

**Reserved**

These bits must be set low for proper operation of the SBS.

**ARESET**

The analogue reset bit (ARESET) allows the analogue circuitry in the SBS to be reset and disabled under software control. When the ARESET bit is set high, all SBS analogue circuitry is held in reset and disabled. This bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset and enable it. Holding SBS in analogue reset state places it into a low power, disabled mode. A hardware reset clears the ARESET bit, thus negating the analogue software reset.

**DRESET**

The digital reset bit (DRESET) allows the digital circuitry in the SBS to be reset under software control. When the DRESET bit is set high, all SBS digital circuitry is held in reset with the exception of this register. This bit is not self-clearing. Therefore, it must be set low to bring the affected circuitry out of reset. Holding SBS in digital reset state places it into a low power, digital stand-by mode. A hardware reset clears the DRESET bit, thus negating the digital software reset.

**Register 001H: SBS Master Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14	R/W	ICMP_SRC[1]	0
Bit 13	R/W	ICMP_SRC[0]	0
Bit 12	R/W	ICMP_VAL	0
Bit 11		Unused	0
Bit 10	R/W	OCMP_SRC[1]	0
Bit 9	R/W	OCMP_SRC[0]	0
Bit 8	R/W	OCMP_VAL	0
Bit 7	R/W	RWSEL_SRC	0
Bit 6	R/W	RWSEL_VAL	1
Bit 5	R/W	PARALLEL_MODE	0
Bit 4	R/W	COLUMN_MODE	0
Bit 3	R/W	PHY_SBI	1
Bit 2	R/W	MF_48	0
Bit 1	R/W	TELECOM_BUS	0
Bit 0	R/W	19M_BUS	0

**ICMP\_SRC[1:0]**

The ICMP\_SRC[1:0] bits select the source for the incoming connection memory page information.

ICMP_SRC[1:0]	Source
00	ICMP_VAL register bit
01	ICMP input pin
10	PAGE bit from the active ILC (as determined by the RWSEL_VAL bit or RWSEL input)
11	Reserved

**ICMP\_VAL**

The ICMP\_VAL bit controls the selection of the connection memory page in each Incoming Memory Switch Unit, IMSU. When ICMP\_VAL is a logic one, connection memory page 1 is selected. When ICMP\_VAL is a logic zero, connection memory page 0 is selected. ICMP\_VAL is sampled at the C1 byte position as defined by the incoming frame pulse signal (IC1FP). Changes to the connection memory page selection are synchronized to the frame boundary of the next frame (in TelecomBus mode), 4 frame multiframe (in SBI mode without CAS), or 48 frame multiframe (in SBI mode with CAS). This bit is only used when ICMP\_SRC[1:0] = 'b00.

### OCMP\_SRC[1:0]

The OCMP\_SRC[1:0] bits select the source for the outgoing connection memory page information.

<b>OCMP_SRC[1:0]</b>	<b>Source</b>
00	OCMP_VAL register bit
01	OCMP input pin
10	PAGE bit from the active ILC (as determined by the RWSEL_VAL bit or RWSEL input)
11	Reserved

### OCMP\_VAL

The OCMP\_VAL bit controls the selection of the connection memory page in each Outgoing Memory Switch Unit, OMSU. When OCMP\_VAL is a logic one, connection memory page 1 is selected. When OCMP\_VAL is a logic zero, connection memory page 0 is selected. OCMP\_VAL is sampled at the C1 byte position as defined by the receive frame pulse signal (RC1FP). Changes to the connection memory page selection are synchronized to the frame boundary of the next frame (in TelecomBus mode), 4 frame multiframe (in SBI mode without CAS), or 48 frame multiframe (in SBI mode with CAS). This bit is only used when OCMP\_SRC[1:0] = 'b00.

### RWSEL\_SRC

The RWSEL\_SRC bit selects the source for the selection of which link, the working or the protect, is active. When RWSEL\_SRC is a logic zero, the RWSEL\_VAL register bit is used as the source for selecting the active link. When RWSEL\_SRC is a logic one, the RWSEL input is used as the source for selecting the active link.

### RWSEL\_VAL

The RWSEL\_VAL bit selects between the receive working and protect links when the RWSEL\_SRC is a logic zero. When RWSEL\_VAL is a logic one, the working link is selected and the SBS listens to the data from the RPWRK and RNWRK inputs. When RWSEL\_VAL is a logic zero, the protect link is selected and the SBS listens to the data from the RPPROT and RNPROT inputs. This bit has no effect when the RWSEL\_SRC bit is a logic one or when the parallel interface is used (PARALLEL\_MODE = 'b1).

### PARALLEL\_MODE

The PARALLEL\_MODE bit selects between the parallel bus or the serial LVDS links on the transmit and receive interfaces. When PARALLEL\_MODE is set to a logic one, parallel mode is enabled. When PARALLEL\_MODE is set to a logic zero, the serial LVDS mode is enabled.

## COLUMN\_MODE

The COLUMN\_MODE bit selects between column switching and DS0 switching. When COLUMN\_MODE is set to a logic one, column switching is enabled and the SBS is configured to switch columns within the SBI336 or TelecomBus. When COLUMN\_MODE is set to a logic zero, DS0 switching is enabled and the SBS is configured to switch DS0's within the SBI336 bus. DS0 switching is not permitted in TelecomBus mode.

## PHY\_SBI

The PHY\_SBI bit configures the direction of the JUST\_REQ[4:1] input/output signals on the incoming and outgoing buses. When PHY\_SBI is set to a logic one, the SBS is configured to be connected to a PHY device and the JUST\_REQ[4:1] signal is an input. When PHY\_SBI is set to a logic zero, the SBS is configured to be connected to a Link layer device and the JUST\_REQ[4:1] signal is an output.

## MF\_48

The MF\_48 bit selects between 4 frame multiframe mode or 48 frame multiframe mode on the SBI336 bus. When MF\_48 is a logic one, 48 frame mode is selected. IC1FP is expected once every 48 frames and OC1FP is output every 48 frames, indicating CAS signaling multiframe alignment. When MF\_48 is a logic zero, 4 frame mode is selected. IC1FP is expected once every 4 frames and OC1FP is output every 4 frames. This bit has no effect when in TelecomBus mode (TELECOM\_BUS = 'b1).

## TELECOM\_BUS

The TELECOM\_BUS bit selects between TelecomBus and SBI bus modes on the incoming and outgoing buses. When TELECOM\_BUS is set to a logic one, TelecomBus mode is selected and all frame pulses must mark C1J1V1 positions. When TELECOM\_BUS is set to a logic zero, SBI bus mode is selected and the all frame pulses only mark the C1 position.

## 19M\_BUS

The 19M\_BUS bit selects between 19 MHz and 77 MHz mode on the incoming and outgoing buses. When 19M\_BUS is set to a logic zero, 19 MHz mode is selected and 4 separate 19 MHz buses are used. When 19M\_BUS is set to a logic one, 77 MHz mode is selected and a single 77 MHz bus is used.

**Register 002H: SBS Version/Part Number**

Bit	Type	Function	Default
Bit 15	R	VERSION[3]	0
Bit 14	R	VERSION[2]	0
Bit 13	R	VERSION[1]	0
Bit 12	R	VERSION[0]	0
Bit 11	R	PART_NUMBER[15]	1
Bit 10	R	PART_NUMBER[14]	0
Bit 9	R	PART_NUMBER[13]	0
Bit 8	R	PART_NUMBER[12]	0
Bit 7	R	PART_NUMBER[11]	0
Bit 6	R	PART_NUMBER[10]	1
Bit 5	R	PART_NUMBER[9]	1
Bit 4	R	PART_NUMBER[8]	0
Bit 3	R	PART_NUMBER[7]	0
Bit 2	R	PART_NUMBER[6]	0
Bit 1	R	PART_NUMBER[5]	0
Bit 0	R	PART_NUMBER[4]	1

VERSION[3:0]

The VERSION[3:0] bits report the binary revision number of the SBS silicon.

PART\_NUMBER[15:4]

The PART NUMBER[15:4] bits represent the 12 most significant bits of the part number of the SBS device.



**Register 003H: SBS Part Number/Manufacturer ID**

Bit	Type	Function	Default
Bit 15	R	PART_NUMBER[3]	0
Bit 14	R	PART_NUMBER[2]	0
Bit 13	R	PART_NUMBER[1]	0
Bit 12	R	PART_NUMBER[0]	0
Bit 11	R	MANUFACTURER_ID[10]	0
Bit 10	R	MANUFACTURER_ID[9]	0
Bit 9	R	MANUFACTURER_ID[8]	0
Bit 8	R	MANUFACTURER_ID[7]	0
Bit 7	R	MANUFACTURER_ID[6]	1
Bit 6	R	MANUFACTURER_ID[5]	1
Bit 5	R	MANUFACTURER_ID[4]	0
Bit 4	R	MANUFACTURER_ID[3]	0
Bit 3	R	MANUFACTURER_ID[2]	1
Bit 2	R	MANUFACTURER_ID[1]	1
Bit 1	R	MANUFACTURER_ID[0]	0
Bit 0	R	JID	1

**PART\_NUMBER[3:0]**

The PART\_NUMBER[3:0] bits represent the 4 least significant bits of the part number of the SBS device.

**MANUFACTURER\_ID[10:0]**

The MANUFACTURER\_ID[10:0] bits represent the 11 bit manufacturer's code assigned to PMC-Sierra, Inc. for inclusion in the JTAG Boundary Scan Identification Code. For more information on JTAG Boundary Scan, refer to Section 12.

**JID**

The JID bit is bit 0 in the JTAG identification code.

**Register 004H: SBS Master Bypass Register**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5	R/W	IMSU_BYPASS	0
Bit 4	R/W	ICASE_BYPASS	0
Bit 3	R/W	ICASM_BYPASS	0
Bit 2	R/W	OMSU_BYPASS	0
Bit 1	R/W	OCASE_BYPASS	0
Bit 0	R/W	OCASM_BYPASS	0

**IMSU\_BYPASS**

The IMSU\_BYPASS bit is used to bypass the functionality of the IMSU block. When IMSU\_BYPASS is a logic one, the incoming memory switch is bypassed and the incoming data bus is passed to the transmit data bus unmodified. This eliminates the one frame delay through the IMSU and places the IMSU in a low power mode. When IMSU\_BYPASS is a logic zero, the IMSU is not bypassed and must be configured.

**ICASE\_BYPASS**

The ICASE\_BYPASS bit is used to bypass the functionality of the ICASE block. When ICASE\_BYPASS is a logic one, the incoming CAS extractor is bypassed and the CAS bits are not extracted from the SBI336 bus. This places the ICASE block in a low power mode. When ICASE\_BYPASS is a logic zero, the ICASE is not bypassed and the CAS bits are extracted from the SBI336 bus.

**ICASM\_BYPASS**

The ICASM\_BYPASS bit is used to bypass the functionality of the ICASM block. When ICASM\_BYPASS is a logic one, the incoming CAS merge block is bypassed and the CAS bits are not inserted into the SBI336 bus. This places the ICASM block in a low power mode. When ICASM\_BYPASS is a logic zero, the ICASM is not bypassed and the CAS bits are inserted into the SBI336 bus.

### OMSU\_BYPASS

The OMSU\_BYPASS bit is used to bypass the functionality of the OMSU block. When OMSU\_BYPASS is a logic one, the outgoing memory switch is bypassed and the receive data bus is passed to the outgoing data bus unmodified. This eliminates the one frame delay through the OMSU and places the OMSU in a low power mode. When OMSU\_BYPASS is a logic zero, the OMSU is not bypassed and must be configured.

### OCASE\_BYPASS

The OCASE\_BYPASS bit is used to bypass the functionality of the OCASE block. When OCASE\_BYPASS is a logic one, the transmit CAS extractor is bypassed and the CAS bits are not extracted from the SBI336 bus. This places the OCASE block in a low power mode. When OCASE\_BYPASS is a logic zero, the OCASE is not bypassed and the CAS bits are extracted from the SBI336 bus.

### OCASM\_BYPASS

The OCASM\_BYPASS bit is used to bypass the functionality of the OCASM block. When OCASM\_BYPASS is a logic one, the transmit CAS merge block is bypassed and the CAS bits are not inserted into the SBI336 bus. This places the OCASM block in a low power mode. When OCASM\_BYPASS is a logic zero, the OCASM is not bypassed and the CAS bits are inserted into the SBI336 bus.

**Register 005H: SBS Master SPE Control #1**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7	R/W	SBI4_SPE3_TYP[1]	0
Bit 6	R/W	SBI4_SPE3_TYP[0]	0
Bit 5	R/W	SBI3_SPE3_TYP[1]	0
Bit 4	R/W	SBI3_SPE3_TYP[0]	0
Bit 3	R/W	SBI2_SPE3_TYP[1]	0
Bit 2	R/W	SBI2_SPE3_TYP[0]	0
Bit 1	R/W	SBI1_SPE3_TYP[1]	0
Bit 0	R/W	SBI1_SPE3_TYP[0]	0

**Register 006H: SBS Master SPE Control #2**

Bit	Type	Function	Default
Bit 15	R/W	SBI4_SPE2_TYP[1]	0
Bit 14	R/W	SBI4_SPE2_TYP[0]	0
Bit 13	R/W	SBI3_SPE2_TYP[1]	0
Bit 12	R/W	SBI3_SPE2_TYP[0]	0
Bit 11	R/W	SBI2_SPE2_TYP[1]	0
Bit 10	R/W	SBI2_SPE2_TYP[0]	0
Bit 9	R/W	SBI1_SPE2_TYP[1]	0
Bit 8	R/W	SBI1_SPE2_TYP[0]	0
Bit 7	R/W	SBI4_SPE1_TYP[1]	0
Bit 6	R/W	SBI4_SPE1_TYP[0]	0
Bit 5	R/W	SBI3_SPE1_TYP[1]	0
Bit 4	R/W	SBI3_SPE1_TYP[0]	0
Bit 3	R/W	SBI2_SPE1_TYP[1]	0
Bit 2	R/W	SBI2_SPE1_TYP[0]	0
Bit 1	R/W	SBI1_SPE1_TYP[1]	0
Bit 0	R/W	SBI1_SPE1_TYP[0]	0

**SBIx\_SPEy\_TYP[1:0]**

The SBIx\_SPEy\_TYP[1:0] bits select the SPE type for the specified SPE within the specified SBI bus. The types for each SPE are independently configured with possible types being T1, E1, DS3/E3 and fractional rate links. These bits only have an effect when in SBI mode (TELECOM\_BUS = 'b0 in the SBS Master Configuration Register). The setting for SBIx\_SPEy\_TYP[1:0] are:

SBIx_SPEy_TYP[1:0]	Payload Type
00	T1
01	E1
10	DS3/E3
11	Fractional Rate

**Register 007H: SBS Receive Synchronization Delay**

Bit	Type	Function	Default
Bit 15	R	TIP	0
Bit 14		Unused	0
Bit 13	R/W	RC1FPDLY[13]	0
Bit 12	R/W	RC1FPDLY[12]	0
Bit 11	R/W	RC1FPDLY[11]	0
Bit 10	R/W	RC1FPDLY[10]	0
Bit 9	R/W	RC1FPDLY[9]	0
Bit 8	R/W	RC1FPDLY[8]	0
Bit 7	R/W	RC1FPDLY[7]	0
Bit 6	R/W	RC1FPDLY[6]	0
Bit 5	R/W	RC1FPDLY[5]	0
Bit 4	R/W	RC1FPDLY[4]	0
Bit 3	R/W	RC1FPDLY[3]	0
Bit 2	R/W	RC1FPDLY[2]	0
Bit 1	R/W	RC1FPDLY[1]	0
Bit 0	R/W	RC1FPDLY[0]	0

**TIP**

The transfer in progress bit (TIP) reports the status of latching performance monitor counting into holding registers. TIP is set high when a transfer is initiated by a write access to the SBS Master Signal Monitor #1, Accumulation Trigger Register (014H). It is set low when all the counters in the SBS have transferred their values to holding registers. The updated counts are now available for reading at the designated registers.

**RC1FPDLY[13:0]**

The receive transport frame delay bits (RC1FPDLY[13:0]) controls the delay, in SYSCLK cycles, inserted by the SBS before processing the C1 characters delivered by the receive serial data links. RC1FPDLY should be set such that after the specified delay the active receive link should have delivered the C1 character. The relationships between RC1FP, RC1FPDLY and the receive serial links is described in the Functional Timing section.

**Register 008H: SBS In-Bank Link User Bits**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3	R/W	TXWUSER[1]	0
Bit 2	R/W	TXWUSER[0]	0
Bit 1	R/W	TXPUSER[1]	0
Bit 0	R/W	TXPUSER[0]	0

**TXWUSER[1:0]**

The Transmit Working USER bits (TXWUSER[1:0]) contain the values to be inserted in the USER[1:0] bits in the header of the working in-band signaling channel.

**TXPUSER[1:0]**

The Transmit Protection USER bits (TXWUSER[1:0]) contain the values to be inserted in the USER[1:0] bits in the header of the protection in-band signaling channel.

**Register 009H: SBS Receive Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8	R/W	RLOCK0	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2	R/W	INCLRC1	0
Bit 1	R/W	INCLRPL	0
Bit 0	R/W	ROP	0

**RLOCK0**

The RLOCK0 bit controls the position of the J1 byte in the Receive TelecomBus. When RLOCK0 is a logic one, the J1 byte is expected to be locked to an offset of 0 (the byte following H3). When RLOCK0 is a logic zero, the J1 byte is expected to be locked to an offset of 522 (the byte following C1). This bit is used to determine where to sample RC1FP in order to find the byte following J1 which will indicate multiframe alignment. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBS Master Configuration Register).

**INCLRPL**

The INCLRPL bit controls whether the RPL input signal participates in the receive parity calculations. When INCLRPL is set to a logic one, the parity calculation includes the RPL input. When INCLRPL is set to a logic zero, parity is calculated without regard to the state of RPL. This bit only takes effect when in TelecomBus mode.

**INCLRC1**

The INCLRC1 bit controls whether the RC1FP input signal participates in the receive parity calculations. When INCLRC1 is set to a logic one, the parity calculation includes the RC1FP input. When INCLRC1 is set to a logic zero, parity is calculated without regard to the state of RC1FP. This bit only takes effect when in TelecomBus mode.



## ROP

The receive odd parity bit (ROP) controls the expected parity on the receive bus. When ROP is set to a logic one, the expected parity on the RDP input is odd. When ROP is set to a logic zero, the parity is even. In SBI bus mode, the parity calculation encompasses the RDATA[7:0], RPL and RV5 signals. In TelecomBus mode, the parity calculation encompasses the RDATA[7:0] and optionally RPL and RC1FP as determined by the INCLRPL and INCLRC1 bits.

**Register 00AH: SBS Transmit Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8	R/W	TLOCK0	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2	R/W	INCLTC1	0
Bit 1	R/W	INCLTPL	0
Bit 0	R/W	TOP	0

**TLOCK0**

The TLOCK0 bit controls the position of the J1 byte in the Transmit TelecomBus. When TLOCK0 is a logic one, the J1 byte is expected to be locked to an offset of 0 (the byte following H3). When TLOCK0 is a logic zero, the J1 byte is expected to be locked to an offset of 522 (the byte following C1). This bit is used to determine where to pulse the TC1FP output when any part of STS1\_TJ1EN[12:1] or STS1\_TV1EN[12:1] are set. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBS Master Configuration Register).

**INCLTC1**

The INCLTC1 bit controls whether the TC1FP output signal participates in the transmit parity calculations. When INCLTC1 is set to a logic one, the parity calculation includes the TC1FP output. When INCLTC1 is set to a logic zero, parity is calculated without regard to the state of TC1FP. This bit only take effect when in TelecomBus mode.

**INCLTPL**

The INCLTPL bit controls whether the TPL output signal participates in the transmit parity calculations. When INCLTPL is set to a logic one, the parity calculation includes the TPL output. When INCLTPL is set to a logic zero, parity is calculated without regard to the state of TPL. This bit only takes effect when in TelecomBus mode.

## TOP

The transmit odd parity bit (TOP) controls the parity generated on the transmit bus. When TOP is set to a logic one, the parity on the TDP output is odd. When TOP is set to a logic zero, the parity is even. In SBI bus mode, the parity calculation encompasses the TDATA[7:0], TPL and TV5 signals. In TelecomBus mode, the parity calculation encompasses the TDATA[7:0] and optionally TPL and TC1FP as determined by the INCLTPL and INCLTC1 bits.

**Register 00BH: SBS Transmit J1 Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_TJ1EN[12]	0
Bit 10	R/W	STS1_TJ1EN[11]	0
Bit 9	R/W	STS1_TJ1EN[10]	0
Bit 8	R/W	STS1_TJ1EN[9]	0
Bit 7	R/W	STS1_TJ1EN[8]	0
Bit 6	R/W	STS1_TJ1EN[7]	0
Bit 5	R/W	STS1_TJ1EN[6]	0
Bit 4	R/W	STS1_TJ1EN[5]	0
Bit 3	R/W	STS1_TJ1EN[4]	0
Bit 2	R/W	STS1_TJ1EN[3]	0
Bit 1	R/W	STS1_TJ1EN[2]	0
Bit 0	R/W	STS1_TJ1EN[1]	0

**STS1\_TJ1EN[12:1]**

The STS1\_TJ1EN[12:1] bit controls the inclusion of the J1 byte identification on the TC1FP output for each of the 12 STS-1's. When STS1\_TJ1EN[x] is a logic one, the TC1FP output will pulse high during the J1 byte position of the associated STS-1 along with the usual C1 byte position. The position of the J1 byte relative to the C1 position is determined by the TLOCK0 bit. When STS1\_TJ1EN[x] is a logic zero, the TC1FP will not pulse high during the J1 byte position of the associated STS-1. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBS Master Configuration Register).

**Register 00CH: SBS Transmit V1 Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_TV1EN[12]	0
Bit 10	R/W	STS1_TV1EN[11]	0
Bit 9	R/W	STS1_TV1EN[10]	0
Bit 8	R/W	STS1_TV1EN[9]	0
Bit 7	R/W	STS1_TV1EN[8]	0
Bit 6	R/W	STS1_TV1EN[7]	0
Bit 5	R/W	STS1_TV1EN[6]	0
Bit 4	R/W	STS1_TV1EN[5]	0
Bit 3	R/W	STS1_TV1EN[4]	0
Bit 2	R/W	STS1_TV1EN[3]	0
Bit 1	R/W	STS1_TV1EN[2]	0
Bit 0	R/W	STS1_TV1EN[1]	0

**STS1\_TV1EN[12:1]**

The STS1\_TV1EN[12:1] bit controls the inclusion of the byte following J1 identification on the TC1FP output for each of the 12 STS-1's. When STS1\_TV1EN[x] is a logic one, the TC1FP output will pulse high during the byte following the J1 position of the associated STS-1 along with the usual C1 byte position. The position of the J1 byte relative to the C1 position is determined by the TLOCK0 bit. When STS1\_TV1EN is a logic zero, the TC1FP will not pulse high during the byte following the J1 position of the associated STS-1. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBS Master Configuration Register).

**Register 00DH: SBS Transmit H1-H2 Pointer Value**

Bit	Type	Function	Default
Bit 15	R/W	H1[7]	0
Bit 14	R/W	H1[6]	0
Bit 13	R/W	H1[5]	0
Bit 12	R/W	H1[4]	0
Bit 11	R/W	H1[3]	0
Bit 10	R/W	H1[2]	0
Bit 9	R/W	H1[1]	0
Bit 8	R/W	H1[0]	0
Bit 7	R/W	H2[7]	0
Bit 6	R/W	H2[6]	0
Bit 5	R/W	H2[5]	0
Bit 4	R/W	H2[4]	0
Bit 3	R/W	H2[3]	0
Bit 2	R/W	H2[2]	0
Bit 1	R/W	H2[1]	0
Bit 0	R/W	H2[0]	0

**H1[7:0]**

The H1[7:0] bits contain the value to be output during the H1 position of the transport overhead of the Transmit TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic zero and the H1H2EN bit is set high. These bits have no effect when H1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**H2[7:0]**

The H2[7:0] bits contain the value to be output during the H2 position of the transport overhead of the Transmit TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic zero and the H1H2EN bit is set high. These bits have no effect when H1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**Register 00EH: SBS Transmit Alternate H1-H2 Pointer Value**

Bit	Type	Function	Default
Bit 15	R/W	H1_ALT[7]	0
Bit 14	R/W	H1_ALT[6]	0
Bit 13	R/W	H1_ALT[5]	0
Bit 12	R/W	H1_ALT[4]	0
Bit 11	R/W	H1_ALT[3]	0
Bit 10	R/W	H1_ALT[2]	0
Bit 9	R/W	H1_ALT[1]	0
Bit 8	R/W	H1_ALT[0]	0
Bit 7	R/W	H2_ALT[7]	0
Bit 6	R/W	H2_ALT[6]	0
Bit 5	R/W	H2_ALT[5]	0
Bit 4	R/W	H2_ALT[4]	0
Bit 3	R/W	H2_ALT[3]	0
Bit 2	R/W	H2_ALT[2]	0
Bit 1	R/W	H2_ALT[1]	0
Bit 0	R/W	H2_ALT[0]	0

**H1\_ALT[7:0]**

The H1\_ALT[7:0] bits contain the value to be output during the H1 position of the transport overhead of the Transmit TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic one and the H1H2EN bit is set high. These bits have no effect when H1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**H2\_ALT[7:0]**

The H2\_ALT[7:0] bits contain the value to be output during the H2 position of the transport overhead of the Transmit TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic one and the H1H2EN bit is set high. These bits have no effect when H1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**Register 00FH: SBS Transmit H1-H2 Pointer Selection**

Bit	Type	Function	Default
Bit 15	R/W	H1H2EN	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_PTR_SEL[12]	0
Bit 10	R/W	STS1_PTR_SEL[11]	0
Bit 9	R/W	STS1_PTR_SEL[10]	0
Bit 8	R/W	STS1_PTR_SEL[9]	0
Bit 7	R/W	STS1_PTR_SEL[8]	0
Bit 6	R/W	STS1_PTR_SEL[7]	0
Bit 5	R/W	STS1_PTR_SEL[6]	0
Bit 4	R/W	STS1_PTR_SEL[5]	0
Bit 3	R/W	STS1_PTR_SEL[4]	0
Bit 2	R/W	STS1_PTR_SEL[3]	0
Bit 1	R/W	STS1_PTR_SEL[2]	0
Bit 0	R/W	STS1_PTR_SEL[1]	0

**H1H2EN**

The H1H2EN bit enables the insertion of the H1 and H2 bytes in the transport overhead. When H1H2EN is a logic one, the values in the internal registers is inserted into the H1 and H2 bytes of the Transmit TelecomBus according to the STS1\_PTR\_SEL[12:1] bits. When H1H2EN is a logic zero, the values from the internal registers is not inserted into the H1 and H2 bytes. This bit has no effect when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**STS1\_PTR\_SEL[12:1]**

The STS1\_PTR\_SEL[12:1] bits select which of the two H1-H2 Pointer registers is used for each of the 12 STS-1's output on the Transmit TelecomBus when the H1H2EN bit is set. When STS1\_PTR\_SEL[x] is a logic zero, the SBS Transmit H1-H2 Pointer Value register is used for the associated STS-1 on the Transmit bus. When STS1\_PTR\_SEL[x] is a logic one, the SBS Transmit Alternate H1-H2 Pointer Value register is used for the associated STS-1 on the Transmit bus. These bits have no effect when H1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).



**Register 010H: SBS Master Interrupt Source**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14	R	SBS_INT	X
Bit 13	R	IMSU_INT	X
Bit 12	R	OMSU_INT	X
Bit 11	R	REFDLL_INT	X
Bit 10	R	SYSDLL_INT	X
Bit 9	R	CSTR_INT	X
Bit 8	R	TW8E_INT	X
Bit 7	R	TP8E_INT	X
Bit 6	R	RW8D_INT	X
Bit 5	R	RP8D_INT	X
Bit 4	R	WPP_INT	X
Bit 3	R	PPP_INT	X
Bit 2	R	WILC_INT	X
Bit 1	R	PILC_INT	X
Bit 0	R	ISTA_INT	X

**SBS\_INT**

If the SBS\_INT bit is a logic one, an interrupt has been generated by the top level circuitry. The SBS Interrupt register must be read to clear this interrupt.

**IMSU\_INT**

If the IMSU\_INT bit is a logic one, an interrupt has been generated by the IMSU block. The IMSU Interrupt register must be read to clear this interrupt.

**OMSU\_INT**

If the OMSU\_INT bit is a logic one, an interrupt has been generated by the OMSU block. The OMSU Interrupt register must be read to clear this interrupt.

**REFDLL\_INT**

If the REFDLL\_INT bit is a logic one, an interrupt has been generated by the REFDLL block. The REFDLL Interrupt register must be read to clear this interrupt.

**SYSDLL\_INT**

If the SYSDLL\_INT bit is a logic one, an interrupt has been generated by the SYSDLL block. The SYSDLL Interrupt register must be read to clear this interrupt.

**CSTR\_INT**

If the CSTR\_INT bit is a logic one, an interrupt has been generated by the CSTR block. The CSTR Interrupt register must be read to clear this interrupt.

**TW8E\_INT**

If the TW8E\_INT bit is a logic one, an interrupt has been generated by the TW8E block. The TW8E Interrupt register must be read to clear this interrupt.

**TPPP\_INT**

If the TP8E\_INT bit is a logic one, an interrupt has been generated by the TP8E block. The TP8E Interrupt register must be read to clear this interrupt.

**RW8D\_INT**

If the RW8D\_INT bit is a logic one, an interrupt has been generated by the RW8D block. The RW8D Interrupt register must be read to clear this interrupt.

**RP8D\_INT**

If the RP8D\_INT bit is a logic one, an interrupt has been generated by the RP8D block. The RP8D Interrupt register must be read to clear this interrupt.

**WPP\_INT**

If the WPP\_INT bit is a logic one, an interrupt has been generated by the WPP block. The WPP Interrupt register must be read to clear this interrupt.

**PPP\_INT**

If the PPP\_INT bit is a logic one, an interrupt has been generated by the PPP block. The PPP Interrupt register must be read to clear this interrupt.

**WILC\_INT**

If the WILC\_INT bit is a logic one, an interrupt has been generated by the WILC block. The WILC Interrupt register must be read to clear this interrupt.

**PILC\_INT**

If the PILC\_INT bit is a logic one, an interrupt has been generated by the PILC block. The PILC Interrupt register must be read to clear this interrupt.

## ISTA\_INT

If the ISTA\_INT bit is a logic one, an interrupt has been generated by the ISTA block. The ISTA Interrupt register must be read to clear this interrupt.

**Register 011H: SBS Interrupt Register**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6	R	ICMP_INT	X
Bit 5	R	OCMP_INT	X
Bit 4	R	OCOL_INT[4]	X
Bit 3	R	OCOL_INT[3]	X
Bit 2	R	OCOL_INT[2]	X
Bit 1	R	OCOL_INT[1]	X
Bit 0	R	RP_INT	X

**ICMP\_INT**

The ICMP\_INT bit is set to a logic one when the ICMP input is sampled by the SBS. In TelecomBus mode, ICMP is sampled during the first C1 position of every frame, as marked by IC1FP. In SBI mode, ICMP is sampled during the first C1 position of every 4 or 48 frame multiframe, as marked by IC1FP. This interrupt may be helpful in scheduling configuration page changes in the IMSU. This interrupt is enabled with the ICMPE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

**OCMP\_INT**

The OCMP\_INT bit is set to a logic one when the OCMP input is sampled by the SBS. In TelecomBus mode, OCMP is sampled during the first C1 position of every frame, as marked by RC1FP. In SBI mode, OCMP is sampled during the first C1 position of every 4 or 48 frame multiframe, as marked by RC1FP. This interrupt may be helpful in scheduling configuration page changes in the OMSU. This interrupt is enabled with the OCMPE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

**OCOL\_INT[4:1]**

If the OCOL\_INT[x] bit is a logic one, an interrupt has been generated from a collision on the associated outgoing bus. A collision is detected when ODETECT[x] is sampled high during the same clock cycle that the OACTIVE[x] is set high. These interrupts are enabled with the OCOLE[4:1] bits in the SBS Interrupt Enable register. These interrupt bits will be cleared when read.

**RP\_INT**

If the RP\_INT is a logic one, an interrupt has been generated from a parity error on the associated receive bus. This is an indication that there may be hardware or configuration problem on the receive bus. This interrupt is enabled with the RPE bit in the SBS Interrupt Enable register. This interrupt bit will be cleared when read.

**Register 012H: SBS Interrupt Enable Register**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6	R/W	ICMPE	0
Bit 5	R/W	OCMPE	0
Bit 4	R/W	OCOLE[4]	0
Bit 3	R/W	OCOLE[3]	0
Bit 2	R/W	OCOLE[2]	0
Bit 1	R/W	OCOLE[1]	0
Bit 0	R/W	RPE	0

**ICMPE**

The ICMPE interrupt enable bit (ICMPE) is an active high interrupt enable. When ICMPE is set to a logic one, an interrupt will be asserted on the INTB output when the ICMP\_INT bit in the SBS Interrupt Register is set high. When ICMPE is set to a logic zero, The ICMP\_INT bit will not cause an interrupt.

**OCMPE**

The OCMPE interrupt enable bit (OCMPE) is an active high interrupt enable. When OCMPE is set to a logic one, an interrupt will be asserted on the INTB output when the OCMP\_INT bit in the SBS Interrupt Register is set high. When OCMPE is set to a logic zero, The OCMP\_INT bit will not cause an interrupt.

**OCOLE[4:1]**

The outgoing collision detect interrupt enable bits (OCOLE[4:1]) are active high interrupt enables. When OCOLE[x] is set to a logic one, the occurrence of a collision detection on the associated outgoing bus will cause an interrupt to be asserted on the INTB output. When OCOLE[x] is set to a logic zero, outgoing collision detection will not cause an interrupt.

## RPE

The receive parity interrupt enable bit (RPE) is an active high interrupt enable. When RPE is set to a logic one, the occurrence of a parity error on the receive bus will cause an interrupt to be asserted on the INTB output. When RPE is set to a logic zero, receive parity errors will not cause an interrupt.

**Register 013H: SBS Loopback Configuration**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7		Unused	0
Bit 6		Unused	0
Bit 5		Unused	0
Bit 4		Unused	0
Bit 3		Unused	0
Bit 2	R/W	O2ILOOP	0
Bit 1	R/W	T82R8LOOP	0
Bit 0	R/W	T2RLOOP	0

**O2ILOOP**

The O2ILOOP bit enables a diagnostic loopback from the outgoing interface to the incoming interface. When O2ILOOP is a logic one, the entire SBI336 or TelecomBus is looped back from the output of the OCASM to the input of the ICASE. When O2ILOOP is a logic zero, no loopback is performed.

**T82R8LOOP**

The T82R8LOOP bit enables a diagnostic loopback from the transmit 8B/10B encoded bus to the receive 8B/10B encoded bus. When T82R8LOOP is a logic one, the entire SBI336 or TelecomBus is looped back from the output of the TW8E and TP8E to the input of the RW8D and RP8D, respectively. When T82R8LOOP is a logic zero, no loopback is performed.

**T2RLOOP**

The T2RLOOP bit enables a diagnostic loopback from the transmit interface to the receive interface. When T2RLOOP is a logic one, the entire SBI336 or TelecomBus is looped back from the output of the ICASM to the input of the OCASE. When T2RLOOP is a logic zero, no loopback is performed.



**Register 014H: SBS Master Signal Monitor #1, Accumulation Trigger**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10	R	RTPLA	X
Bit 9	R	RV5A	X
Bit 8	R	RPLA	X
Bit 7	R	RDATAA	X
Bit 6	R	RC1FPA	X
Bit 5	R	SYSCLKA	X
Bit 4	R	SREFCLKA	X
Bit 3	R	IC1FPA[4]	X
Bit 2	R	IC1FPA[3]	X
Bit 1	R	IC1FPA[2]	X
Bit 0	R	IC1FPA[1]	X

This register provides activity monitoring on major SBS inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. Bits that depend on multiple inputs making a low to high transition must have each input make a low to high transition between subsequent reads before the activity bit will be set high. The corresponding register bit reading low indicates a lack of transitions. This register should be read periodically to detect for stuck at conditions.

Writing to this register delimits the accumulation intervals in the various performance monitor accumulation registers. Counts accumulated in those registers are transferred to holding registers where they can be read. The counters themselves are then cleared to begin accumulating events for a new accumulation interval. To prevent loss of data, accumulation intervals must be 1.0 second or shorter. The bits in this register are not affected by write accesses.

**RTPLA**

The RTPL active bits (RTPLA) detects low to high transitions on the RTPL input. RTPLA is set high when a rising edge has been observed on the RTPL input, and is set low when this register is read.

**RV5A**

The RV5 active bits (RV5A) detects low to high transitions on the RV5 input. RV5A is set high when a rising edge has been observed on the RV5 input, and is set low when this register is read.

#### RPLA

The RPL active bits (RPLA) detects low to high transitions on the RPL input. RPLA is set high when a rising edge has been observed on the RPL input, and is set low when this register is read.

#### RDATAA

The RDATA active bit (RDATAA) detects low to high transitions on the RDATA input bus. RDATAA is set high when rising edges have been observed on all the signals on the RDATA[7:0] bus, and is set low when this register is read.

#### RC1FPA

The RC1FP active bit (RC1FPA) detects low to high transitions on the RC1FP input. RC1FPA is set high on a rising edge of RC1FP, and is set low when this register is read.

#### SYSCCLKA

The SYSCCLK active bit (SYSCCLKA) detects low to high transitions on the SYSCCLK input. SYSCCLKA is set high on a rising edge of SYSCCLK, and is set low when this register is read.

#### SREFCLKA

The SREFCLK active bit (SREFCLKA) detects low to high transitions on the SREFCLK input. SREFCLKA is set high on a rising edge of SREFCLK, and is set low when this register is read.

#### IC1FPA[4:1]

The IC1FP[x] active bits (IC1FPA[x]) detects low to high transitions on the corresponding IC1FP[x] input. IC1FPA[x] is set high on a rising edge of IC1FP[x], and is set low when this register is read.

**Register 015H: SBS Master Signal Monitor #2**

Bit	Type	Function	Default
Bit 15	R	ITPLA[4]	X
Bit 14	R	ITPLA[3]	X
Bit 13	R	ITPLA[2]	X
Bit 12	R	ITPLA[1]	X
Bit 11	R	IV5A[4]	X
Bit 10	R	IV5A[3]	X
Bit 9	R	IV5A[2]	X
Bit 8	R	IV5A[1]	X
Bit 7	R	IPLA[4]	X
Bit 6	R	IPLA[3]	X
Bit 5	R	IPLA[2]	X
Bit 4	R	IPLA[1]	X
Bit 3	R	IDATAA[4]	X
Bit 2	R	IDATAA[3]	X
Bit 1	R	IDATAA[2]	X
Bit 0	R	IDATAA[1]	X

This register provides activity monitoring on major SBS inputs. When a monitored input makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. Bits that depend on multiple inputs making a low to high transition must have each input make a low to high transition between subsequent reads before the activity bit will be set high. The corresponding register bit reading low indicates a lack of transitions. This register should be read periodically to detect for stuck at conditions.

**ITPLA[4:1]**

The ITPL[4:1] active bits (ITPLA[4:1]) detects low to high transitions on the ITPL[4:1] inputs. ITPLA[x] is set high when a rising edge has been observed on the ITPL[x] input, and is set low when this register is read.

**IV5A[4:1]**

The IV5[4:1] active bits (IV5A[4:1]) detects low to high transitions on the IV5[4:1] inputs. IV5A[x] is set high when a rising edge has been observed on the IV5[x] input, and is set low when this register is read.

**IPLA[4:1]**

The IPLA[4:1] active bits (IPLA[4:1]) detects low to high transitions on the IPL[4:1] inputs. IPLA[x] is set high when a rising edge has been observed on the IPL[x] input, and is set low when this register is read.

**IDATAA[4:1]**

The IDATA[4:1] active bits (IDATAA[4:1]) detects low to high transitions on the IDATA[4:1] input buses. IDATAA[x] is set high when rising edges have been observed on all the signals on the IDATA[x][7:0] bus, and is set low when this register is read.

**Register 016H: SBS Master Interrupt Enable**

Bit	Type	Function	Default
Bit 15	R/W	INTE	0
Bit 14	R/W	SBSE	0
Bit 13	R/W	IMSUE	0
Bit 12	R/W	OMSUE	0
Bit 11	R/W	REFDLLE	0
Bit 10	R/W	SYSDLLE	0
Bit 9	R/W	CSTRE	0
Bit 8	R/W	TW8EE	0
Bit 7	R/W	TP8EE	0
Bit 6	R/W	RW8DE	0
Bit 5	R/W	RP8DE	0
Bit 4	R/W	WPPE	0
Bit 3	R/W	PPPE	0
Bit 2	R/W	WILCE	0
Bit 1	R/W	PILCE	0
Bit 0	R/W	ISTAE	0

**SBS\_INT**

If the SBS\_INT bit is a logic one, an interrupt has been generated by the top level circuitry. The SBS Interrupt register must be read to clear this interrupt.

**IMSU\_INT**

If the IMSU\_INT bit is a logic one, an interrupt has been generated by the IMSU block. The IMSU Interrupt register must be read to clear this interrupt.

**OMSU\_INT**

If the OMSU\_INT bit is a logic one, an interrupt has been generated by the OMSU block. The OMSU Interrupt register must be read to clear this interrupt.

**REFDLL\_INT**

If the REFDLL\_INT bit is a logic one, an interrupt has been generated by the REFDLL block. The REFDLL Interrupt register must be read to clear this interrupt.

**SYSDLL\_INT**

If the SYSDLL\_INT bit is a logic one, an interrupt has been generated by the SYSDLL block. The SYSDLL Interrupt register must be read to clear this interrupt.

**CSTR\_INT**

If the CSTR\_INT bit is a logic one, an interrupt has been generated by the CSTR block. The CSTR Interrupt register must be read to clear this interrupt.

**TW8E\_INT**

If the TW8E\_INT bit is a logic one, an interrupt has been generated by the TW8E block. The TW8E Interrupt register must be read to clear this interrupt.

**TPPP\_INT**

If the TP8E\_INT bit is a logic one, an interrupt has been generated by the TP8E block. The TP8E Interrupt register must be read to clear this interrupt.

**RW8D\_INT**

If the RW8D\_INT bit is a logic one, an interrupt has been generated by the RW8D block. The RW8D Interrupt register must be read to clear this interrupt.

**RP8D\_INT**

If the RP8D\_INT bit is a logic one, an interrupt has been generated by the RP8D block. The RP8D Interrupt register must be read to clear this interrupt.

**WPP\_INT**

If the WPP\_INT bit is a logic one, an interrupt has been generated by the WPP block. The WPP Interrupt register must be read to clear this interrupt.

**PPP\_INT**

If the PPP\_INT bit is a logic one, an interrupt has been generated by the PPP block. The PPP Interrupt register must be read to clear this interrupt.

**WILC\_INT**

If the WILC\_INT bit is a logic one, an interrupt has been generated by the WILC block. The WILC Interrupt register must be read to clear this interrupt.

**PILC\_INT**

If the PILC\_INT bit is a logic one, an interrupt has been generated by the PILC block. The PILC Interrupt register must be read to clear this interrupt.

## ISTA\_INT

If the ISTA\_INT bit is a logic one, an interrupt has been generated by the ISTA block. The ISTA Interrupt register must be read to clear this interrupt.

**Register 017H: SBS Free User Register**

Bit	Type	Function	Default
Bit 15		Unused	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11		Unused	0
Bit 10		Unused	0
Bit 9		Unused	0
Bit 8		Unused	0
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

**FREE[7:0]**

The software ID register (FREE) holds whatever value is written into it. Reset clears the contents of this register. This register has no impact on the operation of the SBS.



**Register 020H: ISTA Incoming Parity Configuration**

Bit	Type	Function	Default
Bit 15	R/W	IPE[4]	0
Bit 14	R/W	IPE[3]	0
Bit 13	R/W	IPE[2]	0
Bit 12	R/W	IPE[1]	0
Bit 11	R/W	INCLIC1[4]	0
Bit 10	R/W	INCLIC1[3]	0
Bit 9	R/W	INCLIC1[2]	0
Bit 8	R/W	INCLIC1[1]	0
Bit 7	R/W	INCLIPL[4]	0
Bit 6	R/W	INCLIPL[3]	0
Bit 5	R/W	INCLIPL[2]	0
Bit 4	R/W	INCLIPL[1]	0
Bit 3	R/W	IOP[4]	0
Bit 2	R/W	IOP[3]	0
Bit 1	R/W	IOP[2]	0
Bit 0	R/W	IOP[1]	0

**IPE[4:1]**

The incoming parity interrupt enable bits (IPE[4:1]) are active high interrupt enables. When IPE[x] is set to a logic one, the occurrence of a parity error on the incoming bus will cause an interrupt to be asserted on the INTB output. When IPE is set to a logic zero, incoming parity errors will not cause an interrupt. IPE[4:2] are only valid when in 19 MHz mode.

**INCLIPL[4:1]**

The INCLIPL bits control whether the IPL[x] input signal participates in the incoming parity calculations. When INCLIPL[x] is set to a logic one, the parity signal includes the IPL[x] input. When INCLIPL[x] is set to a logic zero, parity is calculated without regard to the state of IPL[x]. These bits only take effect when in TelecomBus mode. INCLIPL[4:2] are only valid when in 19 MHz mode.

**INCLIC1[4:1]**

The INCLIC1 bits control whether the IC1FP input signal participates in the incoming parity calculations. When INCLIC1[x] is set to a logic one, the parity signal includes the IC1FP input. When INCLIC1[x] is set to a logic zero, parity is calculated without regard to the state of IC1FP. These bits only take effect when in TelecomBus mode. INCLIC1[4:2] are only valid when in 19 MHz mode.

## IOP[4:1]

The incoming odd parity bits (IOP[4:1]) control the expected parity on the incoming bus. When IOP is set to a logic one, the expected parity on the IDP[x] input is odd. When IOP is set to a logic zero, the parity is even. In SBI bus mode, the parity calculation encompasses the IDATA[x][7:0], IPL[x] and IV5[x] signals. In TelecomBus mode, the parity calculation encompasses the IDATA[x][7:0] and optionally IPL[x] and IC1FP as determined by the INCLIPL[x] and INCLIC1[x] bits. IOP[4:2] are only valid when in 19 MHz mode.

**Register 021H: ISTA Incoming Parity Status**

Bit	Type	Function	Default
Bit 15	R	IPI[4]	X
Bit 14	R	IPI[3]	X
Bit 13	R	IPI[2]	X
Bit 12	R	IPI[1]	X
Bit 0-11		Unused	0

## IPI[4:1]

The incoming parity error indication bits (IPI[4:1]) are set high when a parity error has occurred on the associated Incoming bus. These bits are cleared when this register is read. IPI[4:2] are only valid when in 19 MHz mode.

**Register 022H: ISTA TelecomBus Configuration**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 15	R/W	ILOCK0	0
Bit 0-14		Unused	0

**ILOCK0**

The ILOCK0 bit controls the position of the J1 byte in the Incoming TelecomBus. When ILOCK0 is a logic one, the J1 byte is expected to be locked to an offset of 0 (the byte following H3). When ILOCK0 is a logic zero, the J1 byte is expected to be locked to an offset of 522 (the byte following C1). This bit is used to determine where to sample the IC1FP[4:1] input in order to find the byte following J1 which will indicate multiframe alignment. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBS Master Configuration Register).

**Register 028H: IMSU Configuration**

Bit	Type	Function	Default
Bit 5-15		Unused	0
Bit 4	R/W	AUTO_UPDATE	0
Bit 3	R/W	SWAP_PENDINGE	0
Bit 2	R/W	UPDATEE	0
Bit 1	R	SWAP_PENDINGV	0
Bit 0	R	UPDATEV	0

**AUTO\_UPDATE**

The AUTO\_UPDATE bit selects when an off-line page update is performed. When AUTO\_UPDATE is a logic one, the on-line page is automatically copied into the off-line page whenever there is a change to the connection memory page. When AUTO\_UPDATE is a logic zero, the off-line page is not updated when there is a change to the connection memory page. A page update may still be performed by writing to the Interrupt Status and Memory Page Update Register.

**SWAP\_PENDINGE**

A logic one on the SWAP\_PENDINGE bit enables the generation of an interrupt on a change of state of SWAP\_PENDINGV.

**UPDATEE**

A logic one on the UPDATEE bit enables the generation of an interrupt on a change of state from high to low of UPDATEV.

**SWAP\_PENDINGV**

The SWAP\_PENDINGV bit contains the current state of the page swap circuitry. This bit is a logic one when a switch to the connection memory page (CMP) has been recognized but the page swap has not yet happened. This bit is a logic zero when there is not a page swap pending.

**UPDATEV**

The UPDATEV bit contains the current state of the time switch ram off-line page update circuitry. This bit is a logic one when the on-line page is being copied to the offline page. This bit is a logic zero when the on-line page is not being copied.

**Register 029H: IMSU Interrupt Status and Memory Page Update Register**

Bit	Type	Function	Default
Bit 2-14		Unused	0
Bit 1	R	SWAP_PENDINGI	X
Bit 0	R	UPDATEI	X

Writing to this register initiates an update of the off-line page in the time switch ram. The contents of the on-line page are written to the off-line page. During this update, the time switch ram may not be accessed through the indirect registers.

**SWAP\_PENDINGI**

The page swap pending interrupt status bit, SWAP\_PENDINGI, reports and acknowledges a change of state of the SWAP\_PENDINGV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the SWAP\_PENDINGE bit, the INT output reflects the state of this bit.

**UPDATEI**

The off-line page update interrupt status bit, UPDATEI, reports and acknowledges a change of state from high to low of the UPDATEEV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the UPDATEEE bit, the INT output reflects the state of this bit.

**Register 02AH: IMSU Indirect Time Switch Address**

Bit	Type	Function	Default
Bit 15	R/W	RWB	0
Bit 14		Unused	0
Bit 13	R/W	OUT_BYTE[13]	0
Bit 12	R/W	OUT_BYTE[12]	0
Bit 11	R/W	OUT_BYTE[11]	0
Bit 10	R/W	OUT_BYTE[10]	0
Bit 9	R/W	OUT_BYTE[9]	0
Bit 8	R/W	OUT_BYTE[8]	0
Bit 7	R/W	OUT_BYTE[7]	0
Bit 6	R/W	OUT_BYTE[6]	0
Bit 5	R/W	OUT_BYTE[5]	0
Bit 4	R/W	OUT_BYTE[4]	0
Bit 3	R/W	OUT_BYTE[3]	0
Bit 2	R/W	OUT_BYTE[2]	0
Bit 1	R/W	OUT_BYTE[1]	0
Bit 0	R/W	OUT_BYTE[0]	0

This register provides the address and the read/write control for the time switch configuration ram. Writing to this register triggers a ram access. Note that when an indirect write access is to be performed, the Indirect Time Switch Data register must first be setup before writing to this register. There must be a minimum of 4 SYSCLK cycles between consecutive ram write accesses. For a ram read access, it will take a maximum of 8 SYSCLK cycles for the Indirect Time Switch Data Register to contain valid data.

**RWB**

The indirect access control bit (RWB) selects between a write or read access to the time switch configuration RAM. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the Indirect Time Switch Data register. Writing a logic one to RWB triggers an indirect read operation. The read data can be found in the Indirect Time Switch Data Register.

**OUT\_BYTE[13:0]**

The OUT\_BYTE[13:0] bits indicate the ram address to be accessed. Each address in the ram corresponds to a location in the output data bus. The contents stored in each ram address points to the byte from the input data bus which is to be output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079). The byte numbers of the output frame are shown in the following table.

**Row**

<b>1</b>	0	1	2	3	...	1077	1078	1079
<b>2</b>	1080	1081	1082	1083	...	2157	2158	2159
<b>3</b>								
<b>4</b>								
<b>5</b>								
<b>6</b>								
<b>7</b>								
<b>8</b>								
<b>9</b>	8640	8641	8642	8643	...	9717	9718	9719



**Register 02BH: IMSU Indirect Time Switch Data**

Bit	Type	Function	Default
Bit 15	R	VALID	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	IN_BYTE[13]	0
Bit 12	R/W	IN_BYTE [12]	0
Bit 11	R/W	IN_BYTE [11]	0
Bit 10	R/W	IN_BYTE [10]	0
Bit 9	R/W	IN_BYTE [9]	0
Bit 8	R/W	IN_BYTE [8]	0
Bit 7	R/W	IN_BYTE [7]	0
Bit 6	R/W	IN_BYTE [6]	0
Bit 5	R/W	IN_BYTE [5]	0
Bit 4	R/W	IN_BYTE [4]	0
Bit 3	R/W	IN_BYTE [3]	0
Bit 2	R/W	IN_BYTE [2]	0
Bit 1	R/W	IN_BYTE [1]	0
Bit 0	R/W	IN_BYTE [0]	0

This register contains data read from the time switch RAM after an indirect read operation or data to be inserted into the time switch RAM during an indirect write operation. The value held in the ram indicates which byte of the input data bus is to be switched to the output.

**VALID**

The VALID bit reports the presence of valid data from an indirect read. VALID is set to logic one when indirect read access returns data from the off-line RAM and remains asserted until the next time Indirect Time Switch Data register is read.

**Reserved**

The reserved bit should not be modified.

**IN\_BYTE[13:0]**

The IN\_BYTE[13:0] bits indicate which byte in the input frame is to be switched to the output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079).

**Register 030H: ICASM CAS Enable Indirect Access Address Register**

Bit	Type	Function	Default
Bit 10-15	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 CAS enable register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'001' through b'100'.

**Register 031H: ICASM CAS Enable Indirect Access Control Register**

Bit	Type	Function	Default
Bit 15-8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

**RWB**

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the CAS Enable register. Writing a ‘0’ to RWB triggers an indirect write operation. Data to be written is taken from the CAS Enable Indirect Access Data register. Writing a ‘1’ to RWB triggers an indirect read operation. The data read can be found in the CAS Enable Indirect Access Data register.

**HST\_ADDR\_ERR**

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

**BUSY**

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the CAS Enable Indirect Access Control register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the CAS Enable Indirect Access Data register or to determine when a new indirect write operation may commence.

**Register 032H: ICASM CAS Enable Indirect Access Data Register**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 1-15	R	Unused	0
Bit 0	R/W	CAS_EN	0

**CAS\_EN**

The CAS\_EN bit is used to enable the insertion of CAS into the proper location in the associated tributary. When CAS\_EN is a logic one and the associated tributary is a T1, the CAS bits and PP bits are inserted into the PPSSSSFR byte. When CAS\_EN is a logic one and the associated tributary is an E1, the CAS bits are inserted into TS#16 and proper data is placed in the PP byte. When CAS\_EN is a logic zero, both the CAS and PP bits are not inserted.

When CAS insertion is enabled, the latency of the CAS bits through the SBS is two multiframes. For T1 tributaries, this is 48 frames or 6ms. For E1 tributaries, this is 32 frames or 4 ms.

**Register 038H: ISTT Tributary Translator Control RAM Indirect Access Address Register**

Bit	Type	Function	Default
Bit 10-15	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 tributary translator control register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'o01' through b'100'.

**Register 039H: ISTT Tributary Translator Control RAM Indirect Access Control Register**

Bit	Type	Function	Default
Bit 15-8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

**RWB**

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary translator control RAM. Writing a ‘0’ to RWB triggers an indirect write operation. Data to be written is taken from the Tributary Translator Control RAM Indirect Access Data Register. Writing a ‘1’ to RWB triggers an indirect read operation. The data read can be found in the Tributary Translator Control RAM Indirect Access Data.

**HST\_ADDR\_ERR**

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

**BUSY**

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Tributary Translator Control RAM Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Translator Control RAM Indirect Access Data register or to determine when a new indirect write operation may commence.

**Register 03AH: ISTT Tributary Translator Control RAM Indirect Access Data Register**

Bit	Type	Function	Default
Bit 2-15	R	Unused	0
Bit 1	R/W	TVT	0
Bit 0	R/W	JUST_REQ_EN	0

**JUST\_REQ\_EN**

The JUST\_REQ\_EN bit is used to enable T1, E1, DS3, E3 and Fractional rate justification request state machines to convert JUST\_REQ to V5, V5+ and V5- characters to be carried over the serial SBI336S link. When this bit is set to 1 the justification request state machines will convert JUST\_REQ signals to V5 characters. When this bit is set to 0 the state machines will not generate additional V5 characters for the specified link and will only pass existing V5 characters through as nominal rate V5 characters. This bit should be set to 1 when this device is being used in SBI mode and is connected to physical layer device which is clock master of the transmit tributary.

This bit should not be set if the TVT bit is set. This bit has no effect in TelecomBus mode.

**TVT**

The TVT bit configures a T1 or E1 tributary as a transparent virtual tributary. When TVT is set to 1 the T1 or E1 tributary is configured as a TVT and the ERDI and REI bits in the V5 byte are transmitted across the serial link in one of the V5 characters. When TVT is set to 0 the T1 or E1 tributary is configured as a standard T1 or E1 link.

This bit should not be set if the JUST\_REQ\_EN bit is set. This bit has no effect in TelecomBus mode or if the SPE is configured to something other than T1 or E1 data.

**Register 040H: OSTT Tributary Translator Control RAM Indirect Access Address Register**

Bit	Type	Function	Default
Bit 10-15	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 tributary translator control register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'001' through b'100'.



**Register 041H: OSTT Tributary Translator Control RAM Indirect Access Control Register**

Bit	Type	Function	Default
Bit 15-8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

**RWB**

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary translator control RAM. Writing a ‘0’ to RWB triggers an indirect write operation. Data to be written is taken from the Tributary Translator Control RAM Indirect Access Data Register. Writing a ‘1’ to RWB triggers an indirect read operation. The data read can be found in the Tributary Translator Control RAM Indirect Access Data.

**HST\_ADDR\_ERR**

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

**BUSY**

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Tributary Translator Control RAM Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Translator Control RAM Indirect Access Data register or to determine when a new indirect write operation may commence.

**Register 042H: OSTT Tributary Translator Control RAM Indirect Access Data Register**

Bit	Type	Function	Default
Bit 2-15	R	Unused	0
Bit 1	R/W	TVT	0
Bit 0	R/W	JUST_REQ_EN	0

**JUST\_REQ\_EN**

The JUST\_REQ\_EN bit is used to enable T1, E1, DS3, E3 and Fractional rate justification request state machines to convert V5, V5+ and V5- characters to JUST\_REQs. When this bit is set to 1 the justification request state machines will convert V5 characters to the JUST\_REQ signal. When this bit is set to 0 the state machines will not generate JUST\_REQ. This bit should be set to 1 when this device is being used in SBI mode and is connected to link layer device which is clock slave to the transmit tributary.

This bit should not be set if the TVT bit is set. This bit has no effect in TelecomBus mode.

**TVT**

The TVT bit configures a T1 or E1 tributary as a transparent virtual tributary. When TVT is set to 1 the T1 or E1 tributary is configured as a TVT. Being a TVT, the ERDI and REI bits are received from the serial link in one of the V5 characters and are output on ODATA during the V5 byte. When TVT is set to 0 the T1 or E1 tributary is configured as a standard T1 or E1 link.

This bit should not be set if the JUST\_REQ\_EN bit is set. This bit has no effect in TelecomBus mode or if the SPE is configured to something other than T1 or E1 data.

**Register 048H: OMSU Configuration**

Bit	Type	Function	Default
Bit 5-15		Unused	0
Bit 4	R/W	AUTO_UPDATE	0
Bit 3	R/W	SWAP_PENDINGE	0
Bit 2	R/W	UPDATEE	0
Bit 1	R	SWAP_PENDINGV	0
Bit 0	R	UPDATEV	0

**AUTO\_UPDATE**

The AUTO\_UPDATE bit selects when an off-line page update is performed. When AUTO\_UPDATE is a logic one, the on-line page is automatically copied into the off-line page whenever there is a change to the connection memory page. When AUTO\_UPDATE is a logic zero, the off-line page is not updated when there is a change to the connection memory page. A page update may still be performed by writing to the Interrupt Status and Memory Page Update Register.

**SWAP\_PENDINGE**

A logic one on the SWAP\_PENDINGE bit enables the generation of an interrupt on a change of state of SWAP\_PENDINGV.

**UPDATEE**

A logic one on the UPDATEE bit enables the generation of an interrupt on a change of state from high to low of UPDATEV.

**SWAP\_PENDINGV**

The SWAP\_PENDINGV bit contains the current state of the page swap circuitry. This bit is a logic one when a switch to the connection memory page (CMP) has been recognized but the page swap has not yet happened. This bit is a logic zero when there is not a page swap pending.

**UPDATEV**

The UPDATEV bit contains the current state of the time switch ram off-line page update circuitry. This bit is a logic one when the on-line page is being copied to the offline page. This bit is a logic zero when the on-line page is not being copied.

**Register 049H: OMSU Interrupt Status and Memory Page Update Register**

Bit	Type	Function	Default
Bit 2-14		Unused	0
Bit 1	R	SWAP_PENDINGI	X
Bit 0	R	UPDATEI	X

Writing to this register initiates an update of the off-line page in the time switch ram. The contents of the on-line page are written to the off-line page. During this update, the time switch ram may not be accessed through the indirect registers.

**SWAP\_PENDINGI**

The page swap pending interrupt status bit, SWAP\_PENDINGI, reports and acknowledges a change of state of the SWAP\_PENDINGV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the SWAP\_PENDINGE bit, the INT output reflects the state of this bit.

**UPDATEI**

The off-line page update interrupt status bit, UPDATEI, reports and acknowledges a change of state from high to low of the UPDATEEV bit of the MSU Configuration register. This bit is cleared when this register is read. When enabled by the UPDATEEE bit, the INT output reflects the state of this bit.

**Register 04AH: OMSU Indirect Time Switch Address**

Bit	Type	Function	Default
Bit 15	R/W	RWB	0
Bit 14		Unused	0
Bit 13	R/W	OUT_BYTE[13]	0
Bit 12	R/W	OUT_BYTE[12]	0
Bit 11	R/W	OUT_BYTE[11]	0
Bit 10	R/W	OUT_BYTE[10]	0
Bit 9	R/W	OUT_BYTE[9]	0
Bit 8	R/W	OUT_BYTE[8]	0
Bit 7	R/W	OUT_BYTE[7]	0
Bit 6	R/W	OUT_BYTE[6]	0
Bit 5	R/W	OUT_BYTE[5]	0
Bit 4	R/W	OUT_BYTE[4]	0
Bit 3	R/W	OUT_BYTE[3]	0
Bit 2	R/W	OUT_BYTE[2]	0
Bit 1	R/W	OUT_BYTE[1]	0
Bit 0	R/W	OUT_BYTE[0]	0

This register provides the address and the read/write control for the time switch configuration ram. Writing to this register triggers a ram access. Note that when an indirect write access is to be performed, the Indirect Time Switch Data register must first be setup before writing to this register. There must be a minimum of 4 SYSCLK cycles between consecutive ram accesses. For a ram read access, it will take a maximum of 8 SYSCLK cycles for the Indirect Time Switch Data Register to contain valid data.

**RWB**

The indirect access control bit (RWB) selects between a write or read access to the time switch configuration RAM. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the Indirect Time Switch Data register. Writing a logic one to RWB triggers an indirect read operation. The read data can be found in the Indirect Time Switch Data Register.

**OUT\_BYTE[13:0]**

The OUT\_BYTE[13:0] bits indicate the ram address to be accessed. Each address in the ram corresponds to a location in the output data bus. The contents stored in each ram address points to the byte from the input data bus which is to be output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079). The byte numbers of the output frame are shown in the following table.

**Row**

<b>1</b>	0	1	2	3	...	1077	1078	1079
<b>2</b>	1080	1081	1082	1083	...	2157	2158	2159
<b>3</b>								
<b>4</b>								
<b>5</b>								
<b>6</b>								
<b>7</b>								
<b>8</b>								
<b>9</b>	8640	8641	8642	8643	...	9717	9718	9719

**Register 04BH: OMSU Indirect Time Switch Data**

Bit	Type	Function	Default
Bit 15	R	VALID	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	IN_BYTE[13]	0
Bit 12	R/W	IN_BYTE [12]	0
Bit 11	R/W	IN_BYTE [11]	0
Bit 10	R/W	IN_BYTE [10]	0
Bit 9	R/W	IN_BYTE [9]	0
Bit 8	R/W	IN_BYTE [8]	0
Bit 7	R/W	IN_BYTE [7]	0
Bit 6	R/W	IN_BYTE [6]	0
Bit 5	R/W	IN_BYTE [5]	0
Bit 4	R/W	IN_BYTE [4]	0
Bit 3	R/W	IN_BYTE [3]	0
Bit 2	R/W	IN_BYTE [2]	0
Bit 1	R/W	IN_BYTE [1]	0
Bit 0	R/W	IN_BYTE [0]	0

This register contains data read from the time switch RAM after an indirect read operation or data to be inserted into the time switch RAM during an indirect write operation. The value held in the ram indicates which byte of the input data bus is to be switched to the output.

**VALID**

The VALID bit reports the presence of valid data from an indirect read. VALID is set to logic one when indirect read access returns data from the off-line RAM and remains asserted until the next time Indirect Time Switch Data register is read.

**Reserved**

The reserved bit should not be modified.

**IN\_BYTE[13:0]**

The IN\_BYTE[13:0] bits indicate which byte in the input frame is to be switched to the output. In DS0 mode, legal values are 000H to 25F7H (0 to 9719). In column mode, legal values are 000H to 437H (0 to 1079).

**Register 050H: OCASM CAS Enable Indirect Access Address Register**

Bit	Type	Function	Default
Bit 10-15	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 CAS enable register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'001' through b'100'.



**Register 051H: OCASM CAS Enable Indirect Access Control Register**

Bit	Type	Function	Default
Bit 15-8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

**RWB**

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the CAS Enable register. Writing a ‘0’ to RWB triggers an indirect write operation. Data to be written is taken from the CAS Enable Indirect Access Data register. Writing a ‘1’ to RWB triggers an indirect read operation. The data read can be found in the CAS Enable Indirect Access Data register.

**HST\_ADDR\_ERR**

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

**BUSY**

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the CAS Enable Indirect Access Control register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the CAS Enable Indirect Access Data register or to determine when a new indirect write operation may commence.

**Register 052H: OCASM CAS Enable Indirect Access Data Register**

Bit	Type	Function	Default
Bit 1-15	R	Unused	0
Bit 0	R/W	CAS_EN	0

**CAS\_EN**

The CAS\_EN bit is used to enable the insertion of CAS into the proper location in the associated tributary. When CAS\_EN is a logic one and the associated tributary is a T1, the CAS bits and PP bits are inserted into the PPSSSSFR byte. When CAS\_EN is a logic one and the associated tributary is an E1, the CAS bits are inserted into TS#16 and proper data is placed in the PP byte. When CAS\_EN is a logic zero, both the CAS and PP bits are not inserted.

When CAS insertion is enabled, the latency of the CAS bits through the SBS is two multiframes. For T1 tributaries, this is 48 frames or 6ms. For E1 tributaries, this is 32 frames or 4 ms.

**Register 060H: OSTA Outgoing Configuration and Parity**

Bit	Type	Function	Default
Bit 15	R/W	OUTGOING_OE	0
Bit 14	R/W	OLOCK0	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	INCLOC1FP[4]	0
Bit 10	R/W	INCLOC1FP[3]	0
Bit 9	R/W	INCLOC1FP[2]	0
Bit 8	R/W	INCLOC1FP[1]	0
Bit 7	R/W	INCLOPL[4]	0
Bit 6	R/W	INCLOPL[3]	0
Bit 5	R/W	INCLOPL[2]	0
Bit 4	R/W	INCLOPL[1]	0
Bit 3	R/W	OOP[4]	0
Bit 2	R/W	OOP[3]	0
Bit 1	R/W	OOP[2]	0
Bit 0	R/W	OOP[1]	0

**OUTGOING\_OE**

The OUTGOING\_OE bit controls the output enable on the outgoing bus. When OUTGOING\_OE is a logic one, the entire outgoing bus is driven regardless of the state of the per-tributary OUTPUT\_ENABLE bits in register 068H. When OUTGOING\_OE is a logic zero, only the tributaries with their OUTPUT\_ENABLE bit set will be driven. This bit only has an effect when in 19.44 MHz SBI mode (TELECOM\_BUS = 'b0, 19M\_BUS = 'b1 in the SBS Master Configuration Register). In all other modes, the outgoing bus is always driven.

**OLOCK0**

The OLOCK0 bit controls the position of the J1 byte in the Outgoing TelecomBus. When OLOCK0 is a logic one, the J1 byte is expected to be locked to an offset of 0 (the byte following H3). When OLOCK0 is a logic zero, the J1 byte is expected to be locked to an offset of 522 (the byte following C1). This bit is used to determine where to pulse the OC1FP output when any part of STS1\_OJ1EN[12:1] or STS1\_OV1EN[12:1] are set. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBS Master Configuration Register).

**INCLOC1FP[4:1]**

The INCLOC1FP bits control whether the OC1FP output signal participates in the outgoing parity calculations. When INCLOC1FP[x] is set to a logic one, the parity signal includes the OC1FP output. When INCLOC1FP[x] is set to a logic zero, parity is calculated without regard to the state of OC1FP. These bits only take effect when in TelecomBus mode. INCLOC1FP[4:2] are only valid when in 19 MHz mode.

**INCLOPL[4:1]**

The INCLOPL bits control whether the OPL[x] output signal participates in the outgoing parity calculations. When INCLOPL[x] is set to a logic one, the parity signal includes the OPL[x] output. When INCLOPL[x] is set to a logic zero, parity is calculated without regard to the state of OPL[x]. These bits only take effect when in TelecomBus mode. INCLOPL[4:2] are only valid when in 19 MHz mode.

**OOP**

The outgoing odd parity bit (OOP) controls the parity generated on the outgoing bus. When OOP[x] is set to a logic one, the parity on the ODP[x] output is odd. When OOP[x] is set to a logic zero, the parity is even. In SBI bus mode, the parity calculation encompasses the ODATA[x][7:0], OPL[x] and OV5[x] signals. In TelecomBus mode, the parity calculation encompasses the ODATA[x][7:0] and optionally OPL and OC1FP as determined by the INCLOPL[x] and INCLOC1FP[x] bits. OOP[4:2] are only valid when in 19 MHz mode.

**Register 061H: OSTA Outgoing J1 Configuration**

Bit	Type	Function	Default
Bit 12-15		Unused	0
Bit 11	R/W	STS1_OJ1EN[12]	0
Bit 10	R/W	STS1_OJ1EN[11]	0
Bit 9	R/W	STS1_OJ1EN[10]	0
Bit 8	R/W	STS1_OJ1EN[9]	0
Bit 7	R/W	STS1_OJ1EN[8]	0
Bit 6	R/W	STS1_OJ1EN[7]	0
Bit 5	R/W	STS1_OJ1EN[6]	0
Bit 4	R/W	STS1_OJ1EN[5]	0
Bit 3	R/W	STS1_OJ1EN[4]	0
Bit 2	R/W	STS1_OJ1EN[3]	0
Bit 1	R/W	STS1_OJ1EN[2]	0
Bit 0	R/W	STS1_OJ1EN[1]	0

**STS1\_OJ1EN[12:1]**

The STS1\_OJ1EN[12:1] bit controls the inclusion of the J1 byte identification on the OC1FP[4:1] output for each of the 12 STS-1s. When STS1\_OJ1EN[x] is a logic one, the OC1FP[4:1] output will pulse high during the J1 byte position of the associated STS-1 along with the usual C1 byte position. The position of the J1 byte relative to the C1 position is determined by the OLOCK0 bit. When STS1\_OJ1EN[x] is a logic zero, the OC1FP[4:1] will not pulse high during the J1 byte position of the associated STS-1. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBS Master Configuration Register). In 19 MHz mode, the 12 STS-1s are spread across the four outgoing buses. STS1\_OJ1EN[1] controls the first STS-1 of the first bus, STS1\_OJ1EN[2] controls the first STS-1 of the second bus, etc.

**Register 062H: OSTA Outgoing V1 Configuration**

Bit	Type	Function	Default
Bit 12-15		Unused	0
Bit 11	R/W	STS1_OV1EN[12]	0
Bit 10	R/W	STS1_OV1EN[11]	0
Bit 9	R/W	STS1_OV1EN[10]	0
Bit 8	R/W	STS1_OV1EN[9]	0
Bit 7	R/W	STS1_OV1EN[8]	0
Bit 6	R/W	STS1_OV1EN[7]	0
Bit 5	R/W	STS1_OV1EN[6]	0
Bit 4	R/W	STS1_OV1EN[5]	0
Bit 3	R/W	STS1_OV1EN[4]	0
Bit 2	R/W	STS1_OV1EN[3]	0
Bit 1	R/W	STS1_OV1EN[2]	0
Bit 0	R/W	STS1_OV1EN[1]	0

**STS1\_OV1EN[12:1]**

The STS1\_OV1EN[12:1] bit controls the inclusion of the byte following J1 identification on the OC1FP[4:1] output for each of the 12 STS-1s. When STS1\_OV1EN[x] is a logic one, the OC1FP[4:1] output will pulse high during the byte following the J1 position of the associated STS-1 along with the usual C1 byte position. The position of the J1 byte relative to the C1 position is determined by the OLOCK0 bit. When STS1\_OV1EN is a logic zero, the OC1FP[4:1] will not pulse high during the byte following the J1 position of the associated STS-1. This bit only has an effect when in TelecomBus mode (TELECOM\_BUS = 'b1 in the SBS Master Configuration Register). In 19 MHz mode, the 12 STS-1s are spread across the four outgoing buses. STS1\_OV1EN[1] controls the first STS-1 of the first bus, STS1\_OV1EN[2] controls the first STS-1 of the second bus, etc.

**Register 063H: OSTA H1-H2 Pointer Value**

Bit	Type	Function	Default
Bit 15	R/W	H1[7]	0
Bit 14	R/W	H1[6]	0
Bit 13	R/W	H1[5]	0
Bit 12	R/W	H1[4]	0
Bit 11	R/W	H1[3]	0
Bit 10	R/W	H1[2]	0
Bit 9	R/W	H1[1]	0
Bit 8	R/W	H1[0]	0
Bit 7	R/W	H2[7]	0
Bit 6	R/W	H2[6]	0
Bit 5	R/W	H2[5]	0
Bit 4	R/W	H2[4]	0
Bit 3	R/W	H2[3]	0
Bit 2	R/W	H2[2]	0
Bit 1	R/W	H2[1]	0
Bit 0	R/W	H2[0]	0

**H1[7:0]**

The H1[7:0] bits contain the value to be output during the H1 position of the transport overhead of the Outgoing TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic zero and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**H2[7:0]**

The H2[7:0] bits contain the value to be output during the H2 position of the transport overhead of the Outgoing TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic zero and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**Register 064H: OSTA Alternate H1-H2 Pointer Value**

Bit	Type	Function	Default
Bit 15	R/W	H1_ALT[7]	0
Bit 14	R/W	H1_ALT[6]	0
Bit 13	R/W	H1_ALT[5]	0
Bit 12	R/W	H1_ALT[4]	0
Bit 11	R/W	H1_ALT[3]	0
Bit 10	R/W	H1_ALT[2]	0
Bit 9	R/W	H1_ALT[1]	0
Bit 8	R/W	H1_ALT[0]	0
Bit 7	R/W	H2_ALT[7]	0
Bit 6	R/W	H2_ALT[6]	0
Bit 5	R/W	H2_ALT[5]	0
Bit 4	R/W	H2_ALT[4]	0
Bit 3	R/W	H2_ALT[3]	0
Bit 2	R/W	H2_ALT[2]	0
Bit 1	R/W	H2_ALT[1]	0
Bit 0	R/W	H2_ALT[0]	0

**H1\_ALT[7:0]**

The H1\_ALT[7:0] bits contain the value to be output during the H1 position of the transport overhead of the Outgoing TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic one and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**H2\_ALT[7:0]**

The H2\_ALT[7:0] bits contain the value to be output during the H2 position of the transport overhead of the Outgoing TelecomBus when the STS1\_PTR\_SEL[x] bit is a logic one and the OH1H2EN bit is set high. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).



**Register 065H: OSTA H1-H2 Pointer Selection**

Bit	Type	Function	Default
Bit 15	R/W	OH1H2EN	0
Bit 14		Unused	0
Bit 13		Unused	0
Bit 12		Unused	0
Bit 11	R/W	STS1_PTR_SEL[12]	0
Bit 10	R/W	STS1_PTR_SEL[11]	0
Bit 9	R/W	STS1_PTR_SEL[10]	0
Bit 8	R/W	STS1_PTR_SEL[9]	0
Bit 7	R/W	STS1_PTR_SEL[8]	0
Bit 6	R/W	STS1_PTR_SEL[7]	0
Bit 5	R/W	STS1_PTR_SEL[6]	0
Bit 4	R/W	STS1_PTR_SEL[5]	0
Bit 3	R/W	STS1_PTR_SEL[4]	0
Bit 2	R/W	STS1_PTR_SEL[3]	0
Bit 1	R/W	STS1_PTR_SEL[2]	0
Bit 0	R/W	STS1_PTR_SEL[1]	0

**OH1H2EN**

The OH1H2EN bit enables the insertion of the H1 and H2 bytes in the transport overhead on the Outgoing TelecomBus. When OH1H2EN is a logic one, the values in the internal registers is inserted into the H1 and H2 bytes of the Outgoing TelecomBus according to the STS1\_PTR\_SEL[12:1] bits. When OH1H2EN is a logic zero, the values from the internal registers is not inserted into the H1 and H2 bytes. This bit has no effect when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**STS1\_PTR\_SEL[12:1]**

The STS1\_PTR\_SEL[12:1] bits select which of the two H1-H2 Pointer registers is used for each of the 12 STS-1's output on the Outgoing TelecomBus when the OH1H2EN bit is set. When STS1\_PTR\_SEL[x] is a logic zero, the SBS Transmit H1-H2 Pointer Value register is used for the associated STS-1 on the Outgoing bus. When STS1\_PTR\_SEL[x] is a logic one, the SBS Transmit Alternate H1-H2 Pointer Value register is used for the associated STS-1 on the Outgoing bus. These bits have no effect when OH1H2EN is low or when in SBI mode (TELECOM\_BUS = 'b0 in the Master Configuration Register).

**Register 066H: OSTA Tributary Output Enable Indirect Access Address Register**

Bit	Type	Function	Default
Bit 10-15	R	Unused	0
Bit 9	R/W	SBI[2]	0
Bit 8	R/W	SBI[1]	0
Bit 7	R/W	SBI[0]	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0], SPE[1:0] and SBI[2:0]

The TRIB[4:0], SPE[1:0] and SBI[2:0] fields are used to fully specify which SBI336 tributary output enable register the write or read operation will apply.

TRIB[4:0] specifies the tributary number within the SBI336 SPE as specified by the SPE[1:0] and SBI[2:0] fields. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Legal values for SBI[2:0] are b'001' through b'100'.

**Register 067H: OSTA Tributary Output Enable Indirect Access Control Register**

Bit	Type	Function	Default
Bit 15-8	R	Unused	0
Bit 7	R	BUSY	0
Bit 6	R	HST_ADDR_ERR	0
Bit 5	R	Unused	0
Bit 4	R	Unused	0
Bit 3	R	Unused	0
Bit 2	R	Unused	0
Bit 1	R/W	RWB	0
Bit 0	R	Unused	0

**RWB**

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary output enable register. Writing a ‘0’ to RWB triggers an indirect write operation. Data to be written is taken from the Output Enable Indirect Access Data Register. Writing a ‘1’ to RWB triggers an indirect read operation. The data read can be found in the Tributary Output Enable Indirect Access Data Register.

**HST\_ADDR\_ERR**

When set following a host read this bit indicates that an illegal host access was attempted. An illegal host access occurs when an attempt is made to access an out of range tributary. Out of range tributaries accesses occur when SBI[2:0] is not in the range 1-4, SPE[1:0] is not in the range 1-3 and TRIB[4:0] is not in the range 1-28 for T1s, not in the range 1-21 for E1s and not equal to 1 for the remaining tributary types. This bit is cleared when this register is read.

**BUSY**

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Tributary Output Enable Indirect Access Control Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Tributary Output Enable Indirect Access Data register or to determine when a new indirect write operation may commence.

**Register 068H: OSTA Tributary Output Enable Indirect Access Data Register**

Bit	Type	Function	Default
Bit 1-15	R	Unused	0
Bit 0	R/W	OUTPUT_ENABLE	0

**OUTPUT\_ENABLE**

The OUTPUT\_ENABLE bit controls whether or not the Outgoing bus is driven during the associated tributary. This bit only has an effect when the OUTGOING\_OE bit in register 060H is a logic zero. When OUTPUT\_ENABLE is a logic one, the associated tributary is driven onto the Outgoing bus. When OUTPUT\_ENABLE is a logic zero, the associated tributary is not driven and the Outgoing bus is held high impedance. Parity is only generated on enabled links.

**Register 070h: WPP Indirect Address**

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RDWRB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

This register provides selection of configuration pages and of the time-slots to be accessed in the WPP block. Writing to this register triggers an indirect register access.

**PATH[3:0]**

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	Time Division #
0000	Invalid STS-1 path
0001-1100	STS-1 path #1 to STS-1 path #12
1101-1111	Invalid STS-1 path

**IADDR[3:0]**

The internal RAM page bits select which page of the internal RAM is access by the current indirect transfer. Six pages are defined for the monitor (IADDR[3] = '0') : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page, the B1/E1 value page, the Monitor error count page and the received B1/E1 byte.

IADDR[3:0]	RAM Page
0000	STS-1 path Configuration page
0001	PRBS[22:7] page
0010	PRBS[6:0] page

<b>IADDR[3:0]</b>	<b>RAM Page</b>
0011	Reserved
0100	Monitor error count page
0101	Reserved

Four pages are defined for the generator (IADDR [3] = '1') : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page and the B1/E1 value.

<b>IADDR[3:0]</b>	<b>RAM page</b>
1000	STS-1 path Configuration page
1001	PRBS[22:7] page
1010	PRBS[6:0] page
1011	Reserved

### RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RDWRB is set to logic one, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RDWRB is set to logic zero, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

### BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic one upon writing to the Indirect Address Register. BUSY is set to logic zero, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

**Register 071h: WPP Indirect Data**

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

This register contains the data read from the internal RAM after an indirect read operation or the data to be inserted into the internal RAM in an indirect write operation.

**DATA[15:0]**

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RDWRB is set to logic one (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic zero (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

**Register 071h (IADDR = 0h): WPP Monitor STS-1 path Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	X
Bit 10	R/W	Reserved	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	MON_ENA	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 0h (IADDR[3:0] is “0h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured

**MON\_ENA**

Monitor Enable register bit, enables the PRBS monitor for the STS-1 path specified in the PATH[3:0] of register 050h (TPP Indirect Address). If MON\_ENA is set to ‘1’, a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON\_ENA is low, the data at the input of the monitor is ignored.

**INV\_PRBS**

This sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

**RESYNC**

This sets the monitor to re-initialize the PRBS sequence. When set high the monitor’s state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream.



SEQ\_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low the payload contains PRBS bytes, and when high, a sequential pattern is monitored.

Reserved

The reserved bits must be set low for correct operation of the SBS.

**Register 071h (IADDR = 1h): WPP Monitor PRBS[22:7] Accumulator**

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 1h (IADDR[3:0] is “1h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[22:7]**

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 071h (IADDR = 2h): WPP Monitor PRBS[6:0] Accumulator**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 2h (IADDR[3:0] is “2h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[7:0]**

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 071h (IADDR = 4h): WPP Monitor Error count**

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 4h (IADDR[3:0] is “4h” in register 070h).

**ERR\_CNT[15:0]**

The ERR\_CNT[15:0] register contains the cumulative number of errors in the PRBS bytes since the last error reporting event. Errors are accumulated only when the monitor is in the synchronized state. Each PRBS byte will only contribute a single error, even if there are multiple errors within a single PRBS byte. The transfer of the error counter to this holding register is triggered by an indirect write to this register or writing the SBS Master Signal Monitor #1, Accumulation Trigger Register (014H). The error counter is cleared and restarted after its value is transferred to the ERR\_CNT[15:0] holding register. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value.

**Register 071h (IADDR = 8h): WPP Generator STS-1 path Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	LINKENA	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	LINKENA	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	Reserved	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	Reserved	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 8h (IADDR[3:0] is “8h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

**INV\_PRBS**

Sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted, else they will be inserted unmodified.

**FORCE\_ERR**

The Force Error bit is used to force bit errors in the inserted pattern. When a logic one is written, the MSB of the next byte will be inverted, inducing a single bit error. The register clears itself when the operation is complete.

**SEQ\_PRBSB**

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes, and when high, a sequential pattern is inserted.

LINKENA

These two bits specify if PRBS is to be inserted in the path through the TW8E. If LINKENA is high patterns are generated in the SONET/SDH frame to the TW8E, else no pattern is generated and the unmodified SONET/SDH input frame is passed to the TW8E.

Reserved

The reserved bits must be set low for correct operation of the SBS.

**Register 071h (IADDR = 9h): WPP Generator PRBS[22:7] Accumulator**

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address 9h (IADDR[3:0] is “9h” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[22:7]**

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 071h (IADDR = Ah): WPP Generator PRBS[6:0] Accumulator**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the WPP Indirect Data register (Register 071h) when accessing Indirect Address Ah (IADDR[3:0] is “Ah” in register 070h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[6:0]**

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.



**Register 072h: WPP Generator Payload Configuration**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GEN_STS3C[3]	0
Bit 2	R/W	GEN_STS3C[2]	0
Bit 1	R/W	GEN_STS3C[1]	0
Bit 0	R/W	GEN_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming bus for processing by the Working PRBS generator.

**GEN\_STS3C[0]**

The STS-3c/VC-4 payload configuration (GEN\_STS3C[0]) bit selects the payload configuration. When GEN\_STS3C[0] is set to logic one, the STS-1/VC-3 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[0] is set to logic zero, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[0] register bit.

**GEN\_STS3C[1]**

The STS-3c/VC-4 payload configuration (GEN\_STS3C[1]) bit selects the payload configuration. When GEN\_STS3C[1] is set to logic one, the STS-1/VC-3 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[1] is set to logic zero, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[1] register bit.

**GEN\_STS3C[2]**

The STS-3c/VC-4 payload configuration (GEN\_STS3C[2]) bit selects the payload configuration. When GEN\_STS3C[2] is set to logic one, the STS-1/VC-3 paths #3, #7 and #11 are part of a STS-3cVC-4 payload. When GEN\_STS3C[2] is set to logic zero, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[2] register bit.

**GEN\_STS3C[4]**

The STS-3c/VC-4 payload configuration (GEN\_STS3C[3]) bit selects the payload configuration. When GEN\_STS3C[3] is set to logic one, the STS-1/VC-3 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[3] is set to logic zero, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[3] register bit.

**GEN\_STS12C**

The STS-12c/VC-4-4c payload configuration (GEN\_STS12C) bit selects the payload configuration. When GEN\_STS12C is set to logic one, the timeslots #1 to #12 are part of the same concatenated payload defined by GEN\_MSSLEN. When GEN\_STS12C is set to logic zero, the STS-1/STM-0 paths are defined with the GEN\_STS3C[3:0] register bit. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[3:0] register bit.

**Reserved**

The Reserved bits must be set low for correct operation of the SBS.

**Register 073h: WPP Monitor Payload Configuration**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[3]	0
Bit 2	R/W	MON_STS3C[2]	0
Bit 1	R/W	MON_STS3C[1]	0
Bit 0	R/W	MON_STS3C[0]	0

This register configures the payload type of the time-slots in the Receive Working Serial Link for processing by the PRBS monitor section.

**MON\_STS3C[0]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[0]) bit selects the payload configuration. When MON\_STS3C[0] is set to logic one, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON\_STS3C[0] is set to logic zero, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[0] register bit.

**MON\_STS3C[1]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[1]) bit selects the payload configuration. When MON\_STS3C[1] is set to logic one, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON\_STS3C[1] is set to logic zero, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[1] register bit.

### MON\_STS3C[2]

The STS-3c/VC-4 payload configuration (MON\_STS3C[2]) bit selects the payload configuration. When MON\_STS3C[2] is set to logic one, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON\_STS-3c/VC-4 payload. When MON\_STS3C[2] is set to logic zero, the paths are STS-1 (VC-3) payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[2] register bit.

### MON\_STS3C[4]

The STS-3c/VC-4 payload configuration (MON\_STS3C[3]) bit selects the payload configuration. When MON\_STS3C[3] is set to logic one, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON\_STS3C[3] is set to logic zero, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[3] register bit.

### Reserved

The Reserved bits must be set low for correct operation of the SBS.

### MON\_STS12C

The STS-12c/VC-4-4c payload configuration (MON\_STS12C) bit selects the payload configuration. When MON\_STS12C is set to logic one, the timeslots #1 to #12 are part of the same concatenated payload defined by MON\_MSSLEN. When MON\_STS12C is set to logic zero, the STS-1/STM-0 paths are defined with the MON\_STS3C[3:0] register bit. The MON\_STS12C register bit has precedence over the MON\_STS3C[3:0] register bit.

**Register 074h: WPP Monitor Byte Error Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

This register reports and acknowledges PRBS byte error interrupts for all the time-slots in the Receive Working Serial Link.

**MON<sub>x</sub>\_ERRI**

The Monitor Byte Error Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1 paths when an error has been detected. The MON<sub>x</sub>\_ERRI is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1 path *x*. This bit is independent of MON<sub>x</sub>\_ERRE and is cleared after being read.

**Register 075h: WPP Monitor Byte Error Interrupt Enable**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

This register enables the assertion of PRBS byte error interrupts for all the time-slots in the Receive Working bus.

**MON<sub>x</sub>\_ERRE**

The Monitor Byte Error Interrupt Enable register enables the interrupt for each of the 12 STS-1 paths. When MON<sub>x</sub>\_ERRE is set high it allows the Byte Error Interrupt to generate an external interrupt on INT.

**Register 079h: WPP Monitor Synchronization Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

This register reports the PRBS monitor synchronization status change interrupts for all the time-slots in the Receive Working Serial Link.

**MON<sub>x</sub>\_SYNCI**

The Monitor Synchronization Interrupt Status register is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 path goes from Synchronized to Out Of Synchronization state or vice-versa, the **MON<sub>x</sub>\_SYNCI** is set high. This bit is independent of **MON<sub>x</sub>\_SYNCE** and is cleared after it's been read.

**Register 07Ah: WPP Monitor Synchronization Interrupt Enable**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

This register enables the assertion of change of PRBS monitor synchronization status interrupts for all the time-slots in the Receive Working Serial Link.

**MON<sub>x</sub>\_SYNCE**

The Monitor Synchronization Interrupt Enable register allows each individual STS-1 path to generate an external interrupt on INT. When MON<sub>x</sub>\_SYNCE is set high whenever a change occurs in the synchronization state of the monitor in STS-1 path **x**, generates an interrupt on INT.



**Register 07Bh: WPP Monitor Synchronization State**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

This register reports the state of the PRBS monitors for all the time-slots in the Receive Working Serial Link.

**MON<sub>x</sub>\_SYNCV**

The Monitor Synchronization Status register reflects the state of the monitor's state machine. When MON<sub>x</sub>\_SYNCV is set high the monitor's state machine is in synchronization for the STS-1 Path x. When MON<sub>x</sub>\_SYNCV is low the monitor is NOT in synchronization for the STS-1 Path x.

**Register 07Ch: WPP Performance Counters Transfer Trigger**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TIP	0

This register controls and monitors the reporting of the error counter registers.

A write in this register will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low.

**TIP**

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred in the holding register yet. When TIP is low, the value of the error counters is available to be read in the holding registers. This bit can be poll after an error counters transfer request, to determine if the counters are ready to be read.

**Register 080h: PPP Indirect Address**

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RDWRB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

This register provides selection of configuration pages and of the time-slots to be accessed in the PPP block. Writing to this register triggers an indirect register access.

**PATH[3:0]**

The PATH[3:0] bits select which time-multiplexed division is accessed by the current indirect transfer.

PATH[3:0]	Time Division #
0000	Invalid STS-1 path
0001-1100	STS-1 path #1 to STS-1 path #12
1101-1111	Invalid STS-1 path

**IADDR[3:0]**

The internal RAM page bits select which page of the internal RAM is access by the current indirect transfer. Six pages are defined for the monitor (IADDR[3] = '0') : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page, the B1/E1 value page, the Monitor error count page and the received B1/E1 byte.

IADDR[3:0]	RAM Page
0000	STS-1 path Configuration page
0001	PRBS[22:7] page
0010	PRBS[6:0] page

<b>IADDR[3:0]</b>	<b>RAM Page</b>
0011	Reserved
0100	Monitor error count page
0101	Reserved

Four pages are defined for the generator (IADDR [3] = '1') : the configuration page, the PRBS[22:7] page, the PRBS[6:0] page and the B1/E1 value.

<b>IADDR[3:0]</b>	<b>RAM page</b>
1000	STS-1 path Configuration page
1001	PRBS[22:7] page
1010	PRBS[6:0] page
1011	Reserved

### RDWRB

The active high read and active low write (RDWRB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RDWRB is set to logic one, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transfer to the Indirect Data Register. When RDWRB is set to logic zero, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transfer to the addressed location in the internal RAM.

### BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic one upon writing to the Indirect Address Register. BUSY is set to logic zero, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

**Register 081h: PPP Indirect Data**

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

This register contains the data read from the internal RAM after an indirect read operation or the data to be inserted into the internal RAM in an indirect write operation.

**DATA[15:0]**

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RDWRB is set to logic one (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RDWRB is set to logic zero (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which page of the internal RAM is being accessed.

**Register 081h (IADDR = 0h): PPP Monitor STS-1 path Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SEQ_PRBSB	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	W	RESYNC	0
Bit 2	R/W	INV_PRBS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	MON_ENA	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 0h (IADDR[3:0] is “0h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured

**MON\_ENA**

Monitor Enable register bit, enables the PRBS monitor for the STS-1 path specified in the PATH[3:0] of register 050h (TPP Indirect Address). If MON\_ENA is set to ‘1’, a PRBS sequence is generated and compare to the incoming one inserted in the payload of the SONET/SDH frame. If MON\_ENA is low, the data at the input of the monitor is ignored.

**INV\_PRBS**

This sets the monitor to invert the PRBS before comparing it to the internally generated payload. When set high, the PRBS bytes will be inverted, else they will be compared unmodified.

**RESYNC**

This sets the monitor to re-initialize the PRBS sequence. When set high the monitor’s state machine will be forced in the Out Of Sync state and automatically try to resynchronize to the incoming stream.

SEQ\_PRBSB

This bit enables the monitoring of a PRBS or sequential pattern inserted in the payload. When low the payload contains PRBS bytes, and when high, a sequential pattern is monitored.

Reserved

The reserved bits must be set low for correct operation of the SBS.

**Register 081h (IADDR = 1h): PPP Monitor PRBS[22:7] Accumulator**

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 1h (IADDR[3:0] is “1h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[22:7]**

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.



**Register 081h (IADDR = 2h): PPP Monitor PRBS[6:0] Accumulator**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 2h (IADDR[3:0] is “2h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[7:0]**

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 081h (IADDR = 4h): PPP Monitor Error count**

Bit	Type	Function	Default
Bit 15	R	ERR_CNT[15]	X
Bit 14	R	ERR_CNT[14]	X
Bit 13	R	ERR_CNT[13]	X
Bit 12	R	ERR_CNT[12]	X
Bit 11	R	ERR_CNT[11]	X
Bit 10	R	ERR_CNT[10]	X
Bit 9	R	ERR_CNT[9]	X
Bit 8	R	ERR_CNT[8]	X
Bit 7	R	ERR_CNT[7]	X
Bit 6	R	ERR_CNT[6]	X
Bit 5	R	ERR_CNT[5]	X
Bit 4	R	ERR_CNT[4]	X
Bit 3	R	ERR_CNT[3]	X
Bit 2	R	ERR_CNT[2]	X
Bit 1	R	ERR_CNT[1]	X
Bit 0	R	ERR_CNT[0]	X

This register contains the definition of the PPP Indirect Data register (Register 061h) when accessing Indirect Address 4h (IADDR[3:0] is “4h” in register 060h).

**ERR\_CNT[15:0]**

The ERR\_CNT[15:0] register contains the cumulative number of errors in the PRBS bytes since the last error reporting event. Errors are accumulated only when the monitor is in the synchronized state. Each PRBS byte will only contribute a single error, even if there are multiple errors within a single PRBS byte. The transfer of the error counter to this holding register is triggered by an indirect write to this register or by writing the SBS Master Signal Monitor #1, Accumulation Trigger Register (014H). The error counter is cleared and restarted after its value is transferred to the ERR\_CNT[15:0] holding register. No errors are missed during the transfer. The error counter will not wrap around after reaching FFFFh, it will saturate at this value.

**Register 081h (IADDR = 8h): PPP Generator STS-1 path Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	Reserved	0
Bit 12	R/W	LINKENA	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	X
Bit 8	R/W	LINKENA	X
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	SEQ_PRBSB	0
Bit 4	R/W	Reserved	0
Bit 3	W	FORCE_ERR	0
Bit 2		Unused	
Bit 1	R/W	INV_PRBS	0
Bit 0	R/W	Reserved	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 8h (IADDR[3:0] is “8h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

**INV\_PRBS**

Sets the generator to invert the PRBS before inserting it in the payload. When set high, the PRBS bytes will be inverted, else they will be inserted unmodified.

**FORCE\_ERR**

The Force Error bit is used to force bit errors in the inserted pattern. When a logic one is written, the MSB of the next byte will be inverted, inducing a single bit error. The register clears itself when the operation is complete.

**SEQ\_PRBSB**

This bit enables the insertion of a PRBS sequence or a sequential pattern in the payload. When low, the payload is filled with PRBS bytes, and when high, a sequential pattern is inserted.

LINKENA

These two bits specify if PRBS is to be inserted in the path through the TP8E. If LINKENA is high patterns are generated in the SONET/SDH frame to the TP8E, else no pattern is generated and the unmodified SONET/SDH input frame is passed to the TP8E.

Reserved

The reserved bits must be set low for correct operation of the SBS.

**Register 081h (IADDR = 9h): PPP Generator PRBS[22:7] Accumulator**

Bit	Type	Function	Default
Bit 15	R/W	PRBS[22]	0
Bit 14	R/W	PRBS[21]	0
Bit 13	R/W	PRBS[20]	0
Bit 12	R/W	PRBS[19]	0
Bit 11	R/W	PRBS[18]	0
Bit 10	R/W	PRBS[17]	0
Bit 9	R/W	PRBS[16]	0
Bit 8	R/W	PRBS[15]	0
Bit 7	R/W	PRBS[14]	0
Bit 6	R/W	PRBS[13]	0
Bit 5	R/W	PRBS[12]	0
Bit 4	R/W	PRBS[11]	0
Bit 3	R/W	PRBS[10]	0
Bit 2	R/W	PRBS[9]	0
Bit 1	R/W	PRBS[8]	0
Bit 0	R/W	PRBS[7]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address 9h (IADDR[3:0] is “9h” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[22:7]**

The PRBS[22:7] register are the 16 MSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 081h (IADDR = Ah): PPP Generator PRBS[6:0] Accumulator**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	PRBS[6]	0
Bit 5	R/W	PRBS[5]	0
Bit 4	R/W	PRBS[4]	0
Bit 3	R/W	PRBS[3]	0
Bit 2	R/W	PRBS[2]	0
Bit 1	R/W	PRBS[1]	0
Bit 0	R/W	PRBS[0]	0

This register contains the definition of the PPP Indirect Data register (Register 081h) when accessing Indirect Address Ah (IADDR[3:0] is “Ah” in register 080h).

For STS-Nc rates, only the first STS-1 has to be configured.

**PRBS[6:0]**

The PRBS[6:0] register are the 7 LSBs of the LFSR state of the STS-1 path specified in the Indirect Addressing register. It is possible to write in this register to change the initial state of the register.

**Register 082h: PPP Generator Payload Configuration**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	GEN_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	GEN_STS3C[3]	0
Bit 2	R/W	GEN_STS3C[2]	0
Bit 1	R/W	GEN_STS3C[1]	0
Bit 0	R/W	GEN_STS3C[0]	0

This register configures the payload type of the time-slots in the Incoming bus for processing by the Protect PRBS generator.

**GEN\_STS3C[0]**

The STS-3c/VC-4 payload configuration (GEN\_STS3C[0]) bit selects the payload configuration. When GEN\_STS3C[0] is set to logic one, the STS-1/VC-3 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[0] is set to logic zero, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[0] register bit.

**GEN\_STS3C[1]**

The STS-3c/VC-4 payload configuration (GEN\_STS3C[1]) bit selects the payload configuration. When GEN\_STS3C[1] is set to logic one, the STS-1/VC-3 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[1] is set to logic zero, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[1] register bit.

#### GEN\_STS3C[2]

The STS-3c/VC-4 payload configuration (GEN\_STS3C[2]) bit selects the payload configuration. When GEN\_STS3C[2] is set to logic one, the STS-1/VC-3 paths #3, #7 and #11 are part of a STS-3cVC-4 payload. When GEN\_STS3C[2] is set to logic zero, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[2] register bit.

#### GEN\_STS3C[4]

The STS-3c/VC-4 payload configuration (GEN\_STS3C[3]) bit selects the payload configuration. When GEN\_STS3C[3] is set to logic one, the STS-1/VC-3 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When GEN\_STS3C[3] is set to logic zero, the paths are STS-1/VC-3 payloads. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[3] register bit.

#### GEN\_STS12C

The STS-12c/VC-4-4c payload configuration (GEN\_STS12C) bit selects the payload configuration. When GEN\_STS12C is set to logic one, the timeslots #1 to #12 are part of the same concatenated payload defined by GEN\_MSSLEN. When GEN\_STS12C is set to logic zero, the STS-1/STM-0 paths are defined with the GEN\_STS3C[3:0] register bit. The GEN\_STS12C register bit has precedence over the GEN\_STS3C[3:0] register bit.

#### Reserved

The Reserved bits must be set low for correct operation of the SBS.



**Register 083h: PPP Monitor Payload Configuration**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	MON_STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MON_STS3C[3]	0
Bit 2	R/W	MON_STS3C[2]	0
Bit 1	R/W	MON_STS3C[1]	0
Bit 0	R/W	MON_STS3C[0]	0

This register configures the payload type of the time-slots in the Receive Protection Serial Link for processing by the PRBS monitor section.

**MON\_STS3C[0]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[0]) bit selects the payload configuration. When MON\_STS3C[0] is set to logic one, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c/VC-4 payload. When MON\_STS3C[0] is set to logic zero, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[0] register bit.

**MON\_STS3C[1]**

The STS-3c/VC-4 payload configuration (MON\_STS3C[1]) bit selects the payload configuration. When MON\_STS3C[1] is set to logic one, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c/VC-4 payload. When MON\_STS3C[1] is set to logic zero, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[1] register bit.

#### MON\_STS3C[2]

The STS-3c/VC-4 payload configuration (MON\_STS3C[2]) bit selects the payload configuration. When MON\_STS3C[2] is set to logic one, the STS-1/STM-0 paths #3, #7 and #11 are part of a MON\_STS-3c/VC-4 payload. When MON\_STS3C[2] is set to logic zero, the paths are STS-1 (VC-3) payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[2] register bit.

#### MON\_STS3C[4]

The STS-3c/VC-4 payload configuration (MON\_STS3C[3]) bit selects the payload configuration. When MON\_STS3C[3] is set to logic one, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c/VC-4 payload. When MON\_STS3C[3] is set to logic zero, the paths are STS-1/VC-3 payloads. The MON\_STS12C register bit has precedence over the MON\_STS3C[3] register bit.

#### MON\_STS12C

The STS-12c/VC-4-4c payload configuration (MON\_STS12C) bit selects the payload configuration. When MON\_STS12C is set to logic one, the timeslots #1 to #12 are part of the same concatenated payload defined by MON\_MSSLEN. When MON\_STS12C is set to logic zero, the STS-1/STM-0 paths are defined with the MON\_STS3C[3:0] register bit. The MON\_STS12C register bit has precedence over the MON\_STS3C[3:0] register bit.

#### Reserved

The Reserved bits must be set low for correct operation of the SBS.

**Register 084h: PPP Monitor Byte Error Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_ERRI	X
Bit 10	R	MON11_ERRI	X
Bit 9	R	MON10_ERRI	X
Bit 8	R	MON9_ERRI	X
Bit 7	R	MON8_ERRI	X
Bit 6	R	MON7_ERRI	X
Bit 5	R	MON6_ERRI	X
Bit 4	R	MON5_ERRI	X
Bit 3	R	MON4_ERRI	X
Bit 2	R	MON3_ERRI	X
Bit 1	R	MON2_ERRI	X
Bit 0	R	MON1_ERRI	X

This register reports and acknowledges PRBS byte error interrupts for all the time-slots in the Receive Protection Serial Link.

**MON<sub>x</sub>\_ERRI**

The Monitor Byte Error Interrupt Status register is the status of the interrupt generated by each of the 12 STS-1 paths when an error has been detected. The MON<sub>x</sub>\_ERRI is set high when the monitor is in the synchronized state and when an error in a PRBS byte is detected in the STS-1 path **x**. This bit is independent of MON<sub>x</sub>\_ERRE and is cleared after being read.

**Register 085h: PPP Monitor Byte Error Interrupt Enable**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_ERRE	0
Bit 10	R/W	MON11_ERRE	0
Bit 9	R/W	MON10_ERRE	0
Bit 8	R/W	MON9_ERRE	0
Bit 7	R/W	MON8_ERRE	0
Bit 6	R/W	MON7_ERRE	0
Bit 5	R/W	MON6_ERRE	0
Bit 4	R/W	MON5_ERRE	0
Bit 3	R/W	MON4_ERRE	0
Bit 2	R/W	MON3_ERRE	0
Bit 1	R/W	MON2_ERRE	0
Bit 0	R/W	MON1_ERRE	0

This register enables the assertion of PRBS byte error interrupts for all the time-slots in the Receive Protection Serial Link.

**MON<sub>x</sub>\_ERRE**

The Monitor Byte Error Interrupt Enable register enables the interrupt for each of the 12 STS-1 paths. When MON<sub>x</sub>\_ERRE is set high it allows the Byte Error Interrupt to generate an external interrupt on INT.

**Register 089h: PPP Monitor Synchronization Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCI	X
Bit 10	R	MON11_SYNCI	X
Bit 9	R	MON10_SYNCI	X
Bit 8	R	MON9_SYNCI	X
Bit 7	R	MON8_SYNCI	X
Bit 6	R	MON7_SYNCI	X
Bit 5	R	MON6_SYNCI	X
Bit 4	R	MON5_SYNCI	X
Bit 3	R	MON4_SYNCI	X
Bit 2	R	MON3_SYNCI	X
Bit 1	R	MON2_SYNCI	X
Bit 0	R	MON1_SYNCI	X

This register reports the PRBS monitor synchronization status change interrupts for all the time-slots in the Receive Protection Serial Link.

**MON<sub>x</sub>\_SYNCI**

The Monitor Synchronization Interrupt Status register is set high when a change occurs in the monitor's synchronization status. Whenever a state machine of the **x** STS-1 path goes from Synchronized to Out Of Synchronization state or vice-versa, the **MON<sub>x</sub>\_SYNCI** is set high. This bit is independent of **MON<sub>x</sub>\_SYNCE** and is cleared after it's been read.

**Register 08Ah: PPP Monitor Synchronization Interrupt Enable**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	MON12_SYNCE	0
Bit 10	R/W	MON11_SYNCE	0
Bit 9	R/W	MON10_SYNCE	0
Bit 8	R/W	MON9_SYNCE	0
Bit 7	R/W	MON8_SYNCE	0
Bit 6	R/W	MON7_SYNCE	0
Bit 5	R/W	MON6_SYNCE	0
Bit 4	R/W	MON5_SYNCE	0
Bit 3	R/W	MON4_SYNCE	0
Bit 2	R/W	MON3_SYNCE	0
Bit 1	R/W	MON2_SYNCE	0
Bit 0	R/W	MON1_SYNCE	0

This register enables the assertion of change of PRBS monitor synchronization status interrupts for all the time-slots in the Receive Protection Serial Link.

**MON<sub>x</sub>\_SYNCE**

The Monitor Synchronization Interrupt Enable register allows each individual STS-1 path to generate an external interrupt on INT. When MON<sub>x</sub>\_SYNCE is set high whenever a change occurs in the synchronization state of the monitor in STS-1 path **x**, generates an interrupt on INT.

**Register 08Bh: PPP Monitor Synchronization State**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	MON12_SYNCV	X
Bit 10	R	MON11_SYNCV	X
Bit 9	R	MON10_SYNCV	X
Bit 8	R	MON9_SYNCV	X
Bit 7	R	MON8_SYNCV	X
Bit 6	R	MON7_SYNCV	X
Bit 5	R	MON6_SYNCV	X
Bit 4	R	MON5_SYNCV	X
Bit 3	R	MON4_SYNCV	X
Bit 2	R	MON3_SYNCV	X
Bit 1	R	MON2_SYNCV	X
Bit 0	R	MON1_SYNCV	X

This register reports the state of the PRBS monitors for all the time-slots in the Receive Protection Serial Link.

**MON<sub>x</sub>\_SYNCV**

The Monitor Synchronization Status register reflects the state of the monitor's state machine. When MON<sub>x</sub>\_SYNCV is set high the monitor's state machine is in synchronization for the STS-1 Path x. When MON<sub>x</sub>\_SYNCV is low the monitor is NOT in synchronization for the STS-1 Path x.

**Register 08Ch: PPP Performance Counters Transfer Trigger**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TIP	0

This register controls and monitors the reporting of the error counter registers.

A write in this register will trigger the transfer of the error counters to holding registers where they can be read. The value written in the register is not important. Once the transfer is initiated, the TIP bit is set high, and when the holding registers contain the value of the error counters, TIP is set low.

**TIP**

The Transfer In Progress bit reflects the state of the TIP output signal. When TIP is high, an error counter transfer has been initiated, but the counters are not transferred in the holding register yet. When TIP is low, the value of the error counters is available to be read in the holding registers. This bit can be poll after an error counters transfer request, to determine if the counters are ready to be read.



**Register 090H: WILC Transmit FIFO Data High**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 15-0	R/W	TDAT[31:16]	0

When writing data to the transmit FIFO, this register must be written to before register 091H.

TDAT[31:16]

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

**Register 091H: WILC Transmit FIFO Data Low**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 15-0	R/W	TDAT[15:0]	0

Writing to this register will initiate a transfer of TDAT[31:0] into the transmit FIFO.

TDAT[15:0]

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

**Register 093H: WILC Transmit Control Register**

Bit	Type	Function	Default
Bit 15:8	R/W	TX_AUX[7:0]	00000000
Bit 7:6	R	Unused	00
Bit 5:4	R/W	TX_LINK[1:0]	00
Bit 3:2	R	Unused	00
Bit 1	R/W	TX_CRC_SWIZ_EN	0
Bit 0	R/W	TX_BYPASS	0

**TX\_BYPASS**

When this bit is set to ‘1’, the blocks message transmit functions are bypassed. No messages are inserted into the Transmit data. The transmit message FIFO RAM is disabled and thus message data writes are ignored.

**TX\_CRC\_SWIZ\_EN**

When this bit is set to ‘1’, the calculated CRC-16 is bit reversed before being transmitted. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality.

**TX\_LINK[1:0]**

These bits are transmitted in the LINK bits of the message header of the next available message. On reads these bit return the last written value.

**TX\_AUX[7:0]**

These bits form the input to an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developers discretion. Data written to this register will be transmitted in the AUX header byte of each subsequent message to the other end of the inband link. A new value of TX\_AUX will be transmitted at the next available message. Data read from this register will be the data previously written.

**Register 095H: WILC Transmit Status and FIFO Synch Register**

Bit	Type	Function	Default
Bit 15	R	TX_MSG_LVL_VALID	X
Bit 14:13	R	TX_LINK[1:0]	00
Bit 12:11	R	IPAGE[1:0]	XX
Bit 10:8	R	IUSER[2:0]	X00
Bit 7:6	R	Unused	00
Bit 5:2	R	TX_MSG_LVL[3:0]	0000
Bit 1	R	TX_FI_BUSY	0
Bit 0	W	TX_XFER_SYNC	0

**TX\_XFER\_SYNC**

Writing ‘1’ to this bit initializes the next write sequence to be to the beginning of the next message. After a ‘1’ had been written successive writes to the Transmit FIFO will be to location zero of the next available slot. If a partial message has been written, TX\_XFER\_SYNC indicates that the current message is complete and that subsequent writes will be to the next message. If more than 32 bytes are written, the 33rd byte will be the first byte of the next message. The purpose of this bit is to unambiguously align the message boundaries. Another use would be to abandon the current write and move the write pointer to the beginning of the next message. (Previous message data will remain in the unwritten portion of the message being abandoned, which will have to be ignored by the receiving software).

If the message FIFO pointers are already at a message boundary then writing this bit to a ‘1’ will have no affect.

On reads this bit is always returned as a ‘0’.

**TX\_FI\_BUSY**

This bit indicates that the internal hardware is transferring the data from the Transmit FIFO registers (TDAT) into the internal RAM. This bit need not be read by software if the time interval between successive 32 bit transfers is greater than 3 SYSCLK cycles.

**TX\_MSG\_LVL[3:0]**

This indicates the current number of messages in the TXFIFO.

TX_MSG_LVL[3:0]	Number of Messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur. The number of free messages available in the FIFO is given by  $8 - \text{TX\_MSG\_LVL}$ .

#### IUSER[2:0]

These bits are a reflection of the USER[2:0] bits output in the header of the in-band link on the Transmit Working Serial Link. IUSER[2] is sourced from the IUSER2 input to the SBS. IUSER[1:0] is sourced from the TXWUSER[1:0] bits of register 008H.

#### IPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits output in the header of the in-band link on the Transmit Working Serial Link. PAGE[1] reflects the current memory page used by the IMSU. PAGE[0] reflects the current memory page used by the OMSU.

#### TX\_LINK[1:0]

These bits reflect the last written value of the TX\_LINK[1:0] field of the WILC Transmit Control Register. The upper byte of this register therefore reflects all of the configurable bits of the message Header1 byte.

#### TX\_MSG\_LVL\_VALID

This bit indicates that the value of TX\_MSG\_LVL is valid. When read with a logic zero this register should be re-read until TX\_MSG\_LVL\_VALID is a logic one. This bit will be clear for only approximately 0.3% of the time.

**Register 096H: WILC Receive FIFO Data High**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 15-0	R	RDAT[31:16]	0

When reading data out of the receive FIFO, this register must be read before register 097H.

RDAT[31:16]

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages. This register must be read before register 097H.

**Register 097H: WILC Receive FIFO Data Low**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 15-0	R	RDAT[15:0]	0

Reading this register initiates a read access to the next location in the receive FIFO.

RDAT[15:0]

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

**Register 099H: WILC Receive FIFO Control Register**

Bit	Type	Function	Default
Bit 15:3	R	Unused	0
Bit 2	R/W	FAST_RD_EN	0
Bit 1	R/W	RX_CRC_SWIZ_EN	0
Bit 0	R/W	RX_BYPASS	0

**RX\_BYPASS**

When this bit is set to a logic one. The WILC's message receive functions are bypassed and no messages are extracted from the Receive Working Serial Link. The receive message FIFO RAM is disabled and thus message data reads will return undefined data.

**RX\_CRC\_SWIZ\_EN**

When this bit is set to a logic one, the calculated CRC-16 is bit reversed before being compared with CRC-16 bytes of the received message. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality

**FAST\_RD\_EN**

When this bit is set to '1', the time to read the Receive FIFO is reduced by 1 SYSCLK cycle.

For receive FIFO reads induced by writing the RX\_XFER\_SYNC bit to a '1' the time for the completion of the receive FIFO read is reduced from approximately 5 SYSCLK cycles when FAST\_RD\_EN = '0' to approximately 4 SYSCLK cycles when FAST\_RD\_EN = '1'.

For receive FIFO reads induced by reading from the Receive FIFO Data register Low the time for the completion of the receive FIFO read is reduced from approximately 4 SYSCLK cycles when FAST\_RD\_EN = '0' to approximately 3 SYSCLK cycles when FAST\_RD\_EN = '1'.



**Register 09AH: WILC Receive Auxiliary Register**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 15	R	RX_STTS_VALID	X
Bit 14:8	R	Unused	0
Bit 7:0	R	RX_AUX[7:0]	00000000

**RX\_AUX[7:0]**

These bits constitute the output from an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developers' discretion. A read from this register will return the AUX header byte of the last message received (without a CRC-16 error).

**RX\_STTS\_VALID**

This bit indicates that the value of RX\_AUX is valid. When read with a '0' this register should be re-read until RX\_STTS\_VALID is a '1'. This bit will be cleared for less than 0.15% of the time.

**Register 09BH: WILC Receive Status and FIFO Synch Register**

Bit	Type	Function	Default
Bit 15	R	RX_STTS_VALID	X
Bit 14:13	R	RX_LINK[1:0]	00
Bit 12:11	R	OPAGE[1:0]	00
Bit 10:8	R	OUSER[2:0]	000
Bit 7	R	CRC_ERR	0
Bit 6	R	HDR_CRC_ERR	0
Bit 5:2	R	RX_MSG_LVL[3:0]	0000
Bit 1	R	RX_FI_BUSY	0
Bit 0	R	RX_SYNC_DONE	X
Bit 0	W	RX_XFER_SYNC	0

When this register is read, it returns the status for the Receive Message Channel. When a logic one is written into bit 0 of this register, it is used to synchronize the Receive FIFO to the start of a message boundary or perform a message skip.

## RX\_XFER\_SYNC

Writing a logic one to this bit initiates a read sequence from the start of the next *unread* message. The hardware aligns the message read buffer address to the start of the next *unread* message and prefetches the first Dword from the *unread* message buffer so that it is ready to be read from the WILC Receive FIFO Data registers.

An *unread* message in this context means that the s/w has not read any of the message payload data by reading the WILC Receive FIFO Data registers.

After the RX XFER SYNC process has been completed successive reads from the Receive FIFO return the last Dword read from the Receive FIFO and prefetch the next Dword (when available).

This bit must be written to a logic one at the start of a message read sequence.

When multiple complete messages are being read (software knows that there is more than one message in the FIFO using the RX\_MSG\_LVL bits) this bit does not need to be written between individual message reads. It must be written for the 1<sup>st</sup> message.

When software uses a variable length message protocol it may want to abandon reading a message buffer before reading the entire message buffer of 8 DWords (16 Words). In this case this bit must be written with a '1' to move the message pointer to the start of the next message buffer before starting the read of that buffer.

After writing this bit with a logic one software should not start reading the FIFO until the RX\_FI\_BUSY bit has cleared.

In the worst case this will take 5 SYSCLK cycles when FAST\_RD\_EN = '1' and 4 SYSCLK cycles when FAST\_RD\_EN = '0'.

At this point the 1<sup>st</sup> DWORD of the message is available for reading and the CRC\_ERR bit is valid. Software may abandon a CRC errored message without reading the message buffer by writing this bit with a logic one again.

On reads this bit is always returns the RX\_SYNC\_DONE status.

## RX\_SYNC\_DONE

This bit indicates the status of an RX\_XFER\_SYNC operation. When this bit is a logic one it indicates that an RX\_XFER\_SYNC has been done. S/W should check this bit at the start of a message read sequence or when attempting to perform a message skip sequence.

**RX\_FI\_BUSY**

This bit indicates that the internal hardware is transferring data from the Receive FIFO RAM into the Receive FIFO registers. The bit is set following a write to this register with the RX\_XFER\_SYNC bit set or following a read from the WILC Receive FIFO Data Low register.

Following an RX\_XFER\_SYNC write this bit need not be read by software if the time interval to the successive Receive FIFO DATA register read is greater than approximately 5 SYSCLK cycles when FAST\_RD\_EN = '1' or approximately 4 SYSCLK cycles when FAST\_RD\_EN = '0'.

This bit need not be read by software if the time interval between successive Receive FIFO DATA register reads greater than approximately 4 SYSCLK cycles when FAST\_RD\_EN = '1' or approximately 3 SYSCLK cycles when FAST\_RD\_EN = '0'.

This means between a read access from the WILC Received FIFO Data Low register and a read from the WILC Received FIFO Data High register. Note that there is no time restriction between a read accesses from the WILC Received FIFO Data High register and a read from the WILC Received FIFO Data Low register

**RX\_MSG\_LVL[3:0]**

This indicates the current number of messages in the Receive FIFO.

<b>RX_MSG_LVL[3:0]</b>	<b>Number of Messages</b>
0000	0
:	:
1000	8

Values greater than 1000 will not occur.

**HDR\_CRC\_ERR**

If this bit is set to a logic one, the last message slot received was received with an errored CRC-16 field. This bits is updated every message slot. This bit is provided as status only.

**CRC\_ERR**

If this bit it set to '1', the message at the head of the Receive FIFO has an errored CRC-16 field.

The usual sequence would be to read this register before reading the message buffer to check if the message buffer that will be read from next has been received with a CRC error. If a Receive FIFO Synchronization has been started the value of this bit is invalid until the RX\_XFER\_SYNC operation has completed. When FAST\_RD\_EN is a logic one this bit is valid when RX\_FI\_BUSY is a logic zero following a Receive FIFO Synchronization. When FAST\_RD\_EN is a logic zero the values of RX\_FI\_BUSY and CRC\_ERR change concurrently and a further read should be made after RX\_FI\_BUSY is sampled as a logic zero before checking the value of this bit.

#### OUSER[2:0]

These bits are a reflection of the USER[2:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Working Serial Link. OUSER[2] is output from the SBS on OUSER2 when the Working Serial Link is selected.

#### OPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Working Serial Link. When the Working Serial Link is selected, OPAGE[1] controls the active page of the IMSU and OPAGE[0] controls the active page of the OMSU.

#### RX\_LINK[1:0]

These bits are a reflection of the LINK[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Working Serial Link.

#### RX\_STTS\_VALID

This bit indicates that the values of RX\_MSG\_LVL , RX\_LINK, OPAGE, OUSER are valid. When read with a logic zero this register should be re-read until RX\_STTS\_VALID is a logic one. This bit will be cleared for only approximately 0.15% of time.

**Register 09DH: WILC Interrupt Enable and Control Register.**

Bit	Type	Function	Default
Bit 15:13	R	Unused	000
Bit 12:11	R/W	RX_TIMEOUT_VAL[1:0]	00
Bit 10:8	R/W	RX_THRESHOLD_VAL[2:0]	101
Bit 7	R	Unused	0
Bit 6	R/W	RX_TIMEOUTE	0
Bit 5	R/W	RX_THRSHLDE	0
Bit 4	R/W	RX_OVFLWE	0
Bit 3	R/W	RX_LINK_CHGE	0
Bit 2:1	R/W	OPAGE_CHGE[1:0]	00
Bit 0	R/W	OUSER0_CHGE	0

**OUSER0\_CHGE**

Writing a logic one to the RX\_OUSER0\_CHGE bit enables the generation of an interrupt on a change of state from a logic zero to a logic one of received message header bit OUSER[0].

**OPAGE\_CHGE[1:0]**

Writing a logic one to the OPAGE\_CHGE[n] bit enables the generation of an interrupt on a change of state of the received PAGE bits. The OPAGE bits that changed value are indicated by a logic one in the corresponding OPAGE\_CHGI[n].

**RX\_LINK\_CHGE**

Writing a logic one to the RX\_LINK\_CHGE bit enables the generation of an interrupt on a change of state of the received LINK bits. When either of the received LINK bits has changed value the RX\_LINK\_CHGI bit will be set to a logic one.

**RX\_OVFLWE**

Writing a logic one to the RX\_OVFLWE bit enables the generation of an interrupt when RX\_OVFLWI is a logic one.

**RX\_THRSHLDE**

Writing a logic one to the RX\_THRSHLDE bit enables the generation of an interrupt when RX\_THRSHLDI is a logic one.

**RX\_TIMEOUTE**

Writing a logic one to the RX\_TIMEOUTE bit enables the generation of an interrupt when RX\_TIMEOUTI is a logic one.

**RX\_THRESHOLD\_VAL[2:0]**

Variable Threshold dictates the minimum number of messages required to be in the RXFIFO before an interrupt is generated. '000' = 1 message '111' = 8 messages.

<b>RX_THRESHOLD_VAL[2:0]</b>	<b>Messages</b>
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

**RX\_TIMEOUT\_VAL[1:0]**

These bits specify a variable delay, relative to a read from the receive message FIFO, in steps of 125 us, before an interrupt is generated, if the Receive FIFO level is greater than 0. The objective is to stop stale messages collecting in the RXFIFO.

<b>RX_TIMEOUT_VAL[1:0]</b>	<b>Nominal Delay In Frames</b>	<b>Minimum Delay from Message Reception</b>	<b>Maximum Delay from Message Reception</b>	<b>Minimum Delay from FIFO read</b>	<b>Maximum Delay from FIFO read</b>
00	1	152 $\mu$ s	222 $\mu$ s	125 $\mu$ s	250 $\mu$ s
01	2	277 $\mu$ s	347 $\mu$ s	250 $\mu$ s	375 $\mu$ s
10	3	402 $\mu$ s	472 $\mu$ s	375 $\mu$ s	500 $\mu$ s
11	4	527 $\mu$ s	597 $\mu$ s	500 $\mu$ s	625 $\mu$ s

**Register 09FH: WILC Interrupt Reason Register**

Bit	Type	Function	Default
Bit 15:7	R	Unused	0
Bit 6	R	RX_TIMEOUTI	0
Bit 5	R	RX_THRSHLDI	0
Bit 4	R	RX_OVFLWI	0
Bit 3	R	RX_LINK_CHGI	0
Bit 2:1	R	OPAGE_CHGI[1:0]	00
Bit 0	R	OUSER0_CHGI	0

This register contains the status of events that may be enabled to generate interrupts..

All bits in this register are cleared on read.

**OUSER0\_CHGI**

A logic one in this bit indicates that the last received value of the OUSER[0] header bit has changed from a ‘0’ to a ‘1’ from the previously received values. This bit is cleared on a read.

**OPAGE\_CHGI[1:0]**

A logic one in these bits indicates that the last received value of the corresponding OPAGE[1:0] header bits has changed from the previously received values. These bits are cleared on read.

**RX\_LINK\_CHGI**

A logic one in this bit indicates that the last received value of the LINK[1:0] header bits has changed from the previously received values. This bit is cleared on a read.

**RX\_OVFLWI**

A logic one in this bit indicates that a Receive FIFO Overflow has occurred. This bit is cleared on a read.

**RX\_THRSHLDI**

A logic one in this bit indicates that the Receive FIFO Threshold has been reached. This bit is cleared on a read.

**RX\_TIMEOUTI**

A logic one in this bit indicates a Receive FIFO Timeout. This bit is cleared on read.



**Register 0A0H: PILC Transmit FIFO Data High**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 15-0	R/W	TDAT[31:16]	0

When writing data to the transmit FIFO, this register must be written to before register 0A1H.

TDAT[31:16]

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

**Register 0A1H: PILC Transmit FIFO Data Low**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 15-0	R/W	TDAT[15:0]	0

Writing to this register will initiate a transfer of TDAT[31:0] into the transmit FIFO.

TDAT[15:0]

TDAT[31:16] and TDAT[15:0] form the 32 bit wide data word to be written to the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

**Register 0A3H: PILC Transmit Control Register**

Bit	Type	Function	Default
Bit 15:8	R/W	TX_AUX[7:0]	00000000
Bit 7:6	R	Unused	00
Bit 5:4	R/W	TX_LINK[1:0]	00
Bit 3:2	R	Unused	00
Bit 1	R/W	TX_CRC_SWIZ_EN	0
Bit 0	R/W	TX_BYPASS	0

**TX\_BYPASS**

When this bit is set to ‘1’, the blocks message transmit functions are bypassed. No messages are inserted into the Transmit data. The transmit message FIFO RAM is disabled and thus message data writes are ignored.

**TX\_CRC\_SWIZ\_EN**

When this bit is set to ‘1’, the calculated CRC-16 is bit reversed before being transmitted. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality.

**TX\_LINK[1:0]**

These bits are transmitted in the LINK bits of the message header of the next available message. On reads these bit return the last written value.

**TX\_AUX[7:0]**

These bits form the input to an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developers discretion. Data written to this register will be transmitted in the AUX header byte of each subsequent message to the other end of the inband link. A new value of TX\_AUX will be transmitted at the next available message. Data read from this register will be the data previously written.

**Register 0A5H: PILC Transmit Status and FIFO Synch Register**

Bit	Type	Function	Default
Bit 15	R	TX_MSG_LVL_VALID	X
Bit 14:13	R	TX_LINK[1:0]	00
Bit 12:11	R	IPAGE[1:0]	XX
Bit 10:8	R	IUSER[2:0]	X00
Bit 7:6	R	Unused	00
Bit 5:2	R	TX_MSG_LVL[3:0]	0000
Bit 1	R	TX_FI_BUSY	0
Bit 0	W	TX_XFER_SYNC	0

**TX\_XFER\_SYNC**

Writing ‘1’ to this bit initializes the next write sequence to be to the beginning of the next message. After a ‘1’ had been written successive writes to the Transmit FIFO will be to location zero of the next available slot. If a partial message has been written, TX\_XFER\_SYNC indicates that the current message is complete and that subsequent writes will be to the next message. If more than 32 bytes are written, the 33rd byte will be the first byte of the next message. The purpose of this bit is to unambiguously align the message boundaries. Another use would be to abandon the current write and move the write pointer to the beginning of the next message. (Previous message data will remain in the unwritten portion of the message being abandoned, which will have to be ignored by the receiving software).

If the message FIFO pointers are already at a message boundary then writing this bit to a ‘1’ will have no affect.

On reads this bit is always returned as a ‘0’.

**TX\_FI\_BUSY**

This bit indicates that the internal hardware is transferring the data from the Transmit FIFO registers (TDAT) into the internal RAM. This bit need not be read by software if the time interval between successive 32 bit transfers is greater than 3 SYSCLK cycles.

**TX\_MSG\_LVL[3:0]**

This indicates the current number of messages in the TXFIFO.

TX_MSG_LVL[3:0]	Number of Messages
0000	0
:	:
1000	8

Values greater than 1000 will not occur. The number of free messages available in the FIFO is given by  $8 - \text{TX\_MSG\_LVL}$ .

#### IUSER[2:0]

These bits are a reflection of the USER[2:0] bits output in the header of the in-band link on the Transmit Protection Serial Link. IUSER[2] is sourced from the IUSER2 input to the SBS. IUSER[1:0] is sourced from the TXWUSER[1:0] bits of register 008H.

#### IPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits output in the header of the in-band link on the Transmit Protection Serial Link. PAGE[1] reflects the current memory page used by the IMSU. PAGE[0] reflects the current memory page used by the OMSU.

#### TX\_LINK[1:0]

These bits reflect the last written value of the TX\_LINK[1:0] field of the PILC Transmit Control Register. The upper byte of this register therefore reflects all of the configurable bits of the message Header1 byte.

#### TX\_MSG\_LVL\_VALID

This bit indicates that the value of TX\_MSG\_LVL is valid. When read with a logic zero this register should be re-read until TX\_MSG\_LVL\_VALID is a logic one. This bit will be clear for only approximately 0.3% of the time.

**Register 0A6H: PILC Receive FIFO Data High**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 15-0	R	RDAT[31:16]	0

When reading data out of the receive FIFO, this register must be read before register 0A7H.

RDAT[31:16]

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages. This register must be read before register 097H.

**Register 0A7H: PILC Receive FIFO Data Low**

<b>Bit</b>	<b>Type</b>	<b>Function</b>	<b>Default</b>
Bit 15-0	R	RDAT[15:0]	0

Reading this register initiates a read access to the next location in the receive FIFO.

RDAT[15:0]

RDAT[31:16] and RDAT[15:0] form the 32 bit wide data word read from the FIFO. The FIFO is organized as 32 bits wide and 64 words deep, giving a total of eight 32 byte messages.

**Register 0A9H: PILC Receive FIFO Control Register**

Bit	Type	Function	Default
Bit 15:3	R	Unused	0
Bit 2	R/W	FAST_RD_EN	0
Bit 1	R/W	RX_CRC_SWIZ_EN	0
Bit 0	R/W	RX_BYPASS	0

**RX\_BYPASS**

When this bit is set to a logic one. The PILC's message receive functions are bypassed and no messages are extracted from the Receive Working Serial Link. The receive message FIFO RAM is disabled and thus message data reads will return undefined data.

**RX\_CRC\_SWIZ\_EN**

When this bit is set to a logic one, the calculated CRC-16 is bit reversed before being compared with CRC-16 bytes of the received message. This facility can be used for diagnostic testing of CRC-16 generation and checking functionality

**FAST\_RD\_EN**

When this bit is set to '1', the time to read the Receive FIFO is reduced by 1 SYSCLK cycle.

For receive FIFO reads induced by writing the RX\_XFER\_SYNC bit to a '1' the time for the completion of the receive FIFO read is reduced from approximately 5 SYSCLK cycles when FAST\_RD\_EN = '0' to approximately 4 SYSCLK cycles when FAST\_RD\_EN = '1'.

For receive FIFO reads induced by reading from the Receive FIFO Data register Low the time for the completion of the receive FIFO read is reduced from approximately 4 SYSCLK cycles when FAST\_RD\_EN = '0' to approximately 3 SYSCLK cycles when FAST\_RD\_EN = '1'.



**Register 0AAH: PILC Receive Auxiliary Register**

Bit	Type	Function	Default
Bit 15	R	RX_STTS_VALID	X
Bit 14:8	R	Unused	0
Bit 7:0	R	RX_AUX[7:0]	00000000

**RX\_AUX[7:0]**

These bits constitute the output from an Auxiliary channel between CPUs at each end of the link. Their use is at the Software developers' discretion. A read from this register will return the AUX header byte of the last message received (without a CRC-16 error).

**RX\_STTS\_VALID**

This bit indicates that the value of RX\_AUX is valid. When read with a '0' this register should be re-read until RX\_STTS\_VALID is a '1'. This bit will be cleared for less than 0.15% of the time.

**Register 0ABH: PILC Receive Status and FIFO Synch Register**

Bit	Type	Function	Default
Bit 15	R	RX_STTS_VALID	X
Bit 14:13	R	RX_LINK[1:0]	00
Bit 12:11	R	OPAGE[1:0]	00
Bit 10:8	R	OUSER[2:0]	000
Bit 7	R	CRC_ERR	0
Bit 6	R	HDR_CRC_ERR	0
Bit 5:2	R	RX_MSG_LVL[3:0]	0000
Bit 1	R	RX_FI_BUSY	0
Bit 0	R	RX_SYNC_DONE	X
Bit 0	W	RX_XFER_SYNC	0

When this register is read, it returns the status for the Receive Message Channel. When a logic one is written into bit 0 of this register, it is used to synchronize the Receive FIFO to the start of a message boundary or perform a message skip.

## RX\_XFER\_SYNC

Writing a logic one to this bit initiates a read sequence from the start of the next *unread* message. The hardware aligns the message read buffer address to the start of the next *unread* message and prefetches the first Dword from the *unread* message buffer so that it is ready to be read from the WILC Receive FIFO Data registers.

An *unread* message in this context means that the s/w has not read any of the message payload data by reading the WILC Receive FIFO Data registers.

After the RX XFER SYNC process has been completed successive reads from the Receive FIFO return the last Dword read from the Receive FIFO and prefetch the next Dword (when available).

This bit must be written to a logic one at the start of a message read sequence.

When multiple complete messages are being read (software knows that there is more than one message in the FIFO using the RX\_MSG\_LVL bits) this bit does not need to be written between individual message reads. It must be written for the 1<sup>st</sup> message.

When software uses a variable length message protocol it may want to abandon reading a message buffer before reading the entire message buffer of 8 DWords (16 Words). In this case this bit must be written with a '1' to move the message pointer to the start of the next message buffer before starting the read of that buffer.

After writing this bit with a logic one software should not start reading the FIFO until the RX\_FI\_BUSY bit has cleared.

In the worst case this will take 5 SYSCLK cycles when FAST\_RD\_EN = '1' and 4 SYSCLK cycles when FAST\_RD\_EN = '0'.

At this point the 1<sup>st</sup> DWORD of the message is available for reading and the CRC\_ERR bit is valid. Software may abandon a CRC errored message without reading the message buffer by writing this bit with a logic one again.

On reads this bit is always returns the RX\_SYNC\_DONE status.

## RX\_SYNC\_DONE

This bit indicates the status of an RX\_XFER\_SYNC operation. When this bit is a logic one it indicates that an RX\_XFER\_SYNC has been done. S/W should check this bit at the start of a message read sequence or when attempting to perform a message skip sequence.

**RX\_FI\_BUSY**

This bit indicates that the internal hardware is transferring data from the Receive FIFO RAM into the Receive FIFO registers. The bit is set following a write to this register with the RX\_XFER\_SYNC bit set or following a read from the PILC Receive FIFO Data Low register.

Following an RX\_XFER\_SYNC write this bit need not be read by software if the time interval to the successive Receive FIFO DATA register read is greater than approximately 5 SYSCLK cycles when FAST\_RD\_EN = '1' or approximately 4 SYSCLK cycles when FAST\_RD\_EN = '0'.

This bit need not be read by software if the time interval between successive Receive FIFO DATA register reads greater than approximately 4 SYSCLK cycles when FAST\_RD\_EN = '1' or approximately 3 SYSCLK cycles when FAST\_RD\_EN = '0'.

This means between a read access from the PILC Received FIFO Data Low register and a read from the PILC Received FIFO Data High register. Note that there is no time restriction between a read accesses from the PILC Received FIFO Data High register and a read from the PILC Received FIFO Data Low register

**RX\_MSG\_LVL[3:0]**

This indicates the current number of messages in the Receive FIFO.

<b>RX_MSG_LVL[3:0]</b>	<b>Number of Messages</b>
0000	0
:	:
1000	8

Values greater than 1000 will not occur.

**HDR\_CRC\_ERR**

If this bit is set to a logic one, the last message slot received was received with an errored CRC-16 field. This bits is updated every message slot. This bit is provided as status only.

**CRC\_ERR**

If this bit it set to '1', the message at the head of the Receive FIFO has an errored CRC-16 field.

The usual sequence would be to read this register before reading the message buffer to check if the message buffer that will be read from next has been received with a CRC error. If a Receive FIFO Synchronization has been started the value of this bit is invalid until the RX\_XFER\_SYNC operation has completed. When FAST\_RD\_EN is a logic one this bit is valid when RX\_FI\_BUSY is a logic zero following a Receive FIFO Synchronization. When FAST\_RD\_EN is a logic zero the values of RX\_FI\_BUSY and CRC\_ERR change concurrently and a further read should be made after RX\_FI\_BUSY is sampled as a logic zero before checking the value of this bit.

#### OUSER[2:0]

These bits are a reflection of the USER[2:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Protection Serial Link. OUSER[2] is output from the SBS on OUSER2 when the Protection Serial Link is selected.

#### OPAGE[1:0]

These bits are a reflection of the PAGE[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Protection Serial Link. When the Protection Serial Link is selected, OPAGE[1] controls the active page of the IMSU and OPAGE[0] controls the active page of the OMSU.

#### RX\_LINK[1:0]

These bits are a reflection of the LINK[1:0] bits received in the message header of the latest received message (without a CRC-16 error) on the Protection Serial Link.

#### RX\_STTS\_VALID

This bit indicates that the values of RX\_MSG\_LVL , RX\_LINK, OPAGE, OUSER are valid. When read with a logic zero this register should be re-read until RX\_STTS\_VALID is a logic one. This bit will be cleared for only approximately 0.15% of time.

**Register 0ADH: PILC Interrupt Enable and Control Register.**

Bit	Type	Function	Default
Bit 15:13	R	Unused	000
Bit 12:11	R/W	RX_TIMEOUT_VAL[1:0]	00
Bit 10:8	R/W	RX_THRESHOLD_VAL[2:0]	101
Bit 7	R	Unused	0
Bit 6	R/W	RX_TIMEOUTE	0
Bit 5	R/W	RX_THRSHLDE	0
Bit 4	R/W	RX_OVFLWE	0
Bit 3	R/W	RX_LINK_CHGE	0
Bit 2:1	R/W	OPAGE_CHGE[1:0]	00
Bit 0	R/W	OUSER0_CHGE	0

**OUSER0\_CHGE**

Writing a logic one to the RX\_OUSER0\_CHGE bit enables the generation of an interrupt on a change of state from a logic zero to a logic one of received message header bit OUSER[0].

**OPAGE\_CHGE[1:0]**

Writing a logic one to the OPAGE\_CHGE[n] bit enables the generation of an interrupt on a change of state of the received PAGE bits. The OPAGE bits that changed value are indicated by a logic one in the corresponding OPAGE\_CHGI[n].

**RX\_LINK\_CHGE**

Writing a logic one to the RX\_LINK\_CHGE bit enables the generation of an interrupt on a change of state of the received LINK bits. When either of the received LINK bits has changed value the RX\_LINK\_CHGI bit will be set to a logic one.

**RX\_OVFLWE**

Writing a logic one to the RX\_OVFLWE bit enables the generation of an interrupt when RX\_OVFLWI is a logic one.

**RX\_THRSHLDE**

Writing a logic one to the RX\_THRSHLDE bit enables the generation of an interrupt when RX\_THRSHLDI is a logic one.

RX\_TIMEOUTE

Writing a logic one to the RX\_TIMEOUTE bit enables the generation of an interrupt when RX\_TIMEOUTI is a logic one.

RX\_THRESHOLD\_VAL[2:0]

Variable Threshold dictates the minimum number of messages required to be in the RXFIFO before an interrupt is generated. '000' = 1 message '111' = 8 messages.

RX_THRESHOLD_VAL[2:0]	Messages
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

RX\_TIMEOUT\_VAL[1:0]

These bits specify a variable delay, relative to a read from the receive message FIFO, in steps of 125 us, before an interrupt is generated, if the Receive FIFO level is greater than 0. The objective is to stop stale messages collecting in the RXFIFO.

RX_TIMEOUT_VAL[1:0]	Nominal Delay In Frames	Minimum Delay from Message Reception	Maximum Delay from Message Reception	Minimum Delay from FIFO read	Maximum Delay from FIFO read
00	1	152us	222us	125us	250us
01	2	277us	347us	250us	375us
10	3	402us	472us	375us	500us
11	4	527us	597us	500us	625us

**Register 0AFH: PILC Interrupt Reason Register**

Bit	Type	Function	Default
Bit 15:7	R	Unused	0
Bit 6	R	RX_TIMEOUTI	0
Bit 5	R	RX_THRSHLDI	0
Bit 4	R	RX_OVFLWI	0
Bit 3	R	RX_LINK_CHGI	0
Bit 2:1	R	OPAGE_CHGI[1:0]	00
Bit 0	R	OUSER0_CHGI	0

This register contains the status of events that may be enabled to generate interrupts..

All bits in this register are cleared on read.

**OUSER0\_CHGI**

A logic one in this bit indicates that the last received value of the OUSER[0] header bit has changed from a '0' to a '1' from the previously received values. This bit is cleared on a read.

**OPAGE\_CHGI[1:0]**

A logic one in these bits indicates that the last received value of the corresponding OPAGE[1:0] header bits has changed from the previously received values. These bits are cleared on read.

**RX\_LINK\_CHGI**

A logic one in this bit indicates that the last received value of the LINK[1:0] header bits has changed from the previously received values. This bit is cleared on a read.

**RX\_OVFLWI**

A logic one in this bit indicates that a Receive FIFO Overflow has occurred. This bit is cleared on a read.

**RX\_THRSHLDI**

A logic one in this bit indicates that the Receive FIFO Threshold has been reached. This bit is cleared on a read.

**RX\_TIMEOUTI**

A logic one in this bit indicates a Receive FIFO Timeout. This bit is cleared on read.



**Register 0B0H: TW8E Control and Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

This register provides control and reports the status of the TW8E.

**DLCV**

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the working transmit serial data stream. When this bit is set high, the encoded data is inverted to generate the complementary running disparity.

**CENTER**

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

This bit must be set once CSU lock has been achieved.

#### TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the working transmit serial data stream for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the transmit data stream. When TPINS is set low, no test pattern is inserted.

#### FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) enables FIFO overrun/underrun interrupts. An interrupt is generated on a FIFO error event if the FIFOERRE is set to logic one. No interrupt is generated if FIFOERRE is set to logic zero.

#### Reserved

These bits must be set low for correct operation of the SBS.

**Register 0B1H: TW8E Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due the detection of FIFO error.

**FIFOERRI**

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic one on a FIFO overrun/underrun error. FIFOERRI is set to logic zero when this register is read.

**Register 0B2H: TW8E Time-slot Configuration #1**

Bit	Type	Function	Default
Bit 15	R/W	TMODE8[1]	0
Bit 14	R/W	TMODE8[0]	0
Bit 13	R/W	TMODE7[1]	0
Bit 12	R/W	TMODE7[0]	0
Bit 11	R/W	TMODE6[1]	0
Bit 10	R/W	TMODE6[0]	0
Bit 9	R/W	TMODE5[1]	0
Bit 8	R/W	TMODE5[0]	0
Bit 7	R/W	TMODE4[1]	0
Bit 6	R/W	TMODE4[0]	0
Bit 5	R/W	TMODE3[1]	0
Bit 4	R/W	TMODE3[0]	0
Bit 3	R/W	TMODE2[1]	0
Bit 2	R/W	TMODE2[0]	0
Bit 1	R/W	TMODE1[1]	0
Bit 0	R/W	TMODE1[0]	0

This register configures the path termination mode of time-slots 1 to 8 of the TW8E.

**TMODE1[1:0]-TMODE8[1:0]**

The time-slot path termination mode select register bits (TMODE1[1:0]-TMODE8[1:0]) configures the mode settings for time-slots 1 to 8 of the TW8E. Time-slots are numbered in order of transmission on the working transmit serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-8) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	Reserved
0	1	HPT level. This mode must be used when in TelecomBus mode where valid V1/V2 pointers must be preserved.
1	0	LPT level. This mode must be used for SBI336 mode and in TelecomBus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

**Register 0B3H: TW8E Time-slot Configuration #2**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TMODE12[1]	0
Bit 6	R/W	TMODE12[0]	0
Bit 5	R/W	TMODE11[1]	0
Bit 4	R/W	TMODE11[0]	0
Bit 3	R/W	TMODE10[1]	0
Bit 2	R/W	TMODE10[0]	0
Bit 1	R/W	TMODE9[1]	0
Bit 0	R/W	TMODE9[0]	0

This register configures the path termination mode of time-slots 9 to 12 of the TW8E.

**TMODE9[1:0]-TMODE12[1:0]**

The time-slot path termination mode select register bits (TMODE9[1:0]-TMODE12[1:0]) configures the mode settings for time-slots 9 to 12 of the TW8E. Time-slots are numbered in order of transmission on the working transmit serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 9-12) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	Reserved
0	1	HPT level. This mode must be used when in TelecomBus mode where valid V1/V2 pointers must be preserved.
1	0	LPT level. This mode must be used for SBI336 mode and in TelecomBus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

**Register 0B4H: TW8E Test Pattern**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

This register contains the test pattern to be inserted into the working transmit serial data stream.

**TP[9:0]**

The Test Pattern registers (TP[9:0]) contains the test pattern that is used to insert into the working transmit serial data stream for jitter test purpose. When the TPINS bit is set high, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the transmit data stream.

**Register 0B5H: TW8E Analog Control**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	ARSTB	1

This registers controls the analog blocks.

**ARSTB**

Setting this bit low will reset the TWPS and TWLV blocks.

**PISO\_ENB**

Setting this bit high will disable the TWPS circuitry.

**TXLV\_ENB**

Setting this bit high will disable the TWLV circuitry.

**Reserved**

The Reserved bits should not be modified.

**Register 0B8H: TP8E Control and Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	Reserved	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

This register provides control and reports the status of the TP8E.

**DLCV**

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the protection transmit serial data stream. When this bit is set high, the encoded data is inverted to generate the complementary running disparity.

**CENTER**

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

This bit must be set once CSU lock has been achieved.



### TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the protection transmit serial data stream for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the transmit data stream. When TPINS is set low, no test pattern is inserted.

### FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) enables FIFO overrun/underrun interrupts. An interrupt is generated on a FIFO error event if the FIFOERRE is set to logic one. No interrupt is generated if FIFOERRE if is set to logic zero.

### Reserved

These bits must be set low for correct operation of the SBS.

**Register 0B9H: TP8E Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due the detection of FIFO error.

**FIFOERRI**

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic one on a FIFO overrun/underrun error. FIFOERRI is set to logic zero when this register is read.

**Register 0BAH: TP8E Time-slot Configuration #1**

Bit	Type	Function	Default
Bit 15	R/W	TMODE8[1]	0
Bit 14	R/W	TMODE8[0]	0
Bit 13	R/W	TMODE7[1]	0
Bit 12	R/W	TMODE7[0]	0
Bit 11	R/W	TMODE6[1]	0
Bit 10	R/W	TMODE6[0]	0
Bit 9	R/W	TMODE5[1]	0
Bit 8	R/W	TMODE5[0]	0
Bit 7	R/W	TMODE4[1]	0
Bit 6	R/W	TMODE4[0]	0
Bit 5	R/W	TMODE3[1]	0
Bit 4	R/W	TMODE3[0]	0
Bit 3	R/W	TMODE2[1]	0
Bit 2	R/W	TMODE2[0]	0
Bit 1	R/W	TMODE1[1]	0
Bit 0	R/W	TMODE1[0]	0

This register configures the path termination mode of time-slots 1 to 8 of the TP8E.

**TMODE1[1:0]-TMODE8[1:0]**

The time-slot path termination mode select register bits (TMODE1[1:0]-TMODE8[1:0]) configures the mode settings for time-slots 1 to 8 of the TP8E. Time-slots are numbered in order of transmission on the protection transmit serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-8) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	Reserved
0	1	HPT level. This mode must be used when in TelecomBus mode where valid V1/V2 pointers must be preserved.
1	0	LPT level. This mode must be used for SBI336 mode and in TelecomBus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

**Register 0BBH: TP8E Time-slot Configuration #2**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TMODE12[1]	0
Bit 6	R/W	TMODE12[0]	0
Bit 5	R/W	TMODE11[1]	0
Bit 4	R/W	TMODE11[0]	0
Bit 3	R/W	TMODE10[1]	0
Bit 2	R/W	TMODE10[0]	0
Bit 1	R/W	TMODE9[1]	0
Bit 0	R/W	TMODE9[0]	0

This register configures the path termination mode of time-slots 9 to 12 of the TP8E.

**TMODE9[1:0]-TMODE12[1:0]**

The time-slot path termination mode select register bits (TMODE9[1:0]-TMODE12[1:0]) configures the mode settings for time-slots 9 to 12 of the TW8E. Time-slots are numbered in order of transmission on the working protection serial data stream. Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 9-12) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	Reserved
0	1	HPT level. This mode must be used when in TelecomBus mode where valid V1/V2 pointers must be preserved.
1	0	LPT level. This mode must be used for SBI336 mode and in TelecomBus mode with a valid V5 signal but without valid V1/V2 pointers.
1	1	Reserved

**Register 0BCH: TP8E Test Pattern**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

This register contains the test pattern to be inserted into the protection transmit serial data stream.

**TP[9:0]**

The Test Pattern registers (TP[9:0]) contains the test pattern that is used to insert into the protection transmit serial data stream for jitter test purpose. When the TPINS bit is set high, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the transmit data stream.

**Register 0BDH: TP8E Analog Control**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	TXLV_ENB	0
Bit 7	R/W	PISO_ENB	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	Reserved	1
Bit 0	R/W	ARSTB	1

This register controls the analog blocks.

**ARSTB**

Setting this bit low will reset the TPPS and TPLV blocks.

**PISO\_ENB**

Setting this bit high will disable the TPPS circuitry.

**TXLV\_ENB**

Setting this bit high will disable the TPLV circuitry.

**Reserved**

The Reserved bits should not be modified.

**Register 0C0H: RW8D Control and Status**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This register provides control and reports the status of the RW8D.

**FOCA**

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment block. A transition from logic zero to logic one in this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

**FOFA**

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block. A transition from logic zero to logic one in this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

**OCAV**

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.

#### OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block. OFAV is set high when the frame alignment block is in the out-of-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

#### OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

#### OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

#### LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due to LCVs are masked when LCVE is set low.

#### FUOE

The FIFO underrun/overflow status interrupt enable (FUOE) controls the underrun/overflow event interrupts. Interrupts may be generated when the underrun/overflow event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overflow condition is detected. Interrupts due to FIFO underrun or overflow conditions are masked when FUOE is set low.

#### OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is set to logic one to force high-order AIS signals in the data-stream, when the RW8D is in the out-of-frame-alignment state. No insertion into the data stream is done when OFAAIS is set to logic zero.



Reserved

These bits must be set low for correct operation of the SBS.

**Register 0C1H: RW8D Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due to change of character alignment, change of frame alignment, detection of line code violations, and FIFO overrun or underrun events in the RW8D.

**OCAI**

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

**OFAI**

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

## LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events.

## FUOI

The FIFO underrun/overflow event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overflow interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one byte of each other. FUOI is set high when this event is detected. When the interrupt is masked by the FUE bit the FUOI remains valid and may be polled to detect underrun/overflow events.

**Register 0C2H: RW8D LCV Count**

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

This register reports the number of line code violations in the previous accumulation period in the RW8D.

**LCV[15:0]**

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV register is polled by writing this register or by writing to the SBS Master Clock Monitor, Accumulation Trigger register. The write access transfers the internally accumulated error count to the LCV register within 10  $\mu$ s and simultaneously resets the internal counter to begin a new cycle of error accumulation.

**Register 0C3H: RW8D Analog Control**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	ARSTB	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls the WDRU and RWLV analog blocks. Please refer to their respective documents for a description of the functionality of these bits.

**NOTE: THIS REGISTER MUST BE SET TO CC34h FOR PROPER OPERATION OF THE RW8D BLOCKS. FOR DISABLING THIS RECEIVER, THIS REGISTER SHOULD BE SET TO F834H**

**DRU\_ENB**

Setting this bit high will disable the WDRU.

**RX\_ENB**

Setting this bit high will disable the RWLV.

**ARSTB**

Setting this bit low will reset the WDRU and RWLV blocks.

**Reserved**

The Reserved bits should be set as described above.

**Register 0C8H: RP8D Control and Status**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	Reserved	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

This register provides control and reports the status of the RP8D.

**FOCA**

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment block. A transition from logic zero to logic one in this bit forces the character alignment block to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

**FOFA**

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment block. A transition from logic zero to logic one in this bit forces the frame alignment block to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

**OCAV**

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment block. OCAV is set high when the character alignment block is in the out-of-character-alignment state. OCAV is set low when the character alignment block is in the in-character-alignment state.

#### OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment block. OFAV is set high when the frame alignment block is in the out-of-frame-alignment state. OFAV is set low when the frame alignment block is in the in-frame-alignment state.

#### OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

#### OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

#### LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due of LCVs are masked when LCVE is set low.

#### FUOE

The FIFO underrun/overflow status interrupt enable (FUOE) controls the underrun/overflow event interrupts. Interrupts may be generated when the underrun/overflow event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overflow condition is detected. Interrupts due to FIFO underrun or overflow conditions are masked when FUOE is set low.

#### OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is set to logic one to force high-order AIS signals in the data-stream, when the RP8D is in the out-of-frame-alignment state. No insertion into the data stream is done when OFAAIS is set to logic zero.

Reserved

These bits must be set low for correct operation of the SBS.



**Register 0C9H: RP8D Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due to change of character alignment, change of frame alignment, detection of line code violations, and FIFO overrun or underrun events in the RP8D.

**OCAI**

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

**OFAI**

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

## LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected. When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events.

## FUOI

The FIFO underrun/overflow event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overflow interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one byte of each other. FUOI is set high when this event is detected. When the interrupt is masked by the FUE bit the FUOI remains valid and may be polled to detect underrun/overflow events.

**Register 0CAH: RP8D LCV Count**

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

This register reports the number of line code violations in the previous accumulation period in the RP8D.

**LCV[15:0]**

The LCV[15:0] bits reports the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV register is polled by writing this register or by writing to the SBS Master Clock Monitor, Accumulation Trigger register. The write access transfers the internally accumulated error count to the LCV register within 10  $\mu$ s and simultaneously resets the internal counter to begin a new cycle of error accumulation.

**Register 0CBH: RP8D Analog Control**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

This register controls the PDRU and RPLV analog blocks. Please refer to their respective documents for a description of the functionality of these bits.

**NOTE: THIS REGISTER MUST BE SET TO CC34h FOR PROPER OPERATION OF THE RP8D BLOCK. FOR DISABLING THIS RECEIVER, THIS REGISTER SHOULD BE SET TO F834H**

**DRU\_ENB**

Setting this bit high will disable the PDRU.

**RX\_ENB**

Setting this bit high will disable the RPLV.

**ARSTB**

Setting this bit low will reset the PDRU and RPLV blocks.

**Reserved**

The Reserved bits should be set as described above.

**Register 0D0H: CSTR Control**

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	CSU_ENB	0
Bit 3	R/W	CSU_RSTB	1
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	1

Reserved

The Reserved bits must be set to their default values for proper operation.

**CSU\_RSTB**

The CSU\_RSTB signal is a software reset signal that forces the CSU1250 into a reset. In order to properly reset the CSU, CSU\_RSTB should be held low for at least 1 ms.

**CSU\_ENB**

The active low CSU enable control signal (CSU\_ENB) bit can be used to force the CSU1250 into low power configuration if it is set to logic one. For normal operation, it is set to logic zero.

**Register 0D1H: CSTR Configuration and Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	LOCKV	X
Bit 0	R/W	LOCKE	0

**LOCKV**

The CSU lock status bit (LOCKV) indicates whether the clock synthesis unit has successfully locked with the reference clock. LOCKV is set low when the CSU has not successfully locked with the reference SYSCLK. LOCKV is set high when the CSU has locked with the reference SYSCLK.

**LOCKE**

The CSU lock interrupt enable bit (LOCKE) controls the assertion of CSU lock state interrupts by the CSTR. When LOCKE is high, an interrupt is generated when the CSU lock state changes. Interrupts due to CSU lock state are masked when LOCKE is set low.

**Register 0D2H: CSTR Interrupt Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOCKI	0

**LOCKI**

The CSU lock interrupt status bit (LOCKI) responds to changes in the CSU lock state. Interrupts are to be generated as the CSU achieves lock with the reference clock, or loses its lock to the reference clock. As a result, the LOCKI register bit is set high when any of these changes occurs. LOCKI register bit will be cleared when it is read. When LOCKE is set high, LOCKI is used to produce the interrupt output that is reflected in the SBS Master Interrupt Source register. Whether or not the interrupt is masked by the LOCKE bit, the LOCKI bit itself remains valid and may be polled to detect change of lock status events.

**Register 0E0H: REFDLL Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	LOCK	0
Bit 0	R/W	LOCK	0

The REFDLL Configuration Register controls the basic operation of the DLL connected to the SREFCLK input. This DLL is only used when SREFCLK is operating at 77.76 MHz.

**LOCK**

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after phase lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the SREFCLK and the DLL's reference clock. When LOCK is set to logic one, the DLL will not change the tap after the phase detector indicates of zero phase offset between the SREFCLK and the reference clock for the first time.

**ERRORE**

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

**Reserved**

These bits must be set to set low for correct operation of the SBS.



**Register 0E3H: REFDLL Control Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	SREFCLKI	X
Bit 6	R	DLL_REFCLKI	X
Bit 5	R	ERRORI	X
Bit 4	R	CHANGEI	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	CHANGE	0
Bit 0	R	RUN	0

The REFDLL Control Status Register provides information on the operation of the DLL connected to the SREFCLK input. This DLL is only used when SREFCLK is operating at 77.76 MHz.

**RUN**

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the reference clock and the rising edge of SREFCLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic one.

The RUN register bit is cleared only by a system reset (RSTB) or a software reset (in the SBS Master Reset Register). RUN is forced high when the OVERRIDE register is set high or when the VERN\_EN register is set high.

**CHANGE**

The delay line tap change register bit (CHANGE) indicates the DLL has moved to a new delay line tap. CHANGE is set high for eight SREFCLK cycles when the DLL moves to a new delay line tap.

## ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a output clock phase that causes the rising edge of the reference clock to be aligned to the rising edge of SREFCLK. ERROR is set low, when the DLL captures lock again.

ERROR is forced low when the OVERRIDE register is set high or when the VERN\_EN register is set high.

## CHANGEI

The delay line tap change event register bit (CHANGEI) indicates the CHANGE register bit has changed value. When the CHANGE register changes from a logic zero to a logic one, the CHANGEI register bit is set to logic one. The CHANGEI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

## ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRERE interrupt enable is high, the INT output is also asserted when ERRORI asserts. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

## DLL\_REFCLKI

The reference clock event register bit DLL\_REFCLKI provides a method to monitor activity on the reference clock. When the DLL reference clock changes from a logic zero to a logic one, the DLL\_REFCLKI register bit is set to logic one. The DLL\_REFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

## SREFCLKI

The system clock event register bit SREFCLKI provides a method to monitor activity on the system clock. When the SREFCLK primary input changes from a logic zero to a logic one, the SREFCLKI register bit is set to logic one. The SREFCLKI register bit is cleared immediately after it is read thus acknowledging the event has been recorded.

**Register 0E8H: SYSDLL Configuration**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	LOCK	0

The SYSDLL Configuration Register controls the basic operation of the DLL connected to the SYSCLK input.

**LOCK**

The LOCK register is used to force the DLL to ignore phase offsets indicated by the phase detector after phase lock has been achieved. When LOCK is set to logic zero, the DLL will track phase offsets measured by the phase detector between the SYSCLK input and the DLL's reference clock. When LOCK is set to logic one, the DLL will not change the tap after the phase detector indicates of zero phase offset between SYSCLK and the reference clock for the first time.

**ERRORE**

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

**Reserved**

These bits must be set to set low for correct operation of the SBS.

**Register 0EBH: SYSDLL Control Status**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	SYSCCLKI	X
Bit 6	R	DLL_REFCLKI	X
Bit 5	R	ERRORI	X
Bit 4	R	CHANGEI	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	CHANGE	0
Bit 0	R	RUN	0

The SYSDLL Control Status Register provides information on the operation of the DLL connected to the SYSCCLK input.

**RUN**

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of the reference clock and the rising edge of SYSCCLK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic one.

The RUN register bit is cleared only by a system reset (RSTB) or a software reset (in the SBS Master Reset Register). RUN is forced high when the OVERRIDE register is set high or when the VERN\_EN register is set high.

**CHANGE**

The delay line tap change register bit (CHANGE) indicates the DLL has moved to a new delay line tap. CHANGE is set high for eight SYSCCLK cycles when the DLL moves to a new delay line tap.

## ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a output clock phase that causes the rising edge of the reference clock to be aligned to the rising edge of SYSCLK. ERROR is set low, when the DLL captures lock again.

ERROR is forced low when the OVERRIDE register is set high or when the VERN\_EN register is set high.

## CHANGEI

The delay line tap change event register bit (CHANGEI) indicates the CHANGE register bit has changed value. When the CHANGE register changes from a logic zero to a logic one, the CHANGEI register bit is set to logic one. The CHANGEI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

## ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRERE interrupt enable is high, the INT output is also asserted when ERRORI asserts. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

## DLL\_REFCLKI

The reference clock event register bit DLL\_REFCLKI provides a method to monitor activity on the reference clock. When the DLL reference clock changes from a logic zero to a logic one, the DLL\_REFCLKI register bit is set to logic one. The DLL\_REFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

## SYSCLKI

The system clock event register bit SYSCLKI provides a method to monitor activity on the system clock. When the SYSCLK primary input changes from a logic zero to a logic one, the SYSCLKI register bit is set to logic one. The SYSCLKI register bit is cleared immediately after it is read thus acknowledging the event has been recorded.

## 12 Test Features Description

The test mode registers, shown in Table 24, are used for production and board testing.

During production testing, the test mode registers are used to apply test vectors. In this case, the test mode registers (as opposed to the normal mode registers) are selected when A[10] is high.

During board testing, the digital output pins and the data bus are held in a high-impedance state by simultaneously asserting (low) the CSB, RDB, and WRB inputs. All of the TSBs for the SBS are placed in test mode 0 so that device inputs may be read and device outputs may be forced through the microprocessor interface.

Note: The SBS supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port that can be used for board testing. All digital device inputs may be read and all digital device outputs may be forced through this JTAG test port.

**Table 24 Test Mode Register Memory Map**

Address	Register
000H-0FFH	Normal Mode Registers
100H	Master Test Register
101H - 1FFH	Reserved For Test

### 12.1 Master Test and Test Configuration Registers

#### Notes on Test Mode Register Bits

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.
2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

**Register 100H: Master Test**

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	Reserved	X
Bit 5	R/W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable SBS test features. All bits, except PMCTST and PMCATST are reset to zero by a reset of the SBS using either the RSTB input. PMCTST is reset when CSB is logic one. PMCATST is reset when both CSB is high and RSTB is low. PMCTST and PMCATST can also be reset by writing a logic zero to the corresponding register bit.

**HIZIO, HIZDATA**

The HIZIO and HIZDATA bits control the tri-state modes of the SBS . While the HIZIO bit is a logic one, all output pins of the SBS except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

**IOTST**

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each TSB block in the SBS for board level testing. When IOTST is a logic one, all blocks are held in test mode and the microprocessor may write to a block’s test mode 0 registers to manipulate the outputs of the block and consequently the device outputs.

**DBCTRL**

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and PMCTST is set to logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the SBS to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

**PMCTST**

The PMCTST bit is used to configure the SBS for PMC's manufacturing tests. When PMCTST is set to logic one, the SBS microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST can be cleared by setting CSB to logic one or by writing logic zero to the bit.

**PMCATST**

The PMCATST bit is used to configure the analog portion of the SBS for PMC's manufacturing tests.

**12.2 JTAG Test Port**

The SBS JTAG Test Access Port (TAP) allows access to the TAP controller and the four TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to Section 13.

**Table 25 Instruction Register (Length - 3 bits)**

<b>Instructions</b>	<b>Selected Register</b>	<b>Instruction Codes, IR[2:0]</b>
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111



**Table 26 Identification Register**

<b>Length</b>	32 bits
<b>Version Number</b>	0H
<b>Part Number</b>	8610H
<b>Manufacturer's Identification Code</b>	0CDH
<b>Device Identification</b>	086100CDH

**Table 27 Boundary Scan Register**

Pin/ Enable	Register Bit	Cell Type	I.D. Bit
IV5[4]	291	IN_CELL	L
ITAIS[4]	290	IN_CELL	L
ITPL[4]	289	IN_CELL	L
IC1FP[4]	288	IN_CELL	L
IPL[4]	287	IN_CELL	H
IDP[4]	286	IN_CELL	L
IDATA[4][7]	285	IN_CELL	L
IDATA[4][6]	284	IN_CELL	L
IDATA[4][5]	283	IN_CELL	L
IDATA[4][4]	282	IN_CELL	H
IDATA[4][3]	281	IN_CELL	H
IDATA[4][2]	280	IN_CELL	L
IDATA[4][1]	279	IN_CELL	L
IDATA[4][0]	278	IN_CELL	L
ITAIS[2]	277	IN_CELL	L
ITPL[2]	276	IN_CELL	H
IC1FP[2]	275	IN_CELL	L
ALE	274	IN_CELL	L
RDB	273	IN_CELL	L
WRB	272	IN_CELL	L
CSB	271	IN_CELL	L
RWSEL	270	IN_CELL	L
RSTB	269	IN_CELL	L
RC1FP	268	IN_CELL	L
OEB_OACTIVE[4]	267	OUT_CELL	H
OACTIVE[4]	266	OUT_CELL	H
ODETECT[4]	265	IN_CELL	L
OEB_JUST_REQ[4]	264	OUT_CELL	L
JUST_REQ[4]	263	IO_CELL	H
OEB_OC1FP[4]	262	OUT_CELL	H
OC1FP[4]	261	OUT_CELL	L
OEB_OTAIS[4]	260	OUT_CELL	H
OT AIS[4]	259	OUT_CELL	-
OEB_OV5[4]	258	OUT_CELL	-
OV5[4]	257	OUT_CELL	-
OEB_OTPL[4]	256	OUT_CELL	-
OTPL[4]	255	OUT_CELL	-
OEB_OPL[4]	254	OUT_CELL	-

OPL[4]	253	OUT_CELL	-
OEB_ODP[4]	252	OUT_CELL	-
ODP[4]	251	OUT_CELL	-
OEB_D[15]	250	OUT_CELL	-
D[15]	249	IO_CELL	-
OEB_D[14]	248	OUT_CELL	-
D[14]	247	IO_CELL	-
OEB_ODATA[4][7]	246	OUT_CELL	-
ODATA[4][7]	245	OUT_CELL	-
OEB_ODATA[4][6]	244	OUT_CELL	-
ODATA[4][6]	243	OUT_CELL	-
OEB_ODATA[4][5]	242	OUT_CELL	-
ODATA[4][5]	241	OUT_CELL	-
OEB_ODATA[4][4]	240	OUT_CELL	-
ODATA[4][4]	239	OUT_CELL	-
OEB_ODATA[4][3]	238	OUT_CELL	-
ODATA[4][3]	237	OUT_CELL	-
OEB_ODATA[4][2]	236	OUT_CELL	-
ODATA[4][2]	235	OUT_CELL	-
OEB_ODATA[4][1]	234	OUT_CELL	-
ODATA[4][1]	233	OUT_CELL	-
OEB_ODATA[4][0]	232	OUT_CELL	-
ODATA[4][0]	231	OUT_CELL	-
USER_IN	230	IN_CELL	-
OEB_D[13]	229	OUT_CELL	-
D[13]	228	IO_CELL	-
OEB_D[12]	227	OUT_CELL	-
D[12]	226	IO_CELL	-
OEB_D[11]	225	OUT_CELL	-
D[11]	224	IO_CELL	-
OEB_D[10]	223	OUT_CELL	-
D[10]	222	IO_CELL	-
OEB_D[9]	221	OUT_CELL	-
D[9]	220	IO_CELL	-
IV5[2]	219	IN_CELL	-
IPL[2]	218	IN_CELL	-
IDP[2]	217	IN_CELL	-
IDATA[2][7]	216	IN_CELL	-
IDATA[2][6]	215	IN_CELL	-
IDATA[2][5]	214	IN_CELL	-
IDATA[2][4]	213	IN_CELL	-

IDATA[2][3]	212	IN_CELL	-
IDATA[2][2]	211	IN_CELL	-
IDATA[2][1]	210	IN_CELL	-
IDATA[2][0]	209	IN_CELL	-
OEB_D[8]	208	OUT_CELL	-
D[8]	207	IO_CELL	-
OEB_D[7]	206	OUT_CELL	-
D[7]	205	IO_CELL	-
IV5[3]	204	IN_CELL	-
IT AIS[3]	203	IN_CELL	-
ITPL[3]	202	IN_CELL	-
IC1FP[3]	201	IN_CELL	-
IPL[3]	200	IN_CELL	-
IDP[3]	199	IN_CELL	-
IDATA[3][7]	198	IN_CELL	-
OEB_D[6]	197	OUT_CELL	-
D[6]	196	IO_CELL	-
OEB_D[5]	195	OUT_CELL	-
D[5]	194	IO_CELL	-
OEB_D[4]	193	OUT_CELL	-
D[4]	192	IO_CELL	-
IDATA[3][6]	191	IN_CELL	-
IDATA[3][5]	190	IN_CELL	-
IDATA[3][4]	189	IN_CELL	-
IDATA[3][3]	188	IN_CELL	-
IDATA[3][2]	187	IN_CELL	-
OEB_D[3]	186	OUT_CELL	-
D[3]	185	IO_CELL	-
OEB_D[2]	184	OUT_CELL	-
D[2]	183	IO_CELL	-
OEB_D[1]	182	OUT_CELL	-
D[1]	181	IO_CELL	-
OEB_D[0]	180	OUT_CELL	-
D[0]	179	IO_CELL	-
A[8]	178	IN_CELL	-
A[7]	177	IN_CELL	-
A[6]	176	IN_CELL	-
A[5]	175	IN_CELL	-
A[4]	174	IN_CELL	-
A[3]	173	IN_CELL	-
A[2]	172	IN_CELL	-

A[1]	171	IN_CELL	-
IDATA[3][1]	170	IN_CELL	-
IDATA[3][0]	169	IN_CELL	-
OEB_JUST_REQ[3]	168	OUT_CELL	-
JUST_REQ[3]	167	IO_CELL	-
A[0]	166	IN_CELL	-
OEB_USER_OUT	165	OUT_CELL	-
USER_OUT	164	OUT_CELL	-
OEB_JUST_REQ[1]	163	OUT_CELL	-
JUST_REQ[1]	162	IO_CELL	-
OEB_OC1FP[3]	161	OUT_CELL	-
OC1FP[3]	160	OUT_CELL	-
OEB_OTAIS[3]	159	OUT_CELL	-
OTAIS[3]	158	OUT_CELL	-
OEB_OV5[3]	157	OUT_CELL	-
OV5[3]	156	OUT_CELL	-
OEB_OTPL[3]	155	OUT_CELL	-
OTPL[3]	154	OUT_CELL	-
OEB_OPL[3]	153	OUT_CELL	-
OPL[3]	152	OUT_CELL	-
OEB_ODP[3]	151	OUT_CELL	-
ODP[3]	150	OUT_CELL	-
OEB_OACTIVE[3]	149	OUT_CELL	-
OACTIVE[3]	148	OUT_CELL	-
OEB_ODATA[3][7]	147	OUT_CELL	-
ODATA[3][7]	146	OUT_CELL	-
OEB_ODATA[3][6]	145	OUT_CELL	-
ODATA[3][6]	144	OUT_CELL	-
OEB_ODATA[3][5]	143	OUT_CELL	-
ODATA[3][5]	142	OUT_CELL	-
OEB_ODATA[3][4]	141	OUT_CELL	-
ODATA[3][4]	140	OUT_CELL	-
OEB_ODATA[3][3]	139	OUT_CELL	-
ODATA[3][3]	138	OUT_CELL	-
OEB_ODATA[3][2]	137	OUT_CELL	-
ODATA[3][2]	136	OUT_CELL	-
OEB_ODATA[3][1]	135	OUT_CELL	-
ODATA[3][1]	134	OUT_CELL	-
OEB_ODATA[3][0]	133	OUT_CELL	-
ODATA[3][0]	132	OUT_CELL	-
ODETECT[3]	131	IN_CELL	-

OEB_INTB	130	OUT_CELL	-
INTB	129	OUT_CELL	-
OEB_OC1FP[2]	128	OUT_CELL	-
OC1FP[2]	127	OUT_CELL	-
OEB_OV5[2]	126	OUT_CELL	-
OV5[2]	125	OUT_CELL	-
OEB_OPL[2]	124	OUT_CELL	-
OPL[2]	123	OUT_CELL	-
OEB_ODP[2]	122	OUT_CELL	-
ODP[2]	121	OUT_CELL	-
OEB_ODATA[2][7]	120	OUT_CELL	-
ODATA[2][7]	119	OUT_CELL	-
OEB_ODATA[2][6]	118	OUT_CELL	-
ODATA[2][6]	117	OUT_CELL	-
OEB_ODATA[2][5]	116	OUT_CELL	-
ODATA[2][5]	115	OUT_CELL	-
OEB_ODATA[2][4]	114	OUT_CELL	-
ODATA[2][4]	113	OUT_CELL	-
OEB_ODATA[2][3]	112	OUT_CELL	-
ODATA[2][3]	111	OUT_CELL	-
OEB_ODATA[2][2]	110	OUT_CELL	-
ODATA[2][2]	109	OUT_CELL	-
OEB_ODATA[2][1]	108	OUT_CELL	-
ODATA[2][1]	107	OUT_CELL	-
OEB_ODATA[2][0]	106	OUT_CELL	-
ODATA[2][0]	105	OUT_CELL	-
ITAIS[1]	104	IN_CELL	-
IPL[1]	103	IN_CELL	-
IC1FP[1]	102	IN_CELL	-
IV5[1]	101	IN_CELL	-
ITPL[1]	100	IN_CELL	-
IDP[1]	99	IN_CELL	-
IDATA[1][7]	98	IN_CELL	-
IDATA[1][6]	97	IN_CELL	-
IDATA[1][5]	96	IN_CELL	-
IDATA[1][4]	95	IN_CELL	-
IDATA[1][3]	94	IN_CELL	-
IDATA[1][2]	93	IN_CELL	-
IDATA[1][1]	92	IN_CELL	-
IDATA[1][0]	91	IN_CELL	-
OEB_SREFCLK19	90	OUT_CELL	-

SREFCLK19	89	OUT_CELL	-
SREFCLK	88	IN_CELL	-
SYSCLK	87	IN_CELL	-
OEB_JUST_REQ[2]	86	OUT_CELL	-
JUST_REQ[2]	85	IO_CELL	-
OEB_OACTIVE[2]	84	OUT_CELL	-
OACTIVE[2]	83	OUT_CELL	-
ODETECT[2]	82	IN_CELL	-
OCMP	81	IN_CELL	-
ICMP	80	IN_CELL	-
OEB_OTAIS[2]	79	OUT_CELL	-
OTAIS[2]	78	OUT_CELL	-
OEB_OTPL[2]	77	OUT_CELL	-
OTPL[2]	76	OUT_CELL	-
RTAIS	75	IN_CELL	-
RTPL	74	IN_CELL	-
RV5	73	IN_CELL	-
RPL	72	IN_CELL	-
RDP	71	IN_CELL	-
RDATA[7]	70	IN_CELL	-
RDATA[6]	69	IN_CELL	-
RDATA[5]	68	IN_CELL	-
RDATA[4]	67	IN_CELL	-
RDATA[3]	66	IN_CELL	-
RDATA[2]	65	IN_CELL	-
RDATA[1]	64	IN_CELL	-
RDATA[0]	63	IN_CELL	-
RJUST_REQ	62	IN_CELL	-
OEB_OC1FP[1]	61	OUT_CELL	-
OC1FP[1]	60	OUT_CELL	-
OEB_OPL[1]	59	OUT_CELL	-
OPL[1]	58	OUT_CELL	-
OEB_OV5[1]	57	OUT_CELL	-
OV5[1]	56	OUT_CELL	-
OEB_OTPL[1]	55	OUT_CELL	-
OTPL[1]	54	OUT_CELL	-
OEB_OTAIS[1]	53	OUT_CELL	-
OTAIS[1]	52	OUT_CELL	-
OEB_ODATA[1][7]	51	OUT_CELL	-
ODATA[1][7]	50	OUT_CELL	-
OEB_ODATA[1][6]	49	OUT_CELL	-

ODATA[1][6]	48	OUT_CELL	-
OEB_ODATA[1][5]	47	OUT_CELL	-
ODATA[1][5]	46	OUT_CELL	-
OEB_ODATA[1][4]	45	OUT_CELL	-
ODATA[1][4]	44	OUT_CELL	-
OEB_ODATA[1][3]	43	OUT_CELL	-
ODATA[1][3]	42	OUT_CELL	-
ODETECT[1]	41	IN_CELL	-
OEB_OACTIVE[1]	40	OUT_CELL	-
OACTIVE[1]	39	OUT_CELL	-
OEB_TTAIS	38	OUT_CELL	-
TTAIS	37	OUT_CELL	-
OEB_TV5	36	OUT_CELL	-
TV5	35	OUT_CELL	-
Logic zero	34	IN_CELL	-
OEB_TTPL	33	OUT_CELL	-
TTPL	32	OUT_CELL	-
OEB_TPL	31	OUT_CELL	-
TPL	30	OUT_CELL	-
OEB_TDP	29	OUT_CELL	-
TDP	28	OUT_CELL	-
OEB_ODATA[1][2]	27	OUT_CELL	-
ODATA[1][2]	26	OUT_CELL	-
OEB_ODATA[1][1]	25	OUT_CELL	-
ODATA[1][1]	24	OUT_CELL	-
OEB_ODATA[1][0]	23	OUT_CELL	-
ODATA[1][0]	22	OUT_CELL	-
OEB_ODP[1]	21	OUT_CELL	-
ODP[1]	20	OUT_CELL	-
OEB_TDATA[7]	19	OUT_CELL	-
TDATA[7]	18	OUT_CELL	-
OEB_TDATA[6]	17	OUT_CELL	-
TDATA[6]	16	OUT_CELL	-
OEB_TDATA[5]	15	OUT_CELL	-
TDATA[5]	14	OUT_CELL	-
OEB_TDATA[4]	13	OUT_CELL	-
TDATA[4]	12	OUT_CELL	-
OEB_TDATA[3]	11	OUT_CELL	-
TDATA[3]	10	OUT_CELL	-
OEB_TDATA[2]	9	OUT_CELL	-
TDATA[2]	8	OUT_CELL	-



OEB_TDATA[1]	7	OUT_CELL	-
TDATA[1]	6	OUT_CELL	-
OEB_TDATA[0]	5	OUT_CELL	-
TDATA[0]	4	OUT_CELL	-
OEB_TC1FP	3	OUT_CELL	-
TC1FP	2	OUT_CELL	-
OEB_TJUST_REQ	1	OUT_CELL	-
TJUST_REQ	0	OUT_CELL	-

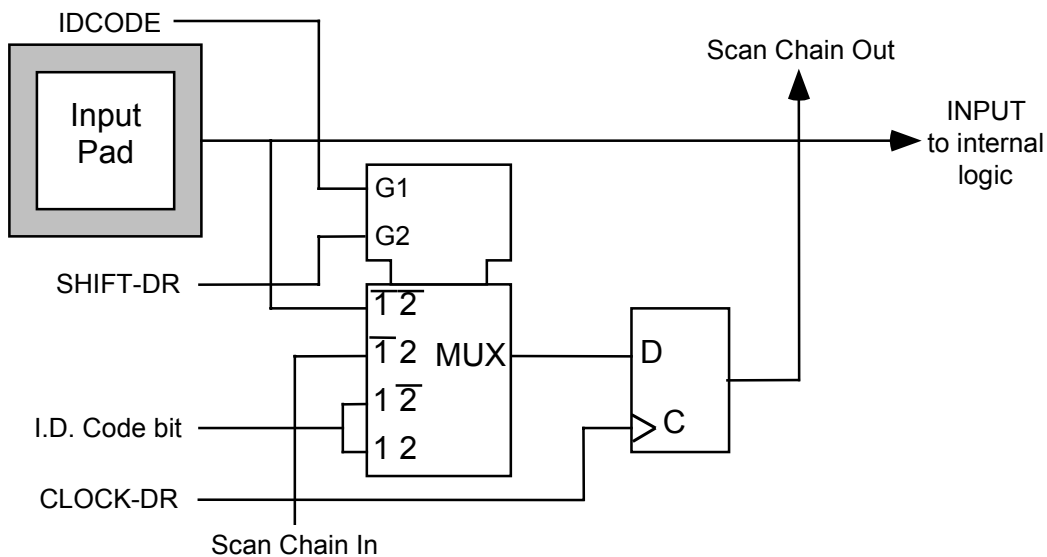
**Notes**

1. When set high, INTB will be set to high impedance.
2. "Enable cell OEB\_pinname" tristates pin pinname when set high.
3. IV5[4] is the first bit of the boundary scan chain.
4. Cells 'Logic zero' are Input Observation cells whose input pad is bonded to VSS internally.

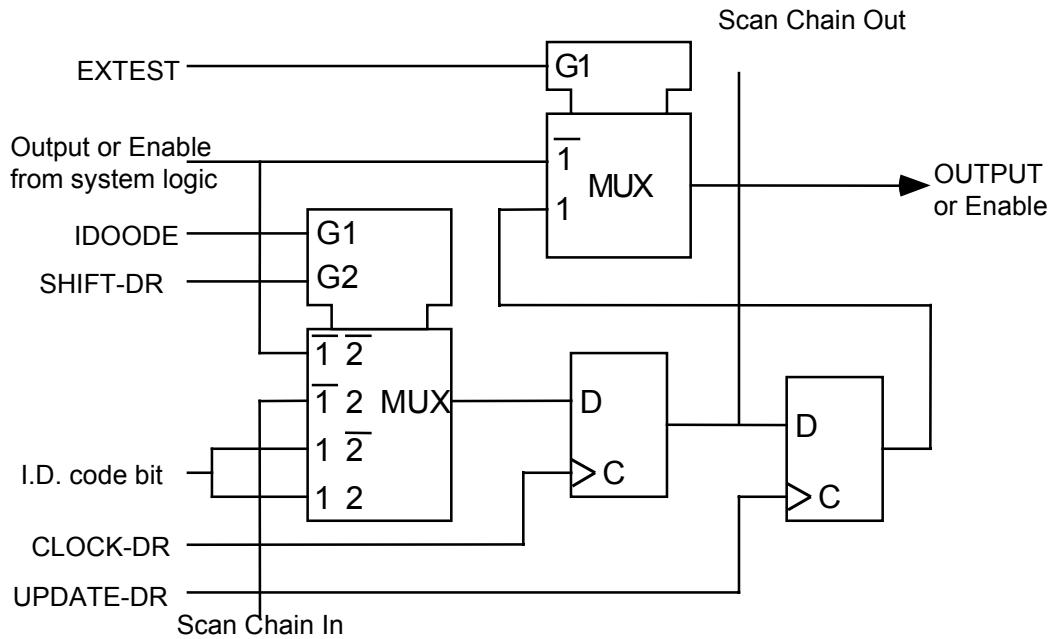
**12.2.1 Boundary Scan Cells**

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register (Table 27).

**Figure 13 Input Observation Cell (IN\_CELL)**



**Figure 14 Output Cell (OUT\_CELL)**



**Figure 15 Bidirectional Cell (IO\_CELL)**

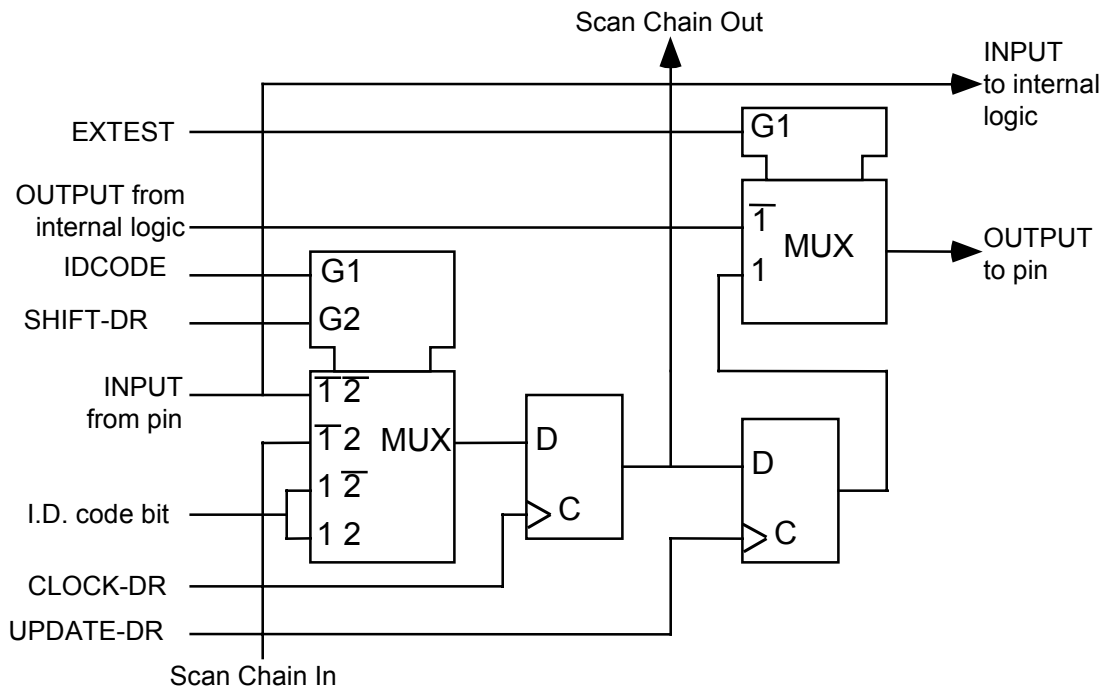
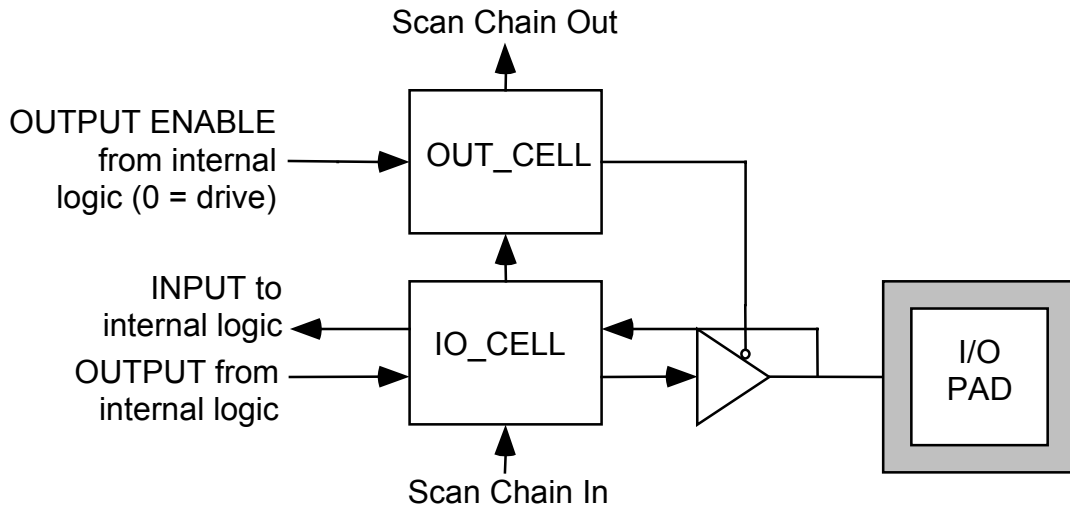


Figure 16 Layout of Output Enable and Bidirectional Cells



## 13 Operation

There are several important aspects regarding the operation of Narrowband-based switch fabrics; these are dealt with in turn in the following sections.

### 13.1 “C1” Synchronization.

Any NSE/SBS fabric can be viewed as a collection of five “columns” of devices:

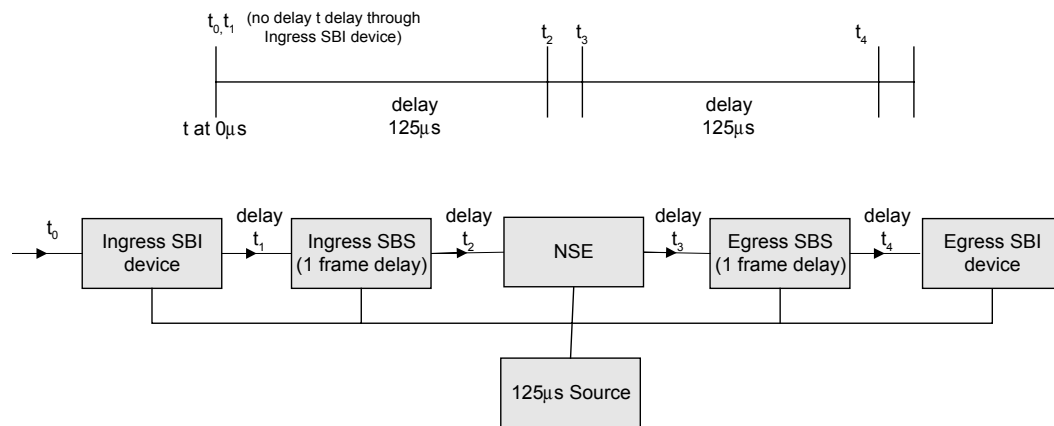
- column 0 consists of the ingress flow from the load devices (e.g., some SBI device)
- column 1 consists of the ingress flow through the SBS devices
- column 2 consists of the NSE-20G device
- column 3 consists of the egress flow through the SBS devices
- column 4 consists of the egress flow through the load devices (e.g. some SBI device).

Note that the devices in columns 0 and 4 are SBI bus devices while columns 1 and 3 are SBS or SBS-lite devices. The dual column references refer to their two separate simplex flows. Path-aligned STS-12 frames are pipelined through this structure in a regular fashion, under control of a single clock source and frame pulse. There are latencies between these columns, and these latencies may vary from path to path. The following design is used to accommodate these latencies.

A timing pulse for SBI frames (2kHz, 500  $\mu$ s) is generated and fed to each device in the fabric. Each chip has a *FrameDelay* register (RC1DLY) which contains the count of 77.76 MHz clock ticks that device should delay from the reference timing pulse before expecting the C1 characters of the ingress STS-12 frames to have arrived. The base timing pulse is called  $t$ . The delays from  $t$  based on the settings of the RC1DLY registers in the successive columns of the devices are called  $t_0, \dots, t_4$ . The first signal,  $t_1$  (equal to  $t_0$ ), determines the start of an STS-12 frame; this signal is used to instruct the ingress load devices (column 0) to start emitting an STS-12 frame (with its special “C1” control character) at that time.  $t_i$  is determined by the customer, based on device and wiring delays to be approximately the earliest time that all “C1” characters will have arrived in the ingress FIFOs of the  $t_i$  column of devices.  $t_i$  is selected to provide assurance that all “C1” characters have arrived at the  $i^{\text{th}}$  column. The  $i^{\text{th}}$  column of devices use the  $t_i$  signal to synchronize emission of the STS-12 frames. The ingress FIFOs permit a variable latency in C1 arrival of up to 24 clock cycles.

Note: The SBS device, being a memory switch, adds a latency of one complete frame plus a few clock ticks to the data.

**Figure 17 “C1” Synchronization Control**



## 13.2 Synchronized Control Setting Changes

The NSE-20G and SBS support dual switch control settings. These dual settings permit one bank of settings to be operational while the other bank is updated as a result of some new connection requests. The CMP input selects the current operational switch control settings. CMP is sampled by the NSE-20G on the base timing pulse  $t$ . The internal blocks sample the registered CMP value as they receive the next C1 character—at least a delay of RC1DLY. The new CMP value is applied on the first A1 character of the following STS-12 frame. This switchover is hitless; the control change does not disrupt the user data flow in any way. This feature is required for the addition of arbitrary new connections, as existing connections may need to be rerouted (see the discussion of the connection routing algorithm in this document).

The DS0-granularity switch settings RAM is organized into two control settings banks, these are switched by the above mechanisms on C1 boundaries. The NSE also has to coordinate the switching of the connected SBS devices (if using the In-Band link facility), so a broader understanding of the issues is required.

To illustrate the system, Sections 13.2.1 to 13.2.3 describe actual examples.

### 13.2.1 SBS/NSE Systems with DS0 and CAS switching

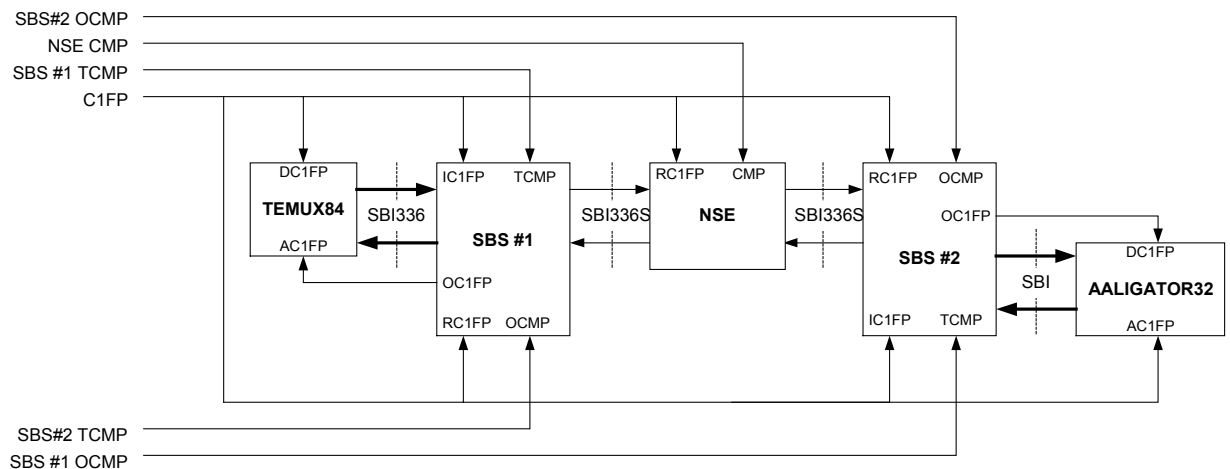
When building a DS0 and Channel Associated Signaling switching system with the SBS, SBS-lite and NSE devices the overall timing is based on the CAS signaling multiframe on the SBI bus. In this configuration the delay through the SBS devices is a single 125  $\mu$ S SBI frame plus a few 77.76 MHz clocks and the delay through the NSE is a few 77.76 MHz clocks. A single C1FP frame synchronization signal is distributed around the system. Internal to the SBS and NSE devices are programmable offsets used to account for propagation delays through the system. The key constraint is that all SBI frames are aligned going into the NSE device.

Compatible devices are PM8316 TEMUX-84, PM7388 FREEDM-336, PM7389 FREEDM-336-84, PM7341 S/UNI-IMA-84, and other future SBI336 devices.

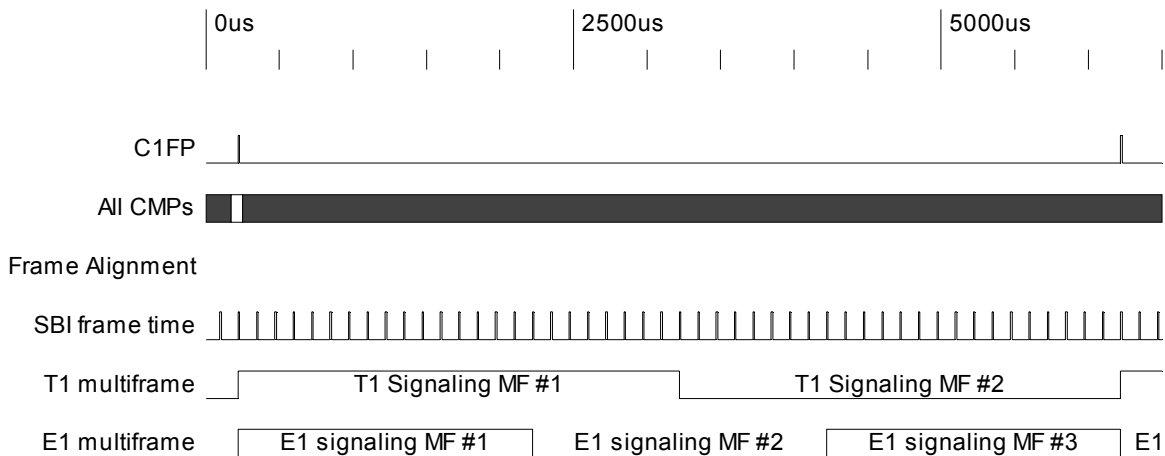
The SBS and NSE devices have two configuration pages controlling the switching of each DS0 with CAS. The SBS has independent configuration pages for each direction of data flow through the device. The NSE has one set of configuration pages. System configuration changes are made by writing to the offline configuration page in all affected devices and then swapping from the old configuration page to the new configuration page. The TCMP and OCMP signals control the current configuration page of the SBS and the CMP signal controls the current configuration page of the NSE. Swapping of configuration pages must be aligned to frame switching through the system to avoid any possible data corruption. The TCMP, OCMP and CMP signals are sampled with the SBS IC1FP and RC1FP signals and the NSE RC1FP signals respectively. The CMP signals can be connected together at the expense of having to ensure all device configuration pages are current.

The following diagram shows how the devices are connected together. The following timing diagrams show the external signals and the internal device frame alignment signal generated from the programmed delays. Although the CMP signals are sampled externally with the C1FP signals they are also delayed internally to coincide with the internally delayed frame signals. These are also shown in the timing diagram. All internal signals are identified by the .INT suffix.

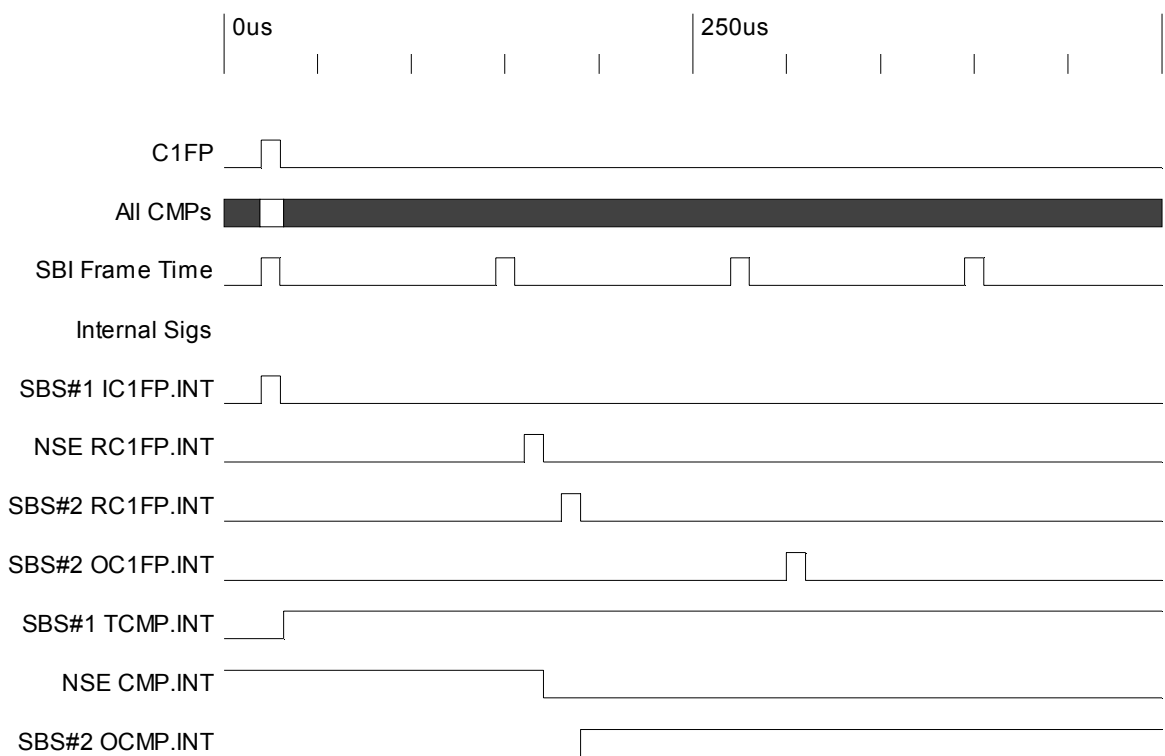
**Figure 18 TEMUX™-84/SBS/NSE/SBS/AALigator™-32 System DS0 Switching with CAS**



**Figure 19 CAS Multiframe timing**



**Figure 20 Switch Timing DSOs with CAS**

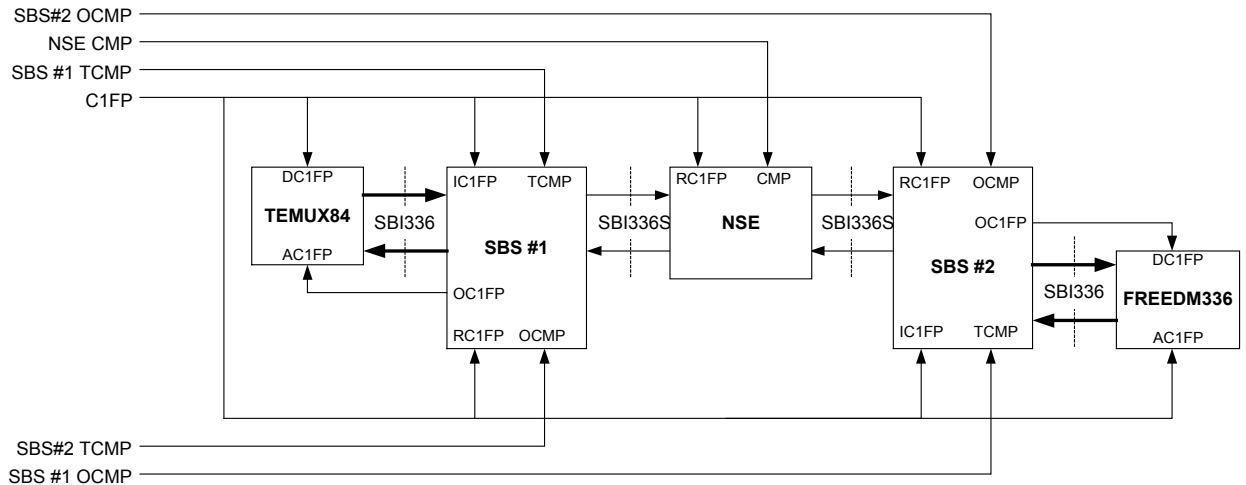


**13.2.2 SBS/NSE Systems switching DS0s without CAS**

This is very similar to the DS0 switching system configuration with CAS described in the previous section. The only difference is that in this system the global C1FP can be reduced to every SBI multiframe rather than the longer 48 frame SBI bus signaling multiframe. The advantage is that there is less latency when making switch configuration changes via the CMP signals.

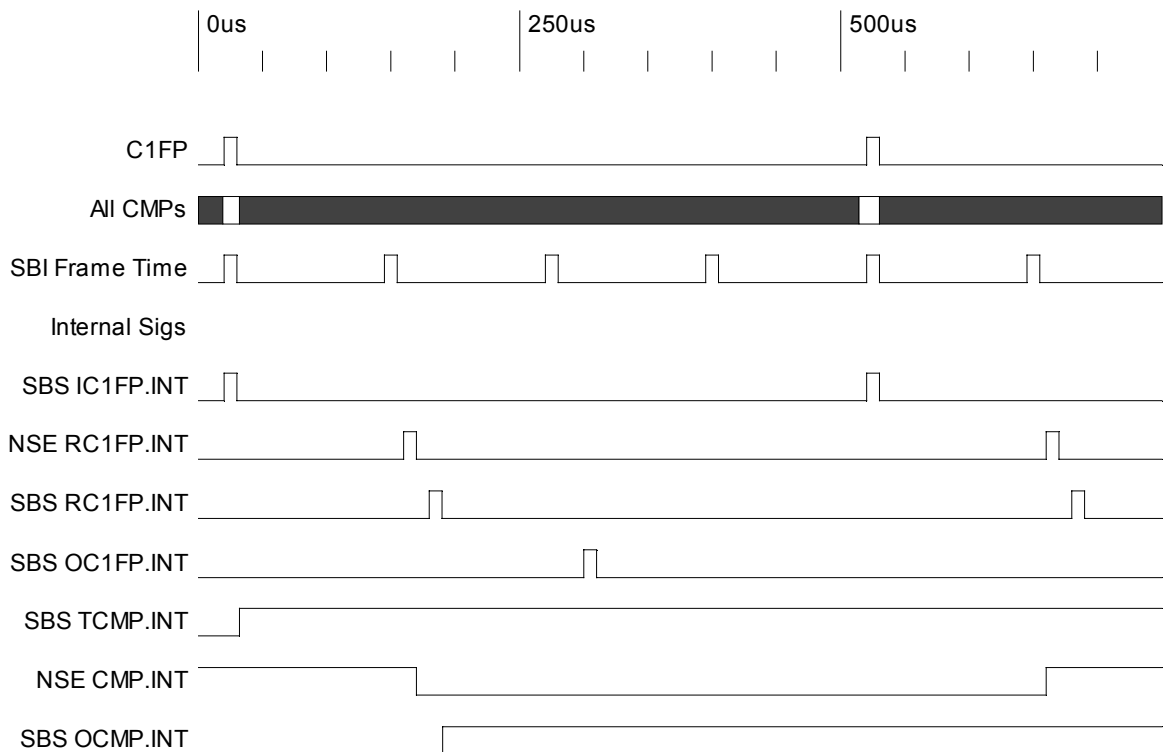
The following diagram shows the system with the FREEDM™-336 which does not require Channel Associated Signaling. Notice that the data latency through the system is the same as the case when switching DS0s with CAS.

**Figure 21 TEMUX-84/SBS/NSE/SBS/FREEDM-336 System DS0 Switching No CAS**



The following timing diagram shows the system timing when in this configuration.

**Figure 22 Switch Timing - DS0s without CAS**





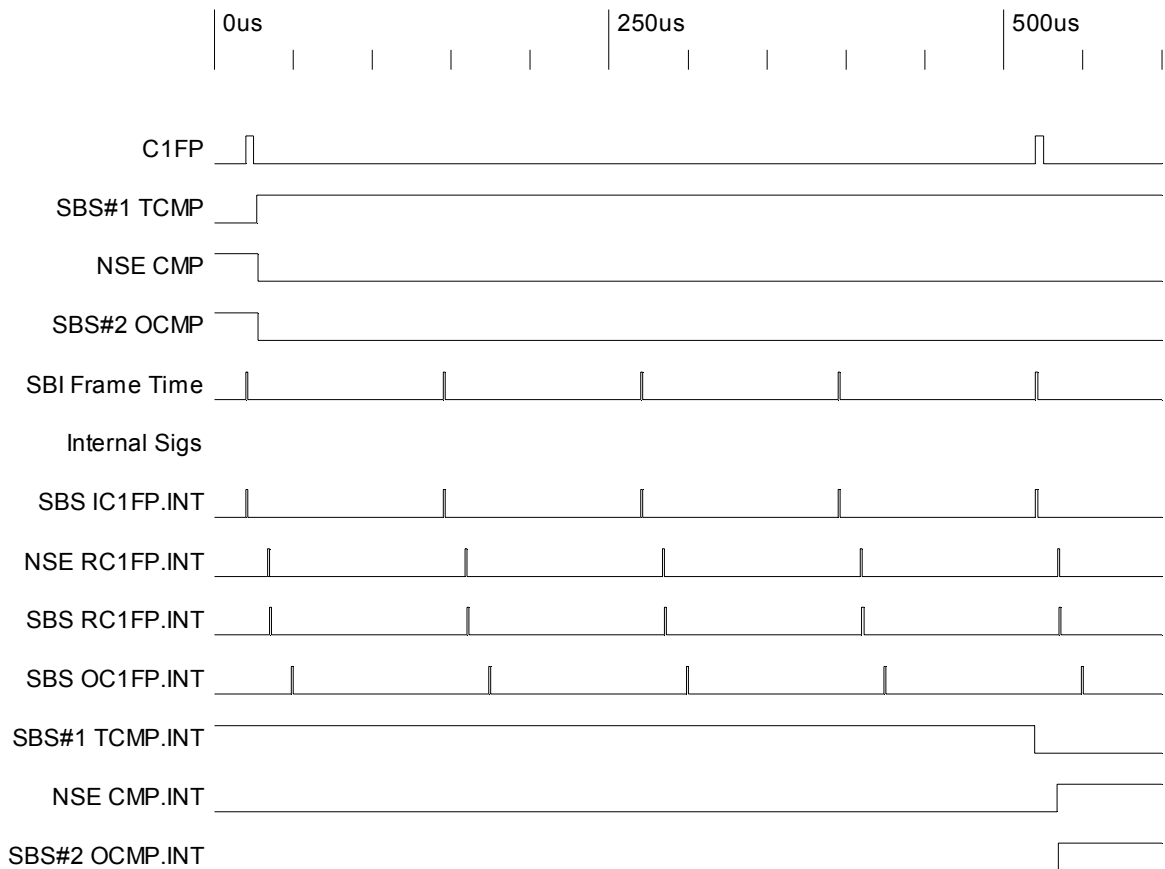
### 13.2.3 SBS/NSE Non-DS0 Level Switching with SBI336 Devices

The SBS and NSE support another mode of operation that has lower latency and lower power when not switching at the DS0 level. In this mode, both of these devices become a column switch rather than a DS0 switch. This saves software configuration since only one row of the switch configuration RAMs has to be configured rather than all nine rows.

When switching DS0 through the system the SBS must store an entire frame of DS0s before routing them to the destination to allow for the last DS0 of a frame to be switched to the first DS0 of the output. When doing column switching, only one row of the SBI structure needs to be stored before switching can take place.

The same diagram from the previous section can be used here. The following timing diagram shows the system timing for this mode of operation.

**Figure 23 Non DS0 Switch Timing**



### 13.3 Switch Setting Algorithm

NSE/SBS fabrics require an algorithm to map from customers' connection requirements to settings in the switch function control registers in these devices. Four constraints apply to this algorithm:

- The algorithm must succeed for arbitrary permutation requests (i.e., neither the fabric nor the algorithm can fail to connect any one-to-one connection request).
- The algorithm must permit connection of 2-cast requests (port replication for either snooping or for advanced redundancy fabrics). In fabrics with spare capacity and multicast/broadcast servers, the algorithm must permit mapping of multicast/broadcast requests, up to the capacity of the fabric and the servers.
- This algorithm must be fast enough to satisfy requirements for response to operator requests for connection changes.
- This algorithm must be fast enough to satisfy requirements for protection responses to equipment failures.

There are several aspects of this problem:

- Reconnection requests may be made individually in which case an incremental connection-setting algorithm is desired, or as complete batches in which case a batch algorithm may be desirable.
- Reconnection requests may be pre-computed for fast protection fall-over mechanisms.

### 13.3.1 Problem Description

The basic scheduling problem is to find the switch settings to properly route a set of connections. This is more formally described using the definitions in the following paragraphs.

**Port:** An STS-12 input/output data stream. The serial ports on the SBS devices and the NSE-20G devices operate at STS-12 rates and utilize STS-12 frames. Since the intention of the NSE-20G is to serve as a DS0-granularity switch, these STS-12 frames must be treated as repeating on a cycle of  $12 \times 9 \times 90 = 9720$  octets. All connections considered by this algorithm are octet connections. Higher aggregations of traffic are handled as collections of octets, and are ignored for the purposes of describing this algorithm.

**Timeslot:** A specific octet location in the 9720 octet cyclic structure.

**Spacetimeslot:** A timeslot on a specific port, identified by a space component and a time component: for example, octet 9 on port 3 of SBS device 2

**Connection:** A mapping of an input spacetimeslot to an output spacetimeslot. Connections come in two varieties, multicast and unicast. Unicast connections are a mapping of a single input spacetimeslot to a single output spacetimeslot. Multicast connections are a mapping of a single spacetimeslot to multiple output spacetimeslots. This algorithm is only concerned with the unicast problem.

### 13.3.2 Naïve Algorithm

We begin by describing a simplified version of the algorithm, applied to a specific SBS/NSE-20G configuration. Figure 24 illustrates the application. Four SBS devices are connected by one port each to an NSE, which is likewise connected by one port to the egress side of each SBS device. Only four ingress/egress ports of 32 on the NSE-20G are in use in this application, but the ideas generalize easily to larger fabrics.

Information flows from left to right. Each edge connects an egress port (on the left) to an ingress port (on the right); each such edge has a capacity of 9720 timeslots.

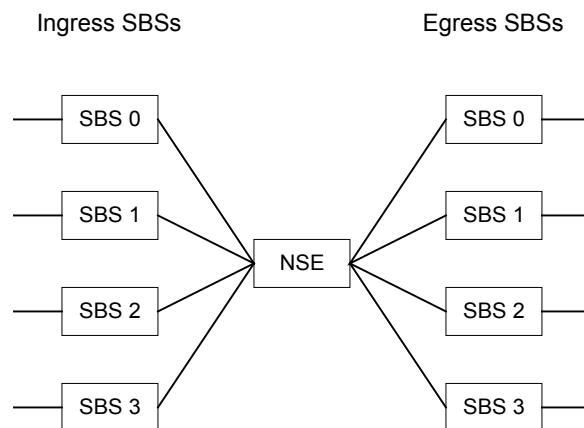
For present purposes, we consider the SBSs to be supporting a single P-SBI port (eight bits at 77.76 MHz, or STS-12). Also, we ignore the “standby” LVDS port. This reduces the SBS from a multi-ported Memory switch (which it in fact is) to a simpler two-ported (P-SBI and Active S-SBI) Time switch. This reduction in complexity makes the following discussion more straightforward, but does not reduce the algorithm’s ability to deal with the more complex cases introduced by the use of the four slower P-SBI ports, or by concurrent use of the standby LVDS port. The nature of switching in this application is illustrated by Figure 19. The two dimensional 4-X-4 matrices represent octet slots in both space (vertical) and time (horizontal).

We trace through the switching processing in the following steps:

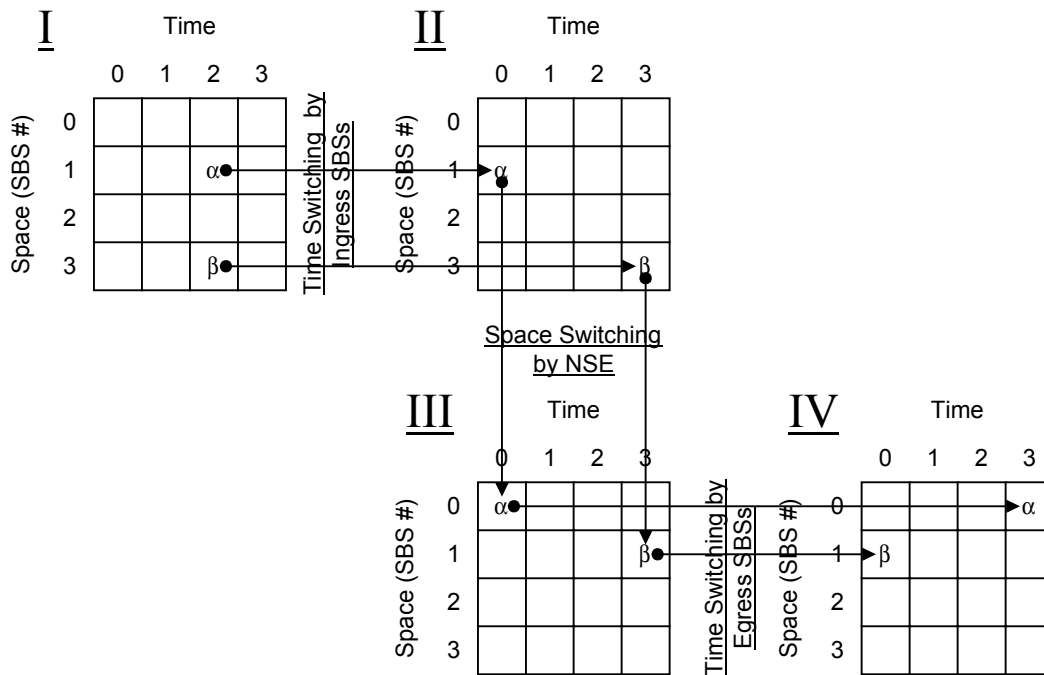
- Matrix I represents the arrival of the 16 octets from the SBI load devices.
- The mapping from Matrix I to Matrix II represents the Time switching action of all four ingress SBSs. Each SBS carries out an arbitrary permutation (including 1-to-many) of the ingress Time slots within each Space row.
- The mapping from Matrix II to Matrix III represents the Space switching action of the NSE. During each Time slot, the NSE-20G carries out an arbitrary permutation (including 1-to-many) of the ingress Space slots.
- The mapping from Matrix III to Matrix IV represents the Time switching action of all four egress SBSs. Each SBS carries out an arbitrary permutation (including 1-to-many) of the ingress Time slots within each Space row.

It is known that any complete permutation from Matrix I to Matrix IV can be carried out in this way. Figure 19 illustrates two particular octets ( $\alpha$  and  $\beta$ ) being switched through the SBS:NSE:SBS Time:Space:Time switch.

**Figure 24 Example Graph**



**Figure 25 Time:Space:Time Switching in one NSE-20G and four Single-Ported SBSs**



$\alpha$ : (S=1, T=2) => SBS => (S=1, T=0) => NSE => (S=0, T=0) => SBS => (S=0, T=3)

$\beta$ : (S=3, T=2) => SBS => (S=3, T=3) => NSE => (S=1, T=3) => SBS => (S=1, T=0)

Consider a request to route an octet from ingress port  $i$  to egress port  $j$ , where  $i$  and  $j$  range from 0 to 3, over four ports corresponding to the four SBS devices. To make this connection, we must find a timeslot in the NSE-20G which can accept an octet from the ingress SBS and send an octet to the egress SBS. If the NSE-20G has these two slots free in the same timeslot, then the SBSs must also have the corresponding slot free. The actual routing of the sample is accomplished in several steps. The octet is:

- Mapped to the free timeslot by the ingress SBS port,
- Picked up by the NSE-20G in that timeslot on the port from the ingress SBS and mapped to the port which leads to the egress SBS,
- Picked up by the egress SBS in the expected timeslot.

It may not be possible to find a free time that connects the ingress SBS to the egress SBS, even though both SBS devices have unused capacity into the NSE-20G core (the ingress SBS may have a free timeslot at time  $i$  and the egress SBS may have a free timeslot at time  $j$ , but  $i \neq j$ ). Such cases require a more complex algorithm which is capable of disconnecting and reconnecting other connections to make space for the new  $i$  to  $j$  connection. (Disconnection and reconnection of other connections is done hitlessly by NSE/SBS fabrics.) This more sophisticated algorithm is described in the remainder of this section.

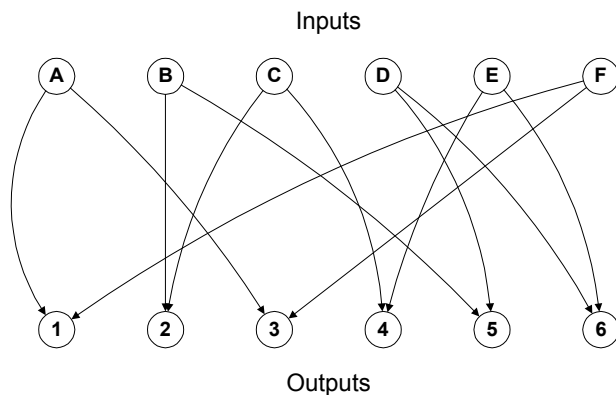
### 13.3.3 Bi-partite graphs

A general solution to the connection problem is a schedule where each connection is assigned to one of the 9720 timeslots in each time stage such that no two connections conflict. This solution then maps to physical switch settings for the SBS and NSE-20G devices. The following definitions allow us to represent the problem as an abstract graph problem:

1. Draw a **graph** where each input and output port is represented as a **node**.
2. Partition the graph so that all of the input ports are in one **partition** and all the output ports are in the other.
3. Draw an **edge** from an input node to an output node if there is a connection from the corresponding input port to the corresponding output port.

This results in a **bipartite graph** where each node has a maximum degree of 9720 (the total number of possible connections from/to a port). A subset of this problem (6 nodes, 2 timeslots) is illustrated in Figure 24. We want to assign the edges (connections) to timeslots such that no coincident edges are assigned to the same timeslot. Notice that a solution to the problem consists of a permutation (or partial permutation) mapping of input nodes onto output nodes for each of the timeslots. These permutation mappings correspond to one set of switch settings for the NSE-20G devices.

**Figure 26 Example Graph**



### 13.3.4 Unicast

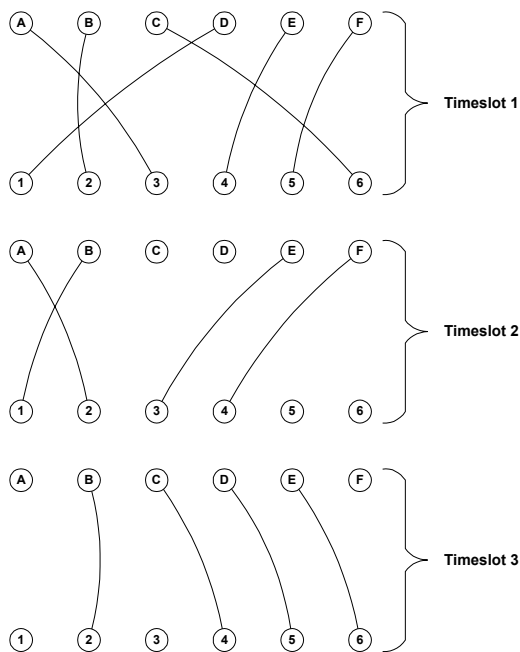
Scheduling unicast connections through the NSE-20G is a relatively simple problem: given  $n$  input ports,  $n$  output ports,  $m$  time slots and a guarantee that no port is oversubscribed, schedule the transfer of all input slots to output slots. This solution uses the time slot interchange on the SBS chips to schedule the flow of inputs to outputs through the NSE-20G fabric with no collisions.

Unicast connections have a perfect solution.

**Example**

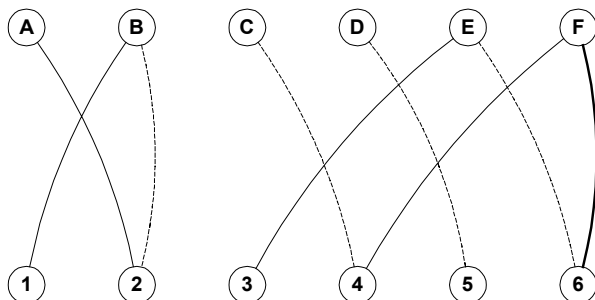
The algorithm is illustrated using an example with 3 timeslots and 6 input/output nodes. The original configuration is shown in Figure 27. The new connection originates at input node **F**, and terminates at output node **6**. This is edge (**F→6**) in the bipartite graph.

**Figure 27 Example Problem**



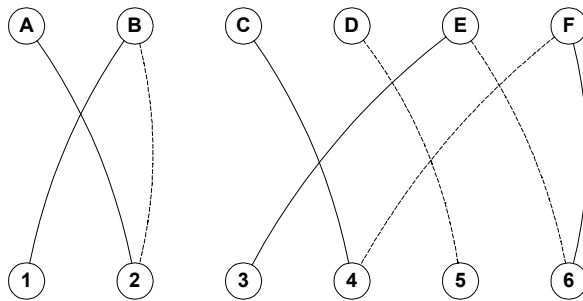
Input node F is available on timeslot 3 and output node 6 is available on timeslot 2. Merging these two timeslots and adding the edge (**F→6**) results in the graph shown in Figure 28. In this graph, the edges assigned to timeslot 3 are shown as dotted lines. The edge (**F→6**) is shown in bold.

**Figure 28 Merged Graph**



There are 3 maximal length paths in the merged graph, (A→2→B→1), (D→5), and (C→4→F→6→E→3). The last path mentioned requires re-labeling. If we start with edge (C→4) and traverse the path, alternately labeling with timeslot 2 and 3, we get the graph in Figure 29. The timeslot labeling in this graph replaces timeslots 2 and 3 in the original graph (and schedule).

**Figure 29 Relabeled Graph**



### 13.3.5 Experimental Results

The performance of PMC-Sierra’s Open Path Algorithm has been studied by implementing it in C++ and running extensive random connection tests.

Tests for NSE/SBS applications of this algorithm used a single NSE-20G connected to 32 SBSs, each carrying a full complement of DS0 connections (258,048 DS0 calls). Many runs were completed in which an initially unloaded switch is presented with a sequence of random call establishment requests up to the point of 100% switching loads. These runs were carried out on a 600 MHz Alpha running Linux. In all of these runs, no octet open path search took longer than 10 μs, thus supporting up to 100,000<sup>1</sup> DS0 call establishments per second. T1s and other aggregates require the establishment of multiple octet open paths; complete T1s can be established at about 3,700 T1/sec. The reasons for this surprisingly good performance are explained in the separate open path algorithm document. It is our opinion that these rates are sufficiently high that the call establishment algorithm should not be a bottleneck in any application of the NSE/SBS, and that this rate is sufficiently high to permit the NSE/SBS to be used for PSTN call establishment rates (up to 100,000 calls/sec in a switch supporting 258,048 full-duplex calls, with the switching core implemented in 1 NSE-20G and 32 SBS chips).

### 13.3.6 Multicast

Scheduling general multicast connections is an entirely different class of problem. With unrestricted multicast, the underlying architecture is non-blocking up to capacity dictated by the number of slots in a frame, but finding the non-blocking schedule is NP-hard. There is no polynomial time running algorithm known to solve this class of problem.

<sup>1</sup> This ignores inband or μP to NSE limitations.

There are two approaches to solving the multicast problem:

- Heuristic algorithms that have statistical probability of success for simple versions of the problem; (and)
- Restricted multicast, where the form of restriction provides a means to solve the scheduling problem.

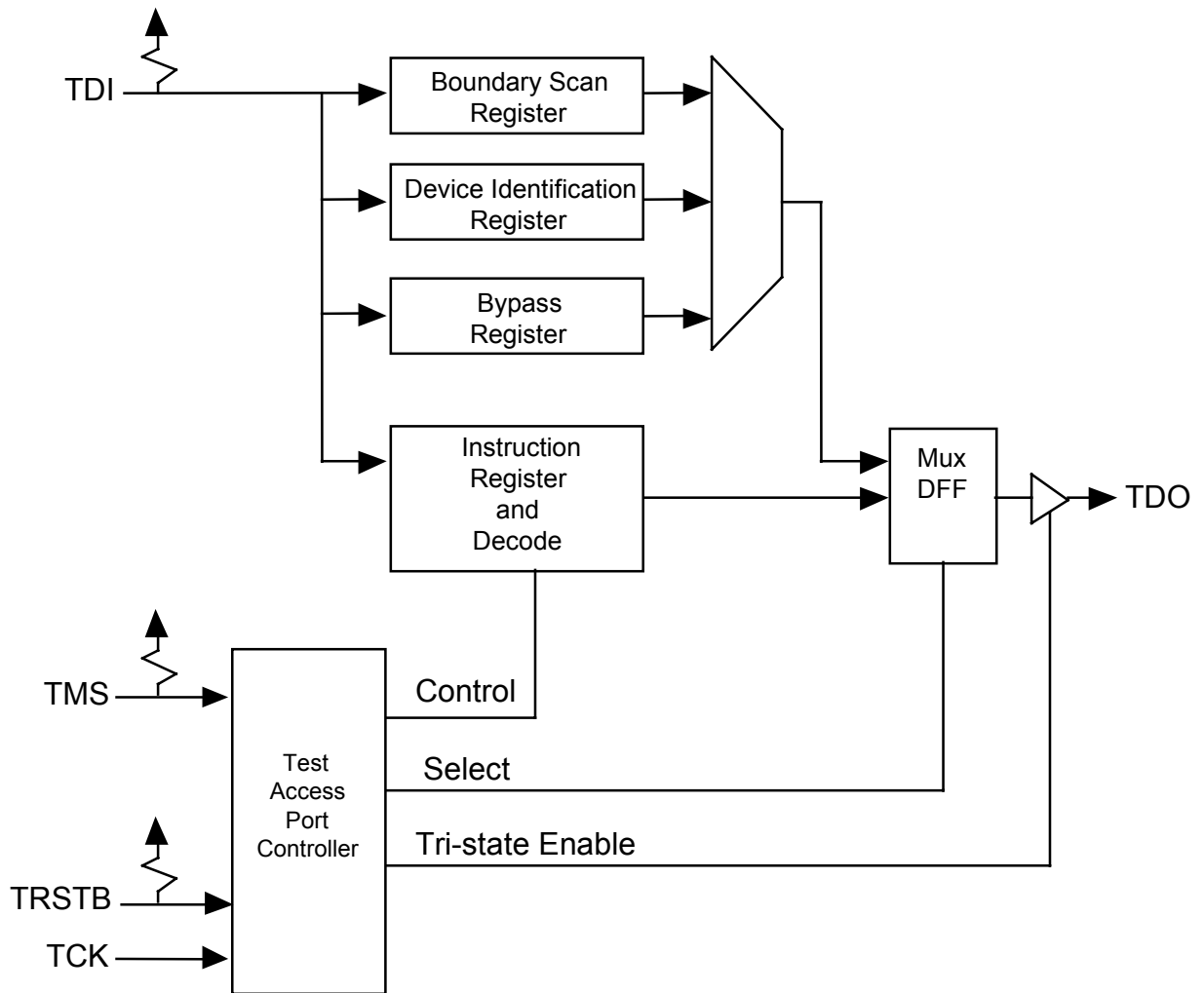
The general multicast problem is not considered in this document. Refer to NSE documentation for descriptions of the use of multicast in a protection switching schemes; the same concepts apply to NSE/SBS fabrics.

## **13.4 JTAG Support**

The SBS supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI, and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Figure 30.



**Figure 30 Boundary Scan Architecture**



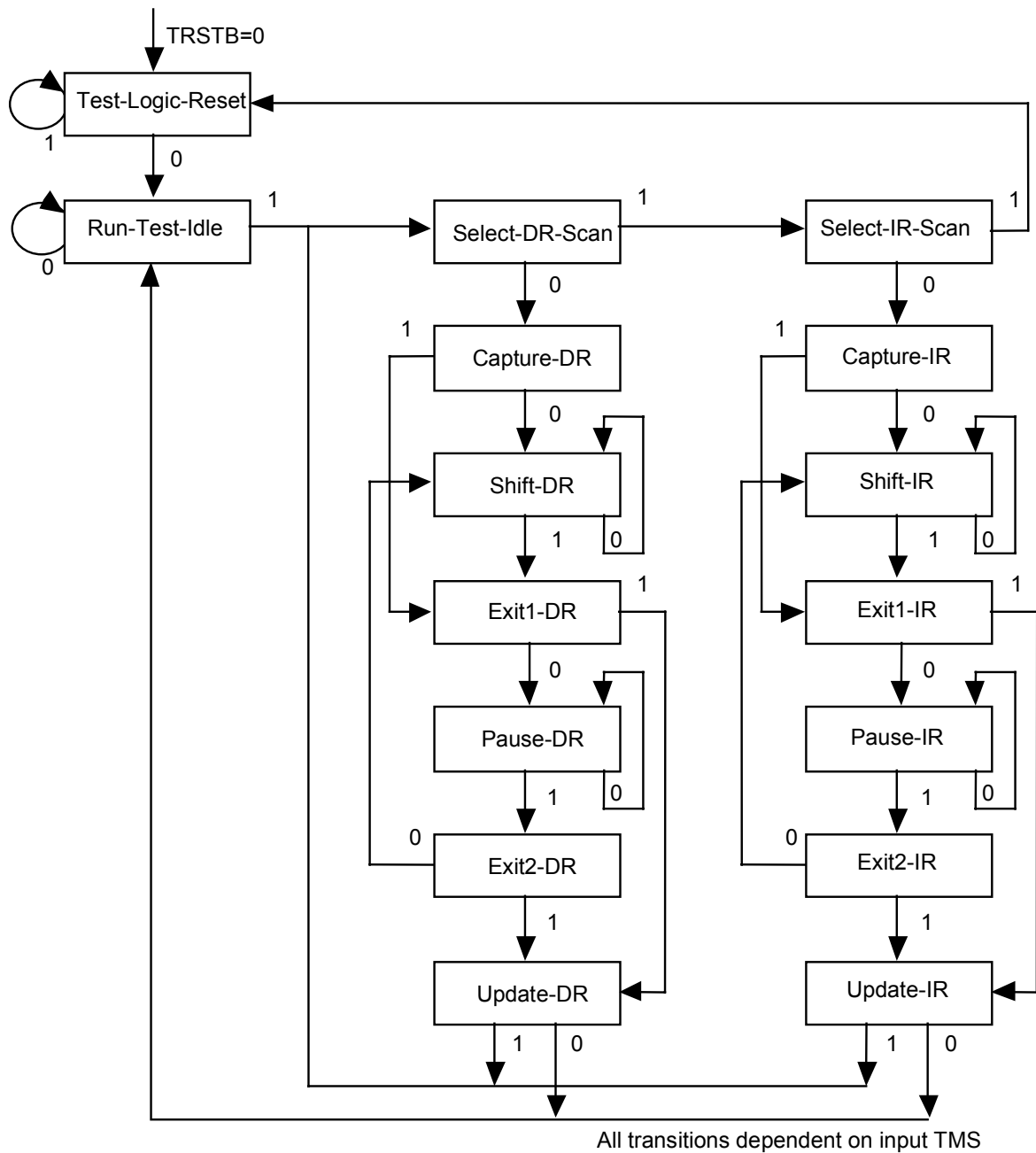
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI, to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI, and forced onto all digital outputs.

### 13.4.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is shown in Figure 31.

**Figure 31 TAP Controller Finite State Machine**



## 13.4.2 States

### **Test-Logic-Reset**

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

### **Run-Test-Idle**

The run test/idle state is used to execute tests.

### **Capture-DR**

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

### **Shift-DR**

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

### **Update-DR**

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

### **Capture-IR**

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

### **Shift-IR**

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

### **Update-IR**

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

## **Boundary Scan Instructions**

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

### **13.4.3 Instructions**

#### **BYPASS**

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

#### **EXTEST**

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

#### **SAMPLE**

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

#### **IDCODE**

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

#### **STCTEST**

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

## 14 Functional Timing

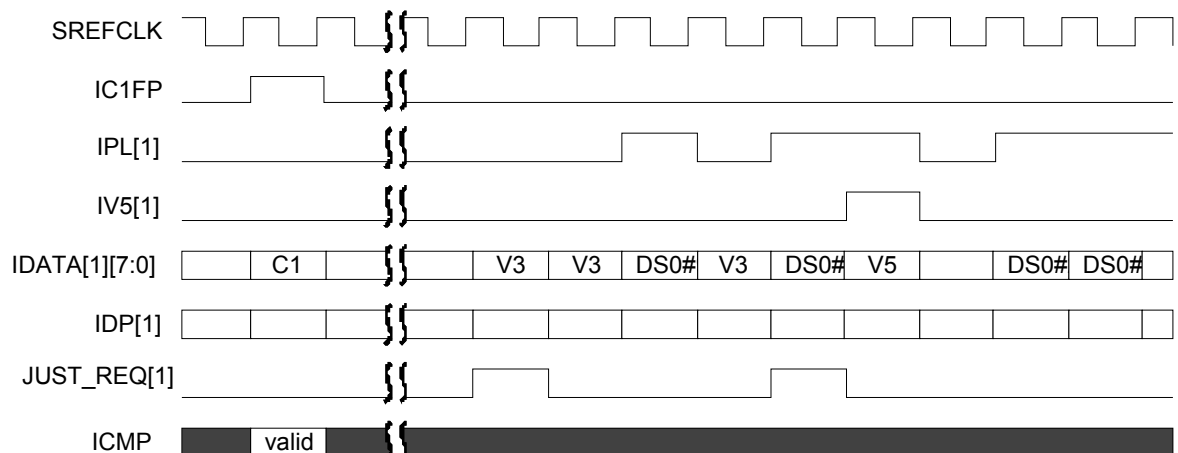
### 14.1 Incoming SBI336 Bus Functional Timing

Figure 32 shows the functional timing for the incoming SBS 77.76 MHz SBI336 bus configured for connection to a physical layer device. When configured for the SBI336 bus timing is provided by a 77.76 MHz SREFCLK which is also connected to SYSCLK. When connecting to a physical layer device the justification request signal, JUST\_REQ, is used by the physical layer device to control link timing from a slave link layer device and is an input to the SBS.

Figure 32 shows a number of capabilities of the SBI bus. IC1FP is a 2 KHz pulse that indicates the SBI336 frame alignment from which all control signals and data are synchronized. The payload signal indicates valid tributary data as well as positive and negative tributary timing adjustments. In Figure 32 the first occurrence of IPL[1] high shows a negative timing adjustment where valid data is carried in the V3 location. The last cycle with IPL[1] low indicates a positive timing adjustment in the tributary octet after V3 where there is no valid data. The IV5[1] signal indicates that the current data octet is the V5 octet used for tributary framing alignment. The JUST\_REQ[1] signal is only valid during the V3 octets and the tributary octets following the V3 octets. The first occurrence of JUST\_REQ[1] high during the V3 octet indicates to the slave link layer device that it should speed next frame by performing a negative timing adjustment. The second occurrence of JUST\_REQ[1] high during the tributary octet after the V3 octet indicates to the slave link layer device that it should slow down by performing a positive timing adjustment during the next frame. The last V3 in the diagram is meant to be the last V3 for all the tributaries.

The ICMP signal selects the active connection memory page in the memory switch. It is sampled at the C1 byte position in every multiframe. ICMP is ignored at all other positions within the SBI frame. The connection memory page is switched on the next SBI bus multiframe boundary after ICMP is sampled. The SBI multiframe can be either 4 or 48 frames, depending on the value of MF\_48 in the SBS Master Configuration Register.

**Figure 32 Incoming SBI336 Functional Timing**



When configured as connecting to a link layer device the JUST\_REQ[1] signal is an output synchronized to OC1FP rather than IC1FP as shown in Figure 32. With the exception of the JUST\_REQ[1] signal, the functional timing of the incoming SBI336 bus is the same when connecting to a Link Layer device as connecting to a physical layer device.

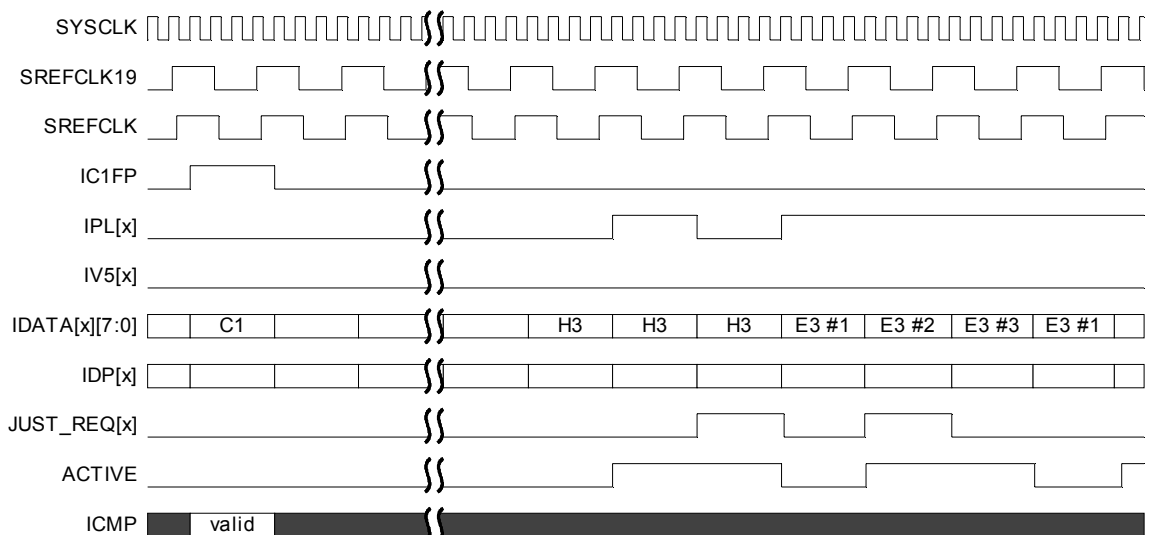
## 14.2 Incoming SBI Bus Functional Timing

Figure 33 shows the functional timing for the four incoming SBI buses. When in SBI mode SREFCLK is a 19.44 MHz clock sourced from SREFCLK19 which is generated from SYSCLK. Figure 33 shows the timing for a 19.44 MHz SBI bus configured as connecting to a link layer device carrying three E3 links. When configured for SBI mode connecting to a link layer device the JUST\_REQ[x] signal is an output synchronized to IC1FP. All other signals in Figure 33 are inputs.

The first occurrence of IPL[x] in Figure 33 shows a negative timing justification during the H3 octet. During this H3 octet there would be actual data for E3#2. The IV5[x] signal would be asserted during any octet carrying a V5 payload indicator. JUST\_REQ[x] in this timing diagram indicates to the link layer device that it should do a positive timing justification on tributary E3#3 and a negative timing justification on tributary E3#2 during the next SBI frame.

With the SBI bus there is also an ACTIVE signal that indicates when a particular SBI device is driving the bus. In Figure 33 the link layer device is configured for E3#2 and E3#3 as indicated by ACTIVE going high during these tributaries.

**Figure 33 Incoming SBI Functional Timing**



When configured as connecting to physical layer device, JUST\_REQ[x] is an input synchronized to OC1FP, therefore JUST\_REQ[x] would not be included in the incoming SBI functional timing diagram when configured for connecting to a physical layer device.

Some SBI devices share a common SBI C1FP signal which locks both the incoming and outgoing SBI buses together. The SBS is not able to support this mode and requires separate incoming IC1FP and outgoing OC1FP SBI frame alignment. This is necessary due to the propagation times through the SBS devices. If these C1FP pulses were to align significant buffering and latency would be added to the system.

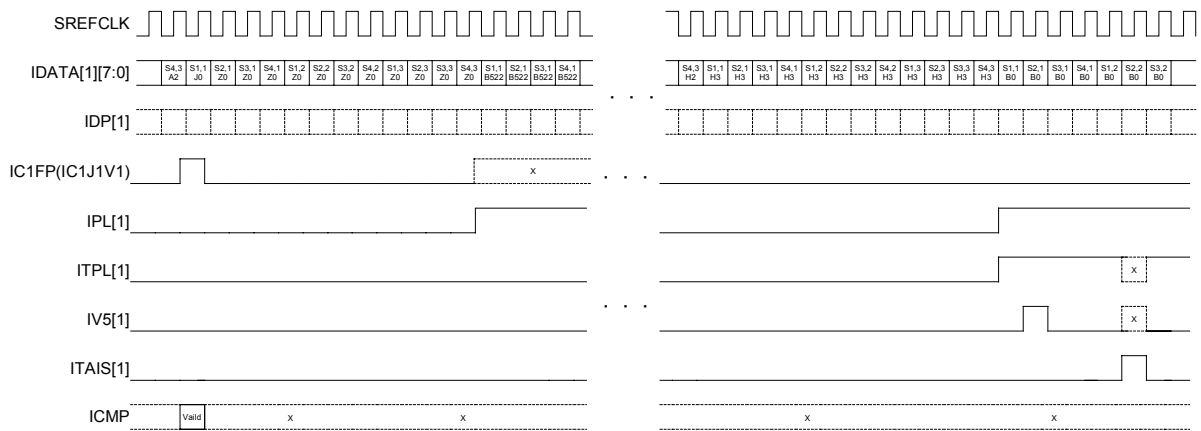
### 14.3 Incoming 77 MHz TelecomBus Functional Timing

Figure 34 shows the timing of the Incoming TelecomBus stream when configured for 77.76 MHz mode. Timing is provided by SREFCLK. SONET/SDH data is carried in the IDATA[1][7:0]. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by S<sub>x,y</sub> and type. Payload bytes are labeled by S<sub>x,y</sub> and B<sub>n</sub>, where 'n' is the active offset of the byte. Within S<sub>x,y</sub>, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The IPL[1] signal is set high to mark payload bytes and is set low at all other bytes. Similarly, ITPL[1] is set high to mark tributary payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal IJ0J1V1 is equivalent to the IC1FP in SBI mode and is set high with IPL[1] set low to mark the J0 byte of a transport frame. IC1J1V1/IC1FP is set high with IPL[1] set high to mark the J1 bytes and V1 multiframe of all the streams within IDATA[1][7:0]. The SBS requires that all J1s follow immediately after the J0(Z0) or the H3 overhead bytes and therefore ignores the IC1J1V1 signal during these 12 J1 locations. The SBS also requires that all H4 multiframes be aligned forcing all V1 bytes to follow the J1 bytes as shown in Figure 35. Multiframe alignment is based on the first V1 indication by IC1J1V1 after the twelve J1 bytes. Tributary path frame boundaries are marked by a logic high on the IV5[1] signal. Tributaries in AIS alarm are indicated by the ITAIS[1] signal.

The ICMP signal selects the active connection memory page in the memory switch. It is only valid at the J0 byte position and is ignored at all other positions within the transport frame. The connection memory page is switched on the next TelecomBus frame boundary after ICMP is sampled at the J0 byte.

In Figure 34 below, STS-3/STM-1 numbers 1, 2, and 4 are configured for STS-3/AU3 operation. STS-3/STM-1 number 3 is configured for STS-3c/AU4 operation. All streams are shown to have an active offset of 522 by the high level on IPL[1] and IC1J1V1/IC1FP at byte S<sub>x,y</sub>/B522. No pointer justifications are shown nor permitted by the SBS. All stream are configured to carry virtual tributaries/tributary units. The payload frame boundary of one such tributary is located at byte S<sub>2,1</sub>/B0, as marked by a high level on IV5[1]. At byte S<sub>2,2</sub>/B0, the tributary carried in stream S<sub>2,2</sub> (2 (STM-1 #2, AU3 #2) is shown to be in tributary path AIS by the high level on ITAIS[1] signal. The arrangement shown in Figure 34 is for illustrative purposes only; other configurations, alarm conditions, active offsets and justification events, etc. are possible.

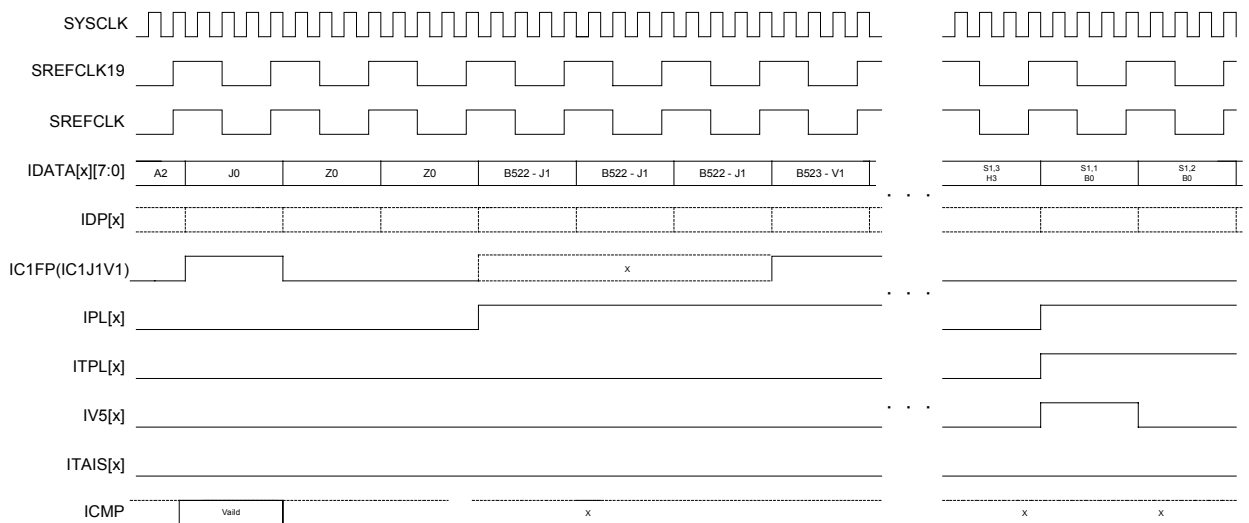
**Figure 34 Incoming 77 MHz TelecomBus Functional Timing**



## 14.4 Incoming 19 MHz TelecomBus Functional Timing

Figure 35 shows the Incoming TelecomBus interface configured for 19.44 MHz mode. The figure is very similar to Figure 34 with one quarter the number of synchronous payload envelopes. Timing is provided by a 19.44 MHz SREFCLK sourced from SREFCLK19 which is generated by the SBS from the 77.76 MHz SYSCLK.

**Figure 35 Incoming 19 MHz TelecomBus Functional Timing**



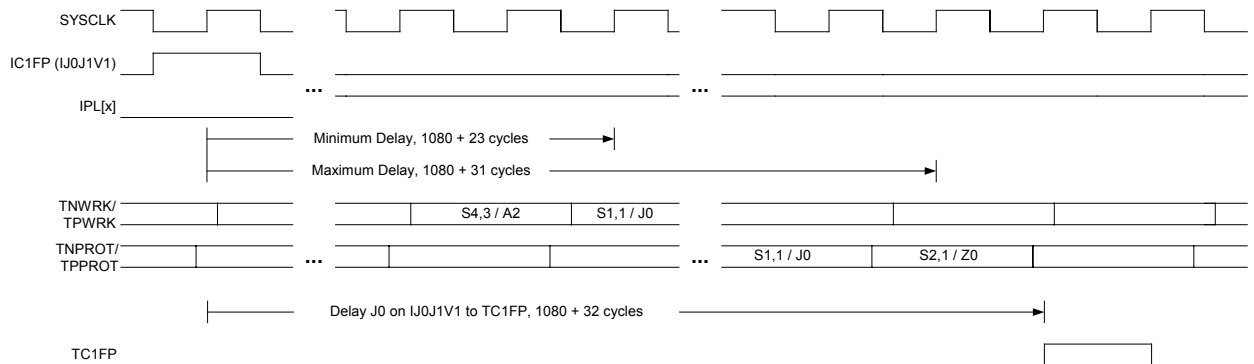
## 14.5 Transmit Serial LVDS Functional Timing

The delay through the SBS is dependent on the operating mode. The timing from the Incoming telecom or SBI bus to the LVDS link differs between TelecomBus mode and SBI mode. The timing when in SBI mode is also dependent on whether the SBS is switching at the DS0 level and above or is switching only at the tributary level. When switching only tributaries in SBI mode we have the same delay through the SBS as when switching tributaries in TelecomBus mode.



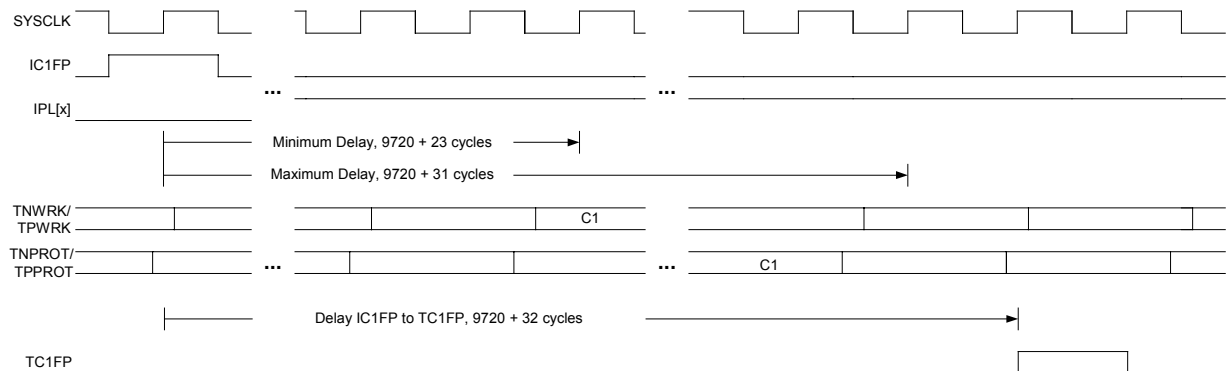
When switching tributaries in SBI mode or when in TelecomBus mode the SBS is acting as a column switch and introduces a minimum delay equivalent to one row in a 77.76 MHz TelecomBus structure or SBI336 bus structure. This minimum delay equates to 1080 SYSCLK cycles. The actual delay will be slightly longer by no more than 31 SYSCLK cycles to allow for other data path delays within the SBS.

**Figure 36 Incoming TelecomBus to LVDS Functional Timing**



When switching DS0s in SBI mode the minimum data delay through the SBS increases to an entire SBI336 frame or 9720 SYSCLK cycles. The actual delay will be slightly longer by no more than 31 SYSCLK cycles to allow for other data path delays within the SBS. The Channel Associated Signaling delay through the SBS will be two full T1 or E1 multiframes which is 4 mS for E1 links and 6 mS for T1 links.

**Figure 37 Incoming SBI Bus to LVDS Timing with DS0 Switching**



The relative delay from the Incoming bus to either of the working and protect LVDS links may be different but will be within a couple of SYSCLK cycles of each other.

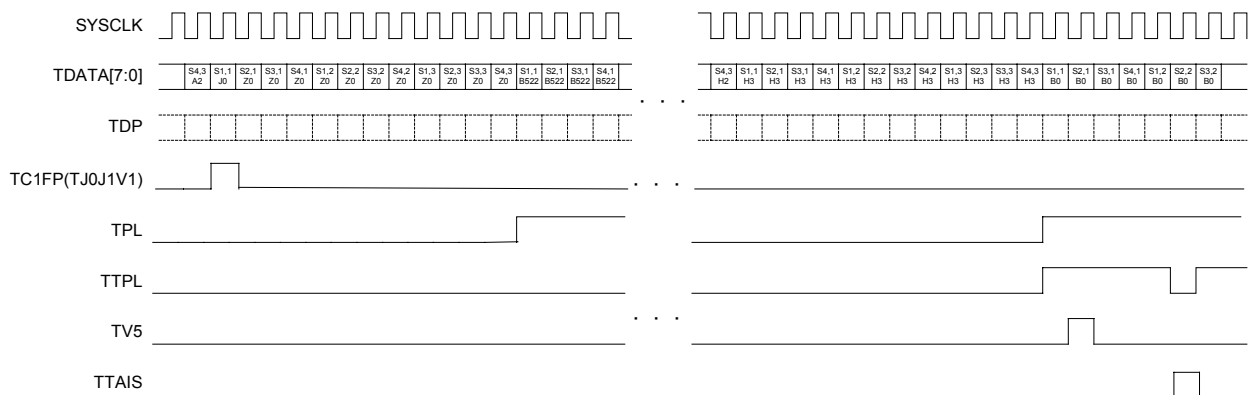
Although Figure 36 and Figure 37 show IC1FP or IJ0J1V1 relative to SYSCLK, IC1FP(IJ0J1V1) is sampled by SREFCLK at either 77.76 MHz or 19.44 MHz.

## 14.6 Transmit TelecomBus Functional Timing

The delay from the Incoming TelecomBus, either four by 19.44 MHz buses or one 77.76 MHz bus, to the transmit TelecomBus is the same as the delay to the serial LVDS interface. There is a slight difference in the overall delay since the fifos of the serial LVDS link are no longer in the path and therefore the absolute delay is more controlled. The total delay is from the incoming TelecomBus to the transmit TelecomBus is 1080+12 77.76 MHz SYSCLK cycles.

Figure 38 shows the transmit TelecomBus functional timing. The transmit TelecomBus has only a couple of small differences from the incoming 77.76 MHz TelecomBus, in fact without column switching they could be identical. The main functional difference is in how the TC1FP(TJ0J1V1) signal is handled. TJ0J1V1 will pulse during the J0 byte position, but must be configured to pulse during the J1 and V1 positions if desired. This is shown in Figure 38.

**Figure 38 Transmit TelecomBus Functional Timing**



## 14.7 Transmit SBI336 Bus Functional Timing

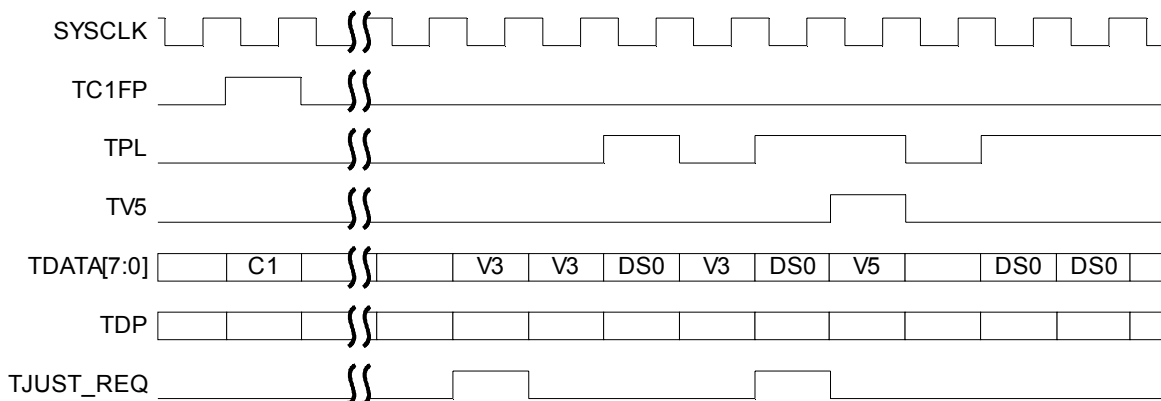
The delay from the Incoming SBI/SBI336 bus to the transmit SBI336 bus is the same as the delay to the serial LVDS interface. There is a slight difference in the overall delay since the FIFOs of the serial LVDS link are no longer in the path and therefore the absolute delay is more controlled.

When switching SBI tributaries the total delay is 1080+12 SYSCLK cycles. When switching DS0s the data delay is 9720+12 SYSCLK cycles and the CAS delay is the T1 or E1 multiframe + 12 clocks.

The transmit SBI336 interface is functionally the same as the incoming 77.76 MHz SBI336 interface. Figure 39 shows the transmit SBI336 bus timing. Like Figure 32 it shows positive and negative timing adjustments via the TPL signal, a V5 tributary frame alignment and positive and negative justification requests via TJUST\_REQ.

The use of TJUST\_REQ on the transmit SBI336 interface is dependent on whether the SBS is configured as connecting to a physical layer device or link layer device. The interface connection type refers to the Incoming and Outgoing SBI buses therefore the configuration of the transmit SBI336 interface is opposite to that of the Incoming SBI336 bus. In Figure 39 TJUST\_REQ is shown as a transmit SBI336 bus output which is consistent with the SBS configured for connection to a physical layer device, meaning that the transmit SBI336 interface is expected to connect to a link layer type device. When the SBS is configured for connection to a link layer device, TJUST\_REQ is not used and is held low.

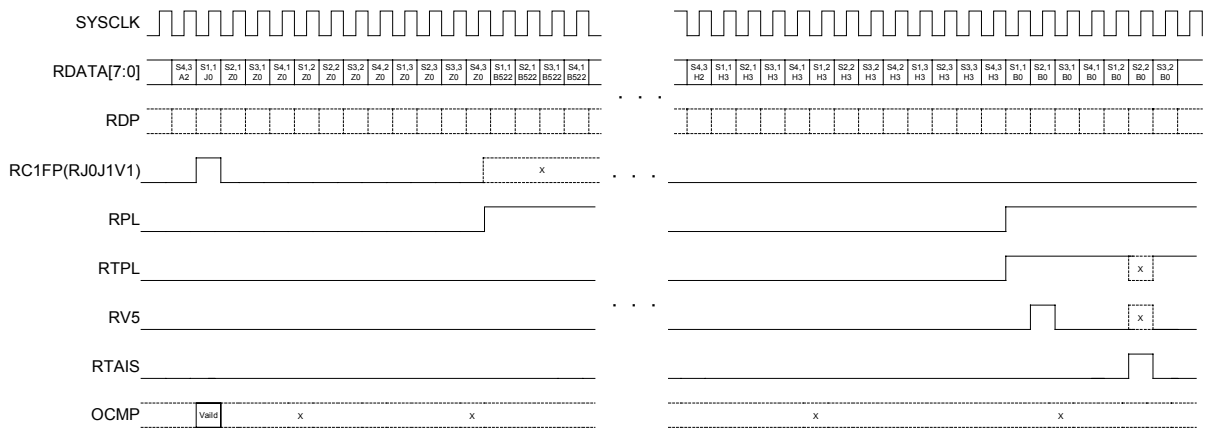
**Figure 39 Transmit SBI336 Functional Timing Diagram**



## 14.8 Receive TelecomBus Functional Timing

Figure 40 shows the receive TelecomBus functional timing. This figure is very similar to the Incoming 77.76 MHz TelecomBus Functional Timing shown in Figure 34. The main difference is that the timing is provided by the 77.76 MHz SYSCLK.

**Figure 40 Receive TelecomBus Functional Timing**

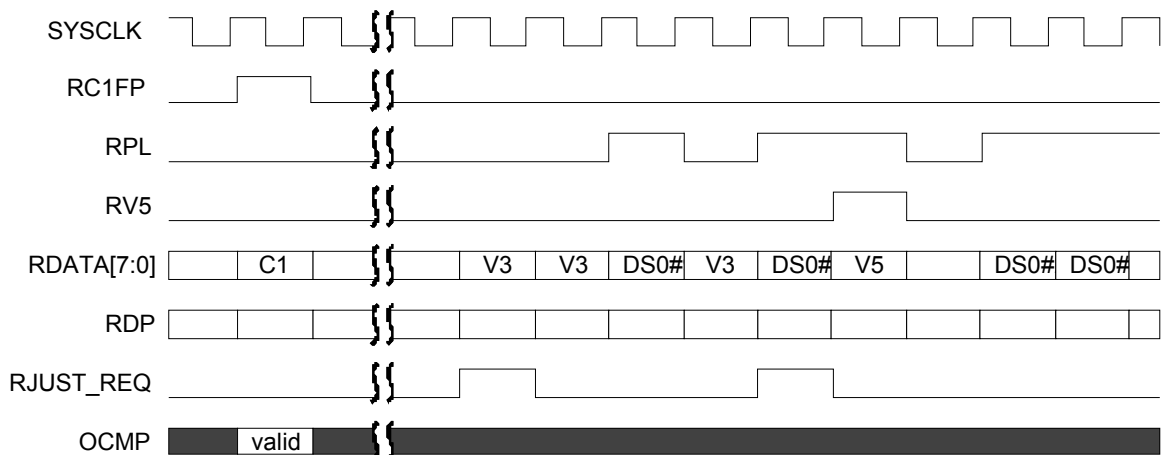


## 14.9 Receive SBI336 Functional Timing

Figure 41 shows the receive TelecomBus functional timing. This figure is very similar to the Incoming SBI336 Functional Timing shown in Figure 32. The main difference is that the timing is provided by the 77.76 MHz SYSCLK.

The use of RJUST\_REQ on the receive SBI336 interface is dependent on whether the SBS is configured as connecting to a physical layer device or link layer device. The interface connection type refers to the Incoming and Outgoing SBI buses therefore the configuration of the receive SBI336 interface is opposite to that of the Outgoing SBI336 bus. In Figure 41 RJUST\_REQ is shown as a receive SBI336 bus input which is consistent with the SBS configured for connection to a link layer device, meaning that the receive SBI336 interface is expected to connect to a physical layer type device. When the SBS is configured for connection to a physical layer device, RJUST\_REQ is not used.

**Figure 41 Receive SBI336 Functional Timing**



## 14.10 Receive Serial LVDS Functional Timing

Figure 42 below shows the relative timing of the receive LVDS links. In TelecomBus mode links carry SONET/SDH frame octets that are encoded in 8B/10B characters. Frame boundaries, tributary justification events and tributary alarm conditions are encoded in special control characters. The upstream devices sourcing the links share a common clock and have a common transport frame alignment that is synchronized by the Receive Serial Interface Frame Pulse signal (RC1FP). Due to phase noise of clock multiplication circuits and backplane routing discrepancies, the links will not be phase aligned to each other (within a tolerance level of 24 byte times) but are frequency locked. The delay from RC1FP being sampled high to the first and last J0 character is shown in Figure 42. In this example, the first J0 is delivered by the working link (RNWRK/RPWRK). The delay to the last J0 represents the time when both links have delivered their J0 character. The minimum value for the internal programmable delay (RC1FPDLY[13:0]) is the delay to the last J0 character plus 15. The maximum value is the delay to the first J0 character plus 31. Consequently, the external system must ensure that the relative delays between all the receive LVDS links be less than 16 bytes. The relative phases of the links in Figure 42 are shown for illustrative purposes only.

**Figure 42 Receive LVDS Link Timing**

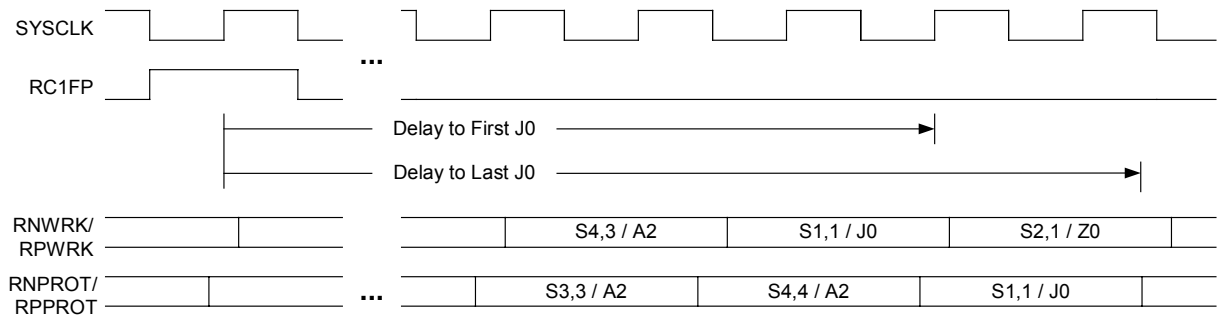
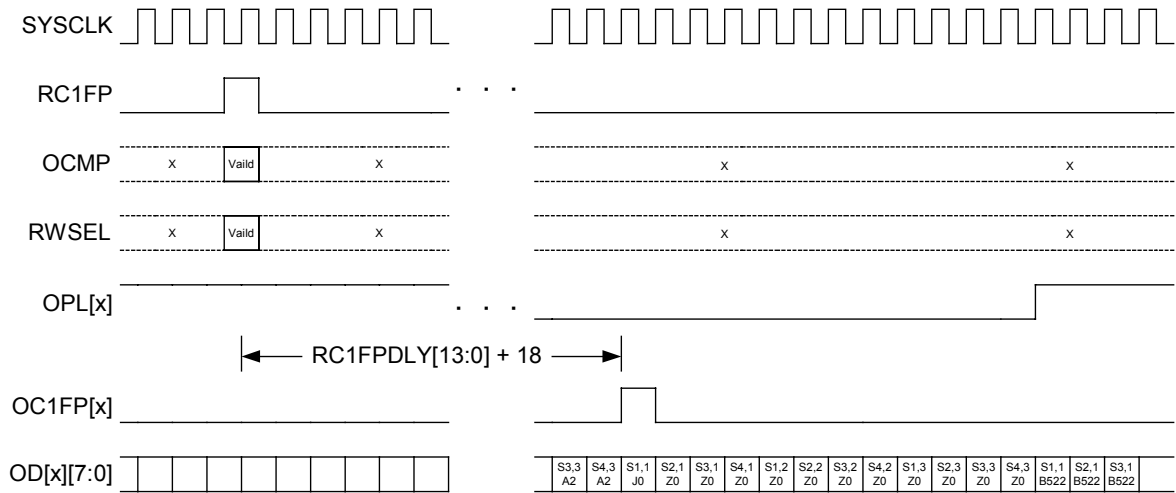


Figure 43 shows the timing relationships around the RC1FP signal. The Outgoing Memory Page selection signal (OCMP) and the Receive Working Serial Data Select signal (RWSEL) are only valid at the SYSCLK cycle located by RC1FP. They are ignored at all other locations within the transport frame. The delay from RC1FP is to the J0 byte on the outgoing SBI or TelecomBus stream is the sum of the value programmed into the RC1FPDLY[13:0] register and processing delay of 18 SYSCLK cycles.

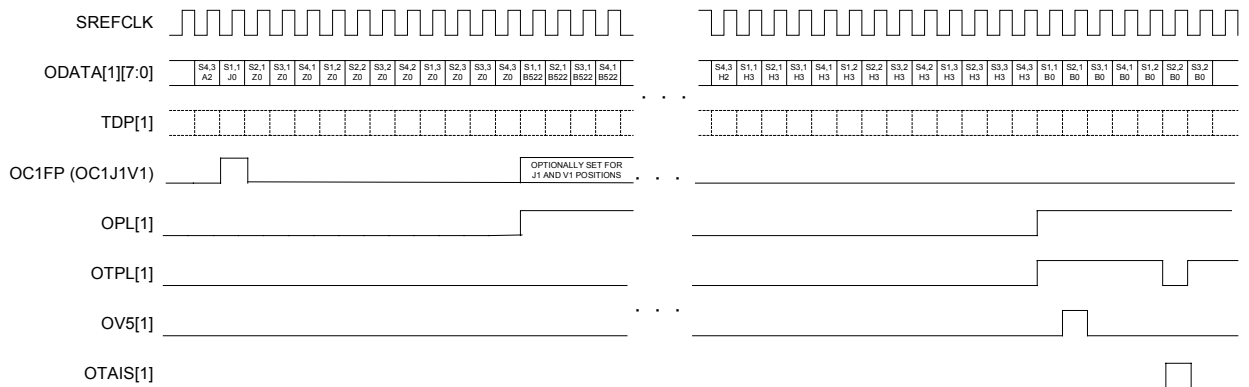
**Figure 43 Outgoing Synchronization Timing**



## 14.11 Outgoing 77.76 MHz TelecomBus Functional Timing

Figure 44 shows the timing of the Outgoing TelecomBus stream. Timing is provided by SREFCLK. SONET/SDH data is carried on the ODATA[1][7:0] signals. The bytes are arranged in order of transmission in an STS-12/STM-4 stream. Each transport/section overhead byte is labeled by S<sub>x,y</sub> and type. Payload bytes are labeled by S<sub>x,y</sub> and B<sub>n</sub>, where 'n' is the active offset of the byte. Within S<sub>x,y</sub>, the STS-3/STM-1 number is given by 'x' and the column number within the STS-3/STM-1 is given by 'y'. The OPL[1] signal is set high to mark payload bytes and is set low at all other bytes. Similarly, OTPL[1] is set high to mark tributary payload bytes and is set low at all other bytes. The composite transport frame and payload frame signal, OC1FP[1] (OJ0J1V1[1]), is set high with OPL[1] set low to mark the J0 byte of a transport frame. OJ0J1V1[1] is optionally set high with OPL[1] also set high to mark the J1 byte and the byte following J1 of all the streams within ODATA[1][7:0]. Tributary path frame boundaries are marked by a logic high on the OTV5[1] signal. Tributaries in AIS alarm are indicated by the OTAIS[1] signal.

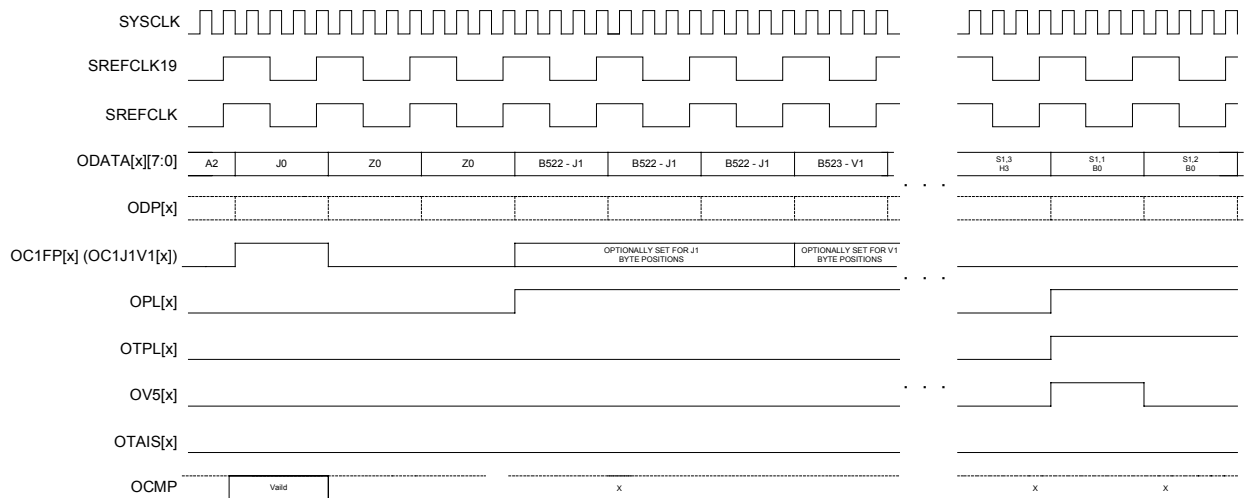
**Figure 44 Outgoing 77.76 MHz TelecomBus Functional Timing**



## 14.12 Outgoing 19.44 MHz TelecomBus Functional Timing

Figure 45 shows the Outgoing TelecomBus interface configured for 19.44 MHz mode. The figure is very similar to Figure 44 with one quarter the number of synchronous payload envelopes. Timing is provided by a 19.44 MHz SREFCLK sourced from SREFCLK19 which is generated by the SBS from the 77.76 MHz SYSCLK.

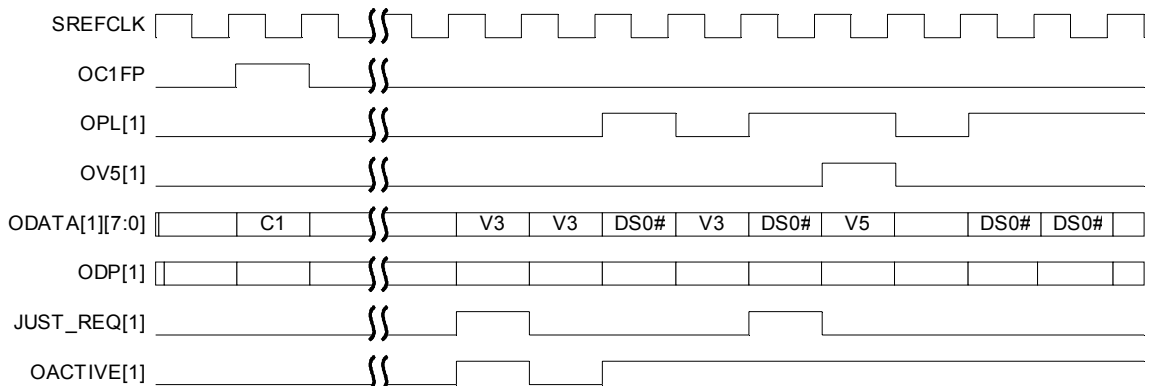
**Figure 45 Outgoing 19.44 MHz TelecomBus Functional Timing**



## 14.13 Outgoing SBI336 Functional Timing

Figure 46 shows the functional timing for the outgoing 77.76 MHz SBI336 bus configured for connection to a link layer device. When configured for the SBI336 bus, timing is provided by a 77.76 MHz SREFCLK which is also connected to SYSCLK. When connecting to a link layer device the justification request signal, JUST\_REQ[1], is output from the SBS and is used to control the link timing. If the SBS is connected to a physical layer device the JUST\_REQ[1] signal is an input synchronized to IC1FP rather than OC1FP. With the exception of the JUST\_REQ[1] signal, the functional timing of the outgoing SBI336 bus is the same when connecting to a physical layer device as connecting to a link layer device.

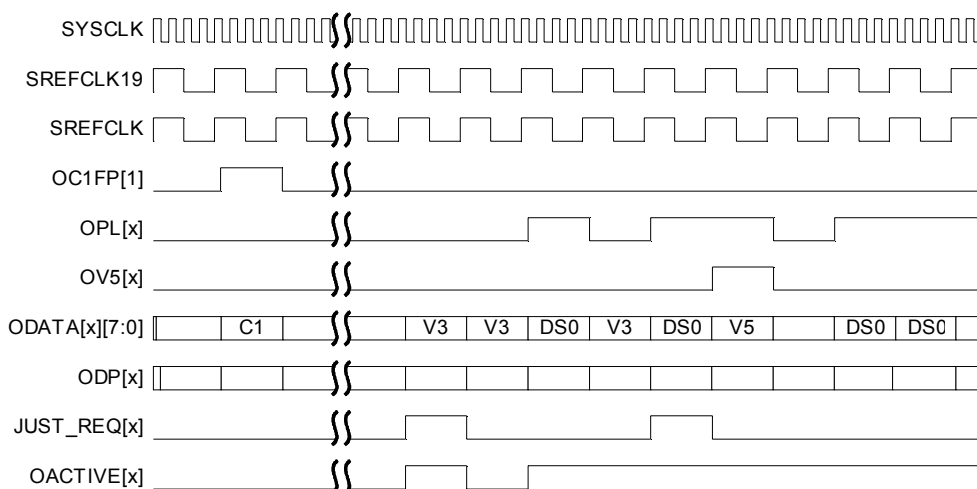
**Figure 46** Outgoing SBI336 Functional Timing



### 14.14 Outgoing SBI Bus Functional Timing

Figure 47 shows the functional timing for 4 outgoing 19.44 MHz SBI buses. When configured for the SBI bus, timing is provided by a 19.44 MHz SREFCLK sourced from SREFCLK19 which is generated by the SBS from the 77.76 MHz SYSCLK. Figure 47 shows the timing for a 19.44 MHz SBI bus configured to connect to a physical layer device. In this figure the JUST\_REQ[x] signal is an input to the SBS aligned to OC1FP and is used by the physical layer device to control the link timing of a slave link layer device. If the SBS is connected to a link layer device, the JUST\_REQ[x] signal would be an output aligned to IC1FP. With the exception of the JUST\_REQ[x] signal, the functional timing of the outgoing SBI bus is the same when connecting to a physical layer device as connecting to a link layer device.

**Figure 47** Outgoing SBI Bus Functional Timing





## 15 Absolute Maximum Ratings

Maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

**Table 28 Absolute Maximum Ratings**

<b>Case Temperature under Bias</b>	-40°C to +85°C
<b>Storage Temperature</b>	-40°C to +125°C
<b>Supply Voltage (DVDDO[x])</b>	-0.3V to +4.6V
<b>Supply Voltage (DVDDI[x])</b>	-0.3V to +3.6V
<b>Voltage on Any Digital Pin</b>	-0.3V to DVDDO + 0.5V
<b>Static Discharge Voltage</b>	±1000 V
<b>Latch-Up Current</b>	±100 mA
<b>DC Input Current</b>	±20 mA
<b>Lead Temperature</b>	+230°C
<b>Absolute Maximum Junction Temperature</b>	+150°C

## 16 D. C. Characteristics

$T_C = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DDO} = 3.3\text{ V} \pm 8\%$ ,  $V_{DDI} = 1.8\text{ V} \pm 5\%$   
(Typical Conditions:  $T_C = 25\text{ }^\circ\text{C}$ ,  $V_{DDO} = 3.3\text{ V}$ ,  $V_{DDI} = 1.8\text{ V}$ )

**Table 29 D.C Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDDO	Power Supply	3.04	3.3	3.56	Vs	
VDDI	Power Supply	1.71	1.8	1.89	Vs	
VIL	Input Low Voltage	0		0.8	Vs	Guaranteed Input Low Voltage.
VIH	Input High Voltage	1.7		VDDO +0.5	Vs	Guaranteed Input High Voltage.
VOL	Output or Bi-directional Low Voltage		0.1	0.4	Vs	Guaranteed output Low Voltage at VDDO =3.04V and IOL = -2ma minimum.
VOH	Output or Bi-directional High Voltage	2.4	2.7		Vs	Guaranteed output High Voltage at VDDO =3.04V and IOH = -2ma minimum.
VT+	Reset Input High Voltage	2.0		VDDO +0.5	Vs	Applies to RSTB and TRSTB only.
VT-	Reset Input Low Voltage	-0.5		0.8	Vs	Applies to RSTB and TRSTB only.
VTH	Reset Input Hysteresis Voltage		0.5		Vs	Applies to RSTB and TRSTB only.
IILPU	Input Low Current	+20	+83	+200	$\mu\text{A}$	VIL = GND. Notes 1 and 3.
IIHPU	Input High Current	-10	0	+10	$\mu\text{A}$	VIH = VDD. Notes 1 and 3.
IIL	Input Low Current	-10	0	+10	$\mu\text{A}$	VIL = GND. Notes 2 and 3.
IIH	Input High Current	-10	0	+10	$\mu\text{A}$	VIH = VDD. Notes 2 and 3.
CIN	Input Capacitance		5		pF	tA=25°C, f = 1 MHz
COUT	Output Capacitance		5		pF	tA=25°C, f = 1 MHz
CIO	Bi-directional Capacitance		5		pF	tA=25°C, f = 1 MHz
IDDOP1	Operating Current			TBD	mA	VDDO = 3.56V, VDDI = 1.89V, Outputs Unloaded (4x19.44 MHz Incoming/Outgoing interface with Parallel Tx/Rx interface)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
IDDOP2	Operating Current			TBD	mA	VDDO = 3.56V, VDDI = 1.89V, Outputs Unloaded (77.76 MHz Incoming Outgoing interface with Serial LVDS Tx/Rx interface)

**Notes on D.C. Characteristics**

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

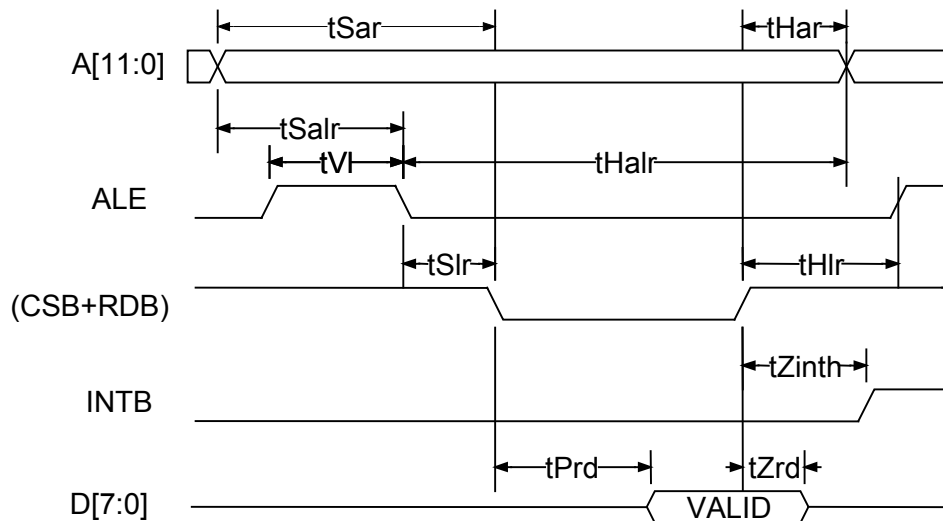
## 17 Microprocessor Interface Timing Characteristics

( $T_C = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DDO} = 3.3\text{ V} \pm 8\%$ ,  $V_{DDI} = 1.8\text{ V} \pm 5\%$ )

**Table 30 Microprocessor Interface Read Access (Figure 48)**

Symbol	Parameter	Min	Max	Units
tSAR	Address to Valid Read Set-up Time	5		ns
tHAR	Address to Valid Read Hold Time	5		ns
tSALR	Address to Latch Set-up Time	5		ns
tHALR	Address to Latch Hold Time	5		ns
tVL	Valid Latch Pulse Width	2		ns
tSLR	Latch to Read Set-up	0		ns
tHLR	Latch to Read Hold	5		ns
tPRD	Valid Read to Valid Data Propagation Delay		15	ns
tZRD	Valid Read Negated to Output Tri-state		15	ns
tZINTH	Valid Read Negated to INTB High		20	ns

**Figure 48 Microprocessor Interface Read Timing**



### Notes on Microprocessor Interface Read Timing

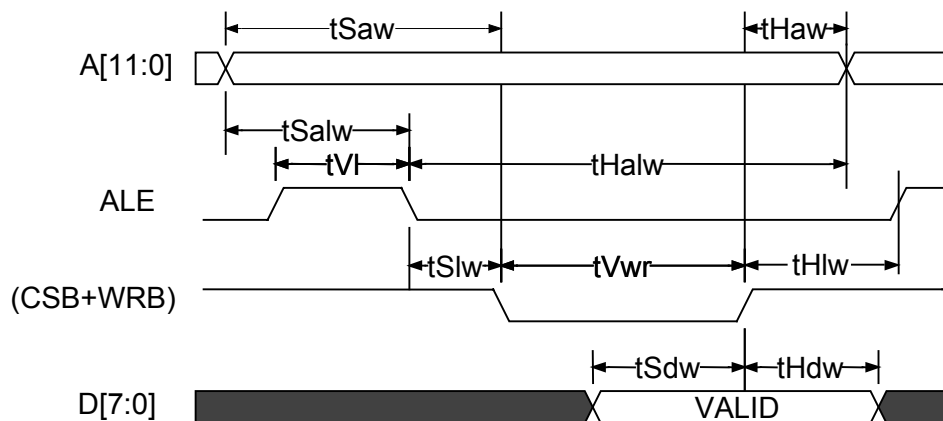
1. Output propagation delay time is the time in nanoseconds from the 1.4 V point of the reference signal to the 1.4 V point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters  $t_{SALR}$ ,  $t_{HALR}$ ,  $t_{VL}$ ,  $t_{SLR}$ , and  $t_{HLR}$  are not applicable.
5. Parameter  $t_{HAR}$  is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 V point of the input to the 1.4 V point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 V point of the input to the 1.4 V point of the clock.

**Table 31 Microprocessor Interface Write Access (Figure 49)**

Symbol	Parameter	Min	Max	Units
tSAW	Address to Valid Write Set-up Time	5		ns
tSDW	Data to Valid Write Set-up Time	10		ns
tSALW	Address to Latch Set-up Time	5		ns
tHALW	Address to Latch Hold Time	5		ns
tVL	Valid Latch Pulse Width	2		ns
tSLW	Latch to Write Set-up	0		ns
tHLW	Latch to Write Hold	5		ns
tHDW	Data to Valid Write Hold Time	5		ns
tHAW	Address to Valid Write Hold Time	5		ns
tVWR	Valid Write Pulse Width	15		ns

**Figure 49 Microprocessor Interface Write Timing**



**Notes on Microprocessor Interface Write Timing**

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALW, tHALW, tVL, tSLW, and tHLW are not applicable.
3. Parameter tHAW is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 V point of the input to the 1.4 V point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 V point of the input to the 1.4 V point of the clock.

## 18 A.C. timing Characteristics

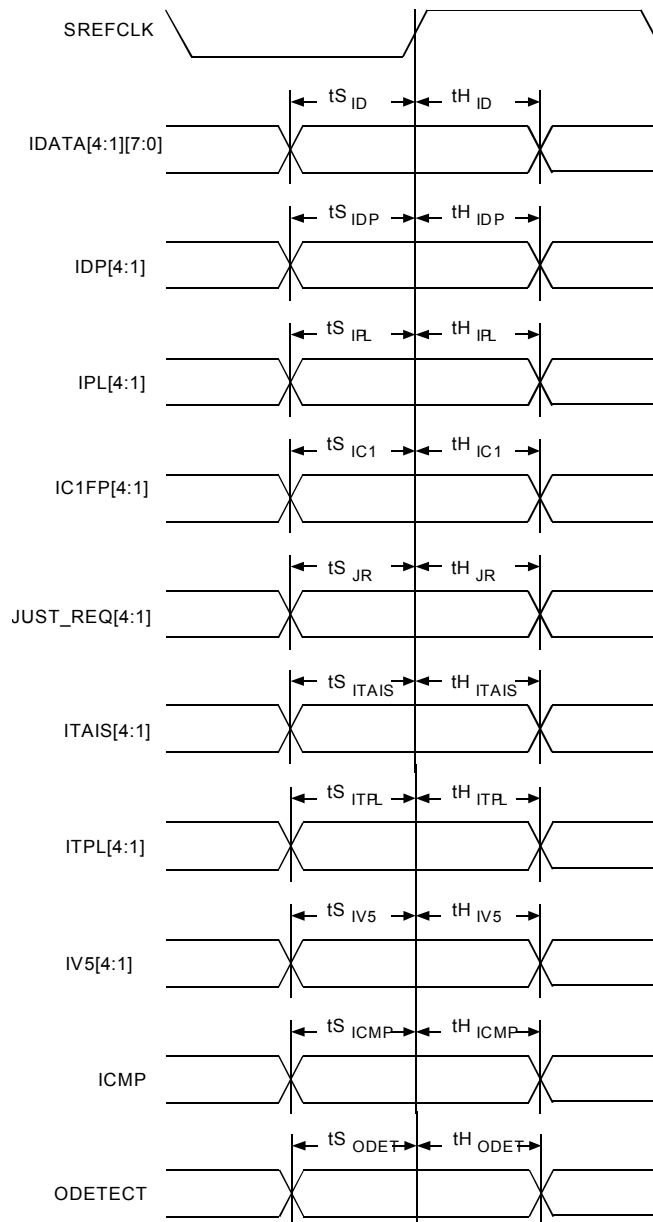
( $T_C = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DDO} = 3.3\text{V} \pm 8\%$ ,  $V_{DDI} = 1.8\text{V} \pm 5\%$ )

### 18.1 SBS Incoming Bus Timing

**Table 32 SBS Incoming Timing (Figure 50)**

Symbol	Description	Min	Max	Units
	SREFCLK Frequency (nominally 19.44 MHz or 77.76 MHz )	-50	+50	ppm
	SREFCLK Duty Cycle	40	60	%
tSID	IDATA[4:1][7:0] Set-up Time	3		ns
tHID	IDATA[4:1][7:0] Hold Time	0		ns
tSIDP	IDP[4:1] Set-up Time	3		ns
tHIDP	IDP[4:1] Hold Time	0		ns
tS PL	IPL[4:1] Set-Up Time	3		ns
tH PL	IPL[4:1] Hold Time	0		ns
tS C1	IC1FP[4:1] Set-Up Time	3		ns
tH C1	IC1FP[4:1] Hold Time	0		ns
tSJR	JUST_REQ[4:1] Set-Up Time	3		ns
tHJR	JUST_REQ[4:1] Hold Time	0		ns
tS TAIS	ITAIS[4:1] Set-Up Time	3		ns
tH TAIS	ITAIS[4:1] Hold Time	0		ns
tS TPL	ITPL[4:1] Set-Up Time	3		ns
tH TPL	ITPL[4:1] Hold Time	0		ns
tS V5	IV5[4:1] Set-Up Time	3		ns
tH V5	IV5[4:1] Hold Time	0		ns
tS CMP	ICMP Set-Up Time	3		ns
tH CMP	ICMP Hold Time	0		ns
tSODET	ODETECT[4:1] Set-Up Time	3		ns
tHODET	ODETECT[4:1] Hold Time	0		ns

**Figure 50 SBS Incoming Timing**



## 18.2 SBS Receive Bus Timing

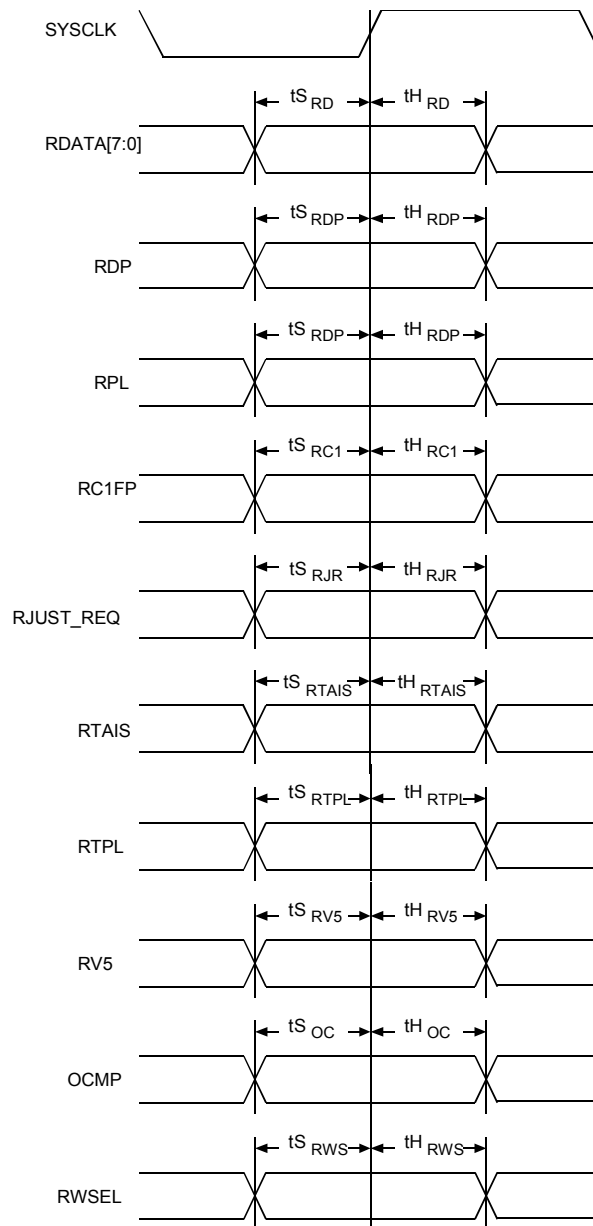
**Table 33 SBS Receive Timing (Figure 51)**

Symbol	Description	Min	Max	Units
	SYSCCLK Frequency (nominally 77.76 MHz )	-50	+50	ppm
	SYSCCLK Duty Cycle	40	60	%
tSRD	RDATA[7:0] Set-up Time	3		ns



<b>Symbol</b>	<b>Description</b>	<b>Min</b>	<b>Max</b>	<b>Units</b>
tHRD	RDATA[7:0] Hold Time	0		ns
tSRDP	RDP Set-up Time	3		ns
tHRDP	RDP Hold Time	0		ns
tSRPL	RPL Set-Up Time	3		ns
tHRPL	RPL Hold Time	0		ns
tSRC1	RC1FP Set-Up Time	3		ns
tHRC1	RC1FP Hold Time	0		ns
tSRJR	RJUST_REQ Set-Up Time	3		ns
tHRJR	RJUST_REQ Hold Time	0		ns
tSRTAIS	RTAIS Set-Up Time	3		ns
tHRTAIS	RTAIS Hold Time	0		ns
tSRPL	RTPL Set-Up Time	3		ns
tHRPL	RTPL Hold Time	0		ns
tSRV5	RV5 Set-Up Time	3		ns
tHRV5	RV5 Hold Time	0		ns
tSOC	OCMP Set-Up Time	3		ns
tHOC	OCMP Hold Time	0		ns
tSRWS	RWSEL Set-Up Time	3		ns
tHRWS	RWSEL Hold Time	0		ns

**Figure 51 SBS Receive Timing**



**Notes on Input Timing**

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 V point of the input to the 1.4 V point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 V point of the clock to the 1.4 V point of the input.

### 18.3 SBS Outgoing Bus Timing

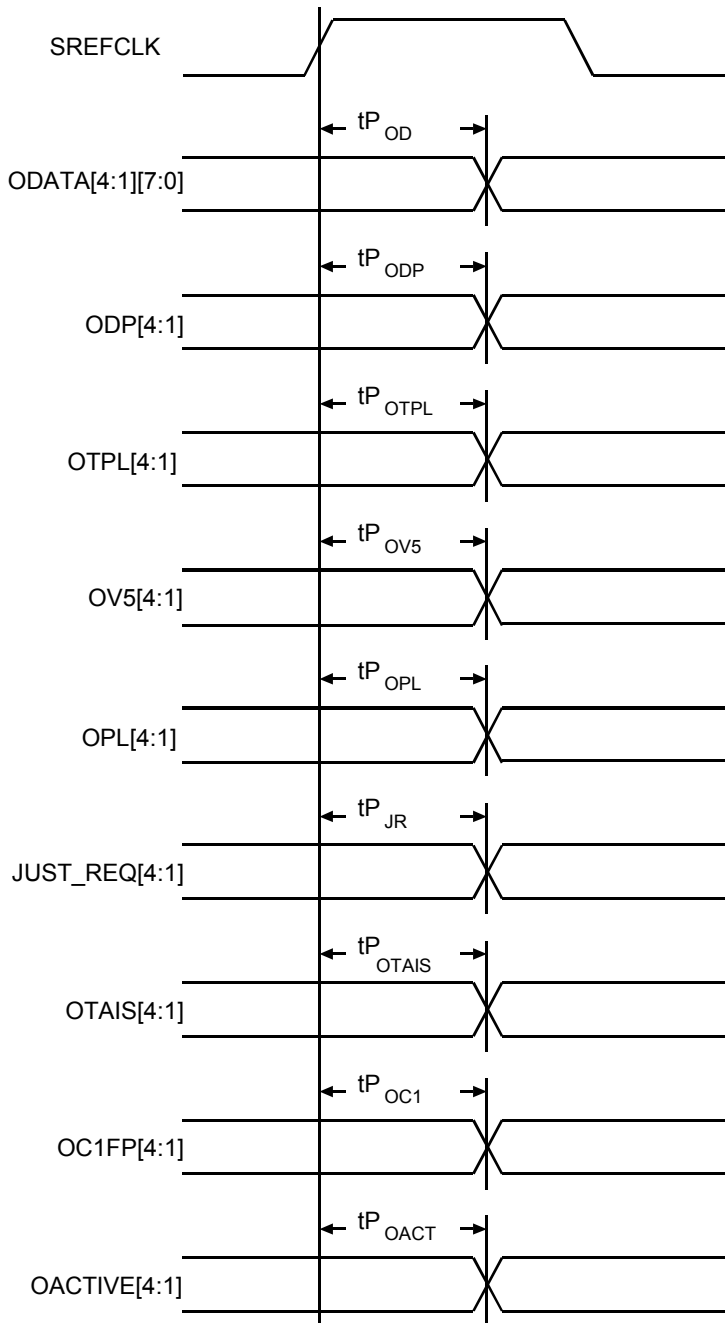
**Table 34 SBS Outgoing Timing with 77.76 MHz SREFCLK (Figure 52)**

Symbol	Description	Min	Max	Units
tPOD	SREFCLK High to ODATA[4:1][7:0] Valid (77.76 MHz SREFCLK)	1	7	ns
tPODP	SREFCLK High to ODP[4:1] Valid (77.76 MHz SREFCLK)	1	7	ns
tPOTPL	SREFCLK High to OTPL[4:1] Valid (77.76 MHz SREFCLK)	1	7	ns
tPOV5	SREFCLK High to OV5[4:1] Valid (77.76 MHz SREFCLK)	1	7	ns
tPOPL	SREFCLK High to OPL[4:1] Valid (77.76 MHz SREFCLK)	1	7	ns
tPJR	SREFCLK High to JUST_REQ[4:1] Valid (77.76 MHz SREFCLK)	1	7	ns
tPOTAIS	SREFCLK High to OTAIS[4:1] Valid (77.76 MHz SREFCLK)	1	7	ns
tPOC1	SREFCLK High to OC1FP[4:1] Valid (77.76 MHz SREFCLK)	1	7	ns
tPOACT	SREFCLK High to OACTIVE[4:1] Valid (77.76 MHz SREFCLK)	1	7	ns

**Table 35 SBS Outgoing Timing with 19.44 MHz SREFCLK (Figure 52)**

Symbol	Description	Min	Max	Units
tPOD	SREFCLK High to ODATA[4:1][7:0] Valid (19.44 MHz SREFCLK)	2	20	ns
tPODP	SREFCLK High to ODP[4:1] Valid (19.44 MHz SREFCLK)	2	20	ns
tPOTPL	SREFCLK High to OTPL[4:1] Valid (19.44 MHz SREFCLK)	2	20	ns
tPOV5	SREFCLK High to OV5[4:1] Valid (19.44 MHz SREFCLK)	2	20	ns
tPOPL	SREFCLK High to OPL[4:1] Valid (19.44 MHz SREFCLK)	2	20	ns
tPJR	SREFCLK High to JUST_REQ[4:1] Valid (19.44 MHz SREFCLK)	2	20	ns
tPOTAIS	SREFCLK High to OTAIS[4:1] Valid (19.44 MHz SREFCLK)	2	20	ns
tPOC1	SREFCLK High to OC1FP[4:1] Valid (19.44 MHz SREFCLK)	2	20	ns
tPOACT	SREFCLK High to OACTIVE[4:1] Valid (19.44 MHz SREFCLK)	2	20	ns

**Figure 52 SBS Outgoing Timing**



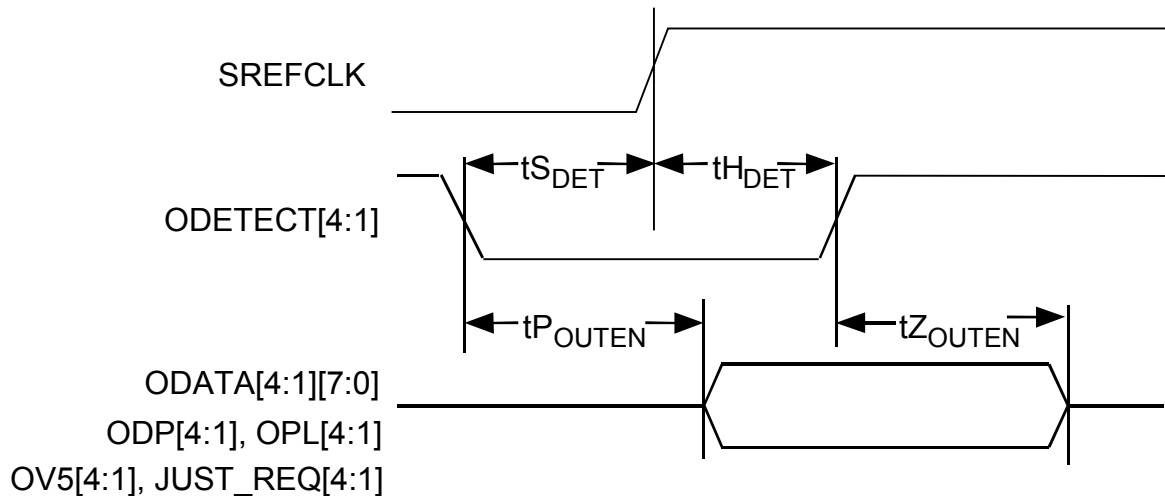
## 18.4 SBS Outgoing Bus Collision Avoidance Timing

**Table 36 SBS Outgoing Bus Collision Avoidance Timing (Figure 53)**

Symbol	Description	Min	Max	Units
$tS_{DET}$	ODETECT[4:1] Set-Up Time	3		ns

Symbol	Description	Min	Max	Units
tHDET	ODETECT[4:1] Hold Time	0		ns
tPOUTEN	ODETECT[4:1] low to all Outgoing Bus Outputs Valid	0	12	ns
tZOUTEN	ODETECT[4:1] high to all Outgoing Bus Outputs Tristate	0	12	ns

**Figure 53 SBS Outgoing Bus Collision Avoidance Timing**

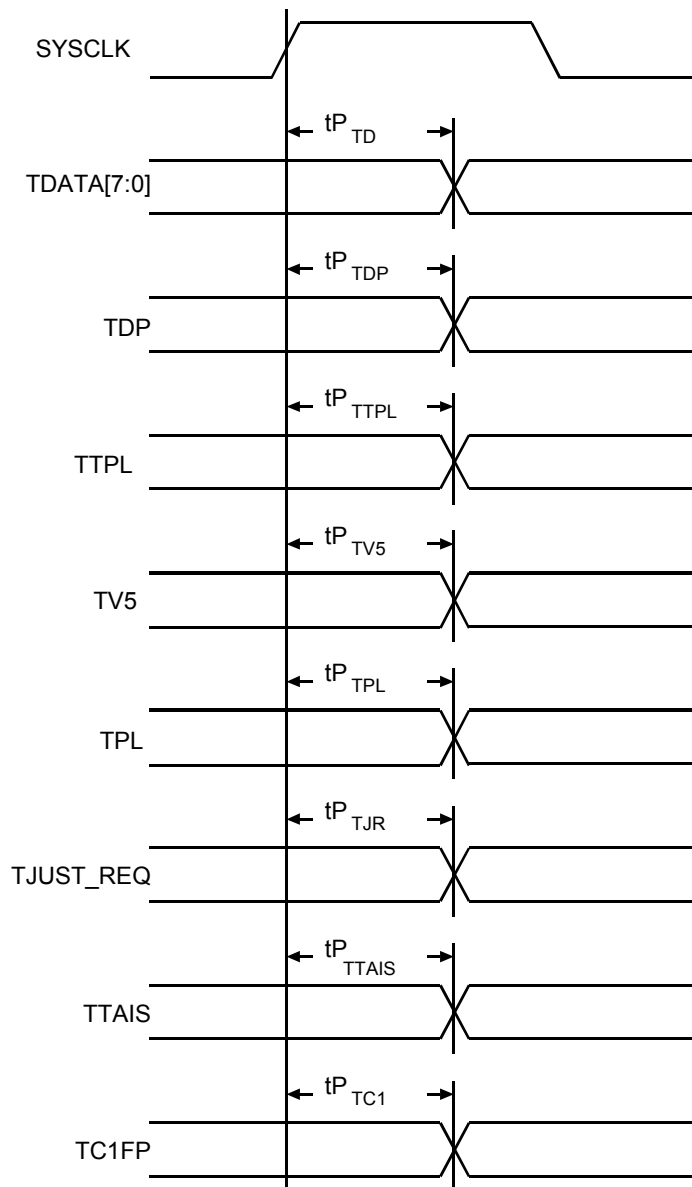


## 18.5 SBS Transmit Bus Timing

**Table 37 SBS Transmit Timing (Figure 54)**

Symbol	Description	Min	Max	Units
tPTD	SYSCLK High to TDATA[7:0] Valid	1	7	ns
tPTDP	SYSCLK High to TDP Valid	1	7	ns
tPTTPL	SYSCLK High to TTPL Valid	1	7	ns
tPTV5	SYSCLK High to TV5 Valid	1	7	ns
tPTPL	SYSCLK High to TPL Valid	1	7	ns
tPTJR	SYSCLK High to TJUST_REQ Valid	1	7	ns
tPTTAIS	SYSCLK High to TTAIS Valid	1	7	ns
tPTC1	SYSCLK High to TC1FP Valid	1	7	ns

**Figure 54 SBS Transmit Timing**



**Notes on Output Timing**

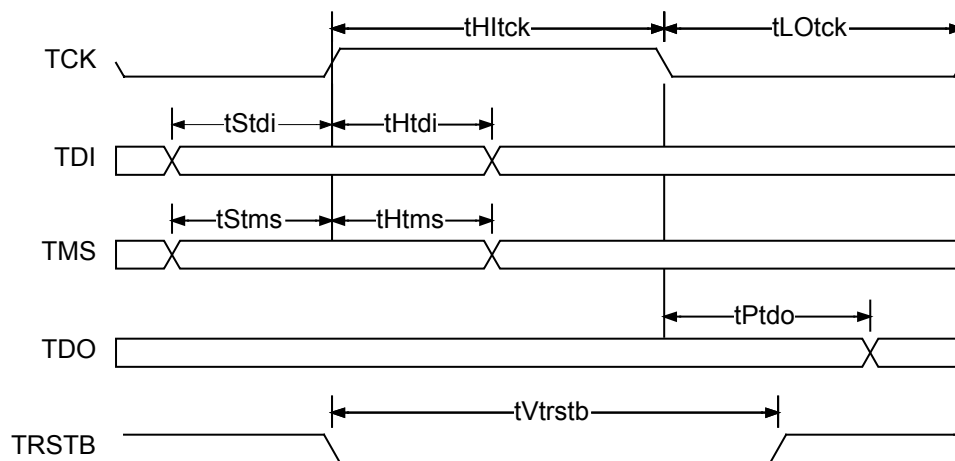
1. Output propagation delay time is the time in nanoseconds from the 1.4 V point of the reference signal to the 1.4 V point of the output.
2. Output propagation delays are measured with a 50 pF load on the outputs operating at 77.76 MHz except where indicated.
3. Output propagation delays are measured with a 100 pF load on the outputs operating at 19.44 MHz except where indicated.

## 18.6 JTAG Port Interface

**Table 38 JTAG Port Interface (Figure 55)**

Symbol	Description	Min	Max	Units
FTCK	TCK Frequency		4	MHz
THITCK	TCK HI Pulse Width	100		ns
THITCK	TCK LO Pulse Width	100		ns
TSTMS	TMS Set-up time to TCK	25		ns
THTMS	TMS Hold time to TCK	25		ns
TSTDI	TDI Set-up time to TCK	25		ns
THTDI	TDI Hold time to TCK	25		ns
TPTDO	TCK Low to TDO Valid	2	35	ns
TVTRSTB	TRSTB Pulse Width	100		ns

**Figure 55 JTAG Port Interface Timing**



## 19 Ordering and Thermal Information

### 19.1 Packaging Information

Part No.	Description
PM8610-BIAP	352-pin Ball Grid Array (UBGA)

### 19.2 Thermal Information

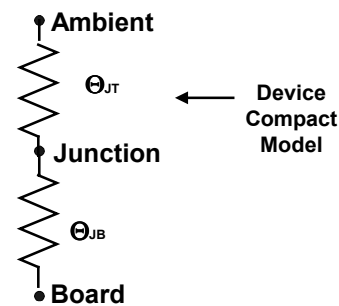
The SBS is designed to operate over a wide temperature range and is suited for industrial applications such as outside plant equipment.

Maximum long-term operating junction temperature to ensure adequate long-term life.	105 °C
Maximum junction temperature for short-term excursions with guaranteed continued functional performance. <sup>1</sup> This condition will typically be reached when local ambient reaches 85 °C.	125 °C
Minimum ambient temperature	-40 °C

Thermal Resistance vs Air Flow <sup>2</sup>			
Airflow	Natural Convection	200 LFM	400 LFM
$\Theta_{JA}$ (°C/W)	16.7	11.45	10.14

Device Compact Model <sup>3</sup>	
$\Theta_{JT}$ (°C/W)	0.3
$\Theta_{JB}$ (°C/W)	7.08

Operating power is dissipated in package (watts) at worst case power supply	
Power (watts)	1.44 <sup>4</sup>



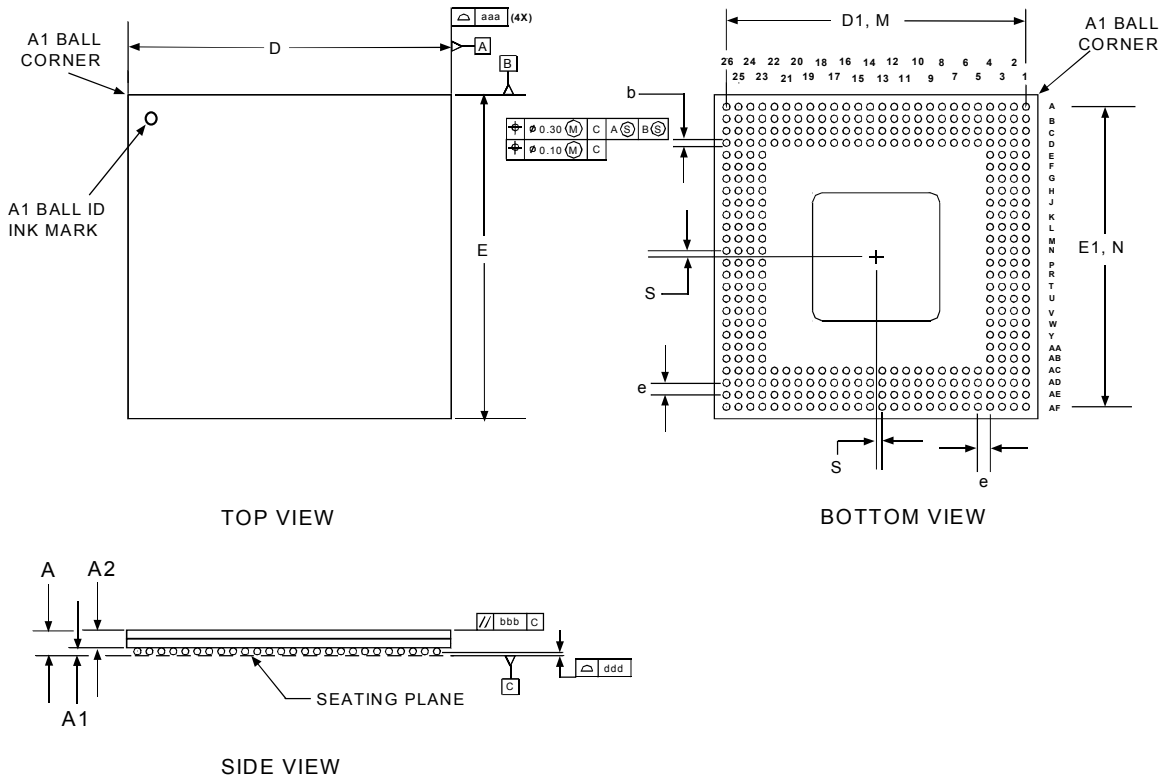
#### Notes

- Short-term is understood as the definition stated in Telcordia Generic Requirements GR-63-Core.
- $\Theta_{JA}$ , the total junction to ambient thermal resistance as measured according to JEDEC Standard JESD51 (2S2P)
- $\Theta_{JB}$ , the junction-to-board thermal resistance and  $\Theta_{JT}$ , the residual junction to ambient thermal resistance are obtained by simulating conditions described in JEDEC Standard, JESD 15-8.
- At 1.44 W in the 352 UBGA package, the SBS will not need any airflow in a dense board application.



## 20 Mechanical Information

Figure 56 352 Pin UBGA 27 mm x 27 mm Body



- NOTES: 1) ALL DIMENSIONS IN MILLIMETER.  
 2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.  
 3) DIMENSION bbb DENOTES PARALLEL.  
 4) DIMENSION ddd DENOTES COPLANARITY.

PACKAGE TYPE : 352 THERMALLY ENHANCED BALL GRID ARRAY - UBGA															
BODY SIZE : 27 x 27 x 1.41 MM															
Dim.	A	A1	A2	D	D1	E	E1	M,N	b	d	e	aaa	bbb	ddd	S
Min.	1.26	0.40	0.86	26.90	-	26.90	-	-	0.50	-	-	-	-	-	0.45
Nom.	1.41	0.50	0.91	27.00	25.00	27.00	25.00	26x26	0.63	-	1.00	-	-	-	0.56
Max.	1.56	0.60	0.96	27.10	-	27.10	-	-	0.70	0.20	-	0.20	0.25	0.20	0.55

## Notes