EPSON

SLA50000H Series

High Density Gate Array

- Ultra-high-speed, high density and low power consumption
- Low voltage operation: 3.3V and 2.0V
- Number of raw gates: 28,710 to 815,468 gates

■ DESCRIPTION

The SLA50000H Series are high-speed, high-density and powerful drive gate arrays using SOG type CMOS 0.35μm processes. For this Series, we have prepared a product line up of gate arrays ranging from 28,710 through 815,468 of raw gates for immediate applications to large-scale and high-speed systems.
To conform to many application fields with low voltage operation, these gate arrays are compatibly usable for 3V systems and 2V systems. Furthermore, we have prepared low noise output cells of "μA" orders for wide range of applications including miniature portable equipment.

■ FEATURES

- Super-high density (adopting 0.35μm silicon gate CMOS with 2-, 3- and 4-metal layers)
- High-speed operation (operation delay of internal gate = 0.140ns at 3.3V, 2-input power NAND standard)
- Internal gate = 3.3 and 2.0V, I/O buffer = 5.0, 3.3 and 2.0V (built-in level shifter)
- Low power consumption (0.70μW/MHz/BC when internal cell = 3.3V)
- Output drivability (I_{OL} = 0.1, 1, 3, 8, 12, 24mA when PCI = 5.0V, I_{OL} = 0.1, 1, 2, 6, 12mA when PCI = 3.3V, I_{OL} = 0.05, 0.3, 0.6, 2, 4mA when 2.0V)
- RAM, PLL*, IrDA* and various function cells available
- Low noise output cell, PCI I/F, USB I/F*, Fail-Safe output, JTAG

■ PRODUCT LINEUP

Master / Features		SLA5028H	SLA5075H	SLA5099	SLA5125H	SLA5177H	SLA5250H	SLA5335H	SLA5442H	SLA5506H	SLA5668H	SLA5815H
	3-layer Metal	SLA502TH	SLA507TH	SLA509T	SLA512TH	SLA517TH	SLA525TH	SLA533TH	SLA544TH	SLA550TH	SLA566TH	SLA581TH
	4-layer Metal	SLA502QH	SLA507QH	SLA509Q	SLA512QH	SLA517QH	SLA525QH	SLA533QH	SLA544QH	SLA550QH	SLA566QH	SLA581QH
Total BCs (Raw Gates)		28,710	75,774	99,198	125,772	177,062	250,160	335,858	442,112	506,688	668,552	815,468
Usable BCs	2-layer Metal	14,355	35,613	46,623	56,597	79,677	112,572	144,418	176,844	202,675	267,420	326,187
	3-layer Metal	25,264	64,407	84,318	100,617	132,796	187,620	251,893	309,478	354,681	467,986	570,827
	4-layer Metal	27,274	71,985	94,238	119,483	168,208	237,652	319,065	397,900	456,019	601,696	733,921
Number of PADs (In Case of Micro Pitch)*		88 (104)	144 (168)	168 (192)	188 (216)	224 (256)	264 (304)	308 (352)	352 (404)	376 (432)	432 (496)	480 (548)
Propagation Delay	Internal Gates	t_{pd} = 0.140ns (standard at 3.3V), 0.21ns (standard at 2.0V)										
	Input Buffers	t_{pd} = 0.38ns (standard at 5.0V) level shifter, 0.4ns (standard at 3.3V), 1.3ns (standard at 2.0V)										
	Output Buffers	t_{pd} = 2.12ns (standard at 5.0V) level shifter, 2.02ns (standard at 3.3V), 3.9ns (standard at 2.0V), CL = 15pF										
I/O Level		CMOS, LVTTL, PCI, USB*										
Input Mode		LVTTL, CMOS, Pull-up/Pull-down, Schmitt, 2.0/3.3V Level interface (Level shifter)										
Output Mode		Normal, Open drain, 3-state, Bi-directional, 2.0/3.3V Level interface (Level shifter)										

*Under development