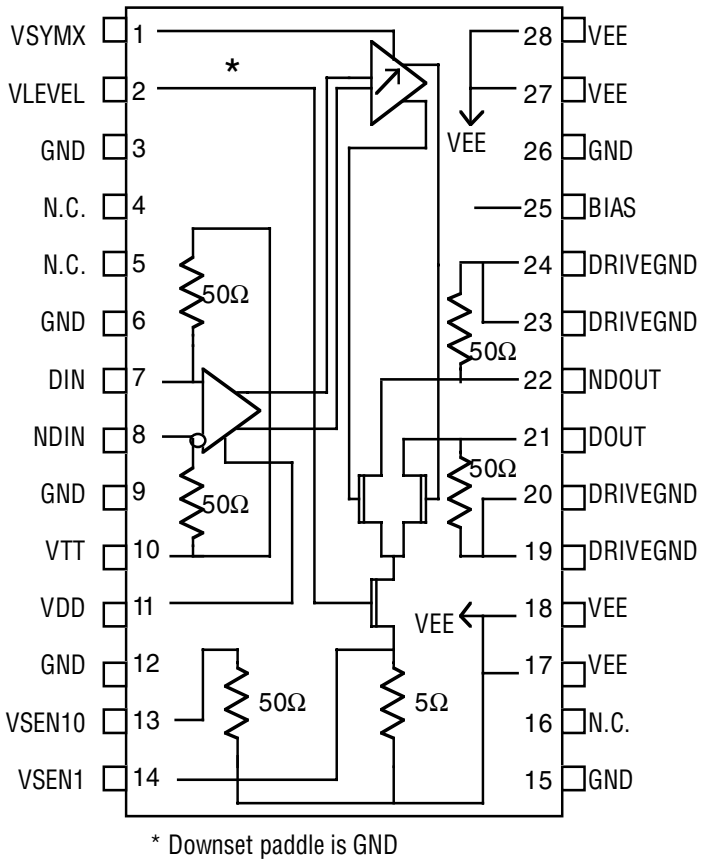


* Downset paddle is GND

TQ8318/19

PRELIMINARY DATA SHEET

OC192/STM64 E/O Driver

Features

- *High performance fully back-terminated 20mA/1V to 60mA/ 3V modulation output driver (TQ8318)*
- *Also available without back-terminations for 25 ohm, 40 mA to 120mA applications (TQ8319)*
- *Output can drive direct coupled Electro-Absorptive Modulator (EAM/EML), or AC coupled differential Mach-Zehnder modulator or Direct Modulated Laser (DML)*
- *NRZ data rates to 10.8Gbs*
- *Output symmetry adjust*
- *0 to 1.0V output offset control*
- *32ps max output risetime*
- *+3.3V CML direct coupled input can be AC coupled for eLVDS and LVPECL inputs*
- *28 pin TSSOP small outline package or die*
- *0°C to +110°C case operating temperature range*

Applications

- *DML with drive to 120mA*
- *Single-ended 50 ohm 1.0-3.0V EAM/EML driver (DC coupled with integral 0 to -1V offset)*
- *6V differential 50 ohm Mach-Zehnder driver (AC coupled)*

The TQ8318/TQ8319 is a low jitter, high performance electro-optic driver intended for directly interfacing CML outputs from a multiplexer or clock recovery device to various EO devices, including cooled and uncooled DFB and FP lasers, high power VCSEL arrays, EA modulators and differential Mach-Zehnder (MZ) modulators. The TQ8318 and the TriQuint TGA1328/8652 can be used in combination for single ended 9V MZ drive applications. The TQ8318/19's symmetry and level controls, low additive jitter, and excellent rise/fall times while driving significant loads allow the highest system level performance at low cost. The devices also include an offset control to allow adjustment of DC bias between 0V and -1V for EAM/EML, or 0-40mA for laser threshold, applications. The 28 pin TSSOP footprint and low jitter makes the devices particularly suitable for high port count WDM circuit packs and modules, and for optical modules. These devices are compatible with CMOS, SiGe or GaAs muxes with CML, eLVDS, or LVPECL outputs.

10.8Gb/s Output Driver

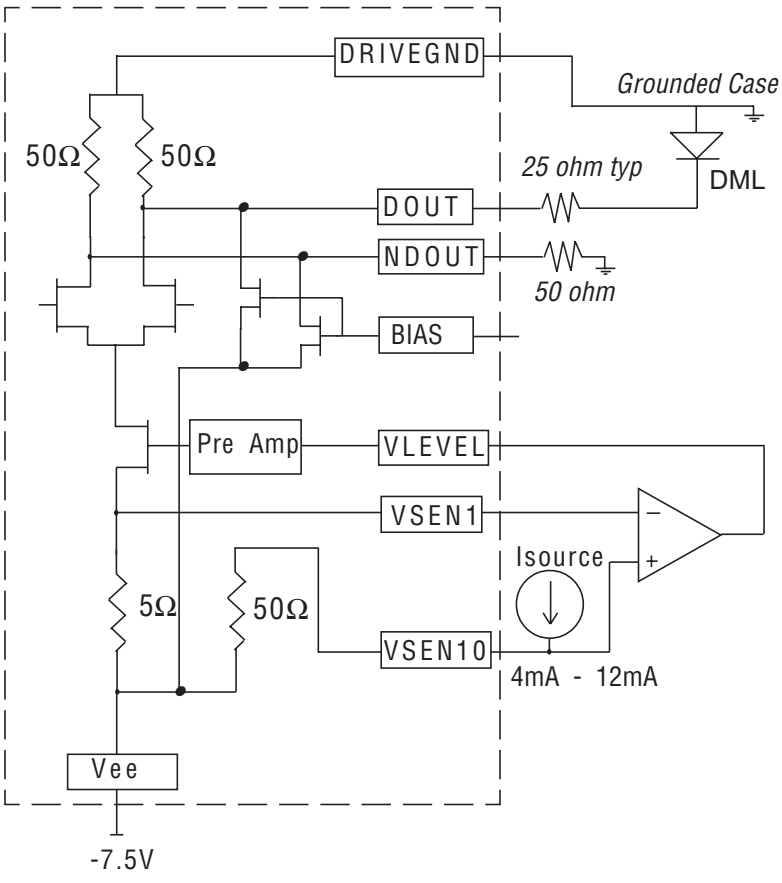
These devices are extremely well suited to driving a variety of Electro-optical devices that utilize a grounded case. A +3.3V/-5V family of devices is available for applications where the driven device does not utilize a grounded case or where these drivers are used in die form.

The TQ8318's 50 ohm back-terminated high power cascoded output stage drives between 1.0V and 3.0V of modulation into a single ended 50 ohm external load (6.0V peak-peak in differential mode), or between 20mA and 60mA for DML applications. A variant without the back-terminations, the TQ8319, may be used in 25 ohm external load applications to modulate up to 120 mA. The separate power supply pins for the output stage are DRIVEGND = 0V and VEE = -7.5V. Note that outputs may be driven as differential or single ended signals at DOUT and NDOUT and that a CML drive level is possible by adjusting the output level control to an appropriate level. Unused output complements must be tied as 50 ohm (TQ8318, 25 ohm for TQ8319) to GND when direct coupling is used.

The data amplitude may be adjusted using VLEVEL and the crossing level of the output data eye can be adjusted using VSYMX. Both of these levels are preset internally if VLEVEL and VSYMX are left open (N.C.). The DC offset, on DOUT and NDOUT may be biased to a DC level with a voltage control on BIAS from 0V/0mA to -1.0V/40mA (25 ohms).

The output current level and voltage amplitude at DOUT and NDOUT may be set using an external feedback control loop. To set the output current level, connect an external current source, Isource, equal to 20% of the desired output, to VSEN10. Connect VLEVEL, VSEN10 and VSEN1 to an amplifier, as shown in Figure 1, with a minimum input common mode range of (Isource*50 ohm) above VEE. The choice of the external current source also sets the output voltage swing. For example, to achieve the maximum swing of 3.0V into 25 ohm (50 ohm internal back-terminated impedance in parallel with a 50 ohm forward load), a 12mA source must be used (Isource*10*25 ohm =120mA*25 ohm = 3.0V). Note that feedback with a back facet monitor or PiN diode provides a more ideal method to control optical output power and extinction ratio, if available. Figure 1 depicts a DML application, though similar considerations can be made for either EAM/EML or differential MZM applications.

Figure1. Level Control Circuit



TriQuint SEMICONDUCTOR

Table 1. TQ8318/19 Pin Descriptions

Signal	***Type***	***Pin Number***	***Description***
DIN	CML Input	7	Serial data input. Internally terminated by 50 Ohms to VTT
NDIN	CML Input	8	Complement of DIN. Internally terminated by 50 Ohms to VTT
DOUT	High Drive Output	21	High power differential driver modulated output.
NDOUT	High Drive Output	22	Complement of DOUT. If unused must be terminated in the same manner as DOUT.
VSYMX	Analog Input	1	Rise/fall time symmetry adjust control signal input. Input impedance is typically 10k Ohm.
VLEVEL	Analog Input	2	Output data amplitude adjust control signal input. Input impedance is typically 10k Ohm.
VSEN10	Analog I/O	13	Output current level reference pin. When driven with an external current source at exactly 1/5 the output current of the TQ8318 (1/10 for the TQ8319) level, the voltage at Vsen10 is equal to that at Vsen1. Can be used to implement a control loop.
VSEN1	Analog Output	14	Output current level sensing pin. Vsen1 voltage is directly proportional to the output current level. Connects internally to 5 Ohm resistor in differential driver current tail.
BIAS	Analog Input	25	Output offset control input
Power Pins			
Signal	***Description***		***Pin Number***
VTT	Input Termination Supply		10
VDD	Pre-drive and I/O VDD Supply		11
GND	Ground Supply		3, 6, 9, 12, 26, 15, Package Down Paddle (required)
VEE	Output Stage Neg. Supply (-7.5V)		28, 27, 18, 17
DRIVEGND	Output Stage Pos. Supply (0V)		24, 23, 20, 19 (Note: These pins are unused in the TQ8319)
NC	Do Not Connect		4, 5, 16

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply voltage	VDD	GND-0.5	4.0	V
Output stage supply return	VEE	-8	GND+0.5	V
CML inputs		GND-0.5	VDD+0.5	V
Control signals		VEE-0.5	GND+0.5	V
Tstg, Storage Temperature		-55	150	°C
Tc, Maximum Case Operating Temperature			110	°C
Tj, Maximum junction temperature			150	°C
Electrostatic Discharge (100pF, 1.5kΩ)			1000	V

Notes: 1. All voltages with respect to GND.

Table 3. Operating Ranges

Signal	Symbol	Parameter	Min	Typ	Max	Units
VDD	VDD	Supply voltage range	3.14	3.3	3.47	V
IDD		Supply current (Note 2)		55		mA
VTT	VTT	Input termination supply voltage range		VDD		V
VEE	VEE	Negative driver supply	-7.13	-7.5	-7.87	V
IEE		Supply current (Notes 3 and 5)		260		mA
DRIVEGND	V_{drive}	Output stage power supply		0		V
	I_{drive}	TQ8318 supply current for output stage (50 ohm load)	20		60	mA
	I_{drive}	TQ8319 supply current for output stage (25 ohm load)	40		120	mA
	T_c	Case temperature measured at the case paddle	0		110	°C
	P_{diss}	Power dissipation (Note 4)		2.45	3.37	W
	P_{diss}	Power dissipation (Note 5)		2.13	2.67	W

Notes: 1. Room Temperature condition
2. VDD at operating range.
3. VDD , VEE , and VTT at operating range.
4. Idrive into specified load and max modulation and 1V offset.
5. Idrive into specified load and max modulation and 0V offset.

Table 4. DC Characteristics—Differential CML Input

Symbol	Parameter	Min	Nom	Max	Unit
V_{ICOM}	Input common mode voltage range	VDD-0.4	—	VDD-0.150	V
V_{IDIFF}	Input differential voltage, per side, pk-pk	300	—	800	mV
R_{IN}	Input termination resistance		50		ohm
C_{IN}	Input capacitance	—	—	TBD	pF
V_{ESD}	ESD breakdown rating	1000	—	—	V

Notes 1. For +3.3V CML operation inputs may be Direct Coupled. To interface LVPECL or to eLVDS, AC coupling is recommended. An internal bias voltage is generated on-chip so VTT may be left open.

Table 5. Control Signal Specifications

Signal	Symbol	Parameter	Min	Typ	Max	Units
VSYMX	V_{def}	Default input level		0.73•VEE		V
	V_{symx}	VSYMX nominal operating range	V_{def}-0.18		V_{def}+0.18	V
	Z_{symx}	VSYMX input impedance		10		k ohm
VLEVEL	V_{def}	Default input level		0.83•VEE		V
	V_{level}	VLEVEL nominal operating range	VEE+0.8		VEE+2.1	V
	A_{amp}	Output data amplitude adjust gain		1.54		V/V
	Z_{level}	VLEVEL input impedance		10		k ohm
VSEN1	V_{sen1}	Output current sensing voltage level for TQ8318		VEE+(2.5•I_{drive})		V
		Output current sensing voltage level for TQ8319		VEE+(5•I_{drive})		V
	Z_{sen1}	VSEN1 equivalent resistance		5		ohm
VSEN10	V_{sen10}	Control current input voltage level		VEE+(50•I_{drive})/5		V
	Z_{sen10}	VSEN10 equivalent resistance		50		ohm
	I_{sen10}	VSEN10 input current range	4		12	mA
	V_{senrat}	VSEN10 to VSEN1 Ratio	9.9	10	10.1	%
BIAS		Nominal output offset control range	VEE		VEE+1.65	V
	V_{def}	Default input level		VEE		V

Notes: 1. Refer to Figure 2. All specifications for output data apply under the following conditions:
Output Data Pattern: 2^{23}-1 PRBS, 9.95328Gbit/s
DOUT and NDOUT termination: Direct Coupled external load is a 50 ohm termination to GND for the TQ8318;
Direct Coupled external load is a 25 ohm termination to GND for the TQ8319

Table 6. 10.8 Gb/s High Speed Output Signal Specifications

Signal	Symbol	Description	Min	Typ	Max	Units
DOUT	Tpw	Output data pulse width	95	100	105	%
NDOUT	Trise	Output data rise time	16	25	32	ps
(Note 2)	Tfall	Output data fall time	16	25	32	ps
	Jpp	Output data peak-peak jitter (Note 3)		3	5	ps
	V_{mean_max}	Output data mean pk-pk for high output applications; Vlevel =(VEE+2.1)V, Vdrive = 0 V, VEE= -7.5V	3.0			V
	V_{mean_min}	Output data mean pk-pk for low output applications; Vlevel = (VEE+0.8)V, Vdrive = 0 V, VEE= -7.5V			1.0	V
	X_{ingmin}	Min. data crossing lvl. adjustment range with VSYMX	20	-	40	%
	X_{ingmax}	Max. data crossing lvl adjustment range with VSYMX	60	-	80	%
	DXing	Absolute variation in output data crossing level over full VLEVEL operating range	-5	-	+5	%
	%over	Overshoot	-	-	10	%
	%under	Undershoot	-	-	10	%
	%ripple	Ripple	-	-	10	%
	RATE	NRZ data rate (Note 5)	TBD		10800	Mbs
	V_{offset}	Offset voltage referred to DRIVEGND (Note 6)	-1.0		TBD	V
	T_{skew}	DOUT to NDOUT magnitude measured at common mode			6	ps

Notes: 1. Refer to Figure 2. All specifications for output data apply under the following conditions:

Output Data Pattern:	*2^{23}-1 PRBS, 9.95328Gbit/s*
DOUT and NDOUT termination:	*Direct Coupled external load is a 50 ohm termination to GND for the TQ8318; Direct Coupled external load is a 25 ohm termination to GND for the TQ8319*
Termination network return loss:	*>20 dB, 0 to 4 GHz*
(TQ8318 only)	*>15 dB, 4 to 12 GHz*
	>6 dB, 12 to 20 GHz
Vlevel:	*over specified operating range*
VSYMX:	*adjusted to give 50% data crossing*

2. This specification applies to the Vmean measurement shown in Figure 2. Vlevel must be adjusted to the specified level and VSYMX must be adjusted for optimum eye crossing level before making data eye measurements. Maximum rise and fall times are measured with a 35ps input rise and fall time.

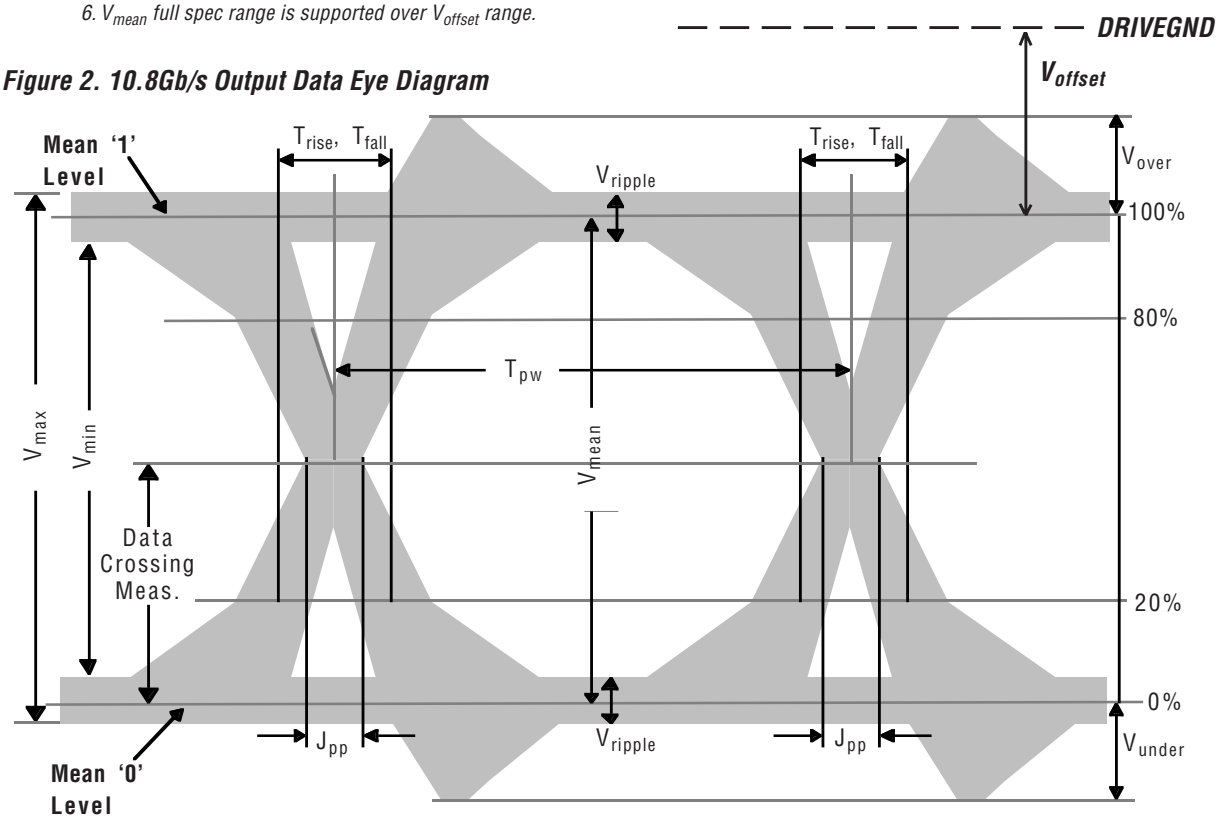
3. Measured at 2^{23}-1 PRBS, 9.95328 Gbit/s, eye crossings

4. Peak to Peak jitter is defined as the difference between the measured jitter on the device and the test system jitter. Jitter is unfiltered broadband measurement.

5. Device will function down to DC however some specs in Table 6 may not be met.

6. V_{mean} full spec range is supported over V_{offset} range.

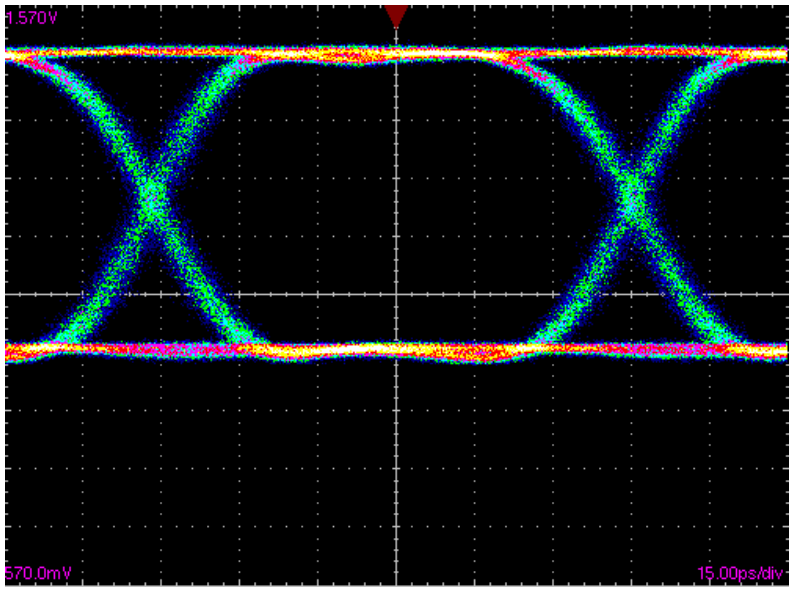
Figure 2. 10.8Gb/s Output Data Eye Diagram



T_{pw} =	half of input waveform period	V_{max} =	maximum peak-to-peak voltage
V_{min} =	minimum peak-to-peak voltage (eye interior)	V_{mean} =	Mean peak-to-peak voltage (mean eye opening)
T_{rise} =	20% to 80% rise time, mean '0' to mean '1'	T_{fall} =	20% to 80% fall time, mean '0' to mean '1'
$\%_{over}$ =	Vover/Vmean X 100%	$\%_{under}$ =	Vunder/Vmean X 100%
$\%_{ripple}$ =	Vripple/Vmean X 100%	J_{pp} =	peak-to-peak data crossing jitter

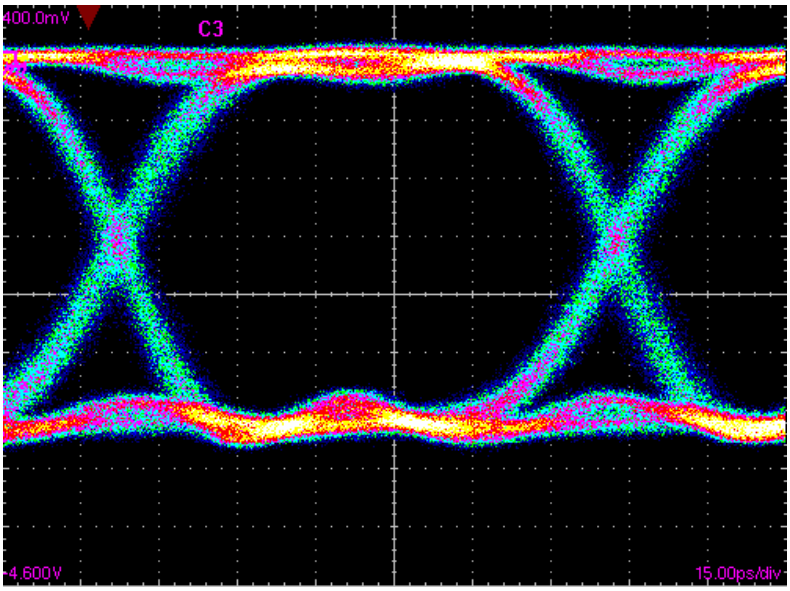
Note: mimimum display persistence of 2s is assumed for the above measurements.

Figure 3. Tek TDS8000 Oscilloscope to cables to 12.5 Gbs HP BERT running at 10.7 Gb/s



Vert: 100mV/div Horiz: 15pS/div Rise: 18.30pS Fall: 20.40pS Jitter: 10.20pS p-p

Figure 4. TQ8318 (in TSSOP) Tested with Instruments and Cables from Figure 3



Vert: 500 mV/div Horiz: 15 pS/div Rise: 22.80 pS Fall: 18.60 pS Jitter: 14.10 pS p-p

Figure 5. Typical output at 12.5 Gb/s for TQ8318 TSSOP

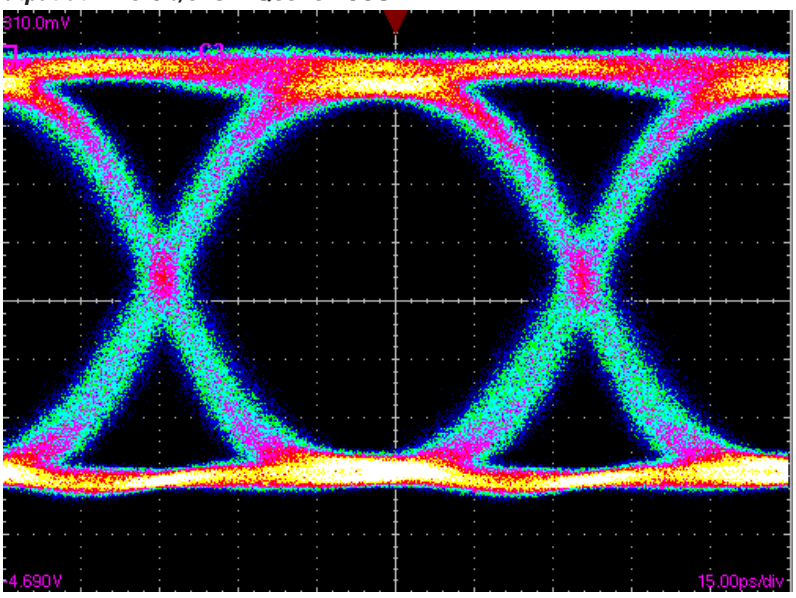
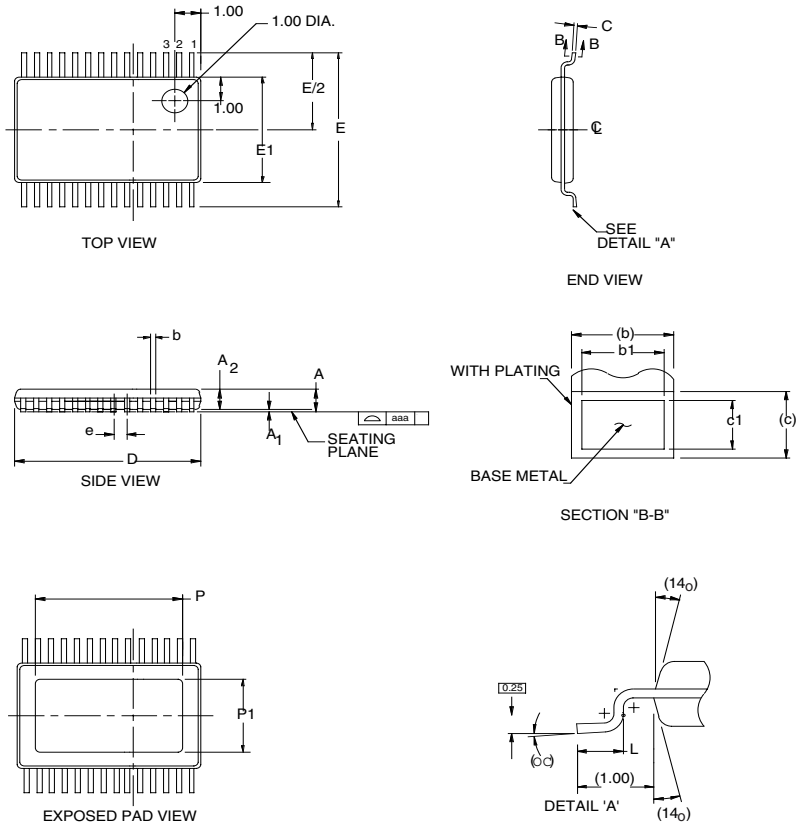


Figure 6. TSSOP-28 Downpaddle Package Mechanical drawing

	MIN	NOM	MAX
A			1.1262
A1	.0254		.1500
A2	.8500		1.0500
b	.1900		.3000
b1	.1900		.2500
c	.0900		.2000
c1	.0900		.1600
D	9.6000		9.8000
E1	4.3000	4.4000	4.5000
e	.6500	.6500	.6500
E		6.4000	
L	.5000	.6000	.7000
N		28	
P		5.0000	
P1	3.0000		3.0100

Note: All dimensions in millimeters (mm).



TriQuint SEMICONDUCTOR

Approximate Actual Size of Package Footprint

Ordering Information

TQ8318	*10.7 Gb/s Backterminated EO Driver +3.3/-7.5V TSSOP Package*
TQ8319	*10.7 Gb/s Unterminated EO Driver +3.3/-7.5V TSSOP Package*
TQ8318-DD	*DC Tested TQ8318 Die*
TQ8318-DA	*AC Tested TQ8318 Die*
TQ8319-DD	*DC Tested TQ8319 Die*
TQ8319-DA	*AC Tested TQ8319 Die*

Related Components:

TQ8317	*10.7 Gb/s Backterminated EO Driver +3.3/-5V TSSOP Package*
TQ8320	*10.7 Gb/s Unterminated EO Driver +3.3/-5V TSSOP Package*
TGA1328	*Single ended 9V driver - die form*
TGA8652	*Single ended 9V driver - packaged form*

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel: (503) 615-9000 (Oregon, USA)**
Email: sales@tqs.com **Fax: (503) 615-8900 (Oregon, USA)**

For technical questions and additional information on specific applications:

Email: applications@tqs.com

Revision 0.0.A August 2001

Known Device Issues as of August 1, 2001

1. There is a 20GHz oscillation that is “bias space” related. The oscillation is a free-running sine wave at approximately 20GHz. No oscillations have been observed if Vbias is left at default (Vbias = Vee). The oscillations have been observed to occur when Voffset is between -0.5V and -1.0V *and* VOUTpp is less than 2.5V.

2. Vbias does not conform to the operation range shown in Table 1 “Absolute Maximum Ratings”. The Bias pin is directly connected to the gate of the FET in the bias current generator. As such, voltages in excess of Vee+2.5V may cause damage to the bias generator. Placing a 2.5k ohm resistor in series with the Vbias pin will prevent damage to the part.

3. The average measured full output voltage offset is -950mV.