GRAPHICS

LCD & CRT Display Controller

V6355D-H LCDC

■ OUTLINE

V6355D (LCDC) is a silicon gate CMOS device. This controller can be connected to both LCD and CRT displays. It is software compatible with IBM-PC and has a function to expand it.

■ FEATURES

- Capable of controlling both LCD and CRT displays.
- Includes 6845 restricted mode and CRT peripheral circuits for IBM-PC.
- Both SRAM and DRAM are usable as VRAM.
- Includes MOUSE and LIGHT PEN interface.
- Cursor position can be specified by any 16 × 16 dot patterns in the bit unit (AND and EXOR screens).
- Includes color palette (16/512 colors).
- LCD intensity controllable (16 or 8 gradation steps)
- Screen modes are available in combinations of the following.
  Horizontal dot number: 640, 320, 512, 256
  Vertical dot number: 192, 200, 204, 64 (64 only with LCD)
  Raster adjustment: 0, 2, 4 or 6 specifiable
- Capable of displaying 16 colors in 640 × 204 by using external circuits.
- CRT monitor selectable from among IBM Color, Monochrome, NTSC system and PAL system.
- Can be interfaced with 3 types of LCD driver.
- Usable with 16 bit bus CPU.
- CMOS 100-pin QFP

■ ELECTRICAL CHARACTERISTICS

① **Absolute Maximum Ratings**

Item	Symbol	Min.	Max.	Unit
Supply voltage	V_{DD}	−0.5	+7.0	V
Input voltage	V_I	−0.5	V_{DD}+0.5	V
Output voltage	V_O	−0.5	V_{DD}+0.5	V
Operating temperature	T_{OP}	0	+70	°C
Storage temperature	T_{STG}	−50	+125	°C

(Vss, AVss=0.0V as standard)

② **Recommended Operating Conditions**

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating temperature	T_{OP}	0	25	70	°C

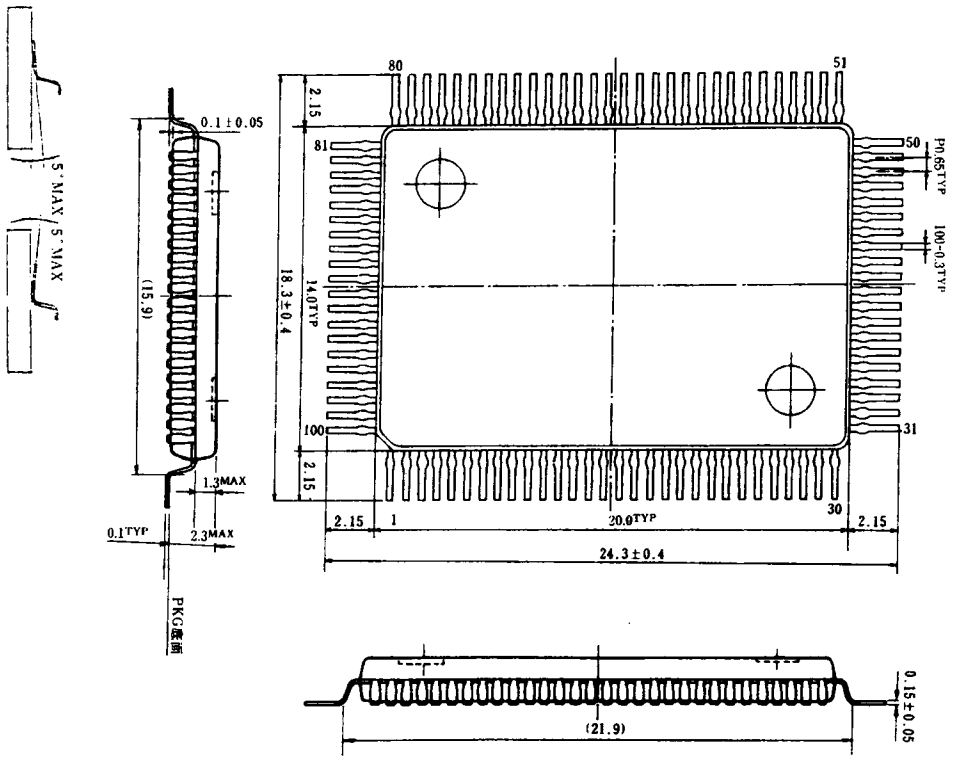
Used with V_{DD} and AV_{DD} at the same voltage and Vss, AVss=0.0V.

③ **DC Characteristic**

Item	Symbol	Conditions	Min.	Max.	Unit
High-level output voltage (TTL)	V_{OH}	I_{OH}= −0.4mA	2.7		V
Low-level output voltage (TTL)	V_{OL}	I_{OL}=0.8mA		0.4	V
High-level output voltage (CMOS)	V_{OH}	I_{OH} <1μA	V_{DD}−0.4		V
Low-level output voltage (CMOS)	V_{OL}	I_{OL} <1μA		0.4	V
High-level input voltage	V_{IH}		2.2		V
Low-level input voltage	V_{IL}			0.8	V
High-level output current	I_{OH}	V_{OH}=2.7V	−0.4		mA
Low-level output current	I_{OL}	V_{OL}=0.4V	0.8		mA
Input leak current	I_L		−10	10	μA
Output leak current (tri-state)	I_{LZ}		−10	10	μA
Supply current (at normal operation)	I_{DD}	R_L=5.6KΩ		70	mA
Supply current (at standby)	I_{DD}	R_L=5.6KΩ		50	mA
High-level clock input voltage	V_{CH}		3.6		V
Low-level clock input voltage	V_{CL}			0.6	V

- V_{DD}, AV_{DD}=5.0V ± 5%, T_{OP}=0 ~ 70°C
  Supply voltage is obtained by adding mean current at V_{DD} and AV_{DD} terminals.
- R_L: Terminal resistance between Y, R, G, B, CH terminals and GND.
  Output leak current (tri-state) is for when $CD_{0\sim7}$, $RD_{0\sim7}$ and $RA_2/GD_3 \sim RA_0/GD_1$ are in the input mode and when $AD_0 \sim AD_{12}/\overline{CAS}$, $\overline{LSEL}$, $\overline{HSEL}$ and MEMRDY are in the high impedance mode.

■ OUTLINE DIMENSIONS



■ BLOCK DIAGRAM