Pin Diagram

This section provides the pin assignment, signal description, block diagram, and pin descriptions for the VG-468 PC Card Socket Controller.

*Pin Diagram
Figure 1-1*

DEFAULT PIN ASSIGNMENT

Top pins: PWRGOOD, *SIOW, *SIOR, BALE, AEN, SA16, SA15, SA14, SA13, SA12, SA11, SA10, SA9, SA8, SA7, SA6, SA5, VCC, SA4, RESETDRV, GND, CLK, SA3, SA2, SA1, SA0, *SBHE, LA23, LA22, LA21, LA20, LA19, LA18, LA17, *MEMR, *MEMW, SD7, SD6, SD5, GND, SD4, SD3, VCC, SD2, SD1, SD0, SD9, SD10, SD11, SD12, SD13

Left pins (top to bottom): A_REG, A_D3, A_*CD1, A_D4, A_D11, A_D5, A_D6, A_D12, A_D13, A_D7, A_*CE1, A_D14, A_D15, GND, A_CA10, A_*OE, VCC, A_*CE2, A_CA11, A*IORD, A_CA9, A_*IOWR, A_CA8, A_CA17, A_CA13, A_CA18, GND, A_CA14, A_CA19, A*WE, A_CA20, A_RDY, A_CA21, A_CA16, A_CA22, A_CA15, A_CA23, A_CA12, A_CA24, A_CA7, A_CA25, GND, A_CA6, A_CA5, A_RESET, A_CA4, A*WAIT, A_CA3, A_*INPACK, A_CA2, A_CA1, A_BVD2

Right pins (top to bottom): SD14, SD15, GND, *SPKROUT, *INTR, *RIO, IOCHRDY, *MEMCS16, *IOCS16, *ZWS, IRO9, IRO7, IRO5, IRO4, IRO3, VCC, IRO10, IRO11, IRO12, IRO14, IRO15, GND, B_*CD2, B_D10, B_WP, GND, B_D2, B_D9, B_D1, B_D8, B_D0, B_BVD1, B_CA0, B_BVD2, B_CA1, B_CA2, B_*INPACK, B_CA3, B_*WAIT, B_CA4, B_RESET, B_CA5, B_CA6, B_CA25, B_CA7, B_CA24, B_CA12, B_CA23, VCC, B_CA15, B_CA22, B_CA16

Bottom pins: A_CA0, A_BVD1, A_D0, A_D8, A_D1, A_D9, VCC, A_D2, A_D10, A_WP, A_*CO2, A_VPP2EN1, A_VPP1EN1, A_*VCCEN, A_GPIO, B_GPIO, B_VCCEN, B_VPP1EN1, B_VPP2EN1, B_REG, B_D3, B_*CO1, GND, B_D4, B_D11, B_D5, B_D6, B_D12, B_D13, B_D7, B_*CE1, B_D14, B_D15, B_CA10, B_*OE, VCC, B_*CE2, B_CA11, B_*IORD, B_CA9, B_*IOWR, B_CA8, B_CA17, B_CA13, B_CA14, B_CA19, B_*WE, B_CA20, B_RDY, B_CA21

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ALTERNATIVE PIN DEFINITIONS

PIN #	DEFAULT	ALTERNATIVE(S)
32,103	RDY/*BSY	*IREO
52,123	BVD2	*SPKR
54,125	BVD1	*STSCHG, *RI
61,132	WP	*IOIS16
67,68	GPIO	*VPPVALID

VADEM VG-468
PC CARD SOCKET
CONTROLLER

Signal Description

Pin #	Signal Names	Type	Characteristics	# Pins
204	AEN	I	TTL Compatible	1
205	BALE	I	TTL Compatible	1
54, 125	BVD1 (*STSCHG/*RI)	I	CMOS Schmitt Trigger	2
52, 123	BVD2 (*SPKR)	I	CMOS Schmitt Trigger	2
15,19,21, 23-26,28,29 31,33-41,43 44,46,48,50 51,53,86,90 92,94-99, 102,104-107 109-115,117 119,121,122 124	CA[25:0]	O	4mA Tri-State	52
63,3,134,74	*CD[2:1]	I	CMOS Schmitt Trigger	4
89,83,18,11	*CE[2:1]	O	4mA Tri-State	4
187	CLK	I	TTL Compatible	1
2,4-10,12,13 55-58,60,62 73,76-82,84 85,126-130 133	D[15:0]	I/O	I = TTL Compatible O = 4mA Output	32
14,27,42,75 101,131,135 154,169,188	GND			10
67,68	GPIO	I/O	I = CMOS Schmitt Trigger O = 4mA Tri-State	2
49,120	*INPACK	I	TTL Compatible	2
152	*INTR	I/O	I = TTL Compatible O = 4mA Tri-State	1
150	IOCHRDY	O	16 mA Tri-State	1
148	*IOCS16	O	16 mA 5V Open Drain	1
20,91	*IORD	O	4mA Tri-State	2
22,93	*IOWR	O	4mA Tri-State	2
136-140 146-142	IRQs	O	4mA Tri-State	10

4

Signal Description (cont.)

Pin #	Signal Names	Type	Characteristics	# Pins
181-175	LA[23:17]	I	TTL Compatible	7
149	*MEMCS16	O	16 mA 5V Open Drain	1
174	*MEMR	I	TTL Compatible	1
173	*MEMW	I	TTL Compatible	1
16,87	*OE	O	4mA Tri-State	2
208	PWRGOOD	I	Schmitt Trigger	1
32,103	RDY/*BSY (*IREQ)	I	CMOS Schmitt Trigger	2
1,72	*REG	O	4mA Tri-State	2
45,116	RESET	O	4mA Tri-State	2
189	RESETDRV	I	Schmitt Trigger with pull-down	1
151	*RIO/LED	I/O	I = TTL Compatible O = 4mA Tri-State	1
203-192,190 186-183	SA[16:0]	I	TTL Compatible	17
182	*SBHE	I	TTL Compatible	1
206	*SIOR	I	TTL Compatible	1
207	*SIOW	I	TTL Compatible	1
155-162, 172-170,168 167,165-163	SD[15:0]	I/O	I = TTL Compatible O = 8mA Tri-State	16
153	*SPKROUT	I/O	I = TTL Compatible O = 4mA Tri-State	1
17,59,88, 108,141,166 191	VCC			7
66,69	*VCCEN	O	4mA Output	2
65,70	VPP1EN1	O	4mA Output	2
64,71	VPP2EN1	O	4mA Output	2
47,118	*WAIT	I	TTL Compatible	2
30,100	*WE/*PRGM	O	4mA Tri-State	2
61,132	WP (*IOIS16)	I	TTL Compatible	2
147	*ZWS	O	16mA 5V Open Drain	1

Pin Descriptions

Symbol	Type	Pin No.	Description
AEN	I	204	System Address Enable. High during DMA cycles, low otherwise.
BALE	I	205	Bus Address Latch Enable. An active high input used to latch LA[23:17] at the beginning of a bus cycle.
BVD1 (*STSCHG/*RI)	I	54,125	If BVD1 is negated by a memory PC Card with a battery, it indicates that the battery is no longer serviceable and data is lost.
			For I/O PC Cards, this signal is held high when either or both the Signal on Change bit and Changed bit in the Card Status Register on the PC Card are set to zero. When both the bits are one, the signal is held low. The Changed bit is the logical OR of the bits CVBAT1, CVBAT2, CWP and CBSYRDY in the Pin Replacement Register on the PC Card. Or this pin is connected to Ring Indicate, which is qualified by Ring Indicate Enable to be passed on to the *RIO pin.
BVD2 (*SPKR)	I	54,123	BVD1 and BVD2 are generated by memory PC Cards with onboard batteries. These signals indicate the health of the battery. Both are asserted high when the battery is in good condition. When BVD2 is negated while BVD1 is still asserted, the battery should be replaced, although data integrity on the memory PC Card is still assured.
			When the I/O interface is selected, BVD2 may be used to provide a single amplitude Digital Audio waveform intended to be passed through to the system's speaker without signal conditioning.
CA[25:12]	O	15,19,21 23-26,28 28,31 33-41,43 44,46,48 50,51,53 86,90,92 94-99,102 104-107 109-115,117 119,121,122 124	Card Address.

6

Pin Descriptions
(continued)

Symbol	Type	Pin No.	Description
*CD[2:1]	I	63,3 134,74	Detects proper card insertion. The signals are connected to ground internally on the PC Card and will be forced low whenever a card is placed in a host socket. Status is available to software through the Interface Status Register.
*CE[2:1]	O	89,83 18,11	Active low card enable signals. *CE1 is used to enable even bytes, *CE2 for odd bytes. A multiplexing scheme based on A0, *CE1, *CE2 allows 8-bit hosts to access all data on Card Data[7:0] if desired.
CLK	I	187	System clock.
D[15:0]	I/O	2,4-10 12,13 55-58 60,62,73 76-82 84,85 126-130 133	Card data.
GPIO	I/O	67,68	General purpose input/output. May be used for one of several purposes. - An active low input indicates that Vpp power line has reached the user specified range. - An input indication a card eject or card insertion pending. - An input source for generating a card status change interrupt. - Programmable chip select output.
*INPACK	I	49,120	Input Acknowledge. Asserted by some PC Cards during I/O read cycles. This signal is used by the VG-468 to control the enable of its input data buffer between the card and CPU.

VADEM VG-468

PRELIMINARY

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*INTR	I/O	152	Interrupt Request output: Active low output requesting a nonmaskable interrupt to the CPU. Also, a resistor strapping input during RESETDRV to determine the mapping of socket A and socket B to one of four groups.
IOCHRDY	O	150	I/O Channel Ready. This active high signal indicates that the current I/O bus cycle has completed. When a PC Card needs to extend a Read or Write cycle, the VG-468 pulls IOCHRDY low. IOCHRDY can be deasserted by either *WAIT, or by programming to add wait states for 16-bit memory and I/O cycles. If *WAIT is used in 16-bit mode, the wait state generator has to be set to 1 wait state.
*IOCS16	O	148	This active low I/O 16-bit chip select signal indicates to the host system the current I/O cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is inactive.
*IORD	O	20,91	I/O Read signal is driven active to read data from the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
*IOWR	O	22,93	I/O Write signal is driven active to write data to the PC Card's I/O space. The *REG signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.
IRQs	O	136-140 146-142	IRQ[15, 14, 12:9, 7, 5:3].
LA[23:17]	I	181-175	Local Address bus used to address memory devices on the ISA-bus. Together with the system address signals, they address up to 16MB on the ISA bus.
*MEMCS16	O	149	This active low 16-bit memory chip select signal indicates to the host system that the current memory cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is inactive.

8

Pin Descriptions
(continued)

Symbol	Type	Pin No.	Description
*MEMR	I	174	Active low signal indicates a memory read cycle.
*MEMW	I	173	Active low signal indicates a memory write cycle.
*OE	O	16,87	Active low signal used to gate memory reads from memory cards.
PWRGOOD	I	208	Power Good is an active high signal which indicates that power to the system is stable. Connect to ground if not used. Combined with RESETDRV, it will indicate to VG-365 whether a cold reset, or a resume reset has occurred, to decide whether to reset the slot configuration registers. System implementations without a "POWERGOOD" as resume indication should tie this signal low.
RDY/*BSY (*IREQ)	I	32,103	Memory PC Cards drive Ready / *Busy low to indicate that the memory card circuits are busy processing a previous write command. It is set high when they are ready to accept a new data transfer command.

For I/O PC Cards, this pin is used as an interrupt request and driven low to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested. |
| *REG | O | 1,72 | Select attribute memory. This signal is set inactive (high) for all accesses to common memory of a PC Card. When it is active, access is limited to Attribute Memory when *WE or *OE are active, and to I/O ports when *IORD or *IOWR are active. I/O PC Cards will not respond to *IORD or *IOWR when the *REG signal is inactive. During DMA operations the *REG signal is inactive. |

**Pin Descriptions
(continued)**

Symbol	Type	Pin No.	Description
RESET	O	45,116	Provides a hard reset to a PC Card and clears the Card Configuration Option Register, thus placing card in an unconfigured (memory interface) state.
RESETDRV	I	189	Active high indicates a main system reset.
*RIO/LED	I/O	151	Ring Indicate Output. Pass through of Ring Indicate output from I/O PC Card. VG-468 can also be configured to activate *RIO on card detect changes. *RIO will be functional in *CS controlled power down. When disk drive LED enable is set this signal becomes a driver for disk drive LED. Also, a resistor strapping input during RESETDRV to determine the functions of pin B_CA[11:4].
SA[16:0]	I	203-192 190 186-183	System Address bus used to address memory and I/O devices on the ISA bus. These signals are latched and are valid throughout the bus cycle.
*SBHE	I	182	System Byte High Enable. When asserted, this active low signal indicates that a data transfer is occurring on the upper byte of the system data bus.
SD[7:0]	I/O	155-162, 172-170, 168,167 165-163	System Data Bus.
*SIOR	I	206	This active low I/O read signal instructs the VG-468 to drive data onto the data bus.
*SIOW	I	207	This active low I/O write signal instructs the VG-468 to latch the data on the data bus.
*SPKROUT	I/O	153	Digital audio signal which provides a single amplitude (digital) audio waveform to drive the system's speaker. Passes through *SPKR from an I/O PC Card. This signal must be held high when no audio signal is present. Also, a resistor strapping input during RESETDRV to determine the mapping of socket A and socket B to one of four groups.

10

Pin Descriptions (continued)

Symbol	Type	Pin No.	Description
*VCCEN	O	66,69	Power Control signal for card Vcc.
VPP1EN1	O	65,70	Power Control signal for card Vpp1.
VPP2EN1	O	64,71	Power Control signal for card Vpp2.
*WAIT	I	47,118	This signal is driven by the PC Card to delay completion of the memory or I/O cycle in progress.
*WE/*PRGM	O	30,100	The host uses *WE for gating memory write data, and for memory PC Cards that employ programmable memory.
WP (*IOIS16)	I	61,132	Reflects the status of the Write Protect switch on some memory PC Cards. If the memory PC Card has no write protect switch, the card will connect this line to ground (the card can always be written) or to Vcc (permanently write protected).
			When the I/O interface is selected, this pin is used for the "I/O is 16-bit Port" function: asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port which is addressed is capable of 16-bit access. If this signal is not asserted during a 16-bit I/O access, the system will generate 8-bit references to the even and odd byte of the 16-bit port being accessed. If 8-bit window size is selected, *IOIS16 is ignored.
*ZWS	O	147	Zero Wait State. An active low output indicates that the PC Card wishes to terminate the present bus cycle without inserting additional wait states. This cycle will not be driven during a 16-bit I/O access.