CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION

# CY7C1007

# 1M x 1 Static R/W RAM



## Features

- High speed
  - $t_{AA}$ = 15 ns
- CMOS for optimum speed/power
- Low active power
  - 770 mW
- Low standby power
  - 250 mW
- Low data-retention power
  - 100 µW at 2.0V
- Automatic power-down when deselected
- TTL-compatible inputs and outputs

## Functional Description

The CY7C1007 is a high-performance CMOS static RAM organized as 1,048,576 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 65% when deselected.

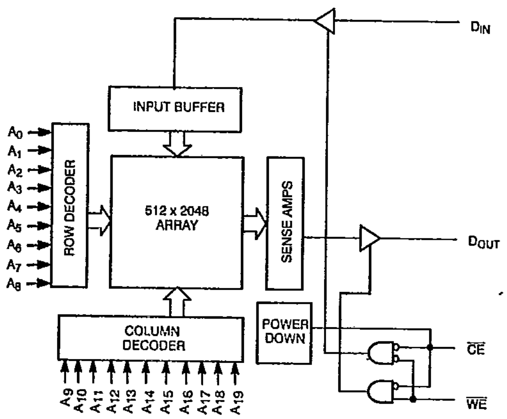
Writing to the device is accomplished by taking chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the input pin ($D_{IN}$) is written into the memory location specified on the address pins ($A_0$ through $A_{19}$).

Reading from the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the data output ($D_{OUT}$) pin.

The output pin ($D_{OUT}$) is placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH) or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7C1007 is available in standard 300-mil-wide DIPs and SOJs.

## Logic Block Diagram

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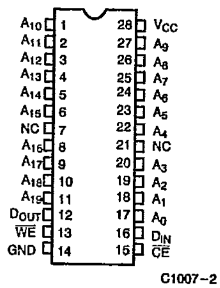
## Pin Configurations

DIP/SOJ
Top View

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## Selection Guide

| | | 7C1007-15 | 7C1007-20 | 7C1007-25 |
|---|---|---|---|---|
| Maximum Access Time (ns) | | 15 | 20 | 25 |
| Maximum Operating Current (mA) | Commercial | 140 | 140 | 140 |
| | Military | | 145 | 145 |
| Maximum Standby Current (mA) | Commercial | 45 | 45 | 45 |
| | Military | | 50 | 50 |

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