SIEMENS

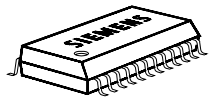
ISDN Remote Power Controller (IRPC)

PSB 2120

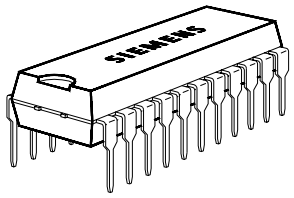
CMOS IC

Features

- Switched mode DC/DC-converter
- Switched mode DC/DC-converter
- CCITT (I.430) ISDN compatible
- Integrated 200 V power FET (only PSB 2120-P in P-DIP-22)
- Low power dissipation
- Supply voltage range 10 V to 60 V
- Input undervoltage detection
- Programmable overcurrent protection
- Soft start
- Control circuit to achieve minimum start-up current
- Power housekeeping input
- Oscillator synchronization input/output
- Polarity reversal detection
- High voltage CMOS-technology 60 V



P-DSO-24-1



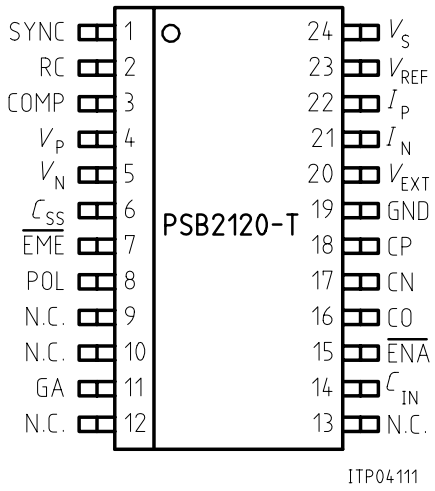
P-DIP-22

Type	Version	Ordering Code	Package
PSB 2120-P	V B5	Q67100-H8645	P-DIP-22
PSB 2120-T	V B5	Q67100-H6278	P-DSO-24-1 (SMD)

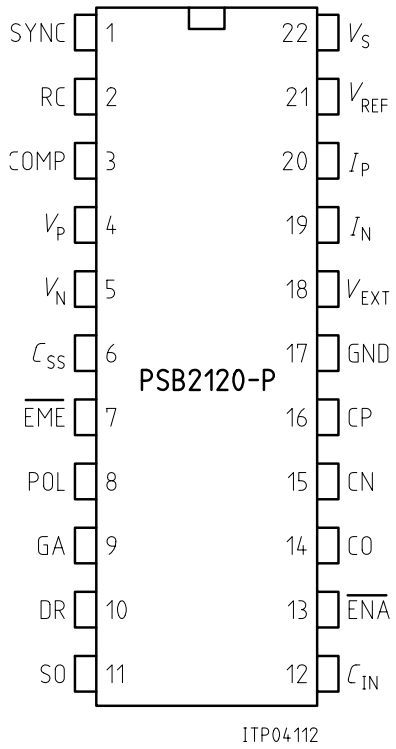
The PSB 2120 is a Pulse Width Modulator (PWM) circuit designed for fixed-frequency switching regulators especially for telephony and ISDN-environments.
The PSB 2120 is fully compatible with the CCITT-power recommendations on the “S”-interface.
Coupled with a few external components it can provide a stable 5 V DC-supply for subscriber terminals (TE’s) or network terminators (NT’s). It can also be programmed for higher output voltages, e.g. to supply the S-lines with 40 V.
In telephony and ISDN-systems a high conversion yield is crucial to maintain functionality in all supply conditions via “S”- or “U”-interfaces. The PSB 2120 design and technology realizes high conversion efficiency and low power dissipation.
It should be recognized that the PSB 2120 can also be used in numerous DC/DC-conversion systems other than ISDN-power supplies.

Pin Configurations
(top view)

P-DSO-24



P-DIP-22



Pin Definitions and Functions

Pin No. P-DSO	Pin No. P-DIP	Symbol	Input (I) Output (O)	Definition	Function
1	1	SYNC	I/O	Synchronization	Input for synchronization of the oscillator to an external frequency, or output to synchronize multiple devices.
2	2	RC	I	RC-Oscillator	The external timing components of the ramp generator are attached to this pin.
3	3	COMP	O	Compensation	Error amplifier output and **P**ulse **W**idth **M**odulator (PWM) input for loop stabilization network.
4	4	V_P	I	Positive Voltage Sense	Non-inverting input of the error amplifier.
5	5	V_N	I	Negative Voltage Sense	Inverting input of the error amplifier.
6	6	C_{SS}	I	Soft Start Capacitor	The capacitor at this pin determines the soft-start characteristic.
7	7	$\overline{EME}$	O	$\overline{Emergency}$	A low input voltage at POL will activate the output $\overline{EME}$.
8	8	POL	I	Polarity Detection	POL is the input to a non inverting Schmitt-trigger.
11	9	GA	O	Gate	Output of the FET-driver.
N.C.	10	DR	O	Drain	Drain connection of the power FET.
N.C.	11	SO	O	Source	Source connection of the power FET.
14	12	C_{IN}	I	Input Capacitor	C_{IN} has to be connected to the input buffer-capacitor and a current limiting charging-resistor.

Pin Definitions and Functions (cont'd)

Pin No. P-DSO	Pin No. P-DIP	Symbol	Input (I) Output (O)	Definition	Function
15	13	$\overline{\text{ENA}}$	I	$\overline{\text{Enable}}$	A high input voltage at this pin will stop the IRPC-function.
16	14	CO	O	Comparator output	Connections of the universal usable comparator.
17	15	CN	I	Comparator neg. input	
18	16	CP	I	Comparator pos. input	
19	17	GND	I	Ground	All analog and digital signals are referred to this pin.
20	18	V_{EXT}	I/O	External supply	Output of the internal CMOS-supply. Via V_{EXT} the internal CMOS-circuits can be supplied from an external DC-supply in order to reduce chip power dissipation.
21	19	I_N	I	Negative current sense	When the voltage difference between these two pins exceeds 100 mV, the digital current limiting becomes active.
22	20	I_P	I	Positive current sense	
23	21	V_{REF}	O	Reference voltage	Output of the 4.0 V reference voltage.
24	22	V_S	I	Supply voltage	V_{BAT} is the positive input voltage.

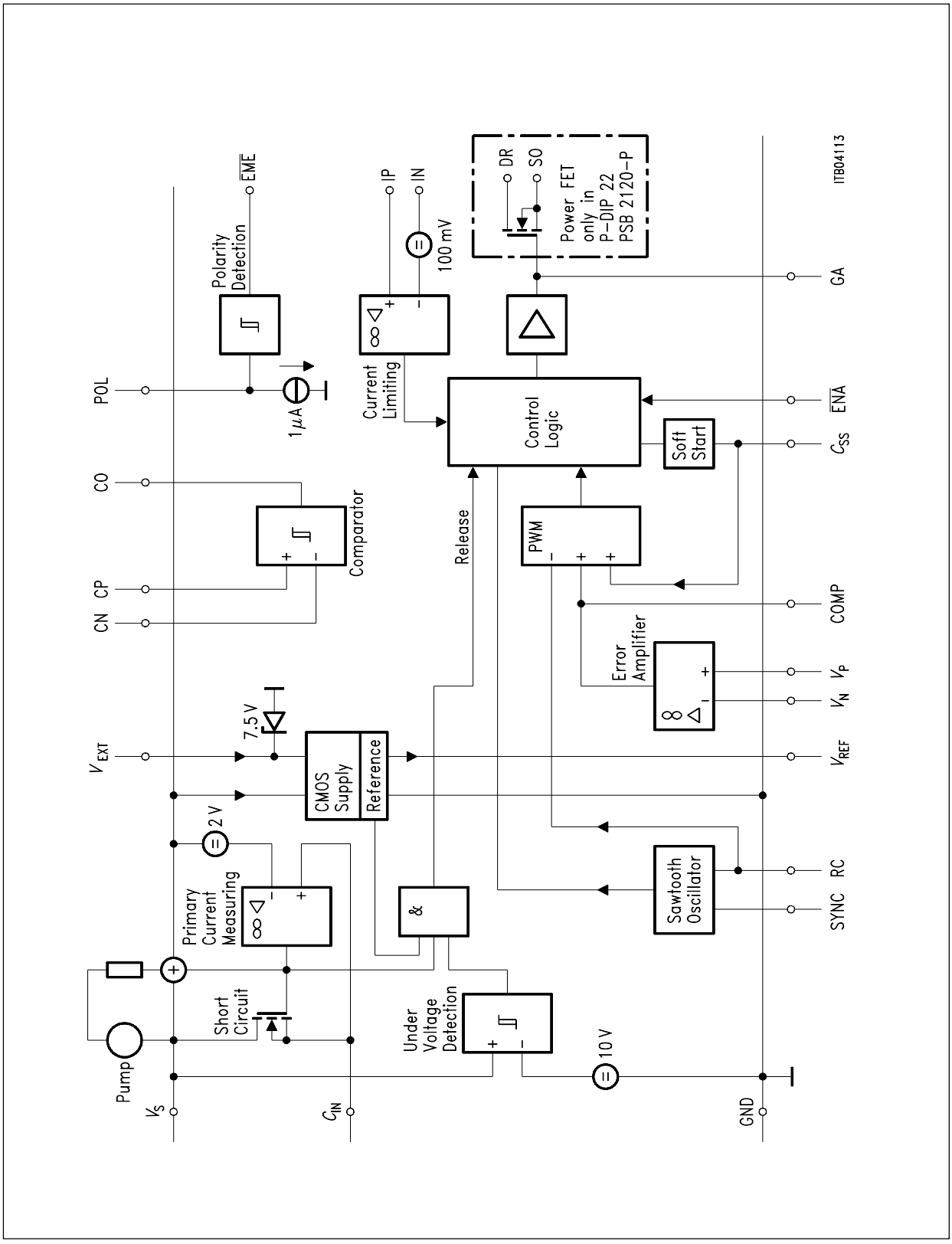


Figure 1
IRPC Functional Diagram

Functional Description

The reference provides a 4.0 V voltage for the regulation loop. A high gain error amplifier compares the reference voltage with the switch mode supply output voltage. The output of the error amplifier is compared with a periodic linear ramp, which is generated by the sawtooth-oscillator circuit. The comparator output is a fixed-frequency, variable pulse width logic signal, which passes through logic circuits to the high voltage power-switching-FET.

A digital current limiting device suppresses the PWM logic signal when the voltage difference at the current limit sense input reaches 100 mV. In this case the control logic inhibits double pulses during one oscillator period.

Start-Up Procedure

Before the switched-mode DC/DC-converter starts, a sequence of several conditions has to be passed in order to avoid any system malfunction.

The primary undervoltage detection inhibits the converter function. This insures that all control functions have stabilized in the proper state when the turn on voltage (ca. 10 V) is reached, and it prevents start-up glitches.

In case of connecting the TE to powered lines or if a line is powered up, the charge current of the primary buffer capacitor is limited by an external resistor (**figure 2**).

This resistor is short-circuited by the PSB 2120 when the voltage drop across it falls below approximately 2.0 V. The residual resistance of this short-circuit is about 3 Ω. In case of a primary undervoltage detection the short-circuit will be always deactivated. So, the DC/DC-converter does not start until the charging of the primary buffer capacitor is completed, and the maximum line input voltage is reached. If this feature is not desired, C_{IN} has to be connected to GND. In this case the primary current measuring circuit turns off, to reduce chip-power dissipation from 9 mW to 6 mW.

In order to avoid high current peaks during the charging of the secondary capacitors or line capacitors in case of supplying an S-interface, a soft start circuit is implemented in the PSB 2120. This circuit requires an external capacitor, connected between C_{SS} and GND.

In addition, the enable input ($\overline{ENA}$) allows an external switch-on/switch-off control. If the DC/DC-converter is disabled via $\overline{ENA}$, the soft-start-capacitor at pin C_{SS} is discharged. This input can also be used for several other functions, e.g. secondary overvoltage protection.

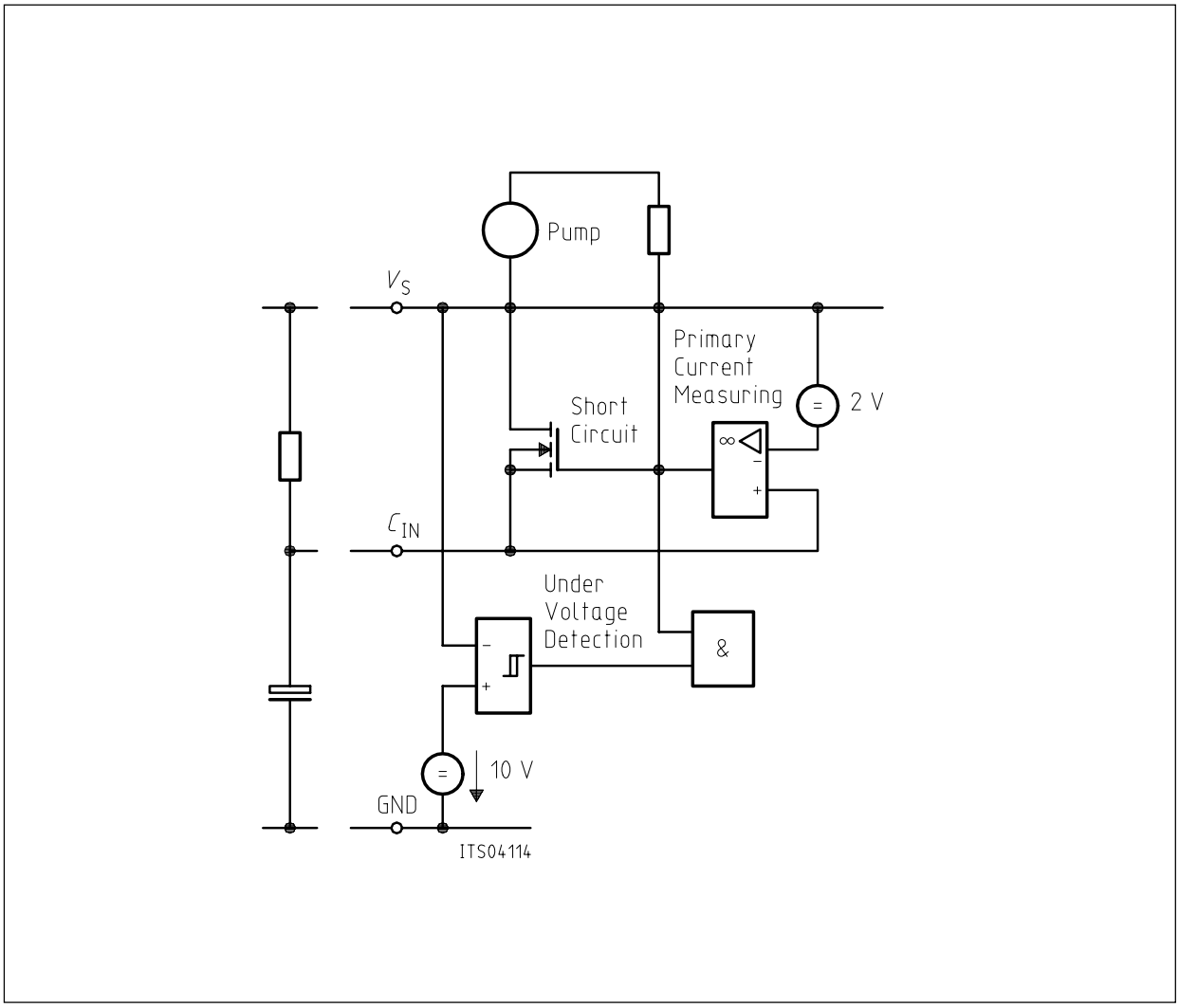


Figure 2

DC/DC-Conversion

The PSB 2120 contains a SIPMOS-transistor for power handling. Non-isolated and isolated SMPS-configurations are possible. Logic and analog circuits are implemented in CMOS in order to achieve low power dissipation.

The error amplifier compares the sensed voltage with a reference attached to V_P and thus controls the Pulse Width Modulator (PWM). The conversion frequency is generated by a sawtooth oscillator which can be controlled by external RC-components (**figure 4**) or by an external synchronization signal. The PSB 2120 is synchronized by the rising edge of the sync signal, whose frequency must be 10 % higher than the free run frequency, determined by the RC-components. The SYNC-pin can also be used as a trigger-output. As long as the capacitor of the sawtooth oscillator is discharged, SYNC is high.

The output of the PWM is processed by the control logic and fed to the SIPMOS-transistor. The control logic suppresses higher oscillations of the regulation loop caused e.g. in case of current limit detection.

Polarity Detection

Emergency conditions are signaled to the TE by the reversed polarity of the line feeding voltage. When polarity reversal is detected via pin POL of the PSB 2120, emergency conditions are signaled to the microprocessor via pin $\overline{\text{EME}}$, which should shut down all activity except simple telephony functions to minimize power dissipation.

The polarity detection circuit can also be used for other detection or protection-functions, e.g. programmable primary undervoltage detection.

Power Housekeeping

An integrated 6 V linear voltage regulator supplies the internal circuits during the start-up phase. Power dissipation of this regulator can be reduced, if an auxiliary winding of the transformer or an external supply is used for that purpose by connecting it to V_{EXT}. If the input voltage at V_{EXT} reaches 6.2 V the internal linear voltage regulator turns off and the internal circuits are fed from this external voltage. In this case the input current at V_{EXT} is approx. 0.5 mA.

Note: An internal 7.5 V Zener-diode protects the V_{EXT} input against overvoltages. The maximum Zener-current is 2 mA! If the external supply isn't stabilized, the input current must be limited (e.g. by a resistor)!

Interface to Microprocessor

The PSB 2120 offers two TTL-compatible signals: $\overline{\text{EME}}$ and CO. The $\overline{\text{EME}}$ (Emergency-output) becomes active, if polarity reversal is detected. CO is the output of a universal usable comparator; e.g.: to generate a microprocessor-reset signal.

PSB 2120 Applications in ISDN-Environments

Figure 3 shows an example out of the wide application field of the PSB 2120. In the network termination one PSB 2120 supplies the internal IC's directly from the U–interface. A second IRPC, also powered from the U-line, supplies the S–interface if the main supply of the NT is out of order. A third IRPC is used in the main supply to regulate the S-line feeding voltage.

In the subscriber terminal the PSB 2120 is used for feeding the internal circuits.

The PSB 2120 accommodates both galvanically isolated and non-isolated configuration. Considering the diversity of DC/DC-converter applications, this part of the specification only shows how to use the special ISDN-features of the PSB 2120.

The switching frequency of the SMPS is programmable by two external components.

Figure 4 shows the switching frequency as a function of R_T and C_T.

The minimum configuration so as to be able to use the PSB 2120 in ISDN-applications is by using a flyback converter (**figure 5**).

The time constant of the soft start circuit is programmed by a capacitor at Pin C_{SS}.

Figure 6 shows the primary start-up current limitation by connecting Pin C_{IN}. To reduce chip-power-dissipation, an auxiliary winding of the transformer is used to switch off the internal linear CMOS-supply (pin V_{EXT}). Polarity reversal is detected by pin POL.

Figure 7 shows the realization of a microprocessor-reset-signal with the universal usable comparator of the IRPC.

Figure 8 shows the PSB 2120 in flyback configuration with transformer isolation.

Figure 9 shows the PSB 2120 in flyback configuration with opto isolation, which is useful for a high reliability galvanically isolated application.

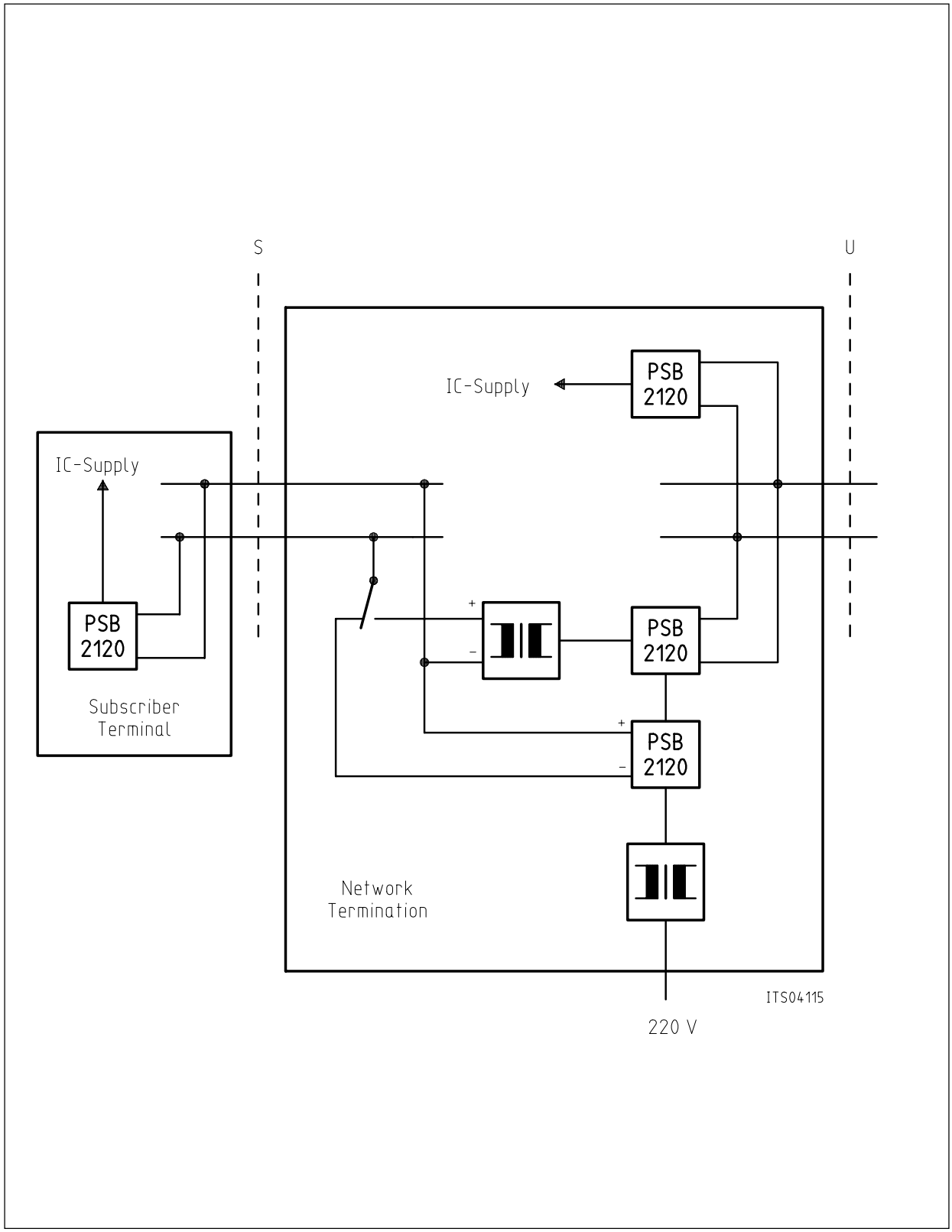
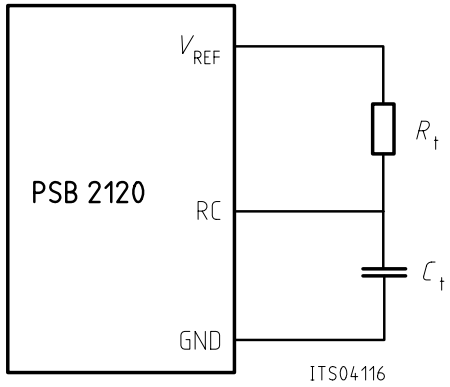


Figure 3
IRPC in ISDN-Concept



Switching Frequency

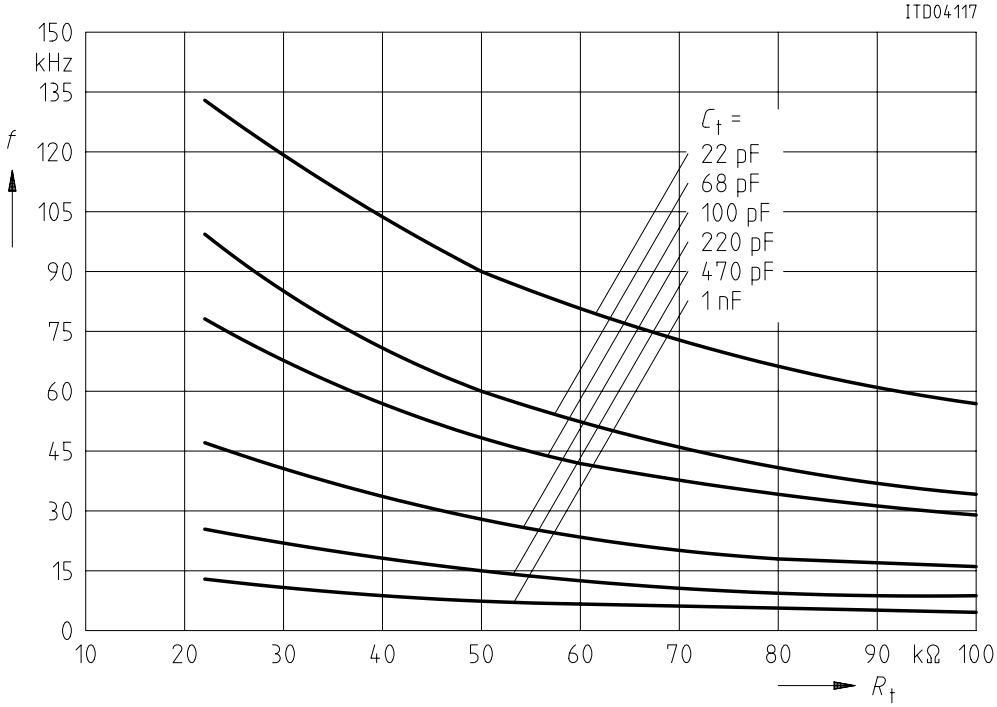


Figure 4
Switching Frequency as a Function of R_T and C_T

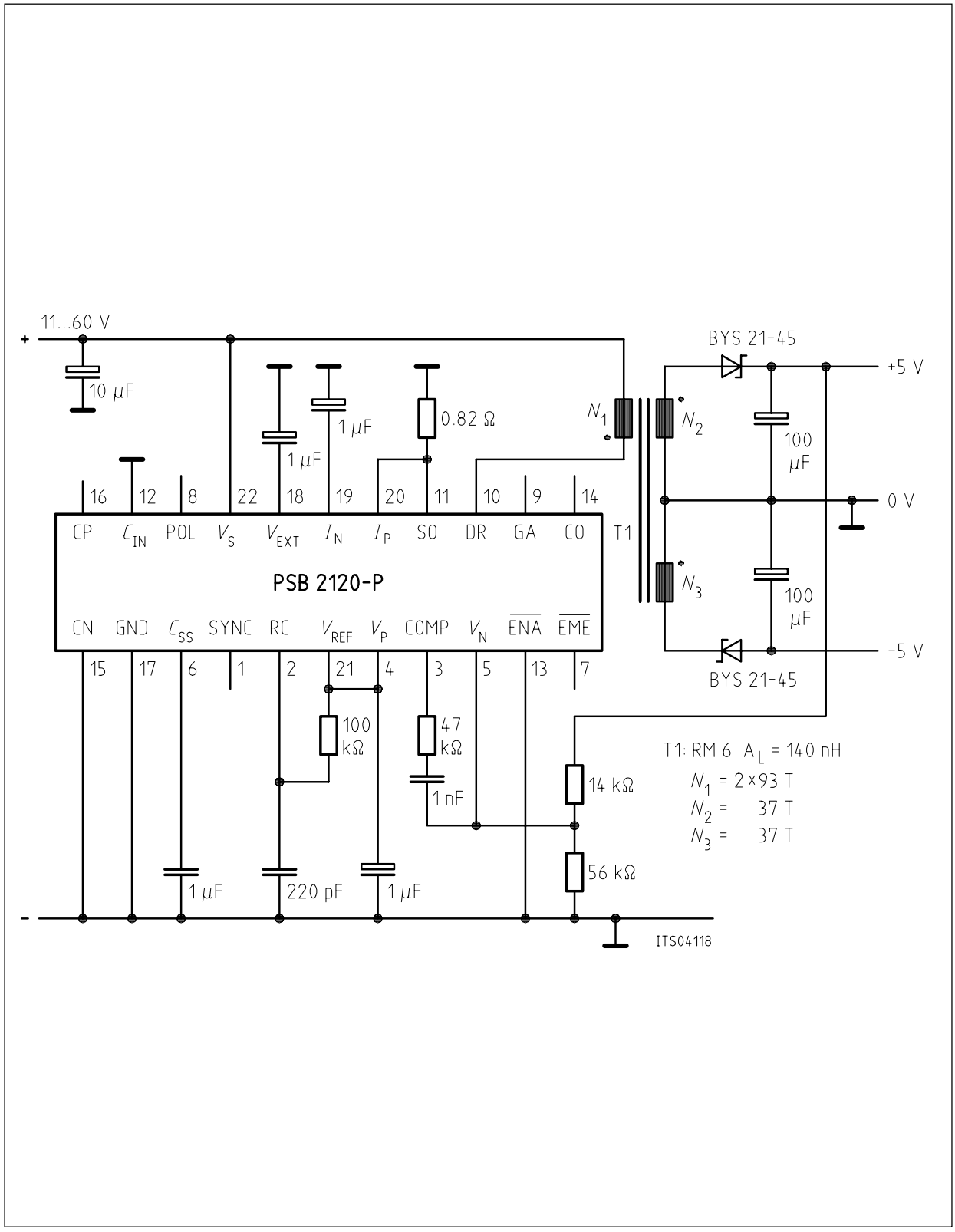


Figure 5
PSB 2120 Minimum Configuration

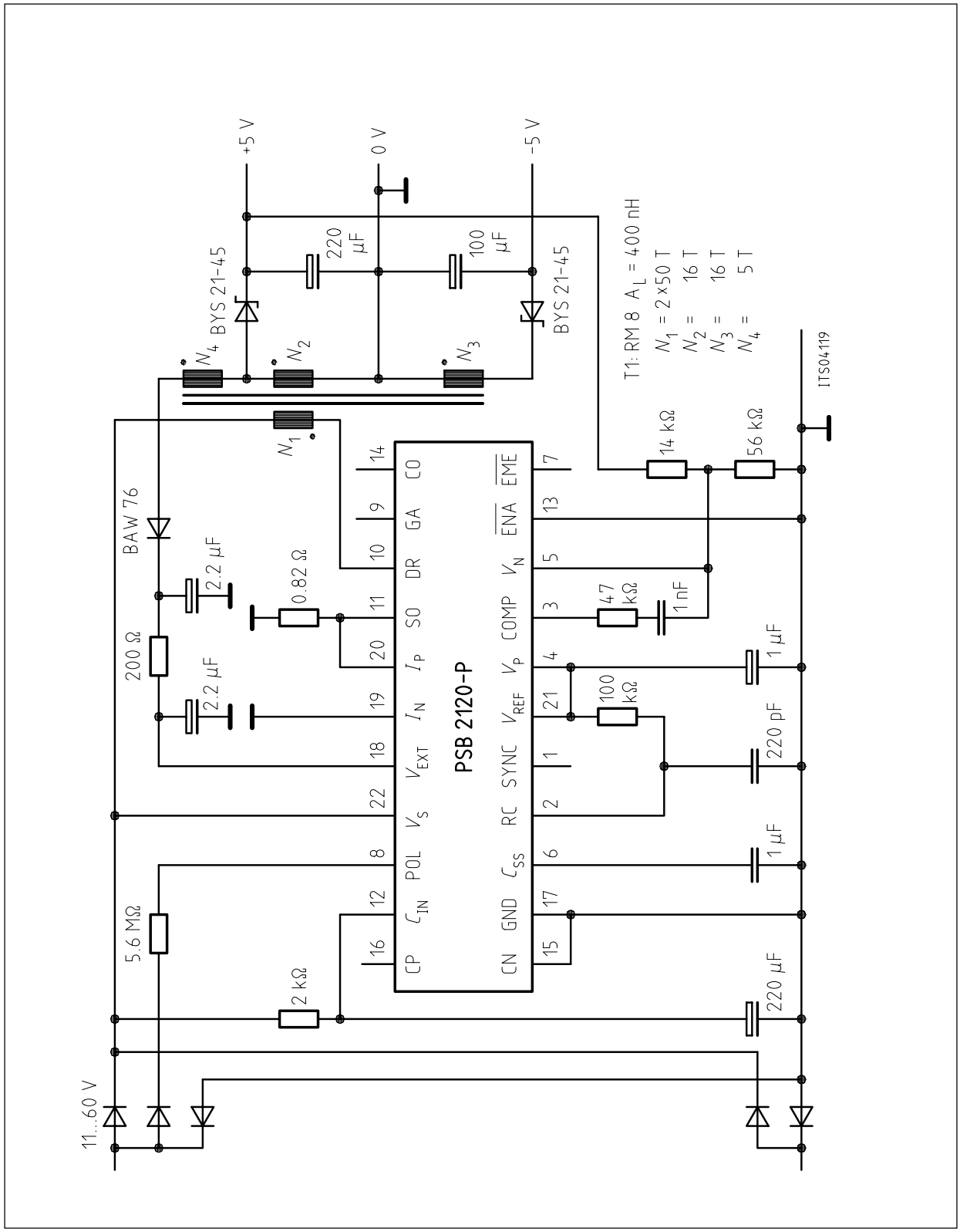
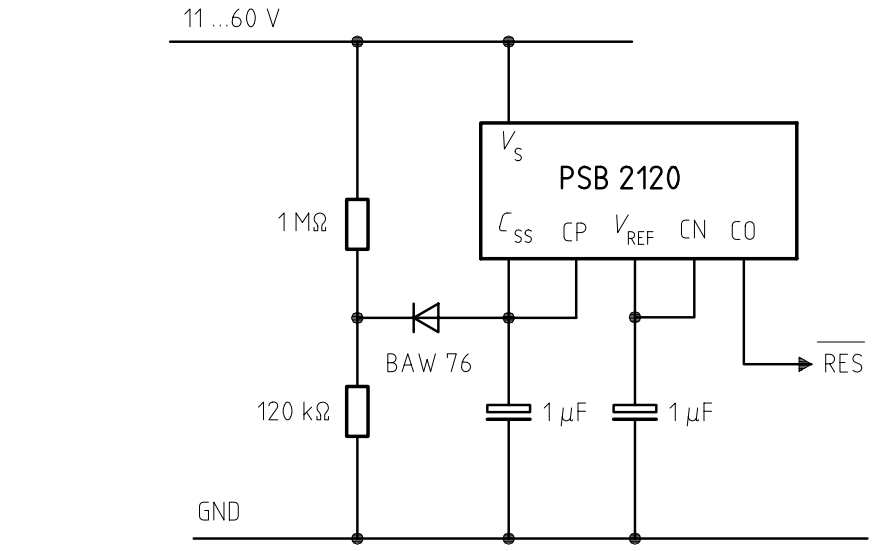
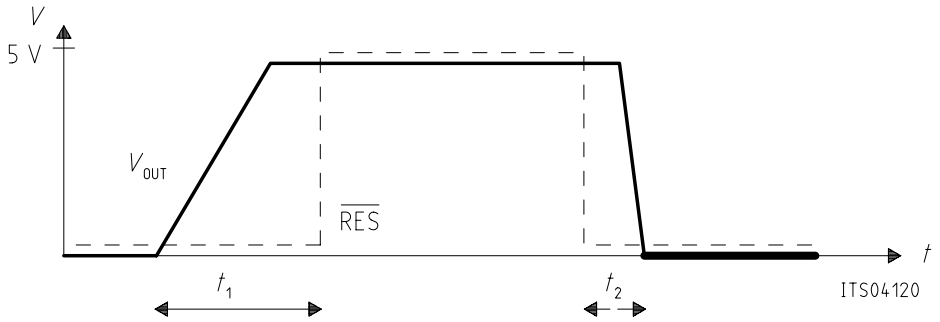


Figure 6
Advanced IRPC-Application with Power Housekeeping and Polarity Reversal Detection





According to the application in **figure 5** and an output power of 500 mW, t_1 will be 400 ms and t_2 50 ms.

Figure 7
Generation of a µP-Reset Signal with the PSB 2120

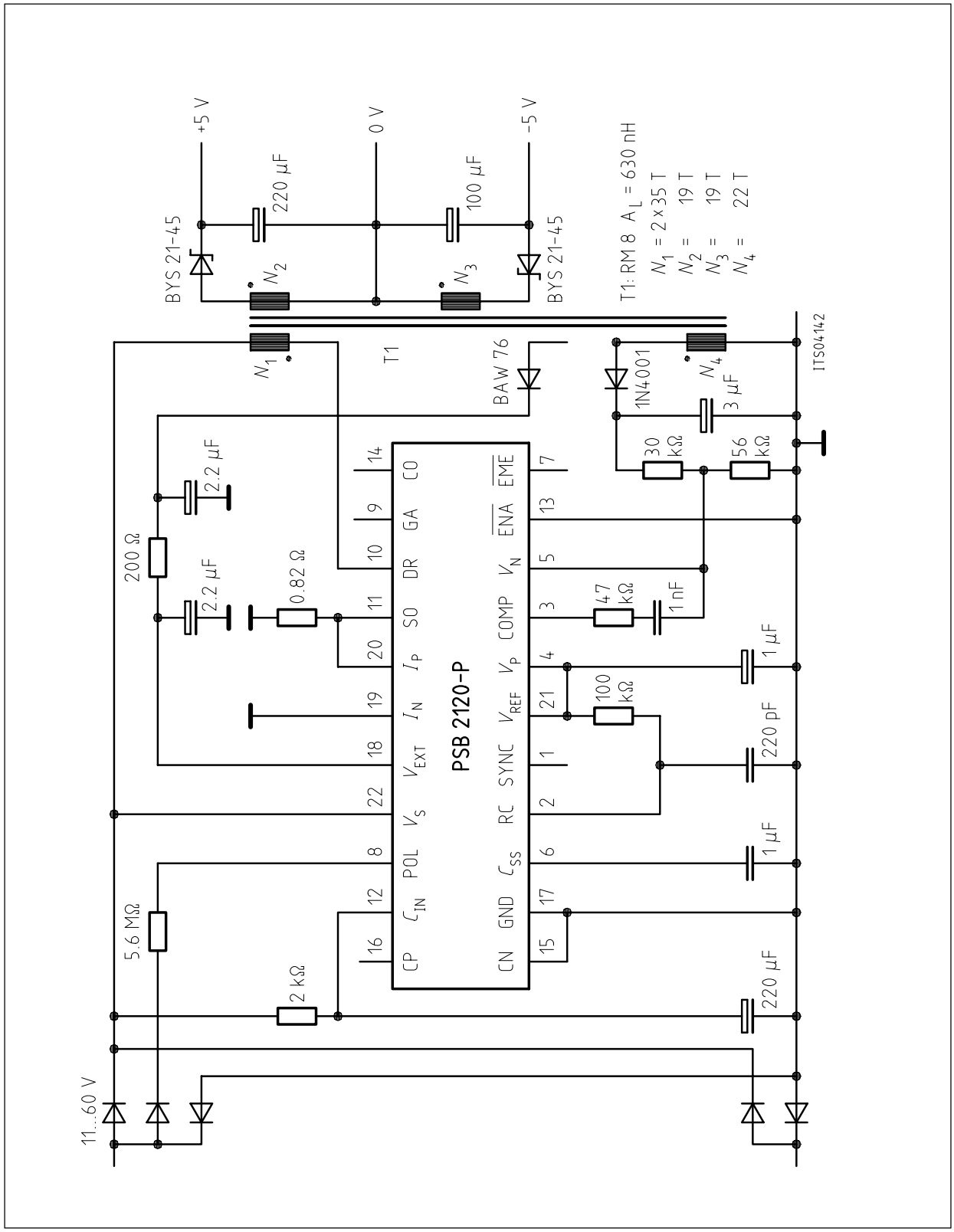


Figure 8
PSB 2120 in Flyback Configuration with Transformer Isolation

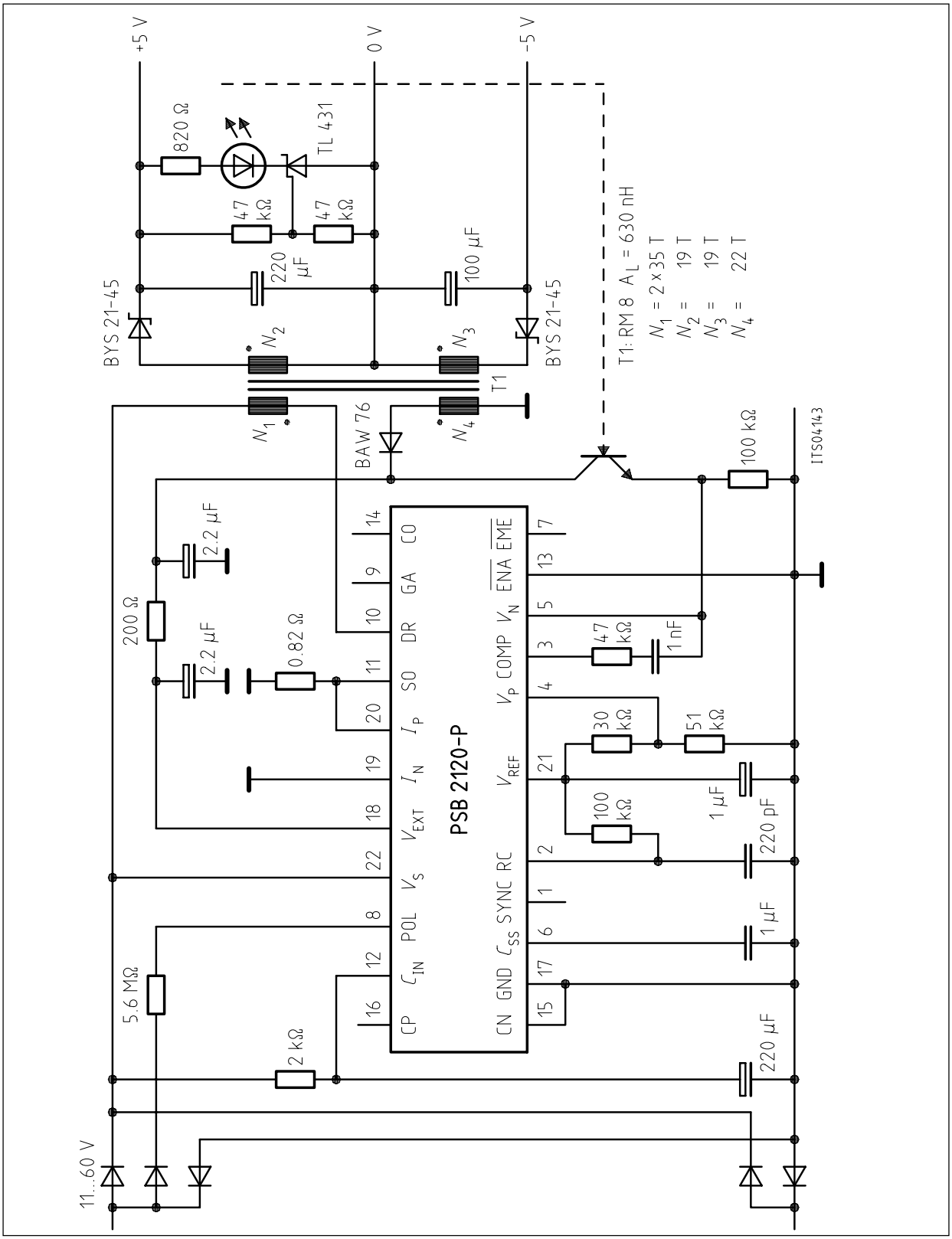


Figure 9
PSB 2120 in Flyback Configuration with Opto Isolation

Absolute Maximum Ratings (All pin references made for P-DIP-22)

Parameter	Symbol	Limit Values	Unit
Supply voltage DR (pin 10) referred to S0 (pin 11)	V_S	200	V
Continuous drain current (pin 10)	I_{DR}	350	mA
Supply voltage V_{BAT} (pin 22) referred to GND	V_{BAT}	60	V
Analog/digital input voltage referred to GND (pins 2, 3, 4, 5, 7, 8, 13, 15, 16, 19, 20)	$V_{I\ A/D}$	6	V
Reference output current (pin 21)	$I_{O\ REF}$	– 5	mA
V_{EXT} input Z-current	$I_{I\ Z}$	2	mA
V_{EXT} output current	I_O	– 5	mA
SYNC-output current (pin 1)	$I_{O\ SYNC}$	– 5	mA
Driver output current (pin 9)	$I_{O\ DR}$	– 5	mA
Ambient temperature under bias	T_A	– 25 to 85	˚C
Storage temperature	T_{stg}	– 40 to 125	˚C
Thermal resistance junction – ambient	T_j	50	K/W

MOS-Handling:
The integrated SIPMOS-transistor (pin 9, 10 and 11) has to be protected against electrostatic charges. The input gate-source (pin 9 and pin 11) must be protected against ± 10 V.

DC Characteristics
T_A = 0 to 70 ˚C, V_S = 11 to 60 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reference V_{REF} T_A = 25 ˚C						
Output voltage	$V_{REF\ O}$	3.92	4.0	4.08	V	I_L = 0 mA, V_S = 40 V
Line regulation	$V_{REF\ Line}$			60	mV	V_S = 20 to 60 V, I_L = 0 mA,
Load regulation	$V_{REF\ Load}$		20	40	mV	I_L = 0.1 to 0.3 mA, V_S = 40 V
Temperature stability	$V_{REF\ TS}$		25		mV	
Load current	$I_{REF\ Load}$			0.5	mA	

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Oscillator SYNC (pin1)**, RC** (pin 2) f_{OSC} = 20 kHz, R_T 39 kΩ ± 1 %, C_T= 1 nF ± 1 %, T_A = 25 ˚C						
Initial accuracy			± 10		%	
Voltage stability of f_{OSC}			1	3	%	
Temperature stability of f_{OSC}			5		%	
Max. frequency	f_{max}	180	250		kHz	R_T = 27 kΩ C_T = 39 pF
H-sawtooth voltage	V_H	3.0	3.2	3.4	V	
L-sawtooth voltage	V_L	1.6	1.8	2.0	V	
H-sync output level	V_{OH}	2.4	3.5	5.25	V	I_L = 0.5 mA $V_{S\,EXT} \leq$ 6.3 V
L-sync output level	V_{OL}		0.2	0.8	V	I_L = 20 µA
Error Amplifier **COMP** (pin 3), $\boldsymbol{V_P}$ (pin 4), $\boldsymbol{V_N}$ (pin 5)						
Input offset voltage	V_{IO}		3	10	mV	V_{CM} = 3.0 V
Input current	I_I		0	25	nA	
Common mode range	V_C	1.8		4.0	V	V_{OFFSET} = ± 15 mV
DC open loop gain	G_{VO}	60	70		dB	
Common mode rejection	k_{CMR}	60	70		dB	
Unit gain bandwidth	f	0.5	1		MHz	C_L (pin) 10 pF
Supply voltage rejection		60	70		dB	
H-output voltage	V_{OH}	4	5.5		V	I_L = 100 µA
L-output voltage	V_{OL}		0.02		V	I_L = 10 µA
Current Limit Comparator $\boldsymbol{I_P}$ (pin 20), $\boldsymbol{I_N}$ (pin 19) T_A = 25 ˚C						
Sense voltage	V_{Sense}	85	100	115	mV	V_S = 40 V
Input current	I_I		0	100	nA	
Input voltage range	V_I	0		1	V	
Response time to signal at GA (pin 9)	t_{Res}		1	2	µs	I_N = 0 V I_P = 0 → 200 mV

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Pulse Width Modulator						
Duty cycle	t_d	0		50	%	
Undervoltage Detection						
Start-up threshold	$V_{UV\ St}$	8.1	10	11	V	
Threshold hysteresis	$V_{UV\ Hy}$		0.3		V	
Soft Start C_{ss} (pin 6)						
Charging current	I_C	2	4	8	µA	
Output Driver GA (pin 9) T_A = 25 ˚C, C_L = C_{GS} – Power FET						
H-output voltage	V_{OH}	4.5			V	I_{Source} = 5 mA
H-output voltage	V_{OH}			V_{EXT}	V	I_{Source} = 0 mA
L-output voltage	V_{OL}		0.3	0.4	V	I_{Sink} = 5 mA
Rise time	t_r		130	200	ns	V_{EXT} = 6.3 V
Fall time	t_f		70	200	ns	V_{EXT} = 6.3 V
Output current	I_O			5	mA	
External Supply V_{EXT} (pin 18)						
Output voltage	V_O		5.8		V	
Output current	I_O			2	mA	
Input voltage	V_I	6.0		7.5	V	
Z-current	I_Z			2	mA	
Enable Input $\overline{\text{ENA}}$ (pin 13)						
H-input voltage	V_{IH}	2.0		5.25	V	
L-input voltage	V_{IL}			0.8	V	
Response time to signal at GA (pin 9)	t_{Res}		0.5	1	µs	T_A = 25 ˚C
H-input current	I_{IH}	0.2	2.5	20	µA	

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Comparator CN (pin 15), **CP** (pin 16), T_A = 25 °C						
Input offset voltage	V_{IO}		3	10	mV	V_{CM} = 3 V
Input bias current	I_I		0	25	nA	
Input voltage range	V_I	1.8		4.5	V	
Response time to signal at CO (pin 14)	t_{Res}		0.2	1	µs	
Short Circuit G_I (pin 12), T_A = 25 °C						
Sense voltage	V_{Sense}	1	2	3	V	$(V_S - V_{CIN})$
	$R_{DS\ (on)}$		3	4	Ω	
Polarity Detection POL (pin 8), **$\overline{\text{EME}}$** (pin 7)						
H-input voltage	V_{IH}	2.0		5.25	V	
L-input voltage	V_{IL}			0.8	V	
H-input current	I_{IH}	0.1	1	10	µA	
Response time to signal at $\overline{\text{EME}}$ (pin 7)	t_{Res}		0.2	1	µs	
Digital Outputs $\overline{\text{EME}}$ (pin 7), **CO** (pin 14) I_{OUT} = 0.5 mA						
H-output voltage	V_{OH}	2.4	3.5	5.25	V	$V_{EXT} \leq$ 6.3 V
L-input voltage	V_{IL}		0.2	0.4	V	
Power FET GA (pin 9), **DR** (pin 10), **SO** (pin 11)						
	$R_{DS\ (on)}$		4	6	Ω	I_D = 300 mA
t_{on}	$t_{d\ (on)}$		55	150	ns	
t_{off}	$t_{d\ (off)}$		110	200	ns	
Leakage current	I_{Leak}			200	nA	V_{DS} = 110 V
Power consumption	P_{tot}		9	10	mA	V_S = 40 V f_{OSC} = 20 kHz V_{EXT} = 6.3 – 6.7 V
	C_{GS}		200		pF	