NEC
NEC Electronics Inc.

μPD42832
32,768 x 8-BIT CMOS XRAM

February 1988

Description

The μPD42832 is a 32,768-word by 8-bit CMOS XRAM designed to operate from a single +5-volt power supply. This device is termed an XRAM because it incorporates some of the best features of both SRAMs (nonmultiplexed addresses, simple interface) and DRAMs (high density at low cost from a one-transistor core cell). Advanced circuitry provides wide operating margins and low power dissipation while maintaining high performance.

The incorporation of an internal refresh address counter and refresh multiplexer allows selection of one of three refreshing modes. A self-refresh cycle provides transparent refreshing without system overhead. A pulse refresh cycle uses the internal address counter; external refresh cycles use the 256 address combinations of A_0-A_7.

Features

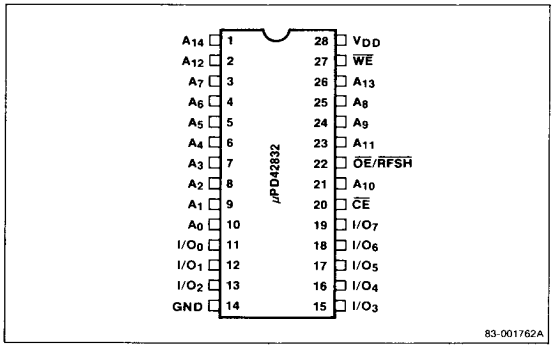
- ☐ 32,768-word by 8-bit organization
- ☐ Single +5-volt ±10% power supply
- ☐ TTL- and CMOS-compatible
- ☐ Low power dissipation
  - — Standby: 1.0 mA ($\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{IH})
  - — Standby: 0.5 mA ($\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{DD})
  - — Self-refresh: 100 μA (-xxL versions)
- ☐ Read, write, and read/modify/write cycles
- ☐ External, pulse, and self-refreshing capabilities
- ☐ SRAM-compatible pin configuration
- ☐ Standard 28-pin plastic DIP and miniflat packaging

Ordering Information

Part Number	Access Time (max)	Self-Refresh Current (max)	Package
μPD42832C-12	120 ns	1.5 mA	28-pin plastic DIP
C-15	150 ns		
μPD42832C-12L	120 ns	100 μA	28-pin plastic DIP
C-15L	150 ns		
μPD42832GU-12L	120 ns	100 μA	28-pin plastic miniflat
GU-15L	150 ns		

Pin Configuration

28-Pin Plastic DIP or Miniflat



Pin Identification

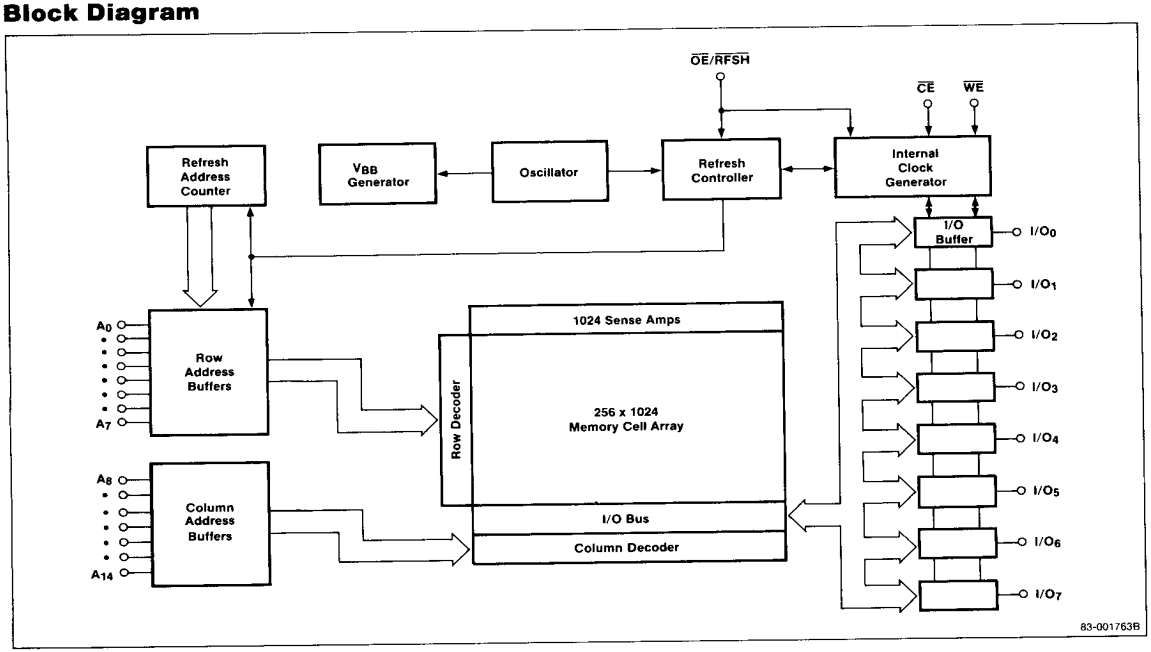
Symbol	Function
A_0-A_{14}	Address inputs
I/O_0-I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$/$\overline{RFSH}$	Output enable/refresh
$\overline{WE}$	Write enable
GND	Ground
V_{DD}	+5-volt power supply

Absolute Maximum Ratings

Voltage on any pin (except V_{DD})	−1.0 to +7.0 V
Supply voltage, V_{DD}	−1.0 to +7.0 V
Short-circuit output current, I_O	50 mA
Power dissipation, P_D	1.0 W
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. Operating conditions should be within the limits specified under DC and AC Characteristics.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{DD} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{DD}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		5.5	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{DD2}			1.0	mA	$\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{IH}
	I_{DD2}			0.5	mA	$\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{DD}
Self-refresh current	I_{DD3}			(Note 1)	mA	$\overline{OE}$/$\overline{RFSH}$ = 0 V; $\overline{CE}$ = V_{DD}
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
I/O leakage current	$I_{O(L)}$	−10		10	μA	I/O = High-Z; V_{OUT} = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4		V_{DD}	V	I_{OH} = −1.0 mA
Output voltage, low	V_{OL}	0		0.4	V	I_{OL} = 2.0 mA

Notes:

(1) μPD42832C-12/-15: I_{DD3} = 1.5 mA max
μPD42832C-12L/-15L: I_{DD3} = 0.1 mA max
μPD42832GU-12L/-15L: I_{DD3} = 0.1 mA max

Capacitance

T_A = +25°C; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit
I/O capacitance	$C_{I/O}$			7	pF
Input capacitance	C_I			5	pF

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$/$\overline{RFSH}$	I/O Pins
Standby	High	X	High	High-Z
Refresh	High	X	Low	High-Z
Read	Low	High	Low	D_{OUT}
External refresh	Low	High	High	High-Z
Write	Low	Low	High	D_{IN}

AC Characteristics

T_A = 0 to +70°C; V_{DD} = 5.0 V ±10%

Parameter	Symbol	μPD42832-12 Min	μPD42832-12 Max	μPD42832-15 Min	μPD42832-15 Max	Unit	Test Conditions
Operating current	I_{DD1}		50		40	mA	(Note 1)
Refresh current	I_{DD4}		50		40	mA	(Note 2)
Pulse refresh current	I_{DD5}		50		40	mA	(Note 3)
Random read or write cycle time	t_{RC}	190		235		ns	
$\overline{CE}$ access time	t_{CEA}		120		150	ns	
Chip disable to output in high-Z	t_{CHZ}	0	35	0	40	ns	(Note 9)
$\overline{OE}$ access time	t_{OEA}		35		40	ns	
Output disable to output in high-Z	t_{OHZ}	0	35	0	40	ns	(Note 9
$\overline{CE}$ to output in low-Z	t_{CLZ}	10		10		ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5		5		ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	
$\overline{CE}$ precharge time	t_P	60		75		ns	
$\overline{CE}$ pulse width	t_{CE}	120	10000	150	10000	ns	
Address setup time before $\overline{CE}$ low	t_{ASC}	0		0		ns	
Address hold time after $\overline{CE}$ low	t_{AHC}	30		40		ns	
$\overline{OE}$ hold time after $\overline{CE}$ low	t_{OHC}	0		0		ns	
$\overline{OE}$ setup time before $\overline{CE}$ low	t_{OSC}	0		0		ns	
Read command setup time before $\overline{CE}$ low	t_{RCS}	0		0		ns	
Read command hold time after $\overline{CE}$ high	t_{RCH}	0		0		ns	
Write command hold time after $\overline{CE}$ low	t_{WCH}	85		105		ns	
Write command pulse width	t_{WP}	85		105		ns	
Write command to $\overline{CE}$ lead time	t_{CWL}	85		105		ns	
Data setup time before $\overline{WE}$ high	t_{DSW}	75		95		ns	
Data hold time after $\overline{WE}$ high	t_{DHW}	0		0		ns	
Data setup time before $\overline{CE}$ high	t_{DSC}	75		95		ns	
Data hold time after $\overline{CE}$ high	t_{DHC}	0		0		ns	
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	35	0	40	ns	(Note 9)
Output active from end of write	t_{WLZ}	5		5		ns	
Read/modify/write cycle time	t_{RWC}	295		365		ns	
$\overline{CE}$ to $\overline{RFSH}$ delay time	t_{RFD}	60		75		ns	
$\overline{RFSH}$ pulse width in pulse refresh	t_{FAP}1000	80	1000	80	1000	ns	
$\overline{RFSH}$ precharge time	t_{FP}	30		30		ns	
Pulse refresh cycle time	t_{FC}	190		235		ns	
$\overline{RFSH}$ to $\overline{CE}$ setup time after pulse refresh	t_{FCE}	225		275		ns	
$\overline{RFSH}$ to $\overline{CE}$ delay time after pulse refresh	t_{FSR}	25		30		ns	
$\overline{RFSH}$ pulse width in self-refresh	t_{FAS}	8000		8000		ns	
$\overline{RFSH}$ to $\overline{CE}$ delay after self-refresh	t_{FRS}	225		275		ns	
Refresh period	t_{REF}		4		4	ms	(Note 10)

Notes:

(1) $t_{RC} = t_{RC}$ (min); I_O = 0 mA.

(2) $t_{RC} = t_{RC}$ (min); $\overline{OE}/\overline{RFSH} = \overline{WE} = V_{IH}$.

Notes [cont]:

(3) $t_{FC} = t_{FC}$ (min); $\overline{CE} = V_{IH}$.

(4) All voltages are referenced to GND.

(5) Once V_{CC} is within specification (≥4.5 V), the μPD42832 is initialized by holding the $\overline{CE}$ and $\overline{OE}$ inputs inactive ($V_{IH} \geq 2.4$ V) for 1 ms or more.

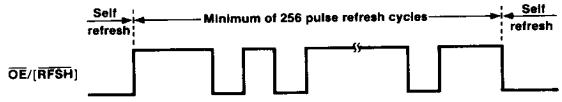
(6) For ac parameter measurements, assume $t_T = 5$ ns.

(7) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(8) Output load = 1 TTL load and 100 pF.

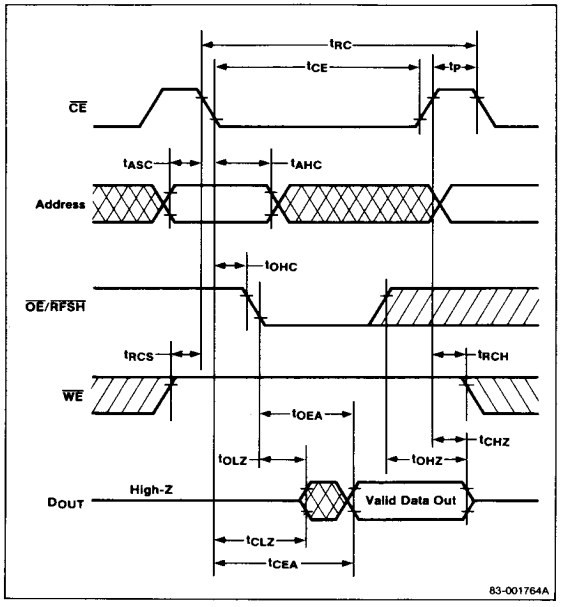
(9) t_{CHZ}, t_{OHZ} and t_{WHZ} define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(10) Pulse refresh cycles and self-refresh cycles use the same internal refresh address counter. Either type will increment the counter in proper sequence. However, external refresh addresses are independent of those generated by the internal counter. Therefore, when the μPD42832 is not in an extended period of self-refresh, the system design must guarantee that the refresh requirement is met by either the external refresh cycle type or the pulse refresh cycle type alone.

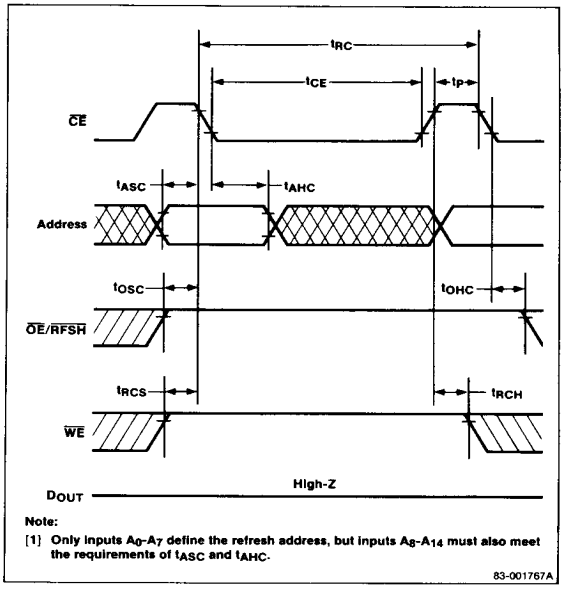


Timing Waveforms (cont)

Read Cycle



External Refresh Cycle



Note:
[1] Only inputs A_0-A_7 define the refresh address, but inputs A_8-A_{14} must also meet the requirements of t_{ASC} and t_{AHC}.

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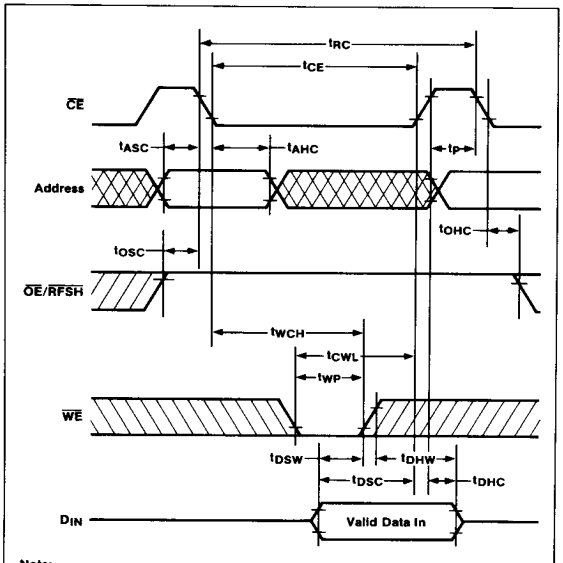
Write Cycle



Note:
[1] If the write cycle follows either a pulse refresh cycle or a self-refresh cycle, timing parameter t_{OSC} may be superseded by t_{FSR}, t_{FCE}, or t_{FRS}.

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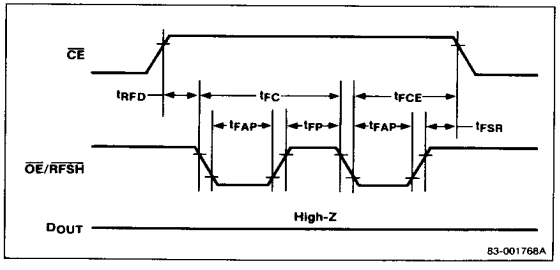
Pulse Refresh Cycle



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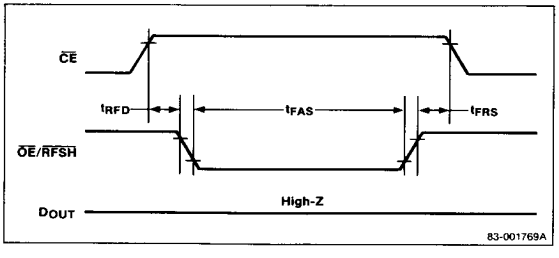
Self-Refresh Cycle



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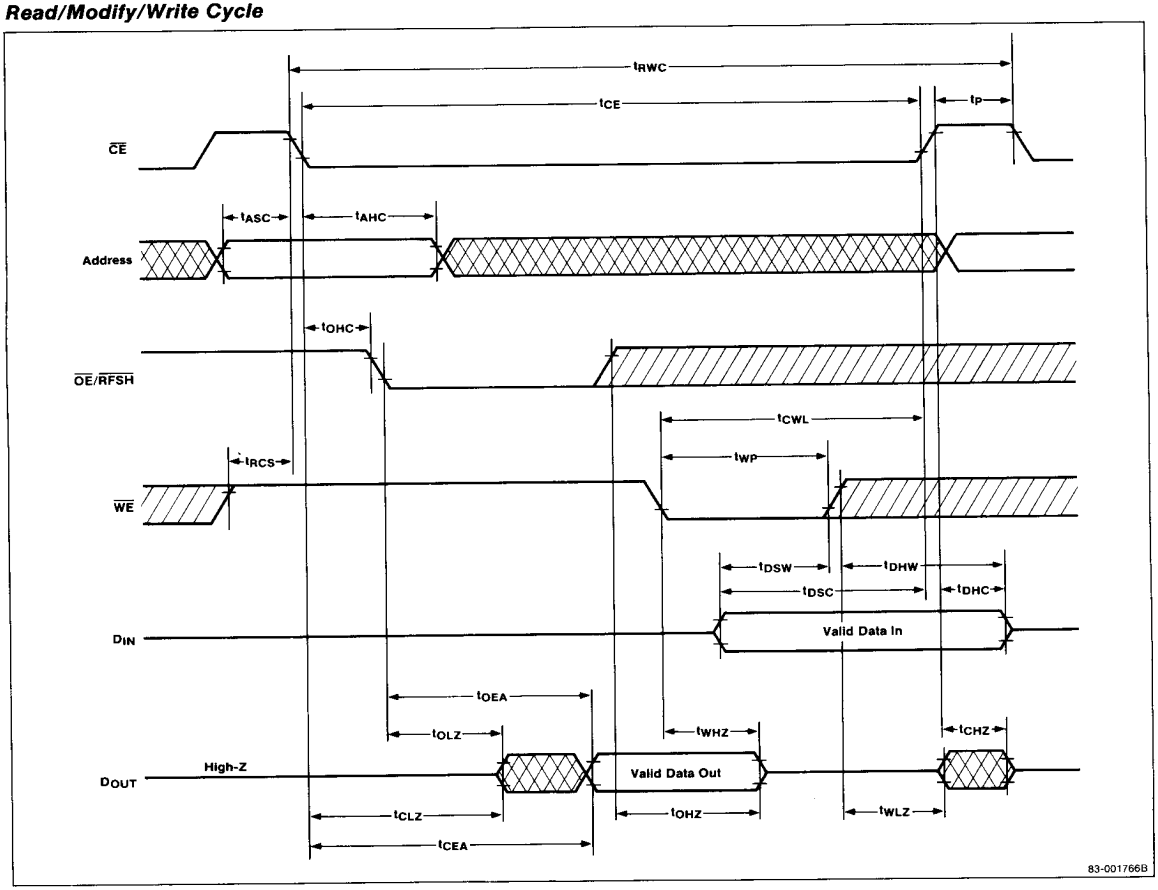
Timing Waveforms (cont)

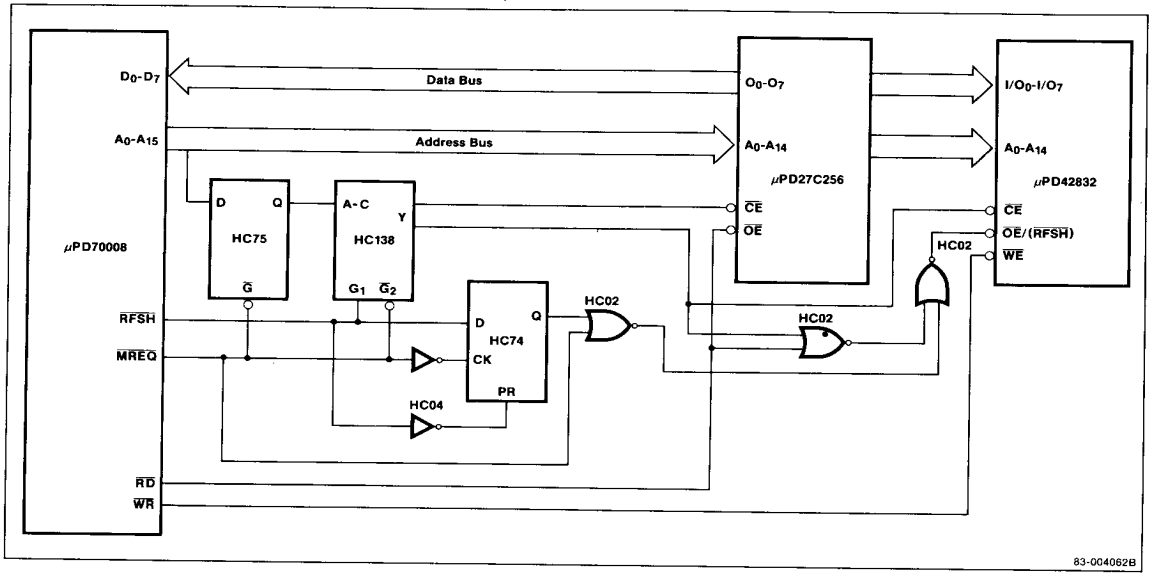
Read/Modify/Write Cycle



μPD42832 Application with the μPD70008 CPU

The μPD70008 is a general-purpose, 8-bit CPU designed and manufactured with the CMOS process. In particular, the μPD70008 is equipped with a standby mode that can significantly reduce power consumption. As shown in the example in figure 1, this application uses the $\overline{RFSH}$ refresh signal to perform a pulse refresh operation during the T_3 and T_4 states of the M1 cycle.

Figure 1. Application of the μPD42832 with the μPD70008 CPU



Package Drawings

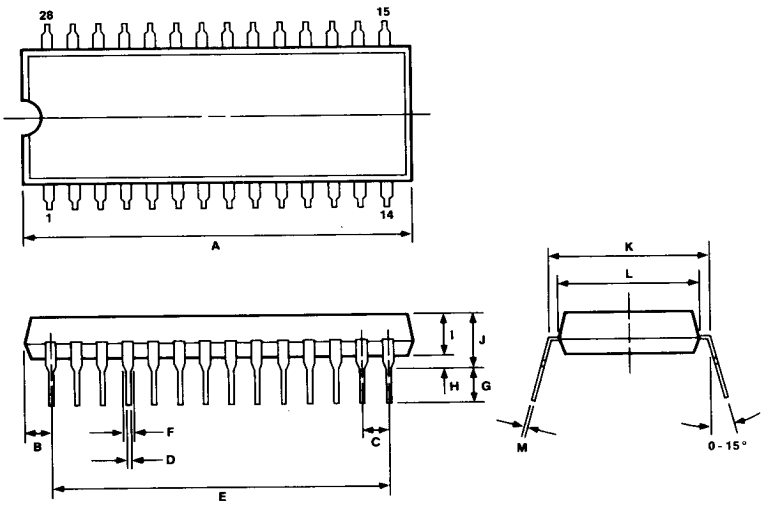
28-Pin Plastic DIP (600-mil)

Item	Millimeters	Inches
A	38.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	33.02	1.300
F	1.2 min	.047 min
G	3.6 ± .30	.142 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.20	.520
M	$.25^{+.10}_{-.05}$	$.010^{+.004}_{-.003}$

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



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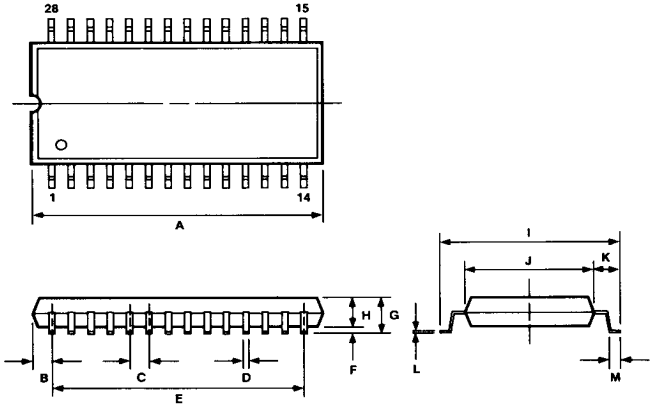
Package Drawings (cont)

28-Pin Plastic Miniflat

Item	Millimeters	Inches
A	19.05 max	.750 max
B	1.27 max	.050 max
C	1.27 [TP]	.050 [TP]
D	.40 ± .10	.016 $^{+.004}_{-.005}$
E	16.51	.650
F	.1 ± .1	.004 $^{+.005}_{-.004}$
G	3.0 max	.118 max
H	2.55	.100
I	11.8 ± .3	.465 $^{+.012}_{-.013}$
J	8.4	.331
K	1.7	.067
L	.15 $^{+.10}_{-.05}$	.006 $^{+.004}_{-.002}$
M	.7 ± .2	.028 $^{+.008}_{-.009}$

Notes:

[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.



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