

9984043 ZILOG INC

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**Z8430 Military  
Z80<sup>®</sup> CTC  
Counter/Timer Circuit**

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T-52-33-05

**Zilog**

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**Military  
Electrical  
Specification**

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July 1985

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**FEATURES**

- Four independently programmable counter/timer channels, each with a readable downcounter and a selectable 16 or 256 prescaler. Downcounters are reloaded automatically at zero count.
- Selectable positive or negative trigger initiates timer operation.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors.
- Interfaces directly to the Z80 CPU or—for baud rate generation—to the Z80 SIO.
- Standard Z80 Family daisy-chain interrupt structure provides fully vectored, prioritized interrupts without external logic. The CTC may also be used as an interrupt controller.

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**GENERAL DESCRIPTION**

The Z80 CTC four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

Programming the CTC is straightforward: each channel is programmed with two bytes; a third is necessary when interrupts are enabled. Once started, the CTC counts down, automatically reloads its time constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified; the CTC internally generates a unique vector for each channel.

The Z80 CTC requires a single +5V power supply and the standard Z80 single-phase system clock. It is fabricated with n-channel silicon-gate depletion-load technology, and packaged in a 28-pin DIP and a 44-pin chip carrier.

## TIMING

**Read Cycle Timing.** Figure 1 shows read cycle timing. This cycle reads the contents of a down-counter without disturbing the count. During clock cycle  $T_2$ , the Z80 CPU initiates a read cycle by driving the following inputs Low:  $\overline{RD}$ ,  $\overline{IORQ}$ , and  $\overline{CE}$ . A 2-bit binary code at inputs  $CS_1$  and  $CS_0$  selects the channel to be read.  $M1$  must be High to distinguish this cycle from an interrupt acknowledge.

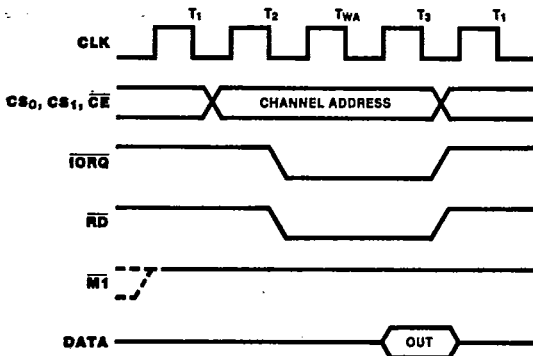


Figure 1. Read Cycle Timing

**Write Cycle Timing.** Figure 2 shows write cycle timing for loading control, time constant, or vector words.

The CTC does not have a write signal input, so it generates one internally when the read ( $\overline{RD}$ ) input is High during  $T_1$ . During  $T_2$   $\overline{IORQ}$  and  $\overline{CE}$  inputs are Low.  $M1$  must be High to distinguish a write cycle from an interrupt acknowledge. A 2-bit binary code at inputs  $CS_1$  and  $CS_0$  selects the channel to be addressed, and the word being written is placed on the Z80 data bus. The data word is latched into the appropriate register with the rising edge of clock cycle  $T_3$ .

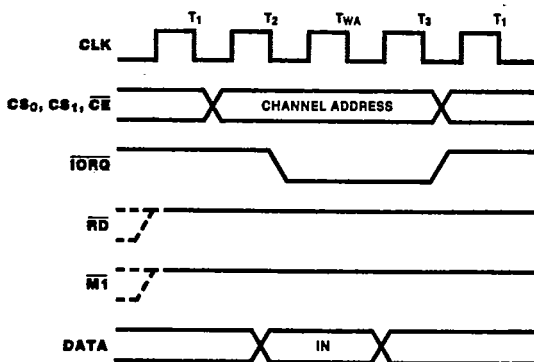


Figure 2. Write Cycle Timing

**Timer Operation.** In the timer mode, a CLK/TRG pulse input starts the timer (Figure 3) on the second succeeding rising edge of CLK. The trigger pulse is asynchronous, and it must have a minimum width. A minimum lead time (210 ns) is required between the active edge of the CLK/TRG and the next rising edge of CLK to enable the prescaler on the following clock edge. If the CLK/TRG edge occurs closer than this, the initiation of the timer function is delayed one clock cycle. This corresponds to the start-up timing discussed in the programming section. The timer can also be started automatically if so programmed by the channel control word.

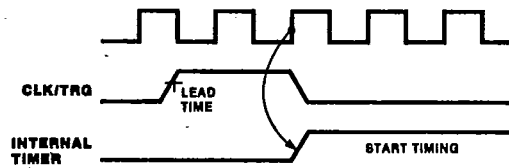


Figure 3. Timer Mode Timing

**Counter Operation.** In the counter mode, the CLK/TRG pulse input decrements the downcounter. The trigger is asynchronous, but the count is synchronized with CLK. For the decrement to occur on the next rising edge of CLK, the trigger edge must precede CLK by a minimum lead time as shown in Figure 4. If the lead time is less than specified, the count is delayed by one clock cycle. The trigger pulse must have a minimum width, and the trigger period must be at least twice the clock period. If the trigger repetition rate is faster than  $1/3$  the clock frequency, then  $T_{sCTR}(Cs)$ , AC Characteristics Specification 26, must be met.

The ZC/TO output occurs immediately after zero count, and follows the rising CLK edge.

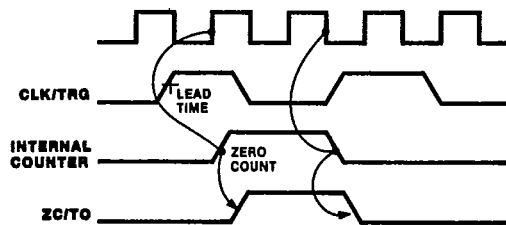


Figure 4. Counter Mode Timing

## INTERRUPT OPERATION

The Z80 CTC follows the Z80 system interrupt protocol for nested priority interrupts and return from interrupt, wherein the interrupt priority of a peripheral is determined by its location in a daisy chain. Two lines—IEI and IEO—in the CTC connect it to the system daisy chain. The device closest to the +5V supply has the highest priority (Figure 5). For additional information on the Z80 interrupt structure, refer to the *Z80 CPU Product Specification* and the *Z80 CPU Technical Manual*.

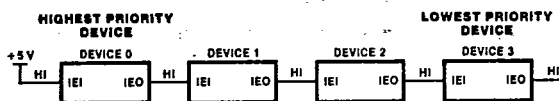


Figure 5. Daisy-Chain Interrupt Priorities

Within the Z80 CTC, interrupt priority is predetermined by channel number: Channel 0 has the highest priority, and Channel 3 the lowest. If a device or channel is being serviced with an interrupt routine, it cannot be interrupted by a device or channel with lower priority until service is complete. Higher priority devices or channels may interrupt the servicing of lower priority devices or channels.

A Z80 CTC channel may be programmed to request an interrupt every time its downcounter reaches zero. Note that the CPU must be programmed for interrupt mode 2. Some time after the interrupt request, the CPU sends an interrupt acknowledge. The CTC interrupt control logic determines the highest priority channel that is requesting an interrupt. Then, if the CTC IEI input is High (indicating that it has priority within the system daisy chain) it places an 8-bit

interrupt vector on the system data bus. The high-order five bits of this vector were written to the CTC during the programming process; the next two bits are provided by the CTC interrupt control logic as a binary code that identifies the highest priority channel requesting an interrupt; the low-order bit is always zero.

**Interrupt Acknowledge Timing.** Figure 6 shows interrupt acknowledge timing. After an interrupt request, the Z80 CPU sends an interrupt acknowledge (M1 and IORQ). All channels are inhibited from changing their interrupt request status when M1 is active—about two clock cycles earlier than IORQ. RD is High to distinguish this cycle from an instruction fetch.

The CTC interrupt logic determines the highest priority channel requesting an interrupt. If the CTC interrupt enable input (IEI) is High, the highest priority interrupting channel within the CTC places its interrupt vector on the data bus when IORQ goes Low. Two wait states (Twa) are automatically inserted at this time to allow the daisy chain to stabilize. Additional wait states may be added.

**Return from Interrupt Timing.** At the end of an interrupt service routine the RETI (Return From Interrupt) instruction initializes the daisy chain enable lines for proper control of nested priority interrupt handling. The CTC decodes the 2-byte RETI code internally and determines whether it is intended for a channel being serviced. Figure 7 shows RETI timing.

If several Z80 peripherals are in the daisy chain, IEI settles active (High) on the chip currently being serviced when the opcode ED16 is decoded. If the following opcode is 4D16, the peripheral being serviced is released and its IEO becomes active. Additional wait states are allowed.

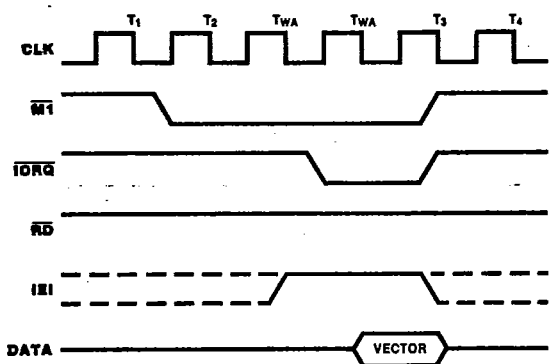


Figure 6. Interrupt Acknowledge Timing

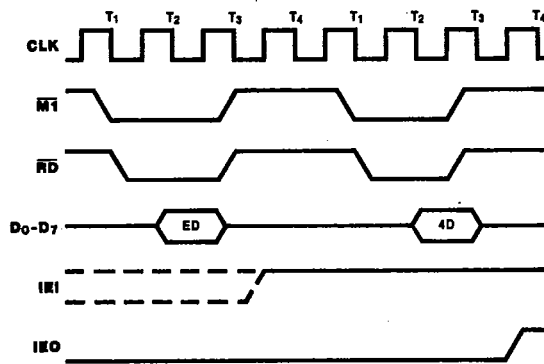


Figure 7. Return From Interrupt Timing

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**ABSOLUTE MAXIMUM RATINGS**

Guaranteed by characterization/design.

Voltages on all pins with respect

to ground. . . . . -0.3V to +7V

Operating Case Temperature. . . See Ordering Information

Storage Temperature Range . . . . . -65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**STANDARD TEST CONDITIONS**

The DC Characteristics and Capacitance sections listed below apply for the following standard test conditions, unless otherwise noted.

Military Operating Temperature Range ( $T_C$ )

-55°C to +125°C

Standard Military Test Condition

+4.5V  $\leq$   $V_{CC}$   $\leq$  +5.5V

All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

All AC parameters assume a load capacitance of 100 pf. AC output timing measurements are referenced to 1.5 volts.

**DC CHARACTERISTICS**

| Symbol    | Parameter                               | Min               | Max                | Unit    | Condition                                 |
|-----------|-----------------------------------------|-------------------|--------------------|---------|-------------------------------------------|
| $V_{ILC}$ | Clock Input Low Voltage                 | -0.3 <sup>c</sup> | +0.45 <sup>a</sup> | V       |                                           |
| $V_{IHC}$ | Clock Input High Voltage                | $V_{CC} - 0.6^a$  | $V_{CC} + 0.3^b$   | V       |                                           |
| $V_{IL}$  | Input Low Voltage                       | -0.3 <sup>c</sup> | +0.8 <sup>a</sup>  | V       |                                           |
| $V_{IH}$  | Input High Voltage                      | +2.2 <sup>a</sup> | $V_{CC}^b$         | V       |                                           |
| $V_{OL}$  | Output Low Voltage                      |                   | +0.4 <sup>a</sup>  | V       | $I_{OL} = 2.0$ mA                         |
| $V_{OH}$  | Output High Voltage                     | +2.4 <sup>a</sup> |                    | V       | $I_{OH} = -250$ $\mu$ A                   |
| $I_{CC}$  | Power Supply Current:                   |                   | +120 <sup>a</sup>  | mA      |                                           |
| $I_{LI}$  | Input Leakage Current                   |                   | $\pm 10^a$         | $\mu$ A | $V_{IN} = 0.4$ to $V_{CC}$                |
| $I_{LO}$  | 3-State Output Leakage Current in Float |                   | $\pm 10^a$         | $\mu$ A | $V_{OUT} = 0.4$ to $V_{CC}$               |
| $I_{OHD}$ | Darlington Drive Current                | -1.5 <sup>a</sup> |                    | mA      | $V_{OH} = 1.5$ V<br>$R_{EXT} = 390\Omega$ |

**CAPACITANCE**

| Symbol    | Parameter          | Max             | Unit |
|-----------|--------------------|-----------------|------|
| CLK       | Clock Capacitance  | 20 <sup>c</sup> | pf   |
| $C_{IN}$  | Input Capacitance  | 5 <sup>c</sup>  | pf   |
| $C_{OUT}$ | Output Capacitance | 15 <sup>c</sup> | pf   |

 $T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz

Unmeasured pins returned to ground.

Parameter Test Status:

a Tested

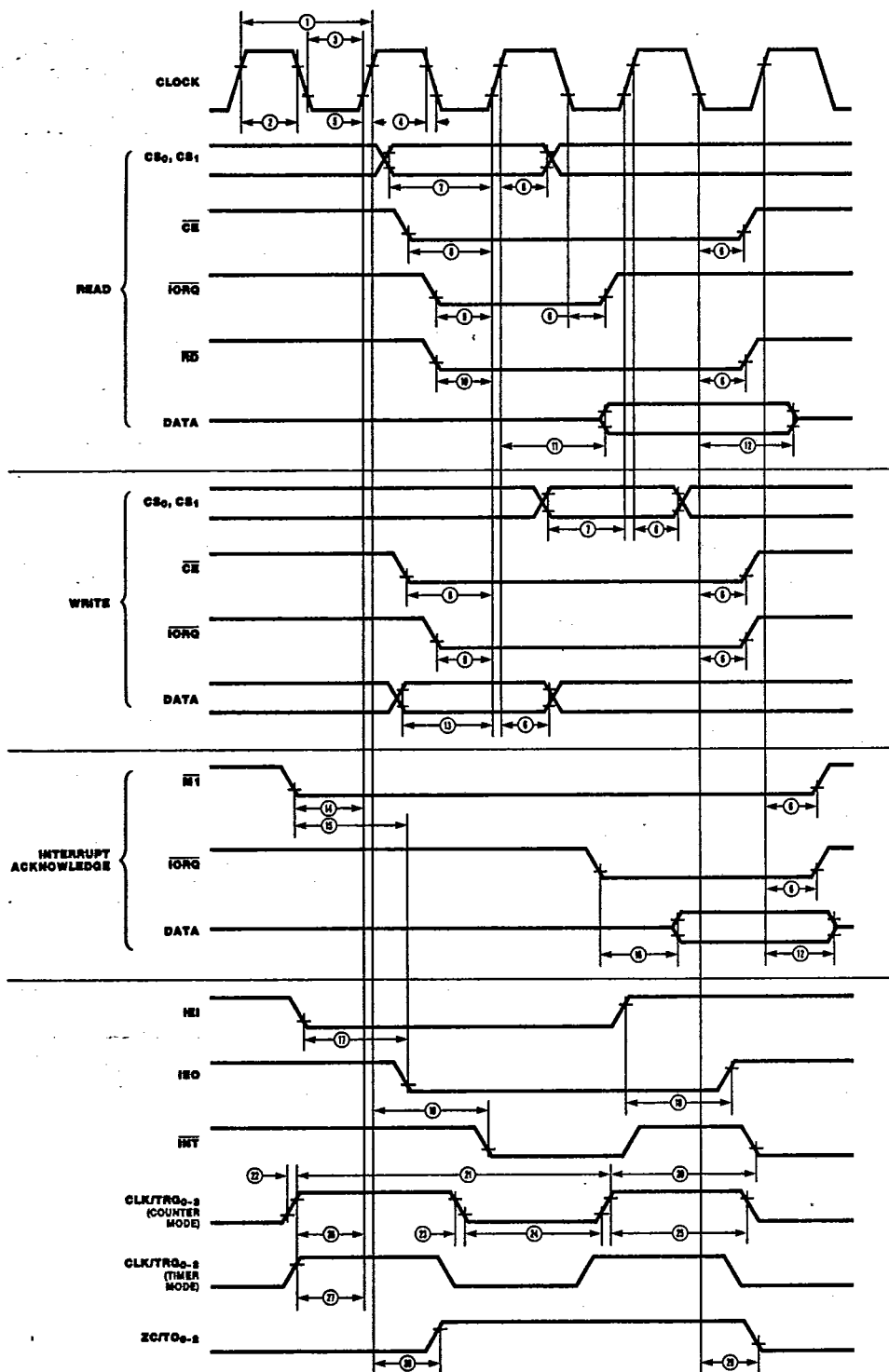
b Guaranteed

c Guaranteed by characterization/design

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## AC CHARACTERISTICS

| Number | Symbol      | Parameter                                                | Z80 CTC           |                                | Z80A CTC          |                                | Notes† |
|--------|-------------|----------------------------------------------------------|-------------------|--------------------------------|-------------------|--------------------------------|--------|
|        |             |                                                          | Min               | Max                            | Min               | Max                            |        |
| 1      | TcC         | Clock Cycle Time                                         | 400 <sup>a</sup>  | [1] <sup>d</sup>               | 250 <sup>a</sup>  | [1] <sup>d</sup>               |        |
| 2      | TwCh        | Clock Width (High)                                       | 170 <sup>b</sup>  | 1000 <sup>a</sup>              | 105 <sup>a</sup>  | 1000 <sup>a</sup>              |        |
| 3      | TwCl        | Clock Width (Low)                                        | 170 <sup>b</sup>  | 1000 <sup>a</sup>              | 105 <sup>a</sup>  | 1000 <sup>a</sup>              |        |
| 4      | TfC         | Clock Fall Time                                          |                   | 30 <sup>b</sup>                |                   | 30 <sup>b</sup>                |        |
| 5      | TrC         | Clock Rise Time                                          |                   | 30 <sup>b</sup>                |                   | 30 <sup>b</sup>                |        |
| 6      | Th          | All Hold Times                                           | 0 <sup>b</sup>    |                                | 0 <sup>b</sup>    |                                |        |
| 7      | TsCS(C)     | CS to Clock ↑ Setup Time                                 | 250 <sup>b</sup>  |                                | 160 <sup>b</sup>  |                                |        |
| 8      | TsCE(C)     | CE to Clock ↑ Setup Time                                 | 200 <sup>a</sup>  |                                | 150 <sup>a</sup>  |                                |        |
| 9      | TsIO(C)     | TORQ ↓ to Clock ↑ Setup Time                             | 250 <sup>b</sup>  |                                | 115 <sup>b</sup>  |                                |        |
| 10     | TsRD(C)     | RD ↓ to Clock ↑ Setup Time                               | 240 <sup>b</sup>  |                                | 115 <sup>b</sup>  |                                |        |
| 11     | TdC(DO)     | Clock ↑ to Data Out Delay                                |                   | 240 <sup>a</sup>               |                   | 200 <sup>a</sup>               | [2]    |
| 12     | TdC(DOz)    | Clock ↑ to Data Out Float Delay                          |                   | 230 <sup>b</sup>               |                   | 110 <sup>b</sup>               |        |
| 13     | TsDI(C)     | Data In to Clock ↑ Setup Time                            | 60 <sup>a</sup>   |                                | 50 <sup>a</sup>   |                                |        |
| 14     | TsM1(C)     | MT to Clock ↑ Setup Time                                 | 210 <sup>b</sup>  |                                | 90 <sup>b</sup>   |                                |        |
| 15     | TdM1(IEO)   | MT ↓ to IEO ↑ Delay (Interrupt immediately preceding M1) |                   | 300 <sup>b</sup>               |                   | 190 <sup>b</sup>               | [3]    |
| 16     | TdIO(DOI)   | TORQ ↓ to Data Out Delay (INTA Cycle)                    |                   | 340 <sup>b</sup>               |                   | 160 <sup>b</sup>               | [2]    |
| 17     | TdIEI(IEOf) | IEI ↓ to IEO ↓ Delay                                     |                   | 190 <sup>b</sup>               |                   | 130 <sup>b</sup>               | [3]    |
| 18     | TdIEI(IEOr) | IEI ↑ to IEO ↑ Delay (After ED Decode)                   |                   | 220 <sup>a</sup>               |                   | 160 <sup>a</sup>               | [3]    |
| 19     | TdC(INT)    | Clock ↑ to INT ↑ Delay                                   |                   | (1) + 200 <sup>d</sup>         |                   | (1) + 160 <sup>d</sup>         | [4,6]  |
| 20     | TdCLK(INT)  | CLK/TRG ↑ to INT ↓                                       |                   | (19) + (26) <sup>d</sup>       |                   | (19) + (26) <sup>d</sup>       | [5,6]  |
|        |             | tsCTR(C) satisfied                                       |                   | (1) + (19) + (26) <sup>d</sup> |                   | (1) + (19) + (26) <sup>d</sup> | [5,6]  |
|        |             | tsCTR(C) not satisfied                                   |                   |                                |                   |                                |        |
| 21     | TcCTR       | CLK/TRG Cycle Time                                       | 2TcC <sup>a</sup> |                                | 2TcC <sup>a</sup> |                                | [5]    |
| 22     | TrCTR       | CLK/TRG Rise Time                                        |                   | 50 <sup>b</sup>                |                   | 50 <sup>b</sup>                |        |
| 23     | TfCTR       | CLK/TRG Fall Time                                        |                   | 50 <sup>b</sup>                |                   | 50 <sup>b</sup>                |        |
| 24     | TwCTRI      | CLK/TRG Width (Low)                                      | 200 <sup>b</sup>  |                                | 200 <sup>b</sup>  |                                |        |
| 25     | TwCTRh      | CLK/TRG Width (High)                                     | 200 <sup>b</sup>  |                                | 200 <sup>b</sup>  |                                |        |

## NOTES:

- [1]  $TcC = TwCh + TwCl + TrC + TfC$ .  
 [2] Increase delay by 10 ns for each 50 pf increase in loading, 200 pf maximum for data lines, and 100 pf for control lines.  
 [3] Increase delay by 2 ns for each 10 pf increase in loading, 100 pf maximum.  
 [4] Timer mode.  
 [5] Counter mode.  
 [6] Parenthetical numbers reference the table number of a parameter, e.g., (1) refers to TcC.

†  $2.5 TcC > (n-2) TdIEI(IEOf) + TdM1(IEO) + TsIEI(IEO) + TTL$  buffer delay, if any. RESET must be active for a minimum of 3 clock cycles. Units are nanoseconds unless otherwise specified.

## Parameter Test Status:

- a Tested  
 b Guaranteed  
 c Guaranteed by characterization/design  
 d Calculated parameter—not directly tested

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**AC CHARACTERISTICS** (Continued)

| Number | Symbol     | Parameter                                                                            | Z80 CTC          |                  | Z80A CTC         |                  | Notes† |
|--------|------------|--------------------------------------------------------------------------------------|------------------|------------------|------------------|------------------|--------|
|        |            |                                                                                      | Min              | Max              | Min              | Max              |        |
| 26     | TsCTR(Cs)  | CLK/TRG ↑ to Clock ↑ Setup<br>Time for Immediate Count                               | 300 <sup>a</sup> |                  | 210 <sup>a</sup> |                  | [5]    |
| 27     | TsCTR(Ct)  | CLK/TRG ↑ to Clock ↑ Setup<br>Time for enabling of Prescaler<br>on following clock ↑ | 300 <sup>a</sup> |                  | 210 <sup>a</sup> |                  | [4]    |
| 28     | TdC(ZC/TO) | Clock ↑ to ZC/TO ↑ Delay                                                             |                  | 260 <sup>a</sup> |                  | 190 <sup>a</sup> |        |
| 29     | TdC(ZC/TO) | Clock ↓ to ZC/TO ↓ Delay                                                             |                  | 190 <sup>a</sup> |                  | 190 <sup>a</sup> |        |

## NOTES:

[1]  $T_{oC} = T_{wCh} + T_{wCl} + T_{rC} + T_{fC}$ .

[2] Increase delay by 10 ns for each 50 pf increase in loading, 200 pf maximum for data lines, and 100 pf for control lines.

[3] Increase delay by 2 ns for each 10 pf increase in loading, 100 pf maximum.

[4] Timer mode.

[5] Counter mode.

[6] Parenthetical numbers reference the table number of a parameter, e.g., (1) refers to  $T_{oC}$ .

†  $2.5 T_{oC} > (n-2) T_{DIE(I/O)} + T_{DM1(I/O)} + T_{sEI(I/O)} + T_{TL}$  buffer delay, if any. RESET must be active for a minimum of 3 clock cycles. Units are nanoseconds unless otherwise specified.

## Parameter Test Status:

- a Tested
- b Guaranteed
- c Guaranteed by characterization/design
- d Calculated parameter—not directly tested

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**PIN DESCRIPTION**

**$\overline{CE}$ .** *Chip Enable* (input, active Low). When enabled the CTC accepts control words, interrupt vectors, or time constant data words from the data bus during an I/O write cycle; or transmits the contents of the downcounter to the CPU during an I/O read cycle. In most applications this signal is decoded from the eight least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four counter-timer channels.

**CLK.** *System Clock* (input). Standard single-phase Z80 system clock.

**CLK/TRG<sub>0</sub>/CLK/TRG<sub>3</sub>.** *External Clock/Timer Trigger* (input, user-selectable active High or Low). Four pins corresponding to the four Z80 CTC channels. In counter mode, every active edge on this pin decrements the downcounter. In timer mode, an active edge starts the timer.

**CS<sub>0</sub>/CS<sub>1</sub>.** *Channel Select* (inputs active High). Two-bit binary address code selects one of the four CTC channels for an I/O write or read (usually connected to A<sub>0</sub> and A<sub>1</sub>).

**D<sub>0</sub>-D<sub>7</sub>.** *System Data Bus* (bidirectional, 3-state). Transfers all data and commands between the Z80 CPU and the Z80 CTC.

**IEI.** *Interrupt Enable In* (input, active High). A High indicates that no other interrupting devices of higher priority in the daisy chain are being serviced by the Z80 CPU.

**IEO.** *Interrupt Enable Out* (output, active High). High only if IEI is High and the Z80 CPU is not servicing an interrupt from any Z80 CTC channel. IEO blocks lower priority devices from interrupting while a higher priority interrupting device is being serviced.

**INT.** *Interrupt Request* (output, open drain, active Low). Low when any Z80 CTC channel that has been

programmed to enable interrupts as a zero-count condition in its downcounter.

**$\overline{IORQ}$ .** *Input/Output Request* (input from CPU, active Low). Used with  $\overline{CE}$  and  $\overline{RD}$  to transfer data and channel control words between the Z80 CPU and the Z80 CTC. During a write cycle,  $\overline{IORQ}$  and  $\overline{CE}$  are active and  $\overline{RD}$  inactive. The Z80 CTC does not receive a specific write signal; rather, it internally generates its own from the inverse of an active  $\overline{RD}$  signal. In a read cycle,  $\overline{IORQ}$ ,  $\overline{CE}$ , and  $\overline{RD}$  are active; the contents of the downcounter are read by the Z80 CPU. If  $\overline{IORQ}$  and M1 are both true, the CPU is acknowledging an interrupt request, and the highest priority interrupting channel places its interrupt vector on the Z80 data bus.

**M1.** *Machine Cycle One* (input from CPU, active Low). When M1 and  $\overline{IORQ}$  are active, the Z80 CPU is acknowledging an interrupt. The Z80 CTC then places an interrupt vector on the data bus if it has highest priority, and if a channel has requested an interrupt (INT).

**$\overline{RD}$ .** *Read Cycle Status* (input, active Low). Used in conjunction with  $\overline{IORQ}$  and  $\overline{CE}$  to transfer data and channel control words between the Z80 CPU and the Z80 CTC.

**RESET.** *Reset* (input active Low). Terminates all downcounts and disables all interrupts by resetting the interrupt bits in all control registers; the ZC/TO and the interrupt outputs go inactive; IEO reflects IEI; D<sub>0</sub>-D<sub>7</sub> go to the high-impedance state.

**ZC/TO<sub>0</sub>-ZC/TO<sub>2</sub>.** *Zero Count/Timeout* (output, active High). Three ZC/TO pins corresponding to Z80 CTC channels 2 through 0 (Channel 3 has no ZC/TO pin). In both counter and timer modes the output is an active High pulse when the downcounter decrements to zero.



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# PACKAGE PINOUTS

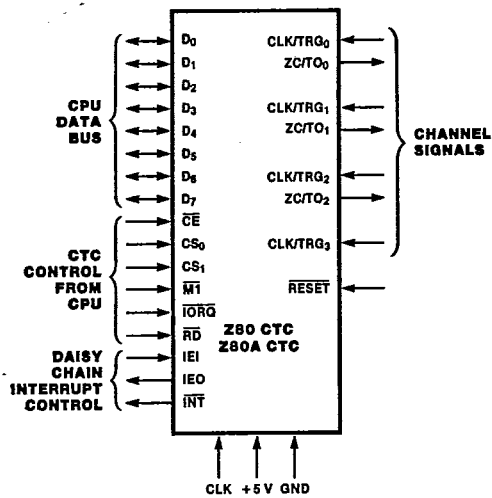


Figure 8. Pin Functions

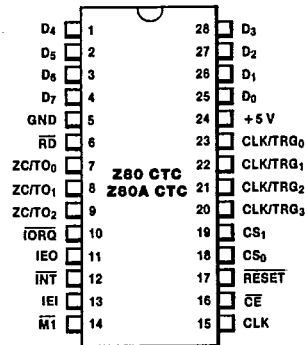


Figure 9a. 28-pin Dual-In-Line Package (DIP), Pin Assignments

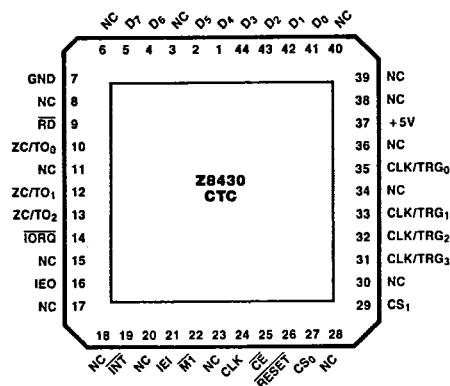


Figure 9b. 44-pin Chip Carrier, Pin Assignments

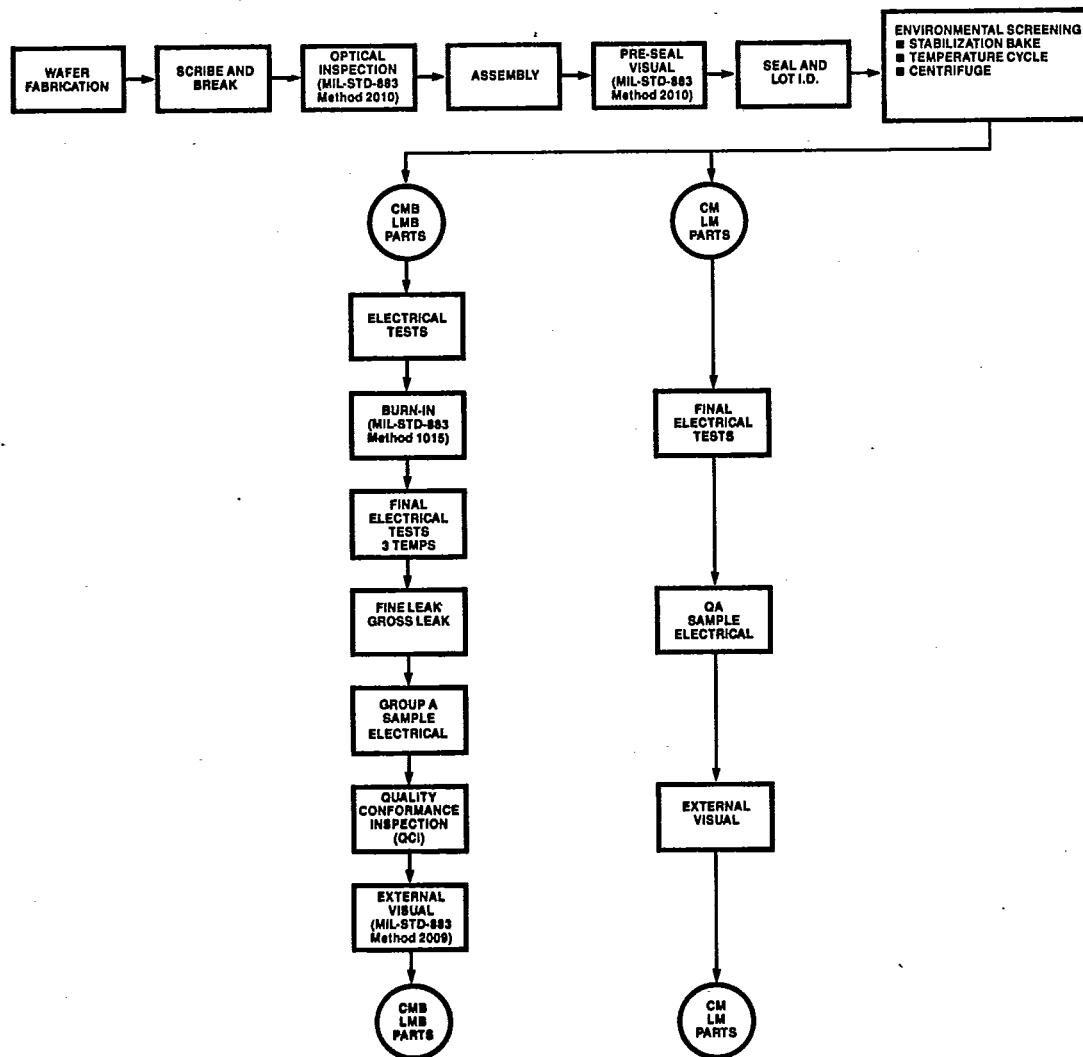
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**MIL-STD-883 MILITARY PROCESSED PRODUCT**

- Mil-Std-883 establishes uniform methods and procedures for testing microelectronic devices to insure the electrical, mechanical, and environmental integrity and reliability that is required for military applications.
- Mil-Std-883 Class B is the industry standard product assurance level for military ground and aircraft application.
- The total reliability of a system depends upon tests that are designed to stress specific quality and reliability concerns that affect microelectronic products.
- The following tables detail the 100% screening and electrical tests, sample electrical tests, and Qualification/Quality Conformance testing required.

**Zilog Military Product Flow**

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**Table I**  
**MIL-STD-883 Class B Screening Requirements**  
**Method 5004**

| Test                                 | Mil-Std-883 Method    | Test Condition                                                                                                                         | Requirement |
|--------------------------------------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Internal Visual                      | 2010                  | Condition B                                                                                                                            | 100%        |
| Stabilization Bake                   | 1008                  | Condition C                                                                                                                            | 100%        |
| Temperature Cycle                    | 1010                  | Condition C                                                                                                                            | 100%        |
| Constant Acceleration (Centrifuge)   | 2001                  | Condition E or D(Note 1), Y <sub>1</sub> Axis Only                                                                                     | 100%        |
| Initial Electrical Tests             |                       | Zilog Military Electrical Specification<br>Static/DC T <sub>C</sub> = +25°C                                                            | 100%        |
| Burn-In                              | 1015                  | Condition D(Note 2), 160 hours,<br>T <sub>A</sub> = +125°C                                                                             | 100%        |
| Interim Electrical Tests             |                       | Zilog Military Electrical Specification<br>Static/DC T <sub>C</sub> = +25°C                                                            | 100%        |
| PDA Calculation                      |                       | PDA = 5%                                                                                                                               | 100%        |
| Final Electrical Tests               |                       | Zilog Military Electrical Specification<br>Static/DC T <sub>C</sub> = +125°C, -55°C<br>Functional, Switching/AC T <sub>C</sub> = +25°C | 100%        |
| Fine Leak                            | 1014                  | Condition A <sub>2</sub>                                                                                                               | 100%        |
| Gross Leak                           | 1014                  | Condition C                                                                                                                            | 100%        |
| Quality Conformance Inspection (QCI) |                       |                                                                                                                                        |             |
| Group A                              | Each Inspection Lot   | 5005 (See Table II)                                                                                                                    | Sample      |
| Group B                              | Every Week            | 5005 (See Table III)                                                                                                                   | Sample      |
| Group C                              | Periodically (Note 3) | 5005 (See Table IV)                                                                                                                    | Sample      |
| Group D                              | Periodically (Note 3) | 5005 (See Table V)                                                                                                                     | Sample      |
| External Visual                      | 2009                  |                                                                                                                                        | 100%        |
| QA—Ship                              |                       |                                                                                                                                        | 100%        |

**NOTES:**

1. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
2. In process of fully implementing of Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
3. Performed periodically as required by Mil-Std-883, paragraph 1.2.1 b(17).

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**Table II Group A**  
**Sample Electrical Tests**  
**MIL-STD-883 Method 5005**

| Subgroup    | Tests        | Temperature (T <sub>c</sub> ) | LTPD<br>Max Accept = 2 |
|-------------|--------------|-------------------------------|------------------------|
| Subgroup 1  | Static/DC    | +25°C                         | 2                      |
| Subgroup 2  | Static/DC    | +125°C                        | 3                      |
| Subgroup 3  | Static/DC    | -55°C                         | 5                      |
| Subgroup 7  | Functional   | +25°C                         | 2                      |
| Subgroup 8  | Functional   | -55°C and +125°C              | 5                      |
| Subgroup 9  | Switching/AC | +25°C                         | 2                      |
| Subgroup 10 | Switching/AC | +125°C                        | 3                      |
| Subgroup 11 | Switching/AC | -55°C                         | 5                      |

## NOTES:

- The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail electrical specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.
- A single sample may be used for all subgroup testing. Where required size exceeds the lot size, 100% inspection shall be allowed.
- Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.

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**Table III Group B**  
**Sample Test Performed Every Week to**  
**Test Construction and Insure Integrity of Assembly Process.**  
**MIL-STD-883 Method 5005**

| Subgroup                                                              | MIL-Std-883<br>Method | Test Condition                                                                                                                                                                                   | Quantity or<br>LTPD/Max Accept |
|-----------------------------------------------------------------------|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|
| <b>Subgroup 1</b><br>Physical Dimensions                              | 2016                  |                                                                                                                                                                                                  | 2/0                            |
| <b>Subgroup 2</b><br>Resistance to Solvents                           | 2015                  |                                                                                                                                                                                                  | 4/0                            |
| <b>Subgroup 3</b><br>Solderability                                    | 2003                  | Solder Temperature<br>+ 245°C ± 5°C                                                                                                                                                              | 15(Note 1)                     |
| <b>Subgroup 4</b><br>Internal Visual and Mechanical                   | 2014                  |                                                                                                                                                                                                  | 1/0                            |
| <b>Subgroup 5</b><br>Bond Strength                                    | 2011                  | C                                                                                                                                                                                                | 15(Note 2)                     |
| <b>Subgroup 6</b> (Note 3)<br>Internal Water Vapor Content            | 1018                  | 1000 ppm.<br>maximum at + 100°C                                                                                                                                                                  | 3/0 or 5/1                     |
| <b>Subgroup 7</b> (Note 4)<br>Seal<br>7a) Fine Leak<br>7b) Gross Leak | 1014                  | 7a) A <sub>2</sub><br>7b) C                                                                                                                                                                      | 5                              |
| <b>Subgroup 8</b> (Note 5)<br>Electrostatic Discharge Sensitivity     | 3015                  | Zilog Military Electrical<br>Specification<br>Static/DC T <sub>C</sub> = + 25°C<br>A = 20-2000V<br>B = >2000V<br>Zilog Military Electrical<br>Specification<br>Static/DC T <sub>C</sub> = + 25°C | 15/0                           |

## NOTES:

1. Number of leads inspected selected from a minimum of 3 devices.
2. Number of bond pulls selected from a minimum of 4 devices.
3. Test applicable only if the package contains a dessicant.
4. Test not required if either 100% or sample seal test is performed between final electrical tests and external visual during Class B screening.
5. Test required for initial qualification and product redesign.

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**Table IV Group C**  
**Sample Test Performed Periodically to Verify Integrity of the Die.**  
**MIL-STD-883 Method 5005**

| Subgroup                           | Mil-Std-883 Method | Test Condition                                                                   | Quantity or LTPD/Max Accept |
|------------------------------------|--------------------|----------------------------------------------------------------------------------|-----------------------------|
| <b>Subgroup 1</b>                  |                    |                                                                                  |                             |
| Steady State Operating Life        | 1005               | Condition D <sup>(Note 1)</sup> , 1000 hours at +125°C                           | 5                           |
| End Point Electrical Tests         |                    | Zilog Military Electrical Specification<br>T <sub>C</sub> = +25°C, +125°C, -55°C |                             |
| <b>Subgroup 2</b>                  |                    |                                                                                  |                             |
| Temperature Cycle                  | 1010               | Condition C                                                                      |                             |
| Constant Acceleration (Centrifuge) | 2001               | Condition E or D <sup>(Note 2)</sup> , Y <sub>1</sub> Axis Only                  |                             |
| Seal                               | 1014               |                                                                                  | 15                          |
| 2a) Fine Leak                      |                    | 2a) Condition A <sub>2</sub>                                                     |                             |
| 2b) Gross Leak                     |                    | 2b) Condition C                                                                  |                             |
| Visual Examination                 | 1010 or 1011       |                                                                                  |                             |
| End Point Electrical Tests         |                    | Zilog Military Electrical Specification<br>T <sub>C</sub> = +25°C, +125°C, -55°C |                             |

**NOTE:**

1. In process of fully implementing Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.

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**Table V Group D**  
**Sample Test Performed Periodically to Insure Integrity of the Package.**  
**MIL-STD-883 Method 5005**

| Subgroup                                                         | MIL-Std-883 Method | Test Condition                                                                   | Quantity or LTPD/Max Accept |
|------------------------------------------------------------------|--------------------|----------------------------------------------------------------------------------|-----------------------------|
| <b>Subgroup 1</b><br>Physical Dimensions                         | 2016               |                                                                                  | 15                          |
| <b>Subgroup 2</b><br>Lead Integrity                              | 2004               | Condition B <sub>2</sub> or D <sup>(Note 1)</sup>                                | 15                          |
| <b>Subgroup 3</b><br>Thermal Shock                               | 1011               | Condition B minimum,<br>15 cycles minimum                                        | 15                          |
| Temperature Cycling                                              | 1010               | Condition C, 100 cycles minimum                                                  |                             |
| Moisture Resistance                                              | 1004               |                                                                                  |                             |
| Seal                                                             | 1014               |                                                                                  |                             |
| 3a) Fine Leak                                                    |                    | 3a) Condition A <sub>2</sub>                                                     |                             |
| 3b) Gross Leak                                                   |                    | 3b) Condition C                                                                  |                             |
| Visual Examination                                               | 1004 or 1010       |                                                                                  |                             |
| End Point Electrical Tests                                       |                    | Zilog Military Electrical Specification<br>T <sub>C</sub> = +25°C, +125°C, -55°C |                             |
| <b>Subgroup 4</b><br>Mechanical Shock                            | 2002               | Condition B minimum                                                              | 15                          |
| Vibration Variable Frequency                                     | 2007               | Condition A minimum                                                              |                             |
| Constant Acceleration (Centrifuge)                               | 2001               | Condition E or D <sup>(Note 2)</sup> , Y <sub>1</sub> Axis Only                  |                             |
| Seal                                                             | 1014               |                                                                                  |                             |
| 4a) Fine Leak                                                    |                    | 4a) Condition A <sub>2</sub>                                                     |                             |
| 4b) Gross Leak                                                   |                    | 4b) Condition C                                                                  |                             |
| Visual Examination                                               | 1010 or 1011       |                                                                                  |                             |
| End Point Electrical Tests                                       |                    | Zilog Military Electrical Specification<br>T <sub>C</sub> = +25°C, +125°C, -55°C |                             |
| <b>Subgroup 5</b><br>Salt Atmosphere                             | 1009               | Condition A minimum                                                              | 15                          |
| Seal                                                             | 1014               |                                                                                  |                             |
| 5a) Fine Leak                                                    |                    | 5a) Condition A <sub>2</sub>                                                     |                             |
| 5b) Gross Leak                                                   |                    | 5b) Condition C                                                                  |                             |
| Visual Examination                                               | 1009               |                                                                                  |                             |
| <b>Subgroup 6</b><br>Internal Water Vapor Content                | 1018               | 5,000 ppm. maximum water<br>content at +100°C                                    | 3/0 or 5/1                  |
| <b>Subgroup 7</b> <sup>(Note 3)</sup><br>Adhesion of Lead Finish | 2025               |                                                                                  | 15 <sup>(Note 4)</sup>      |
| <b>Subgroup 8</b> <sup>(Note 5)</sup><br>Lid Torque              | 2024               |                                                                                  | 5/0                         |

## NOTES:

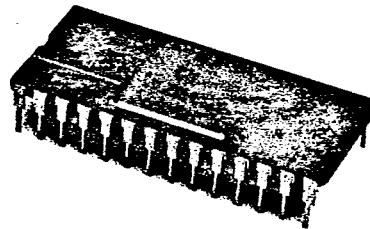
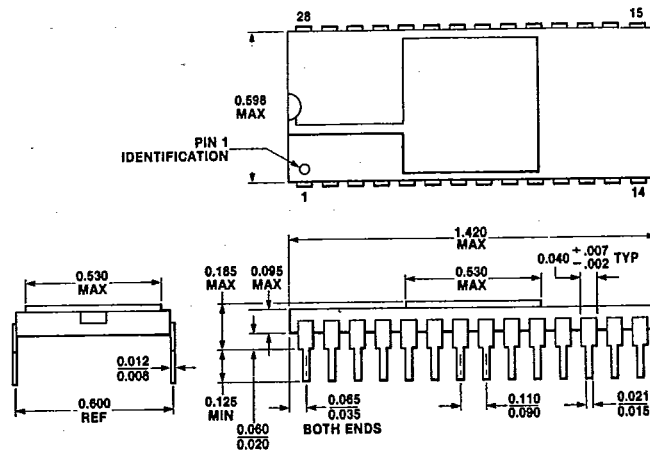
1. Lead Integrity Condition D for leadless chip carriers.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
3. Not applicable to leadless chip carriers.
4. LTPD based on number of leads.
5. Not applicable for solder seal packages.

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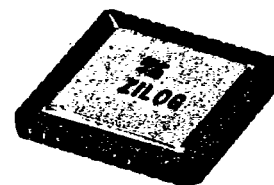
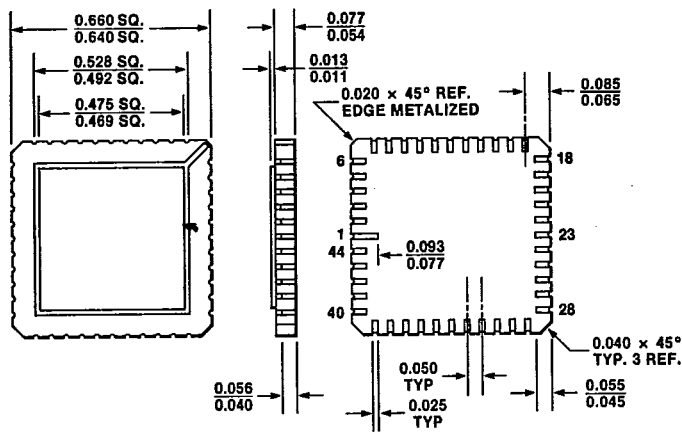
03E 08300 D

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PACKAGE INFORMATION



28-Pin Ceramic Package (DIP)



44-Pin Ceramic Leadless Chip Carrier (LCC)

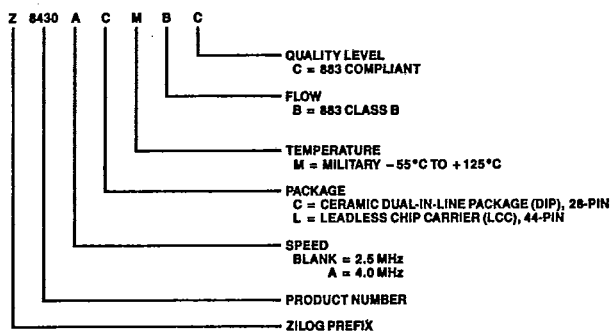


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# ZILOG ORDERING INFORMATION



## AVAILABLE MILITARY PRODUCTS

**Z80 CTC, 2.5 MHz**

|                   |                   |
|-------------------|-------------------|
| <b>28-pin DIP</b> | <b>44-pin LCC</b> |
| Z8430 CM          | Z8430 LM          |
| Z8430 CMBC        | Z8430 LMBC        |

**Z80A CTC, 4.0 MHz**

|                   |                   |
|-------------------|-------------------|
| <b>28-pin DIP</b> | <b>44-pin LCC</b> |
| Z8430A CM         | Z8430A LM         |
| Z8430A CMBC       | Z8430A LMBC       |