AMD

Mobile AMD-K6® Processor

Power Supply Design

Application Note

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Revision History

Date	Rev	Description
Jan 1999	A	Initial published release.
Apr 1999	B	Revised "Output Voltage Response Measurement Utility" on page 19 to reflect the latest recommended utility.
May 1999	C	Changed title and added first sentence on page 1 to reflect that the information in this document applies to the mobile AMD-K6® processor family.
May 1999	C	Revised the Introduction section.
May 1999	C	Added Example 3 on page 14, Figure 9 on page 17, and Figure 10 on page 18.
May 1999	C	Added "Bulk Decoupling for the I/O Supply" on page 24.
May 1999	C	Added new vendor to "Voltage Regulator Vendor Information" on page 40.

Application Note

Mobile AMD-K6® Processor Power Supply Design

Unless otherwise noted, the information in this application note pertains to all mobile processors in the AMD-K6® family, which includes the Mobile AMD-K6 processor, the Mobile AMD-K6-2 processor, and the Mobile AMD-K6-III-P processor.

Introduction

This application note is intended to guide the board designer through the process of developing a reliable power supply for the mobile AMD-K6 processor family. AMD encourages designers to support adjustable voltage by using regulators with VID inputs. This programmable voltage feature facilitates the transition to the next generation of processors. Additionally, as mobile processors are pushed for higher performance and faster clock speeds, the current requirements will continue to rise. Higher currents will require more decoupling capacitors, and can be planned for by including pads on the board today even if they are not populated. Designs that support higher currents will extend the life of a mobile system.

This application note also provides basic guidelines on circuit decoupling for reduction of noise generated by fast current transients.

For power supply design information for desktop AMD-K6 processors, see the *AMD-K6® Processor Power Supply Design Application Note*, order# 21103.

This document contains the following sections:

- **Mobile AMD-K6® Processor Family Power Requirements—** Lists the power requirements for the mobile AMD-K6 processor family with an overview of power supply design considerations. This section describes the basic elements of a power supply and the constraints of different design approaches.
- **Decoupling and Layout Recommendations—**Describes the decoupling and layout recommendations of the power supply design. Proper decoupling is required in order to deliver a reliable power source across the power planes and to reduce the noise generated from the fast current transients.
- **Power Supply Solutions—**Describes several voltage regulator circuits that are developed by voltage regulator vendors. These circuits can be used to generate the proper core and I/O voltages for the mobile AMD-K6 processors. AMD recommends that board designers consult with the voltage regulator vendors to obtain the most updated information.
- For more information about the mobile AMD-K6 processor family, refer to the following:
  - *Mobile AMD-K6® Processor Data Sheet*, order# 21049
  - *Mobile AMD-K6®-2 Processor Data Sheet*, order# 21896
  - *Mobile AMD-K6®-III-P Processor Data Sheet*, order# 22655

Mobile AMD-K6® Processor Family Power Requirements

Voltage Planes

Two separate supply voltages are required to support the mobile AMD-K6 processors—V_{CC2} and V_{CC3}. V_{CC2} provides the core voltage for the processor and V_{CC3} provides the I/O voltage.

The power supply pin assignments for the mobile AMD-K6 processors 321-pin CPGA package (See Figure 1 on page 4) are as follows:

V_{CC2} (Core): A-07, A-09, A-11, A-13, A-15, A-17, B-02, E-15, G-01, J-01, L-01, N-01, Q-01, S-01, U-01, W-01, Y-01, AA-01, AC-01, AE-01, AG-01, AJ-11, AN-09, AN-11, AN-13, AN-15, AN-17, AN-19

V_{CC3} (I/O): A-19, A-21, A-23, A-25, A-27, A-29, E-21, E-27, E-37, G-37, J-37, L-33, L-37, N-37, Q-37, S-37, T-34, U-33, U-37, W-37, Y-37, AA-37, AC-37, AE-37, AG-37, AJ-19, AJ-29, AN-21, AN-23, AN-25, AN-27, AN-29

The power supply pin assignments for the Mobile AMD-K6 and the Mobile AMD-K6-2 processor 360-pin CBGA package (See Figure 2 on page 5) are as follows:

V_{CC2} (Core): F04, F05, F06, F07, G06, G07, H08, H09, H12, H13, J04, J05, J08, J09, J10, J11, J12, J13, K04, K05, K06, K07, K10, K11, L04, L05, L08, L09, L10, L11, L12, L13, M08, M09, M12, M13, N06, N07, P04, P05, P06, P07

V_{CC3} (I/O): D07, D08, D09, D12, D13, E07, E08, E09, E12, E13, F10, F11, F14, G10, G11, G14, G15, G16, H14, H15, H16, K17, M14, M15, M16, N10, N11, N14, N15, N16, P10, P11, P14, R07, R08, R09, R12, R13, T07, T08, T09, T12, T13

Note: *The Mobile AMD-K6-III-P processor is not available in the CBGA package.*

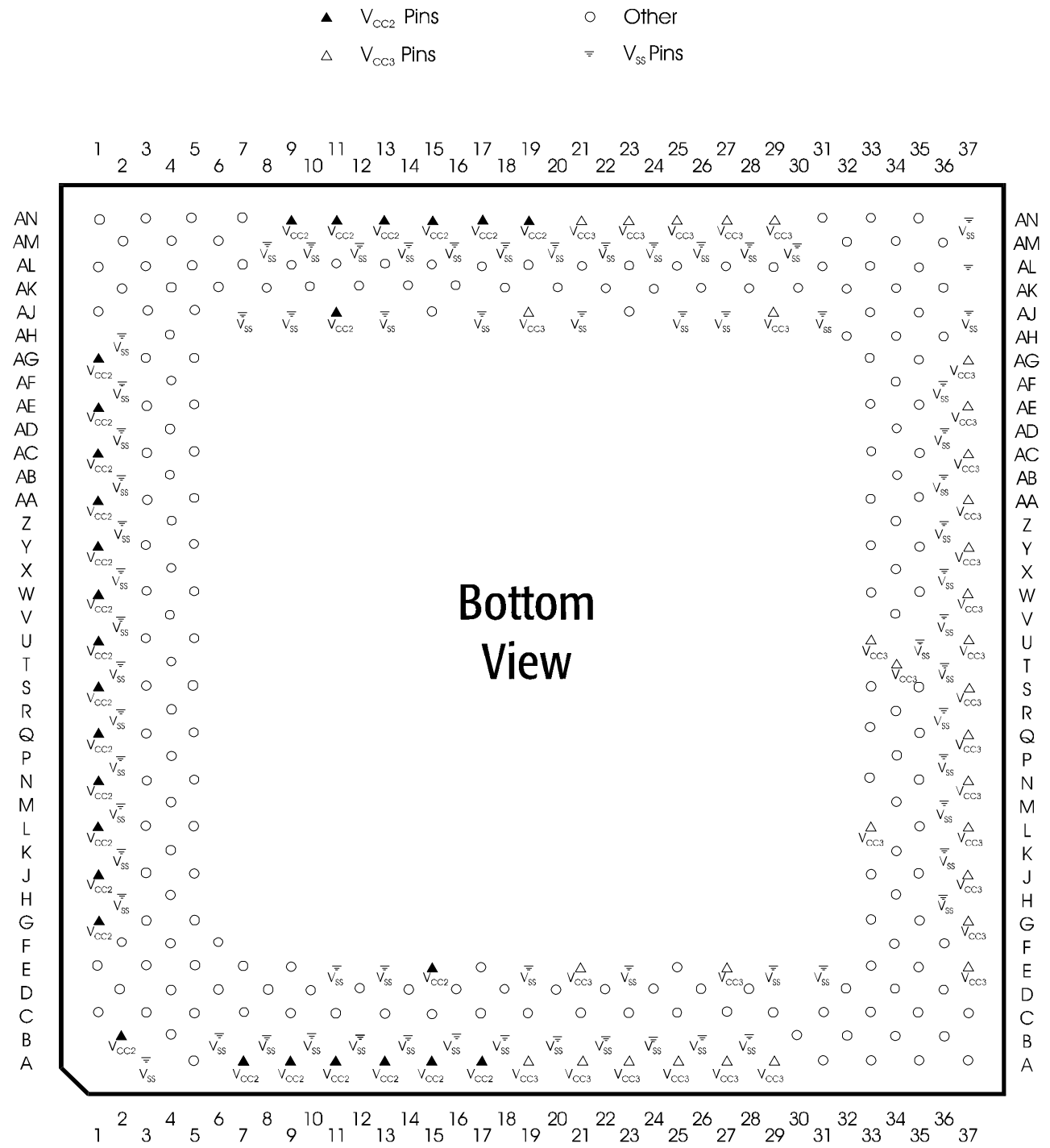


Figure 1. 321-Pin CPGA V_{CC} and Ground Pins Location

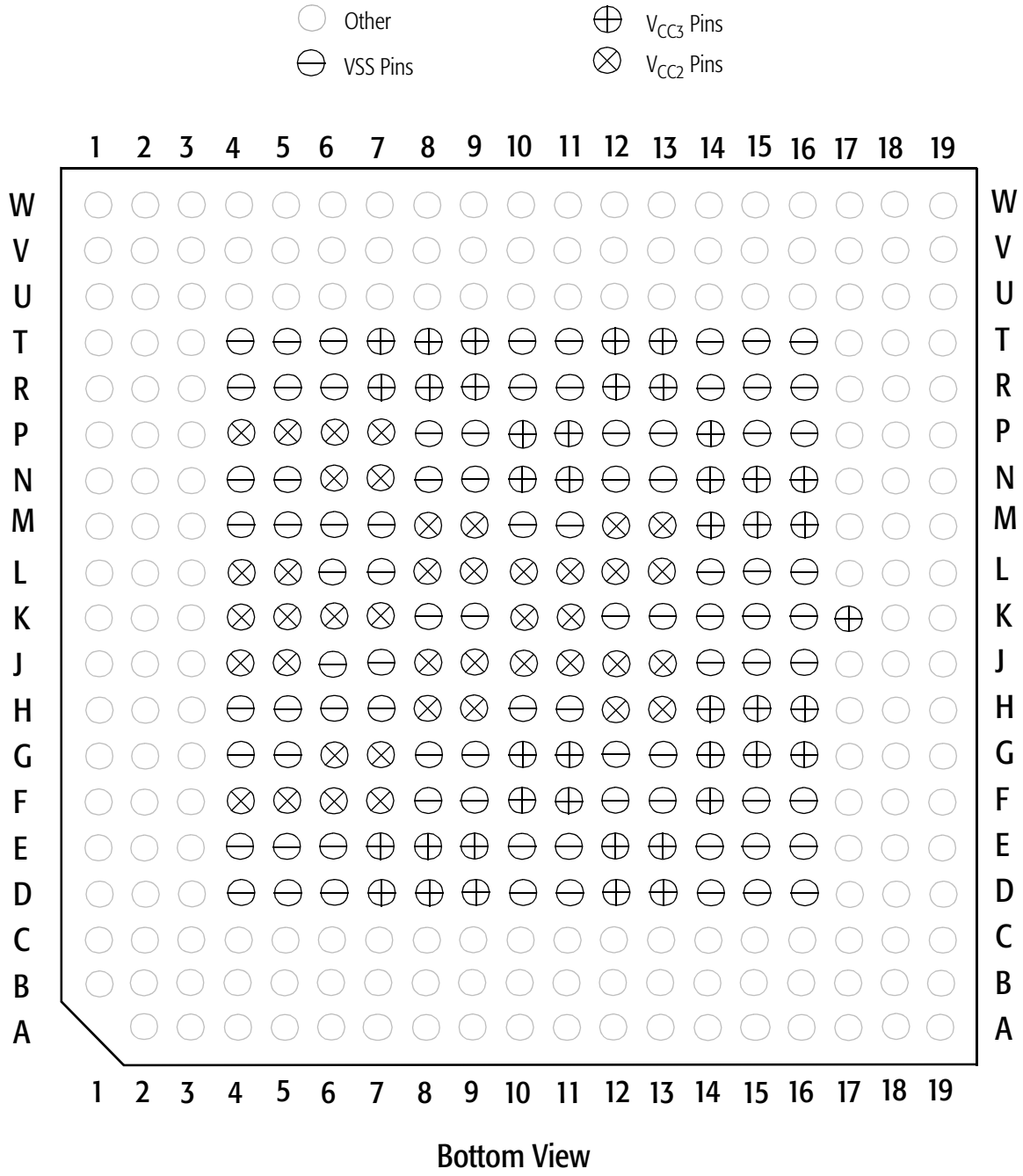


Figure 2. 360-Pin CBGA V_{CC} and Ground Pins Location

Power Supply Specification

The maximum current used for power calculations is based on maximum V_{CC} whereas the current used for maximum thermal power calculations is based on nominal V_{CC}. Refer to the Thermal Solution Design Application Note, order# 21085 for more details on thermal calculations

For voltage and current specifications of the mobile AMD-K6 processor family, refer to their respective data sheets at http://www.amd.com/K6/k6docs/.

Selecting a Power Supply Design

Most PC platforms today require DC-to-DC voltage conversion circuits to supply lower voltages to the processor core and I/O. Two types of regulators are used—linear and switching. Figure 3 shows the linear and switching regulators.

A linear regulator provides excellent dynamic-load response in the low-voltage, high-current environment. It also contributes to simplified design and lower cost. However, the efficiency loss and heat generated by a linear regulator should be addressed by board designs. Although most desktop system designs can tolerate the efficiency loss, mobile designs cannot. In a high-current model, the power dissipation from the linear regulator can be as much as that of the processor itself. In order for the voltage regulator thermal solution to meet the case temperature requirement, the linear regulator requires a larger heatsink. Linear regulators are not recommended for mobile designs because of the heat and low efficiency.

A switching regulator meets the efficiency and size limitations of mobile board designs. Switching regulators are found in most notebook computers that require both low-profile design and power-dissipation reduction. The switching regulator uses a series switch in conjunction with the output capacitor (C_O) to control the ON/OFF ratio in order to obtain an average output voltage. Because the switch turns off frequently, only a small amount of power is lost during conversion.

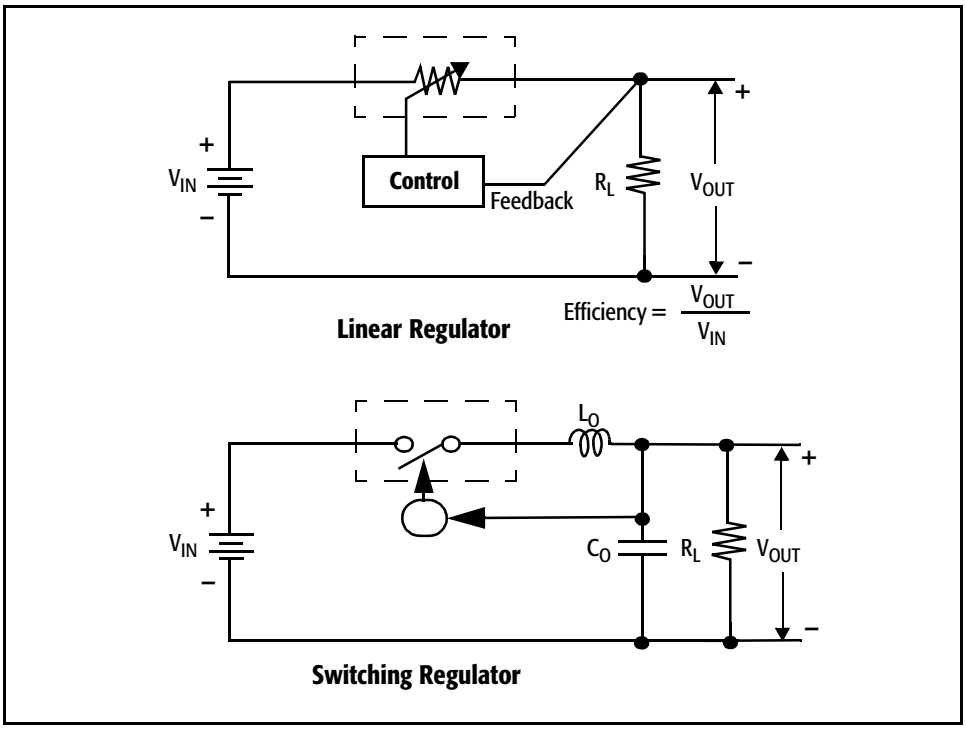


Figure 3. Linear and Switching Voltage Regulators

Switching Regulator

A switching regulator varies the switch duty cycle (ON/OFF ratio) according to the output feedback. A large output capacitor (C_O) is used in the switching design to achieve a constant average output. The switching regulator delivers higher efficiency than a linear regulator, but the tradeoffs are higher ripple voltages (noise) and slower transient current response time. A series inductor is used to supply current to the load during the switch OFF time, adding complexity to the design. In addition, the inductor and the output capacitor increase the overall cost of the switching regulator design relative to a linear regulator design.

The power supply design must account for a minimized current (I_{CC2} and I_{CC3}) drain when the mobile AMD-K6 processors enter the Stop Grant state. The power supply must ensure the minimal current drain does not cause any adverse side effects (drift out of regulation, over-compensation, or shutdown) that could corrupt or damage the functionality of the processor.

The mobile AMD-K6 processors voltage tolerance requirement on both core and I/O voltage pins can be handled by commonly available linear and switching regulators. This application note describes several high-accuracy designs (starting on page 31)

that provide the processor with accurate and stable voltage supplies.

In the basic asynchronous circuit design shown in Figure 4, Q1 turns on to charge C_{out} and builds up the magnetic field in L1. When the feedback from the sense input is too high, the controller turns Q1 off. Current is supplied to the load by the collapsing magnetic field in L1 and the discharge of C_{out}. When the sense feedback detects a drop in the load voltage, the controller turns on Q1 to recharge the circuit. CR2 supplies a return path for L1 when it is supplying current.

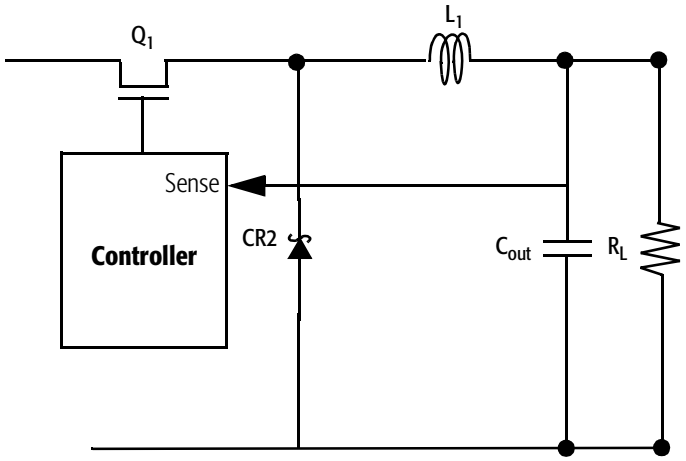


Figure 4. Basic Asynchronous Design

The operation of the basic synchronous circuit design shown in Figure 5 is essentially the same as the asynchronous design. Q1 turns on to charge C_{out} and builds up the magnetic field in L1. When the feedback from the sense input is too high, the controller turns Q1 off. Current is supplied to the load by the collapsing magnetic field in L1 and the discharge of C_{out}. When the sense feedback detects a drop in the load voltage, the controller turns on Q1 to recharge the circuit. Q2 supplies a return path for L1 when it is supplying current. When Q1 is on, Q2 is off and when Q1 is off, Q2 is on. The main reason the synchronous design is more efficient than the asynchronous design is because the power dissipated in Q2 is lower than the power dissipated in CR2.

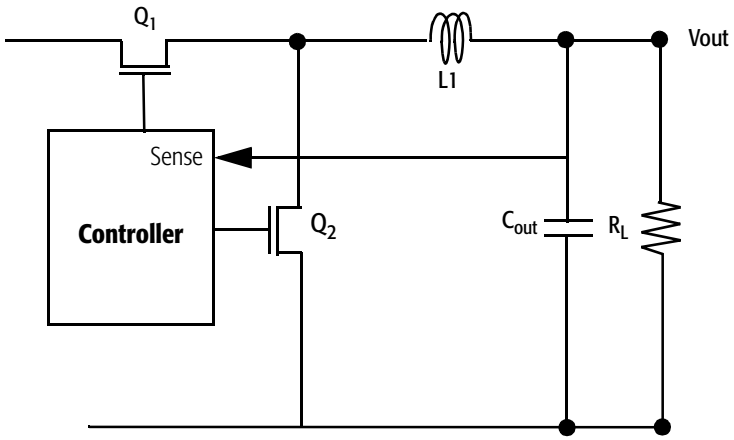


Figure 5. Basic Synchronous Design

Another consideration is power dissipation in the lower MOSFET Q2 (synchronous) or diode CR2 (asynchronous). As the output voltage decreases, the power dissipation in CR2 (Q2) increases. The higher power dissipation may require using a different package type or adding a heat sink to dissipate the additional power.

To determine if the transistors or the diode need a heat sink, use the following equation:

$$P = I^2R \bullet \text{duty cycle (Q1)}$$

$$P = I^2R \bullet (1 - \text{duty cycle}) \text{ (Q2)}$$

$$\text{Duty cycle} \sim V_{out}/V_{in}$$

Compare these calculations with the specifications of the device used.

Other specifications to consider are the input-voltage range and the number of outputs provided. The input-voltage range must be matched to the batteries and charger. Ensure that the charger voltage does not exceed the input-voltage range of the regulator when the battery is removed. Generally, the battery stack consists of 5 to 12 NiCd cells or 2 to 3 Li-Ion cells.

Some parts supply multiple outputs. These devices can save critical space in a mobile design. However, these devices limit some of the voltage and current options, and should be evaluated based on the total requirements of the end product.

Mobile systems typically require 12V, 5V, 3.3V, and the specified CPU core voltage for the AMD-K6 processor Models 7, 8 and 9. Each of these voltages can be generated directly from the battery (a technique called distributed power). The more common approach involves producing a 5V main supply and generating the other voltages from this 5V source. This technique is less efficient, yielding a shorter battery life. For example, assume a 90% efficiency to generate 5V from the battery and 90% efficiency to generate 3.3V from 5V. This yields an overall efficiency of 81% between the battery and the 3.3V supply. Efficiency is very important because it contributes directly to battery life. To achieve high efficiency at low currents, many converters have a pulse-skipping mode. Some companies call this hysteretic mode or burst mode. All of the examples starting on page 33 use synchronous converter designs because they are the most efficient (90%–95%). The additional Schottky diode in some designs provides an additional efficiency improvement at low currents.

Space and weight are also important considerations for mobile designs. Some solutions listed use fewer components than others. Some use more expensive components. The size of the inductor can be reduced by running the controller at a higher frequency.

When choosing a vendor, pick one that meets all the needs of the end product. The product lines of some vendors include battery charger circuits and backlight inverters for the display.

In addition, locate the supply as close as possible to the CPU. This placement reduces the distance current transients must travel in the V_{CC} and GND planes, thereby reducing EMI.

Decoupling and Layout Recommendations

Power Distribution

In order to maintain a stable voltage supply during fast transients, power planes with high frequency and bulk decoupling capacitors are required. Figure 6 shows a power distribution model for the power supply and the processor. The bulk capacitors (C_B) are used to minimize ringing, and the processor decoupling capacitors (C_F) are spread evenly across the circuit to maintain stable power distribution.

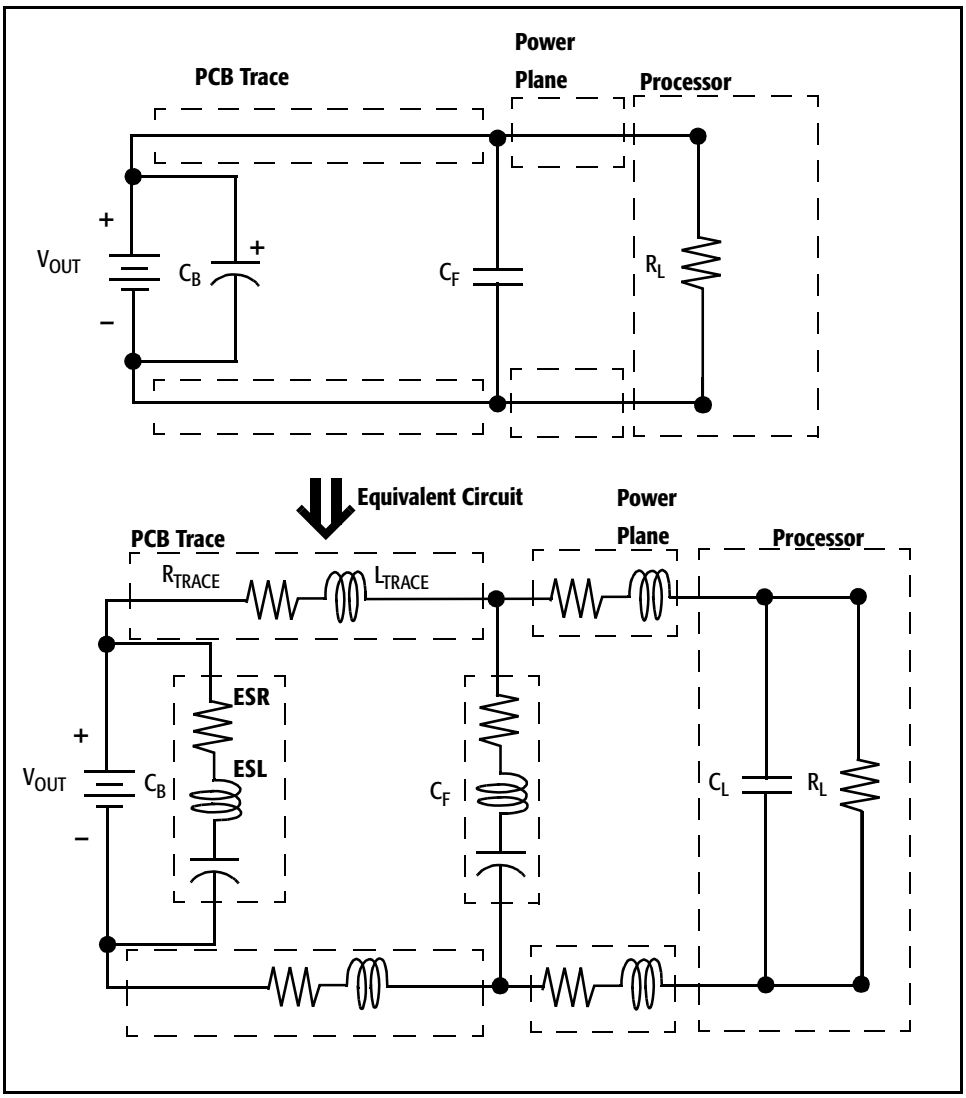


Figure 6. Power Distribution Model

Current Transient Response

In the power distribution model shown in Figure 6, C_B represents bulk capacitors for the power supply and C_F represents high-frequency capacitors for processor decoupling. The bulk capacitors supply current to the processor during sudden excessive current demands that cannot be supplied by the voltage regulator (for example, transistioning from the Stop Grant state to normal mode). The required C_B can be calculated by the following equation (ideal case):

$$C \geq \frac{\Delta I}{\Delta V} \bullet \Delta t$$

Where:

- ΔI is the maximum processor current transient
- ΔV is the tolerance times the nominal processor voltage
- Δt is the voltage regulator response time

Example 1

Assuming the maximum processor current transient is 6A, the voltage tolerance of the processor is 100 mV, and the voltage regulator response time is 10µs, the minimum capacitance for the bulk decoupling is:

$$C_B \geq (6A/0.100V) \bullet 10\mu s = 600\mu F$$

ESR (equivalent series resistance) and ESL (equivalent series inductance) are introduced in the model shown in Figure 6. C_B contains ESR and ESL, which cause voltage drop during current transient activity (See Figure 7). The resistive and inductive effect of the capacitors must be taken into account when designing processor decoupling. Low ESL and ESR capacitors should be used to obtain better voltage and current output characteristics. The voltage error budget for ESL is shown in Table 1 on page 15. Taking into account the ESR, the following equation is used to calculate C_B:

$$C \geq \frac{\Delta I}{(\Delta V - (\Delta I \bullet ESR))} \bullet \Delta t$$

Example 2

Example 1 assumes the maximum processor current transient is 6A, the voltage tolerance of the processor is less than 100mV, and the voltage regulator response time is 10µs.

Assuming five tantalum capacitors with 55-mΩ ESR (the parallel resistance is 11mΩ) are used as bulk capacitors, the minimum bulk capacitance is:

$$C_0 \geq ((6A/(0.100V - [6A \bullet 11m\Omega])) \bullet 10\mu s = 1764\mu F$$

In Example 2, the effect of the ESR requires the addition of more capacitance than the ideal shown in Example 1.

In order to achieve more margin, the total error budget should be distributed between set point tolerance, ESL, and ESR as shown in Figure 7 on page 14 and Table 1 on page 15. Although the drop from ESL is a small factor, it is not negligible. If aluminum electrolytic capacitors are used instead of tantalum capacitors, the ESL drop is larger.

Example 3

This example assumes the maximum processor current transient is 8.5A, the voltage tolerance of the processor is less than 100mV, and the voltage regulator response time is 10µs.

Assuming seven tantalum capacitors with 55-mΩ ESR (the parallel resistance is 8mΩ) are used as bulk capacitors, the minimum bulk capacitance is:

$$C_0 \geq ((8.5A/(0.100V - [8.5A \bullet 8m\Omega])) \bullet 10\mu s = 2656\mu F$$

In order to achieve more margin, the total error budget should be distributed between set point tolerance, ESL, and ESR as shown in Figure 7 and Table 1 on page 15. Although the drop from ESL is a small factor, it is not negligible. If aluminum electrolytic capacitors are used instead of tantalum capacitors, the ESL drop is larger.

Note: *For additional higher current calculations, see the AMD-K6® Power Supply Design Application Note, order# 21103.*

The high-frequency decoupling capacitors (C_F), which are typically smaller in capacitance and ESL, maintain the voltage output during average load change until C_B can react. See "High-Frequency Decoupling" on page 25 for more information.

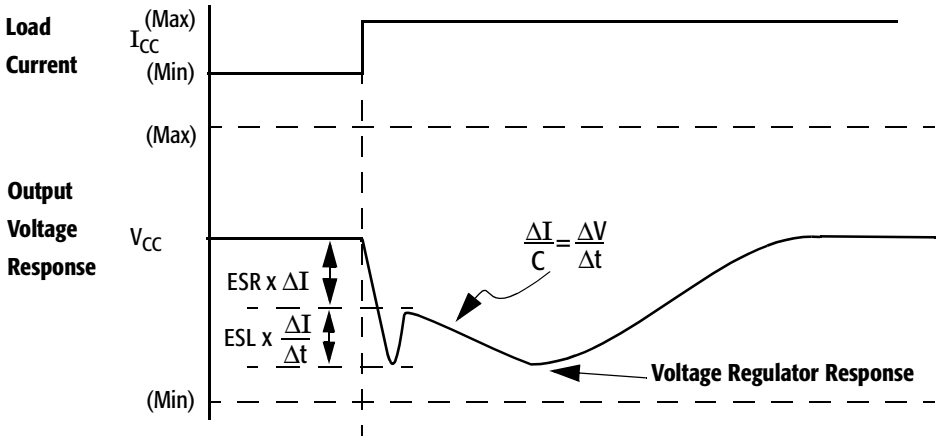


Figure 7. Load Current Step versus Output Voltage Response

Allocation of the voltage error budget can be determined from Figure 7. Given a total error budget of 100mV and using good capacitors (five 470-µF capacitors with a 55-mΩ ESR are assumed), voltage drops can be allocated as shown in Table 1.

Table 1. Voltage Error Budget

Error Budget Component	Calculations*	Budgeted Drop
V (Set Point)	1%	0.020V
V (ESR)	11 mΩ x 5.6A (11 mΩ = 55 mΩ/5)	0.062V
V (ESL)	0.24 nH x (6A/100 nsec) {0.24 nH = (0.6 nH + 0.6 nH via)/5}	0.014V
Total		0.096V

Note:
* *Calculations assume 5 capacitors*

Figure 8 shows the voltage drop as a function of bulk decoupling. The graph was calculated using 55-mΩ ESR 470-µF capacitors, and gives the designer a visual representation of how much bulk decoupling is required. For example, at 1880 µF, the voltage is 1.72V (6A current transient), leaving little margin for DC-tolerance errors. At 2820 µF, the voltage is 1.75V, allowing 0.05V for set point tolerance.

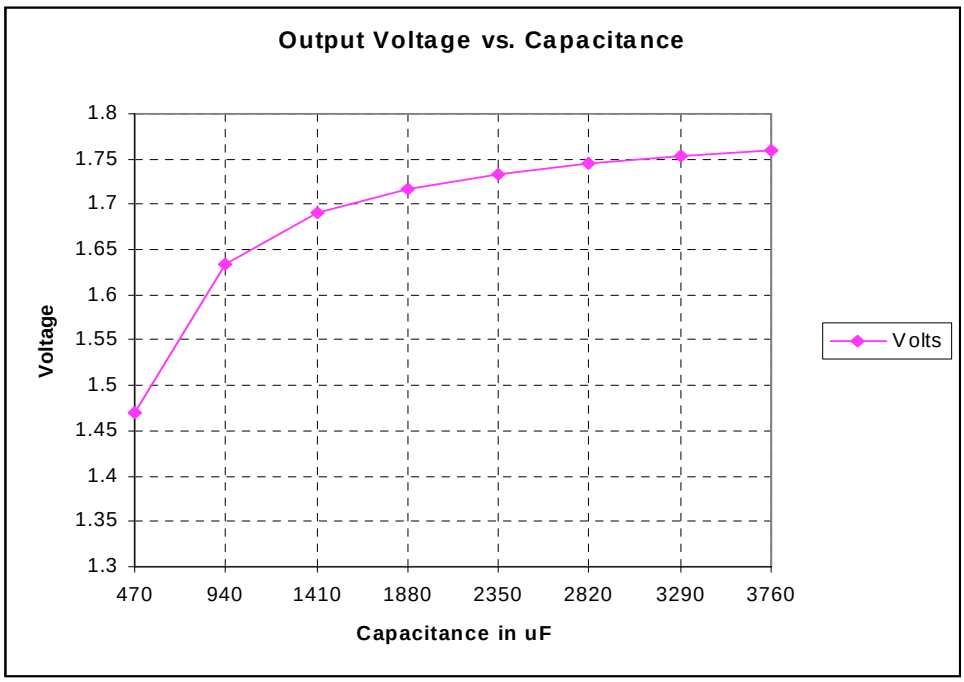


Figure 8. Bulk Decoupling versus Output Voltage Response for a 1.8V Processor Core @ 6.25 amps

Similarly, Figure 9 shows the voltage drop as a function of bulk decoupling. The graph was calculated using 55-mΩ ESR 470-µF capacitors, and gives the designer a visual representation of how much bulk decoupling is required. For example, at 1880 µF, the voltage is 1.92V (6A current transient), leaving little margin for DC-tolerance errors. At 2820 µF, the voltage is 1.95V, allowing 0.05V for set point tolerance.

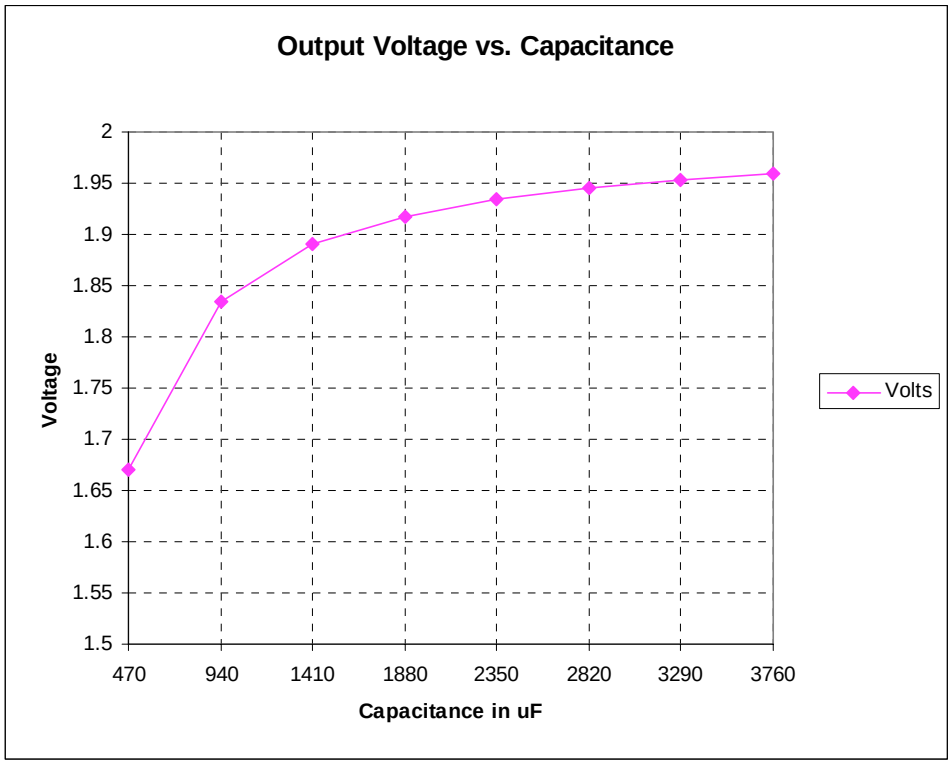


Figure 9. Bulk Decoupling versus Output Voltage Response for a 2.0V Processor Core @ 6.0 amps

Similarly, Figure 10 shows the voltage drop as a function of bulk decoupling. The graph was calculated using 55-mΩ ESR 470-µF capacitors, and gives the designer a visual representation of how much bulk decoupling is required. For example, at 2350 µF, the voltage is 2.11V (8.5A current transient), leaving little margin for DC-tolerance errors. At 3760 µF, the voltage is 2.14V, allowing 0.04V for set point tolerance.

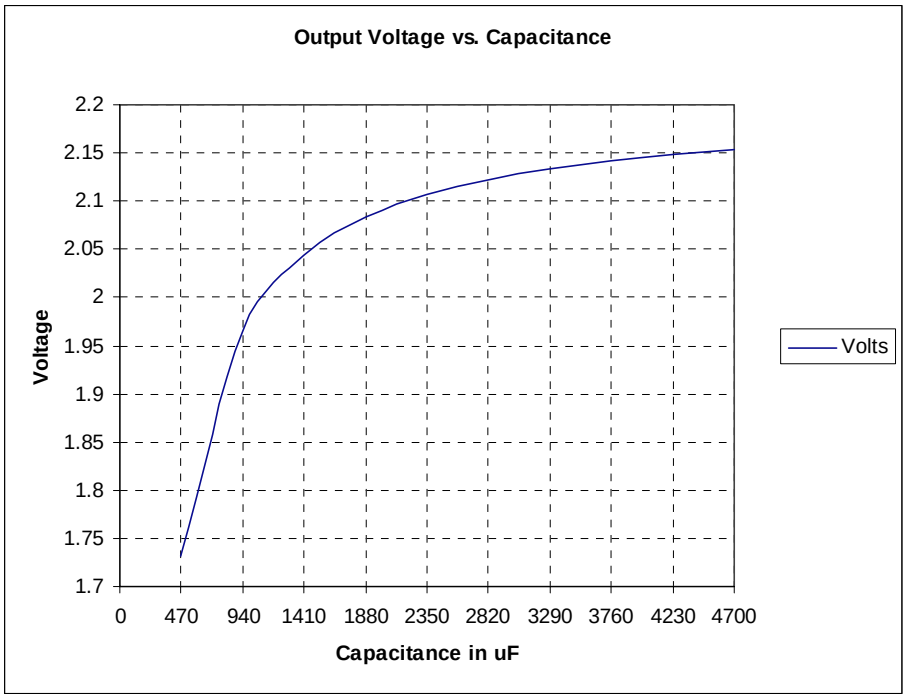


Figure 10. Bulk Decoupling versus Output Voltage Response for a 2.2V Processor Core @ 8.5 amps

Output Voltage Response Measurement Techniques

To measure output voltage response, run a program such as DOS EDIT and toggle STPCLK# every 40 µs or slower. (AMD has developed the Maxpwr99.exe utility. See "Output Voltage Response Measurement Utility" for more information.) Measure the voltage at the back of the board right under the processor. Use a scope probe with a ground connection next to the tip. The 3 inch to 6 inch ground leads that come off the side of a scope probe have too much inductance for this type of measurement. The scope bandwidth can be limited to 20MHz,

giving a clear indication of the power supplied. While limiting the scope bandwidth for bulk decoupling verification gives a clear indication of the low frequency issues, AMD recommends rechecking with at least a 250-MHz bandwidth for verifying the high-frequency decoupling.

AMD used a Tektronix 684B scope with 6245 probes and an HP54720 with 54701 probes. (There was no significant difference between these two instruments.) The data was taken over a 40-second window with the scope set to infinite persistence. AMD made measurements running Winstone® under the Windows® 95 operating system, running DOS EDIT pull down, and running Maxpwr99.exe while toggling STPCLK#. The latter case created the worst measured-case current transient. In addition, this is the case that requires the maximum decoupling capacitance.

The table "Voltage Regulator Vendor Information" on page 40 lists some possible power supply solutions. The listed regulators are ones that AMD believes can meet the processor requirements (with proper decoupling). AMD has not tested any of the mobile power supplies.

Output Voltage Response Measurement Utility

AMD has developed the Maxpwr99.exe utility to assist in designing systems that comply with the AMD-K6 processors power and thermal requirements. This utility can verify that the supply voltage remains stable during a transition to a higher power/current consumption level.

This utility is DOS based. For systems based on the Windows 95 or Windows 98 operating systems, re-boot in DOS mode or boot from a bootable DOS floppy disk that contains the utility. For systems based on the Windows NT® and OS/2 operating systems, boot from a bootable DOS floppy disk that contains the utility.

The command line for this utility is as follows: (***Note:*** *Do not execute the utility in a DOS window or with a memory manager loaded.*)

```
c:\>Maxpwr99.exe
```

The Maxpwr99.exe utility is available under a non-disclosure agreement. Contact your local AMD sales office for information.

Decoupling Capacitance and Component Placement

The high-frequency decoupling capacitors (C5–C31 in Figure 12 on page 22) should be located as close to the processor power and ground pins as possible. To minimize resistance and inductance in the lead length, the use of surface mounted capacitors is recommended. When possible, use traces to connect capacitors directly to the processor's power and ground pins. The decoupling capacitors can be placed in the Socket 7 cavity on the same side of the processor (component side) or the opposite side (bottom side).

Suggested component placement for the decoupling capacitors are shown in Figure 12 on page 22 for CPGA packages and in Figure 13 on page 23 for CBGA packages. The values of the capacitors are specified in Table 4 on page 24. Capacitor recommendations are shown in Table 5 on page 24. The split voltage planes should be isolated if they are in the same layer of the circuit board. To separate the two power planes, an isolation region with a minimum width of 0.254 mm is recommended. The ground plane should never be split.

These recommendations are based on single-sided component assembly and space constraints. The designer should assume these are minimum requirements. If double-sided component assembly is used, it is preferable to use more capacitors of a smaller value, which reduces the total ESR and total ESL of the capacitors. For example, instead of four 470-µF capacitors, use ten 47-µF capacitors. (Check the device specifications shown in Table 2 on page 20. Occasionally a lower value capacitance has a higher ESR.) As the effective ESR is lowered, the total required capacitance is reduced. The breakdown voltage and case size both affect the ESR value.

Table 2. Representative ESR Values

Capacitance	Device 1	Device 2
470 µF	55 mΩ	100 mΩ
270 µF	70 mΩ	100 mΩ
100 µF	90 mΩ	100 mΩ
68 µF	95 mΩ	100 mΩ
47 µF	120 mΩ	250 mΩ

Via inductance can be reduced when using double-sided component assembly. Components can share vias on the top side and bottom side. This technique reduces the effective via inductance.

Figure 11 shows another way to reduce via inductance—parallel vias. This technique is usually used on bulk decoupling capacitors. The inductance contribution numbers shown in Table 3 indicate that a poor layout can negate a good component.

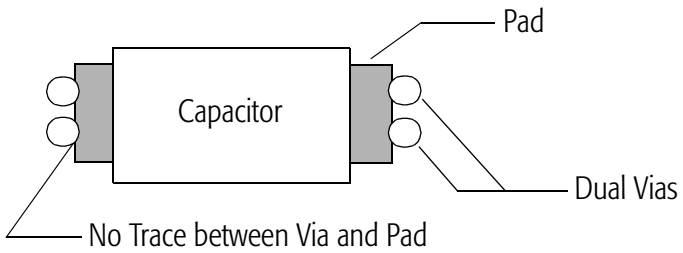


Figure 11. Via Layout For Low Inductance

Table 3. Inductance Contributions of Components

Component	Induction	Comment
Capacitor	0.6 nH (approximately)	ESL
Via	0.7 nH (approximately)	–
100 mil Trace	1.6 nH (approximately)	10 mil wide trace

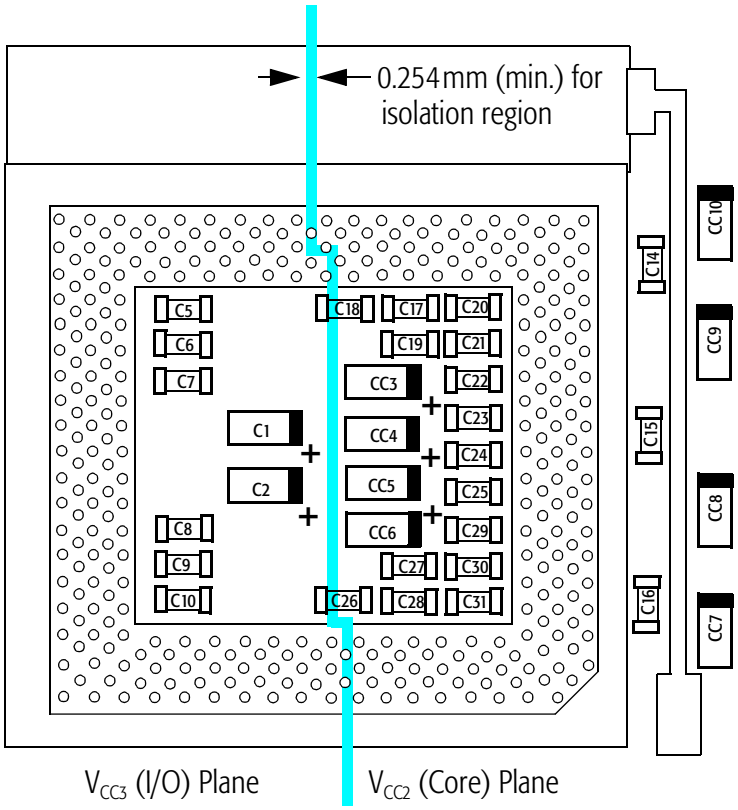
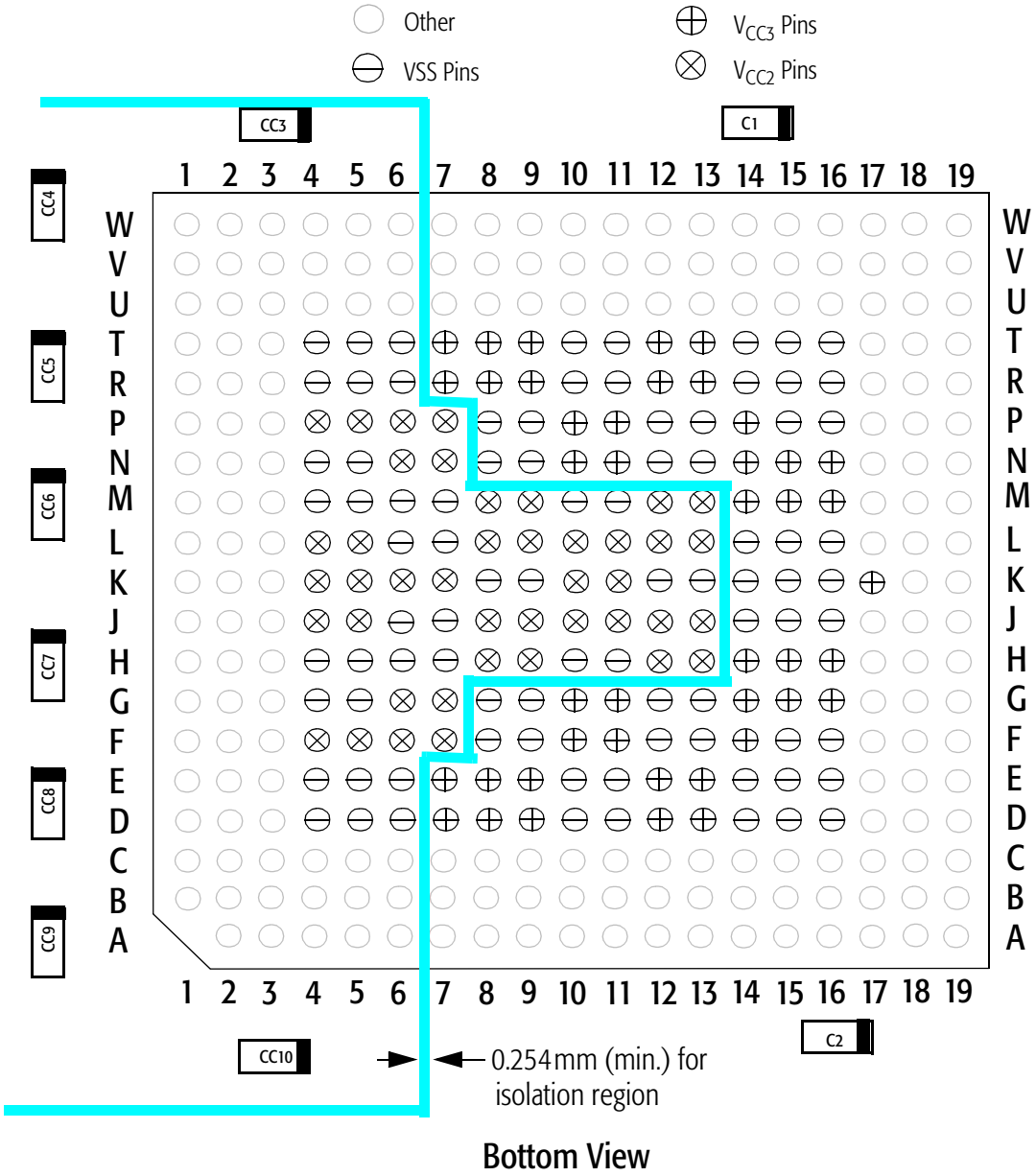


Figure 12. CPGA Suggested Component Placement



Note: *High-frequency capacitor placement is very layout dependent and is not shown in this figure.*

Figure 13. CBGA Suggested Component Placement

Table 4 lists the recommended capacitor values.

Table 4. Decoupling Capacitor Values

Item	Qty	Location	Value	Footprint	Description	Note
1	2	C1, C2	47µF	AVX Size V	Surface tantalum capacitor, AVX part number TPSV476*025R0300 or equivalent	V_{CC3} Decoupling
2	8	CC3–CC10	470µF	AVX Size V	Surface tantalum capacitor, AVX part number TPSV477*006R0100 or equivalent	V_{CC2} Decoupling
3	24	C5–C31	0.1µF	0805	–	C5–C10 for V_{CC3} C14–C31 for V_{CC2}

Table 5 lists recommended capacitor types.

Table 5. Capacitor Recommendations

Manufacturer	Type	Comment	Web
AVX	TPS	exceptional	/www.avxcorp.com
Vishay Sprague	594D	exceptional	/vishay.com/vishay/sprague
Sanyo	SA/SG	excellent	/www.sanyovideo.com
Chem-con	LVX	good	/www.chemi-con.com
Mallory	T495	good	/www.nacc-mallory.com
Nemco	SLR series	good	/www.nemcocaps.com
Panasonic	EEF	good	/www.panasonic.com/pic
Panasonic	FA	good	/www.panasonic.com/pic
Vishay Sprague	593D	good	/vishay.com/vishay/sprague
Elna	RJH/RJJ	good	/www.elna-america.com

The recommendations in Table 5 are not the only possibilities. Based on parts availability and the controller chosen, many solutions exist. The intent of these recommendations is to give insight into the requirements, and not to specify a particular solution. Many vendors prefer to use aluminum electrolytics instead of tantalum capacitors. This approach is acceptable as long as good quality, low-ESR parts are used.

Bulk Decoupling for the I/O Supply

The data sheet specifies the V_{CC3} current at about 0.6 amps. This number only specifies the maximum current consumed by the processor without any load. To calculate the peak demand on the I/O supply, consider what happens when all 64 data bus

lines switch from low to high. A typical PC board trace impedance appears as 50Ω during the switching time. Therefore, the theoretically computed current demand is I = 3.3 V/50 Ω = 66 mA. If this is multiplied by 64 drivers, the result is 4.22 A. However, the driver acts as a constant current source/sink of about 20 mA for the first 200 psec then it behaves as a 40 mA current source/sink until it is approximately 1 volt from V_{CC3} when driving high, or 1 volt from ground when driving low. From this point the current linearly decreases to zero. Thus instead of a maximum of 4.22 A, the current is limited to 64 • 40 mA = 2.56 A current demand to charge the bus. Using the same techniques as the previous core, the bulk decoupling for the I/O can be computed as follows:

This example assumes a maximum processor I/O current transient of 2.6A, the voltage tolerance of the processor is less than 145 mV, and the voltage regulator response time is 1µs. A linear regulator is assumed in this example to have a 1µs response time.

Using three tantalum capacitors with 100-mΩ ESR (the parallel resistance is 33mΩ) as bulk capacitors, the minimum bulk capacitance is calculated as:

$$C_0 \geq ((2.6A/(0.145V - [2.6A \bullet 33m\Omega])) \bullet 1\mu s = 44\mu F$$

Three 22 µF tantalum capacitors with 100-mΩ ESR meet this requirement. However, if the regulator response time is 10 µs then 440 µF would be required. It is difficult to find a 22 µF tantalum capacitors with an ESR this low. Therefore, it is necessary to use a much larger value of capacitance to get this low of an ESR. Two 470 µF, 55 mΩ ESR parts would meet the requirement. Three 100 µF capacitors with an ESR of 100 mΩ would also work.

High-Frequency Decoupling

Inductance is also a concern for the high-frequency decoupling capacitors. Case size can be a significant factor affecting capacitor inductance. For example, a 0603 case has significantly more inductance than a 0612 case. AMD recommends the 0612, 1206, 0805, and 0603 case in order of best to worst. Inductance can also be reduced by directly connecting the capacitor to the power pin of the processor. In order to minimize its inductance, this trace must be short and as wide as possible. This technique effectively removes two via

inductances between the capacitor and the processor as shown in Figure 15 on page 28. The dotted line shows that connecting the capacitor directly to the processor eliminates two series inductances. However, this trace also has inductance—if it is too long or too narrow it can be worse than the vias.

Figure 14 on page 28 shows the effect of the inductance at higher frequencies. (The numbers outside the X and Y axis indicate the minimum and maximum values plotted). The inductance used is 1.8nH (0.7nH for each of the two vias and 0.4nH for the capacitor itself). The capacitor is a 0.1-µF X7R multilayer Ceramic MLC. The inductance of a capacitor is a function of the case type. An 0612 case is assumed here.

The following steps show how the number of required capacitors is calculated:

1. Decide what to allow as a ripple voltage budget. In this example calculation the ripple-voltage budget (dv) is 30 mV.
2. The measured AC transient current is 0.75A. This transient current has a typical duration (dt) of 2.5 nsec. The amount of capacitance required can now be determined using the following equation:

   $I = C\ (dv/dt)$

   $C = I\ (dt/dv) = 0.75A\ (2.5nsec/30mV) = 0.625\mu F$

   This equation indicates that if the capacitors didn't have inductance, only six 0.1-µF capacitors would be required.
3. Determine the number of capacitors required based on the inductance of the capacitor. Use the following formula:

   $V = L\ (di/dt) = L \bullet (0.75A/2.5nsec) = 30mV$

   Solving for L, the allowed budget is 100pH.
4. The inductance of the capacitor and via = 1.8nH (0.7nH for each of the two vias and 0.4nH from the capacitor itself). Because each capacitor usually has two vias (one on each end), the effective via inductance must be:

   $2 \bullet 0.7nH + 0.4nH = 1.8nH$

5. Solving the following equations for N:

   $1.8nH/N = 100pH$

   $N = 1.8nH/100pH = 18$

   The number of capacitors required is 18.

The following steps repeat the calculation for I/O decoupling:

1. Determine the amount of capacitance required using the following equation:

   $I = C\ (dv/dt)$

   $C = I\ (dt/dv) = 0.5\ (2.5nsec/145mV) = 0.0086\mu F$

   This equation indicates that if the capacitors didn't have inductance, only one 0.1-µF capacitor would be required.

2. Using 0.5A as a typical I_{CC3} value, repeat the calculations to account for inductance:

   Note: *The ripple budget is 145mV because the I/O drivers are not as sensitive to supply variations as the core and the current transient is smaller.*

   $L = V\ (dt/di) = 0.145\ (2.5nsec/.5A) = 725pH$

   Solving for L, the allowed budget is 725pH.

   The number of capacitors = 1.8nH/725pH = 2.5. Therefore, only three capacitors are required on the I/O. AMD recommends six capacitors.

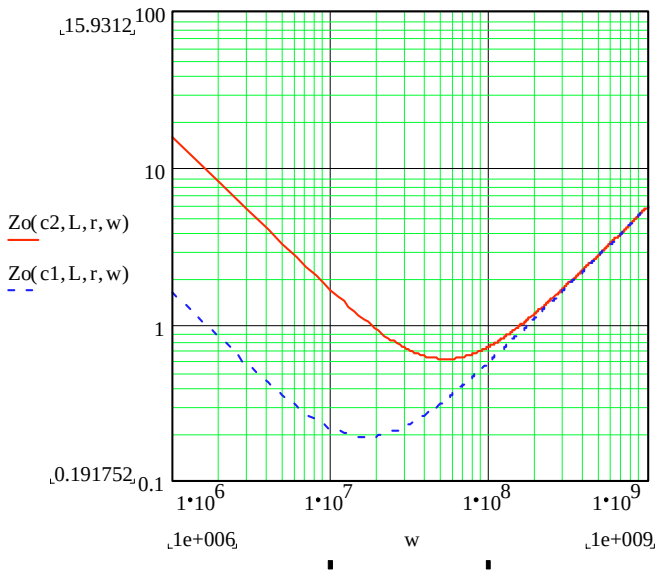


Figure 14. 0.1µF (c1) and 0.01 µF (c2) X7R Capacitor Impedance vs. Frequency

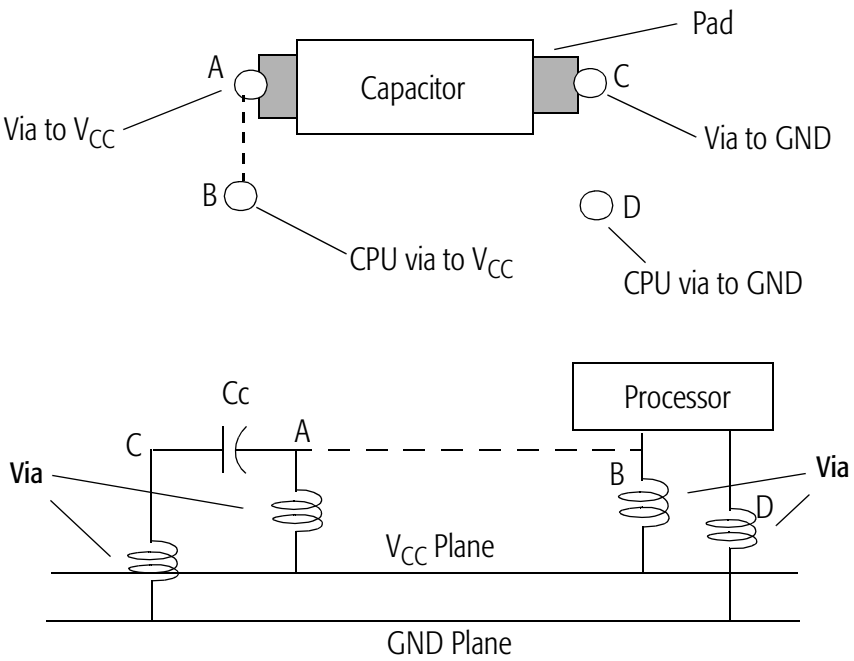


Figure 15. Decoupling Inductance

Power Sequencing

Although the mobile AMD-K6 processor requires dual power supply voltages, there are no special power sequencing requirements. The best procedure is to minimize the time between which V_{CC2} and V_{CC3} are either both on or both off (See Figure 16). However, a good design practice ensures V_{CC3} is always greater than V_{CC2}.

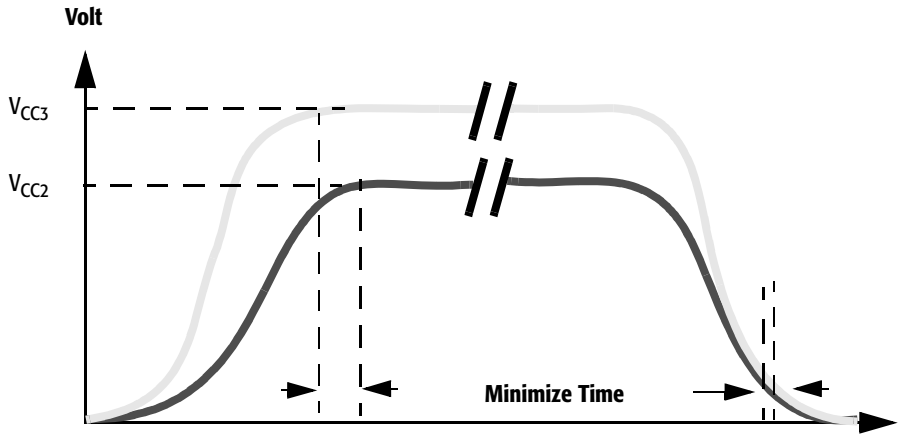


Figure 16. Power Sequencing

Power Supply Solutions

The solutions provided in this section are not all-inclusive. Obtain additional circuit diagrams and application assistance from the manufacturers. The manufacturers can customize designs to an OEM's requirements. The schematics shown in this document have not been tested by AMD and are provided as examples only.

Digital-to-Analog Converter (DAC)

Voltage Identification (VID) codes provide a way to program the Digital-to-Analog Converter (DAC) to supply a reference for different output voltages. Many manufacturers have DAC-controlled devices, however, some do not follow the VID defined codes. The devices listed in the table "Voltage Regulator Vendor Information" on page 40 use the VID codes. Table 6 shows the codes and corresponding voltages.

Table 6. Voltage Output VID Codes

D4	D3	D2	D1	D0	Output Voltage		D4	D3	D2	D1	D0	Output Voltage
1	0	0	0	0	3.50V		0	0	0	0	0	2.05V
1	0	0	0	1	3.40V		0	0	0	0	1	2.00V
1	0	0	1	0	3.30V		0	0	0	1	0	1.95V
1	0	0	1	1	3.20V		0	0	0	1	1	1.90V
1	0	1	0	0	3.10V		0	0	1	0	0	1.85V
1	0	1	0	1	3.00V		0	0	1	0	1	1.80V
1	0	1	1	0	2.90V		0	0	1	1	0	1.75V
1	0	1	1	1	2.80V		0	0	1	1	1	1.70V
1	1	0	0	0	2.70V		0	1	0	0	0	1.65V
1	1	0	0	1	2.60V		0	1	0	0	1	1.60V
1	1	0	1	0	2.50V		0	1	0	1	0	1.55V
1	1	0	1	1	2.40V		0	1	0	1	1	1.50V
1	1	1	0	0	2.30V		0	1	1	0	0	1.45V
1	1	1	0	1	2.20V		0	1	1	0	1	1.40V
1	1	1	1	0	2.10V		0	1	1	1	0	1.35V
1	1	1	1	1	OFF		0	1	1	1	1	1.30V

To meet the special requirements of Mobile parts new VID codes separate from the desktop controllers are used. These new mobile VID codes are defined in Table 7.

.

Table 7. Mobile Voltage Output VID Codes

D4	D3	D2	D1	D0	Output Voltage		D4	D3	D2	D1	D0	Output Voltage
1	0	0	0	0	1.275V		0	0	0	0	0	2.00V
1	0	0	0	1	1.250V		0	0	0	0	1	1.95V
1	0	0	1	0	1.225V		0	0	0	1	0	1.90V
1	0	0	1	1	1.200V		0	0	0	1	1	1.85V
1	0	1	0	0	1.175V		0	0	1	0	0	1.80V
1	0	1	0	1	1.150V		0	0	1	0	1	1.75V
1	0	1	1	0	1.125V		0	0	1	1	0	1.70V
1	0	1	1	1	1.100V		0	0	1	1	1	1.65V
1	1	0	0	0	1.075V		0	1	0	0	0	1.60V
1	1	0	0	1	1.050V		0	1	0	0	1	1.55V
1	1	0	1	0	1.025V		0	1	0	1	0	1.50V
1	1	0	1	1	1.000V		0	1	0	1	1	1.45V
1	1	1	0	0	0.975V		0	1	1	0	0	1.40V
1	1	1	0	1	0.950V		0	1	1	0	1	1.35V
1	1	1	1	0	0.925V		0	1	1	1	0	1.30V
1	1	1	1	1	OFF		0	1	1	1	1	OFF

Elantech EL7571

The EL7571 switching regulator is a flexible, high-efficiency, PWM controller that includes a 5-bit DAC adjustable output. This regulator employs synchronous rectification to deliver up to 15A at efficiencies greater than 85% over a supply voltage range of 4.5V to 12.6V. (Efficiencies up to 92% can be achieved at 10A.) Figure 17 shows an EL7571 reference design. The VID code allows the output to be set between 1.3V and 2.05V (in 50mV increments) and 2.1V and 3.5V (in 100mV increments) with a 1% accuracy. Table 8 on page 34 shows the bill of materials for the EL7571.

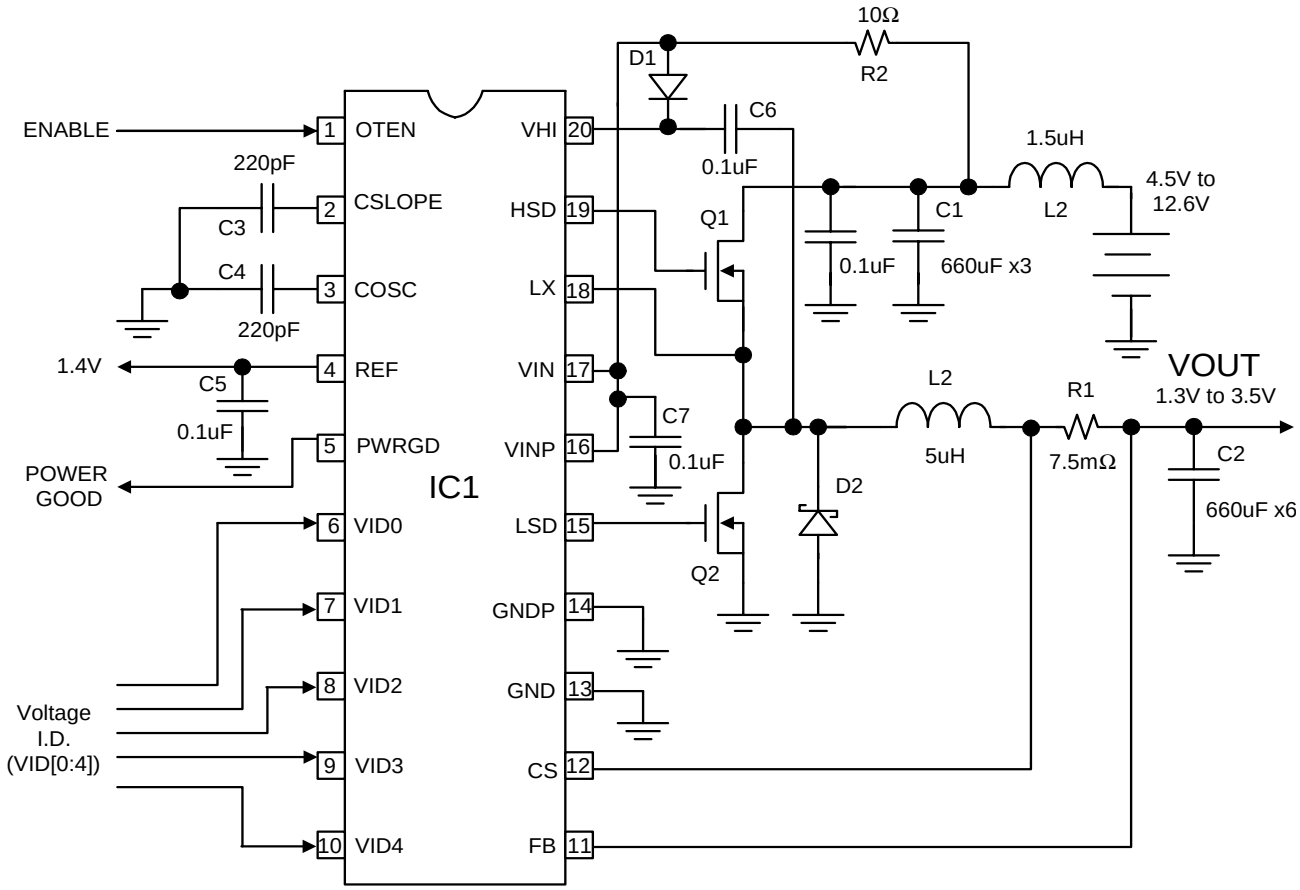


Figure 17. Elantech EL7571 Switching Power Supply Design

Contact Information.

Elantec Corporation
675 Trade Zone Blvd.
Milpitas, CA 95035-1323
Tel: (408) 945-1323
Fax: (408) 945-9305

www.elantec.com

Table 8. Elantec EL 7571 Bill of Materials

Reference	Description	Part Number	Manufacturer
C1, C2	680µF	LXF16VB681M10X20LL	United Chem-Con
C3, C4	220pF	Chip capacitor	any
C5, C6, C7	0.1µF	Chip capacitor	any
D1	Diode	BAV99	Motorola, et-al
D2	Diode	32CTQ030	International Rectifier
IC1	Controller	EL 7571CM	Elantec
L1	5.1µH	PE-53700	Pulse Engineering
L2	1.5µH	T30-26 7T AWG #20	Micro Metals
R1	15mΩ	WSL-2512	Dale
R2	10Ω	Chip resistor	any
R3	10Ω	Chip resistor	any
Q1, Q2	MOSFET	Si4410	Siliconix

Linear Technology LT1435

The LT1435 is designed to be configured as a synchronous buck converter with a minimum of external components. The input voltage can range from 4.5V to 24V (limited by the external MOSFETs). The circuit highlights the capabilities of the LTC1435, which uses a current mode, constant frequency architecture to switch a pair of N-channel power MOSFETs while providing 99% maximum duty cycle. Operating efficiencies exceeding 90% are obtained. Figure 18 on page 36 shows an LT1435 reference design that can deliver up to 6A. Vout = 1.19 (1 + R1/R2). Table 9 on page 37 shows the bill of materials for the LT1435.

Contact Information.

Linear Technology Corporation
1630 McCarthy Blvd.
Milpitas, CA 95035-7417
Tel: (408) 432-1900
Fax: (408) 434-0507

www.linear.com

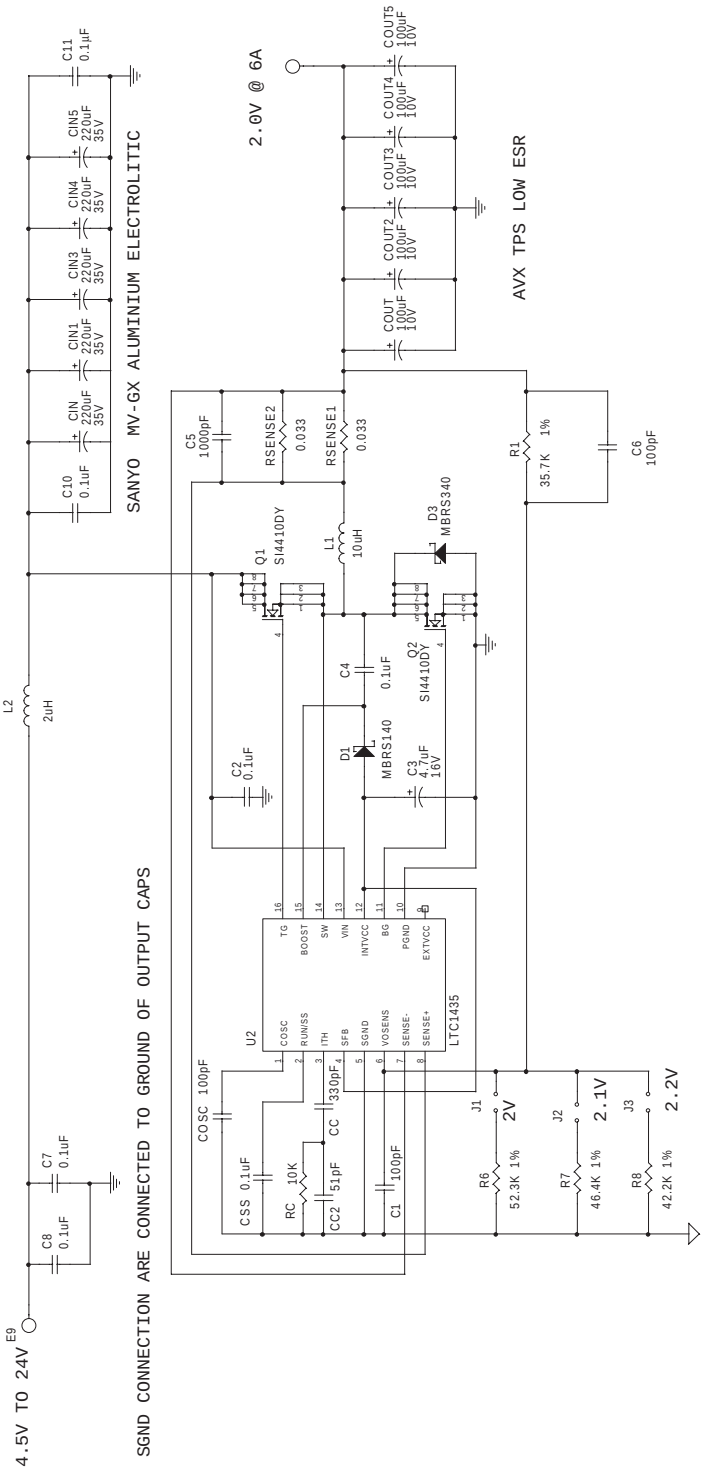


Figure 18. Linear LT1435 2.0V Switching Power Supply Design

Table 9. Linear LT1435 Bill Of Materials

Reference	Description	Part Number	Manufacturer
CC	330 pF 50 V 10% NPO chip capacitor	08055A331KAT1A	AVX
CC2	51 pF 50 V 10% NPO chip capacitor	08055A510KAT1A	AVX
CIN, CIN1, 3, 4, 5	220 µF 35 V 20% Alum Elec. capacitor	MV-GX	Sanyo
COUT1–5	100 µF 10 V 20% tantalum capacitor	TPSD107M010R0080	AVX
C1, C6, Cosc	100 pF 50 V 10% NPO chip capacitor	08055A101KAT1A	AVX
C2, C4, CSS, C7–8, C10–11	0.1 µF 50 V 10% Y5V chip capacitor	08055G104KAT1A	AVX
C3	4.7 µF 16 V 20% tantalum capacitor	TAJB475M016	AVX
C5	1000 pF 50 V 10% X7R chip capacitor	08055C102KAT1A	AVX
D1	BVR = 40 V – 1 A Schottky diode	MBRS150	Motorola
D2	BVR = 40 V – 3 A Schottky diode	MBRS340T3	Motorola
JP1	2 mm pin header	2802S-03-G2	Comm Con
JP2	2 mm pin header	2802S-10-G2	Comm Con
L1	10 µH inductor	BI HM77-25006 PE53663	BI Tech Pulse Engineering
L2	2 µH inductor EMI filter (optional)	DO3316P-222	Coil Craft
Q1, Q2	N-Channel MOSFET	Si4410DY	Siliconix
R1	35.7 k 1/10 W 1% chip resistor	CR21-3572F-T	AVX
R6	52.3 k 1/10 W 1% chip resistor	CR21-5232F-T	AVX
R7	46.4 k 1/10 W 1% chip resistor	CR21-4642F-T	AVX
R8	42.2 k 1/10 W 1% chip resistor	CR21-4222F-T	AVX
RC	10 k 1/10 W 5% chip resistor	CR21-103J-T	AVX
RSENSE	33 milli Ω 1/2 W 1% resistor	LR2010-01-R033-F	IRC
U1	16-Lead narrow small outline IC	LTC1435CS	LTC
	Jumper	CCIJ2mm-138-G	Comm Con

Maxim MAX798

The MAX798 current-mode converter shown in Figure 19 converts the input voltage (from the wall adapter or the battery pack) down to the desired 1.8V. The MAX798 can achieve efficiencies up to 96% and has an input-voltage rage of 4.5V to 30V. The input voltage is switched by the MOSFETs N1 and N2. This switched voltage is filtered by the LC filter, consisting of L1, C4, and C5. R1 and R2 divide the 1.8V output voltage to 1.6V for the feedback reference (Vout = 1.6V • (1 + R1/R2). The values in the bill of material (See Table 10 on page 39) provide 1.8V at 5.6A. The 560-pF capacitor improves stability by increasing the loop phase at crossover, which increases the phase margin. Maxim's MAX1710/11 has VID inputs.

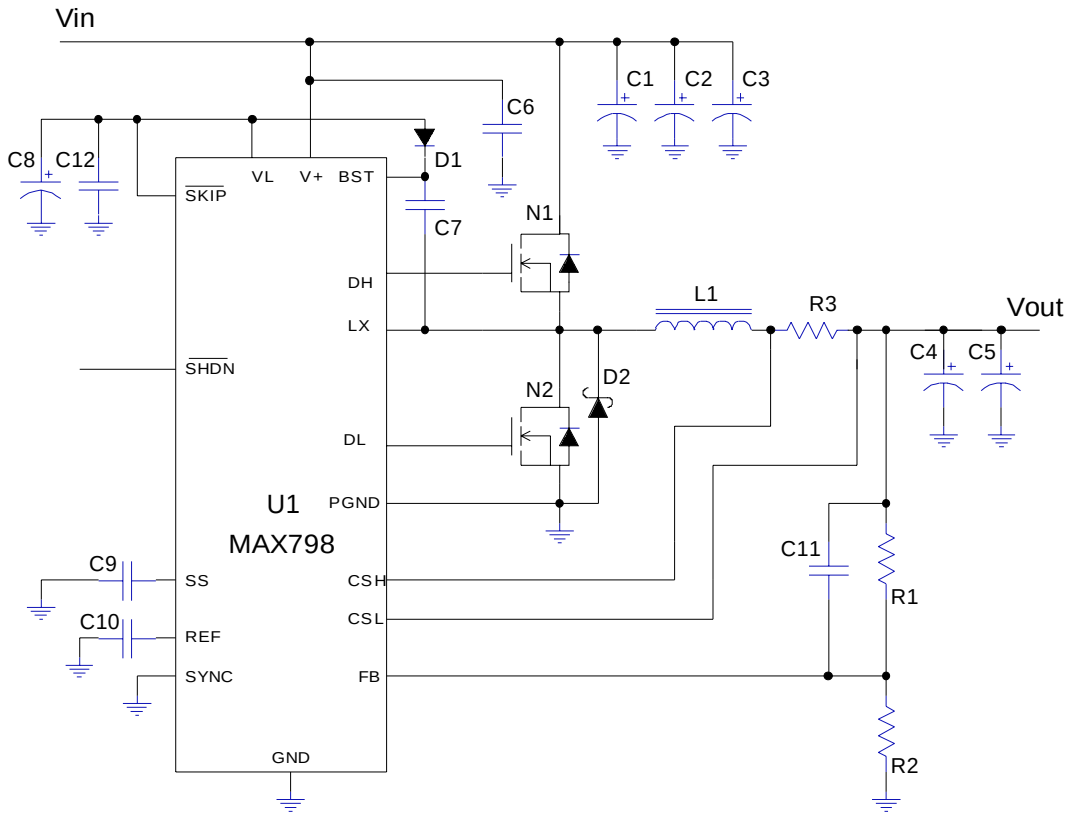


Figure 19. Maxim MAX798 Switching Power Supply Design

Contact Information.

Maxim Integrated Products
120 San Gabriel Drive
Sunnyvale, CA 92841
Tel: (408) 737-7600
Fax: (408) 737-7194

www.maxim-ic.com

Table 10. Maxim MAX798 Bill of Materials

Reference	Description	Part Number	Manufacturer
C1–C3	10µF 30V Os-Con capacitor	30SA10	Sanyo
C4, C5	470µF 4V low ESR capacitor	594D477X0004R2T	Sprague
C6, C7	0.1µF ceramic capacitor	any	any
C8	4.7µF 16V Low ESR Tantalum capacitor	595D475X0016A2B	Sprague
C9	0.01µF ceramic capacitor	any	any
C10	0.33µF ceramic capacitor	any	any
C11	560pF ceramic capacitor	any	any
C12	1.0µF ceramic capacitor	any	any
DS1	Schottky Diode, 100mA, 30V	CMPSH-3	Central Semi
DS2	Schottky Diode, 1A, 30V	MBRS130LT3	Motorola
L1	4.7µH inductor	CDRH127-4R7MC	Sumida
N1, N2	N-Channel MOSFET 30V	Si4412DY	Siliconix
R1	4.22k, 0.1% resistor	any	any
R2	16.9k, 0.1% resistor	any	any
R3	13mΩ 1% Current sense resistor *	WSL-2512-R013F	Dale
U1	DC-DC converter	MAX798ESE	Maxim

Note:
* *2.0 V at 6A.*

Voltage Regulator Vendor Information

Company Name and Contact	Part Number	Type	Remarks*
Cherry Contact: George Shuline (401)886-3821	CS5156	Switching Regulator	a) 5 bit VID 1.3 V min
Elantech Contact: Steve Sacarisen (408) 945-1323 x 345	EL7571	Switching Regulator	a) 5 bit VID 1.3 V min
Linear Technology Corporation Contact: Mike Gillespie (408) 428-2060	LT1435/36/37 LT1439/1339 LTC1538/39	Switching Regulator Switching Regulator Switching Regulator	a) Voltage set by resistors b) Voltage set by resistors c) Voltage set by resistors
Maxim Integrated Products Contact: Nancie George-Adeh (408) 737-7600	MAX798 MAX1630/31/32 MAX1710/11	Switching Regulator Switching Regulator Switching Regulator	a) Voltage set by resistors b) Voltage set by resistors c) 4bit/bit DAC 0.925V min
Micro Linear Contact: Doyle Slack (408) 433-5200	ML4880	Switching Regulator	
Semtech Corporation Contact: Alan Moore (805) 498-2111	SC1401	Switching Regulator	Voltage set by resistors
STMicroelectronics 20041 Agrate Brianza -Italy Via C. Olivetti, 2 Contact: Nicola Tricomi Tel. +39 039 6036512	L4992 L5955	Switching Regulator Switching Regulator	a) Voltage set by resistors b) 4bit/bit DAC 1.35V min., 2.0V max.
Unitrode Contact: John O'Connor (603) 429-8504 www.unitrode.com	UCC3870-1	Switching Regulator	Voltage set by resistors or external DAC—input range 4–36 volts

Note:

* *These regulators all have a wide input-voltage range*