Am29SL400C

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **Am29SL400C** Revision **A** Amendment **+5** Issue Date **March 3, 2005**

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ADVANCE INFORMATION

Am29SL400C

4 Megabit (512 K x 8-Bit/256 K x 16-Bit) CMOS 1.8 Volt-only Super Low Voltage Flash Memory

Distinctive Characteristics

- **Single power supply operation**
  - 1.65 to 2.2 V for read, program, and erase operations
  - Ideal for battery-powered applications
- **Manufactured on 0.32 µm process technology**
- **High performance**
  - Access times as fast as 100 ns
- **Ultra low power consumption (typical values at 5 MHz)**
  - 1 µA Automatic Sleep Mode current
  - 1 µA standby mode current
  - 5 mA read current
  - 20 mA program/erase current
- **Flexible sector architecture**
  - One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and seven 64 Kbyte sectors (byte mode)
  - One 8 Kword, two 4 Kword, one 16 Kword, and seven 32 Kword sectors (word mode)
  - Supports full chip erase
  - Sector Protection features:
    A hardware method of locking a sector to prevent any program or erase operations within that sector
    Sectors can be locked in-system or via programming equipment
    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - Reduces overall programming time when issuing multiple program command sequences
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 erase cycle guarantee per sector**
- **20-year data retention at 125°C**
- **Package option**
  - 48-ball FBGA
  - 48-pin TSOP
- **Compatibility with JEDEC standards**
  - Pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - Hardware method to reset the device to reading array data

Publication# **Am29SL400C** Rev: **A** Amendment**+5**

General Description

The Am29SL400C is an 4Mbit, 1.8 V volt-only Flash memory organized as 524,288 bytes or 262,144 words. The device is offered in 48-pin TSOP and 48-ball FBGA packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed and erased in-system with a single 1.8 volt V_{CC} supply. No V_{PP} is required for write or erase operations. The device can also be programmed in standard EPROM programmers.

The standard device offers access times of 100, 110, 120, and 150 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 1.8 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

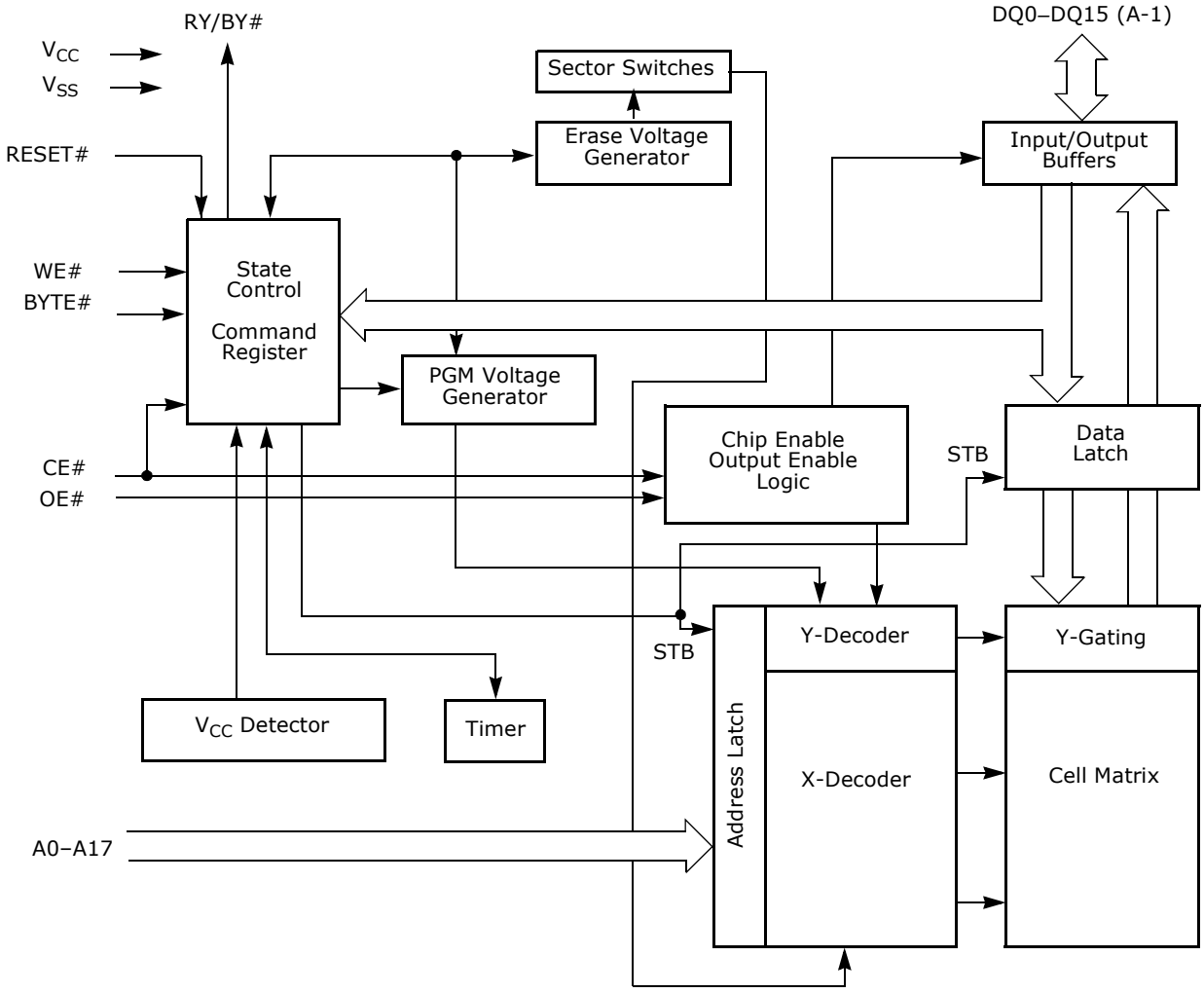
Table of Contents

Product Selector Guide

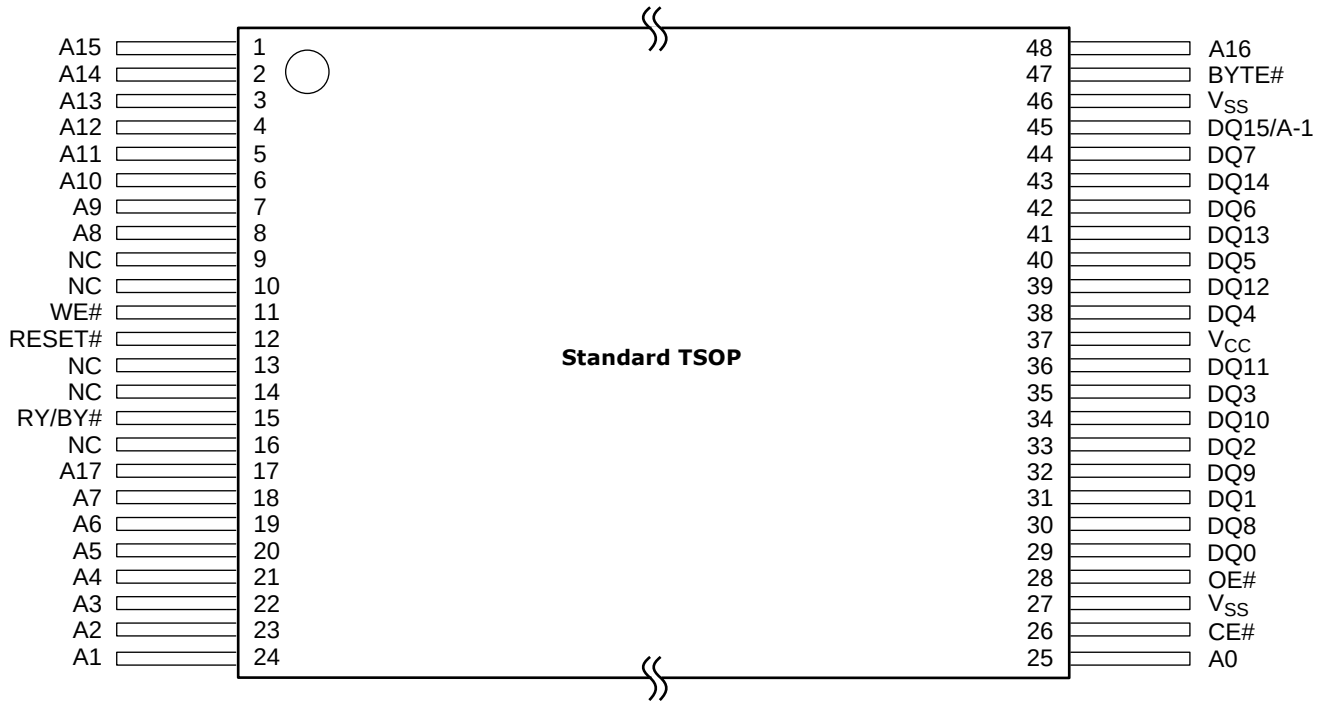
Family Part Number		Am29SL400C			
Speed Options	Regulated Voltage Range V_{CC} = 1.7–2.2 V	**-100R**			
	Standard Voltage Range V_{CC} = 1.65–2.2 V		**-110**	**-120**	**-150**
Max access time, ns (t_{ACC})		100	110	120	150
Max CE# access time, ns (t_{CE})		100	110	120	150
Max OE# access time, ns (t_{OE})		35	45	50	65

Note: *See "AC Characteristics" for full specifications.*

Block Diagram



Connection Diagrams



Connection Diagram

48-Ball FBGA
(Top View, Balls Facing Down)

A6	B6	C6	D6	E6	F6	G6	H6
A13	A12	A14	A15	A16	BYTE#	DQ15/A-1	V_{SS}
A5	B5	C5	D5	E5	F5	G5	H5
A9	A8	A10	A11	DQ7	DQ14	DQ13	DQ6
A4	B4	C4	D4	E4	F4	G4	H4
WE#	RESET#	NC	NC	DQ5	DQ12	V_{CC}	DQ4
A3	B3	C3	D3	E3	F3	G3	H3
RY/BY#	NC	NC	NC	DQ2	DQ10	DQ11	DQ3
A2	B2	C2	D2	E2	F2	G2	H2
A7	A17	A6	A5	DQ0	DQ8	DQ9	DQ1
A1	B1	C1	D1	E1	F1	G1	H1
A3	A4	A2	A1	A0	CE#	OE#	V_{SS}

Special Handling Instructions for FBGA Packages

Special handling is required for Flash Memory products in molded packages (TSOP, BGA, PLCC, PDIP, SSOP). The package and/or data integrity may be compromised if the package body is exposed to temperatures about 150°C for prolonged periods of time.

Pin Configuration

A0–A17 = 18 addresses

DQ0–DQ14= 15 data inputs/outputs

DQ15/A-1 = DQ15 (data input/output, word mode),
A-1 (LSB address input, byte mode)

BYTE# = Selects 8-bit or 16-bit mode

CE# = Chip enable

OE# = Output enable

WE# = Write enable

RESET# = Hardware reset pin, active low

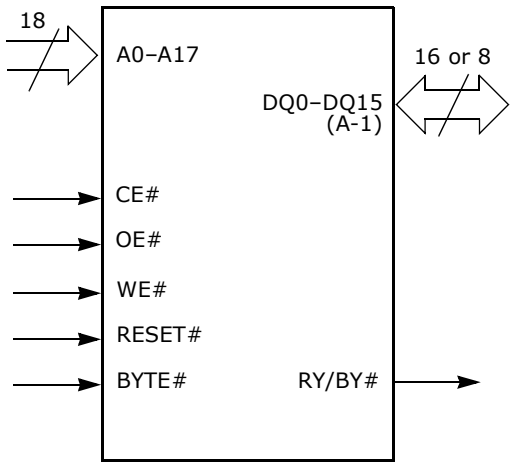
RY/BY# = Ready/Busy# output

V_{CC} = 1.65–2.2 V single power supply

V_{SS} = Device ground

NC = Pin not connected internally

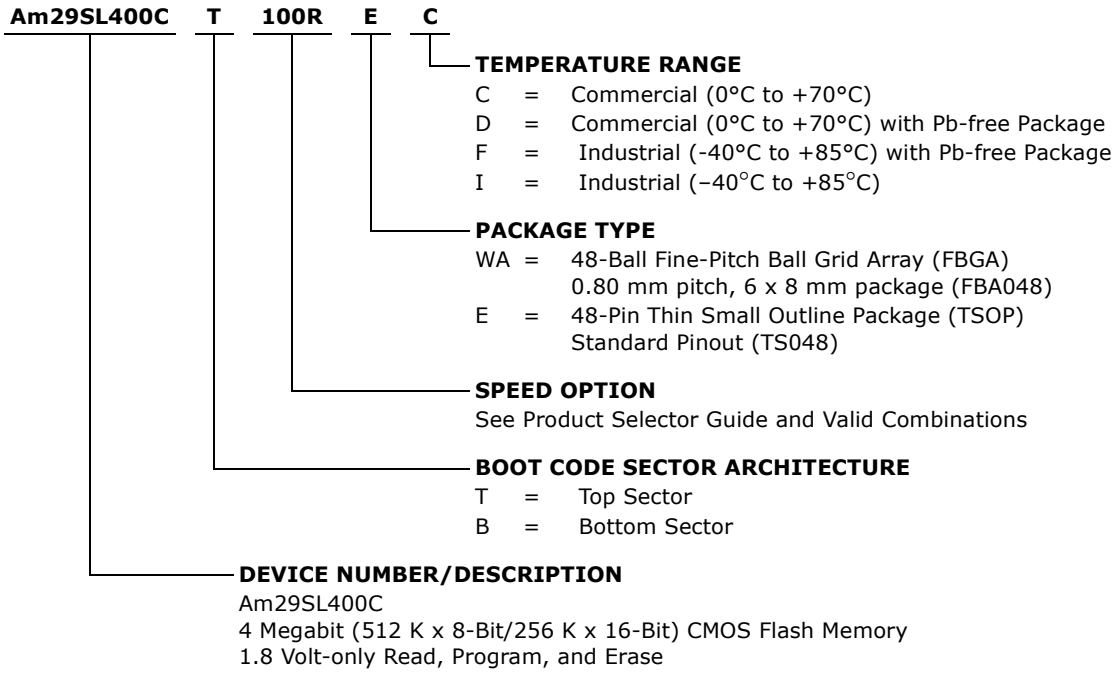
Logic Symbol



Ordering Information

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations for TSOP Packages	
Order Number	
AM29SL400CT100R, AM29SL400CB100R	EC, EI, ED, EF
AM29SL400CT110, AM29SL400CB110	
AM29SL400CT120, AM29SL400CB120	
AM29SL400CT150, AM29SL400CB150	

Valid Combinations for FBGA Packages			
Order Number		**Package Marking**	
AM29SL400CT100R, AM29SL400CB100R	WAC WAI WAD, WAF	A400CT10R, A400CB10R	C, I, D, F
AM29SL400CT110, AM29SL400CB110		A400CT11V, A400CB11V	
AM29SL400CT120, AM29SL400CB120		A400CT12V, A400CB12V	
AM29SL400CT150, AM29SL400CB150		A400CT15V, A400CB15V	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29SL400C Device Bus Operations

Operation	CE#	OE#	WE #	RESET#	Addresses (Note 1)	DQ0–DQ7	DQ8–DQ15	
							BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	
Standby	$V_{CC} \pm 0.2$ V	X	X	$V_{CC} \pm 0.2$ V	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	Sector Address, A6 = H, A1 = H, A0 = L	D_{IN}	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	High-Z

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 10 ± 1.0 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:

1. *Addresses are A17:A0 in word mode (BYTE# = V_{IH}), A17:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Protection/Unprotection" section.*

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See *Reading Array Data, on page 14* for more information. Refer to the AC Read Operations table for timing specifications and to Figure 14, on page 28 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to *Word/Byte Configuration, on page 9* for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The *Word/Byte Program Command Sequence, on page 15* has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 on page 11 and Table 3 on page 11 indicate the address space that each sector occupies. A *sector address* consists of the address bits required to uniquely select a sector. *Command Definitions, on page 18* has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to *Autoselect Mode, on page 11* and *Autoselect Command Sequence, on page 15* for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The *AC Characteristics, on page 28* contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to *Write Operation Status, on page 18* for more information, and to *AC Characteristics, on page 28* for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.2$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.2$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

The device also enters the standby mode when the RESET# pin is driven low. Refer to the next section, RESET#: Hardware Reset Pin.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in *DC Characteristics, on page 24* represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 50 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.2$ V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.2$ V, the standby current is greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a *0* (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is *1*), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 15, on page 29 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Am29SL400CT Top Boot Block Sector Address Table

Sector	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
								(x8) Address Range	(x16) Address Range
SA0	0	0	0	X	X	X	64/32	00000h–0FFFFh	00000h–07FFFh
SA1	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
SA2	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
SA3	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
SA4	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
SA5	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
SA6	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
SA7	1	1	1	0	X	X	32/16	70000h–77FFFh	38000h–3BFFFh
SA8	1	1	1	1	0	0	8/4	78000h–79FFFh	3C000h–3CFFFh
SA9	1	1	1	1	0	1	8/4	7A000h–7BFFFh	3D000h–3DFFFh
SA10	1	1	1	1	1	X	16/8	7C000h–7FFFFh	3E000h–3FFFFh

Table 3. Am29SL400CB Bottom Boot Block Sector Address Table

Sector	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
								(x8) Address Range	(x16) Address Range
SA0	0	0	0	0	0	X	16/8	00000h–03FFFh	00000h–01FFFh
SA1	0	0	0	0	1	0	8/4	04000h–05FFFh	02000h–02FFFh
SA2	0	0	0	0	1	1	8/4	06000h–07FFFh	03000h–03FFFh
SA3	0	0	0	1	X	X	32/16	08000h–0FFFFh	04000h–07FFFh
SA4	0	0	1	X	X	X	64/32	10000h–1FFFFh	08000h–0FFFFh
SA5	0	1	0	X	X	X	64/32	20000h–2FFFFh	10000h–17FFFh
SA6	0	1	1	X	X	X	64/32	30000h–3FFFFh	18000h–1FFFFh
SA7	1	0	0	X	X	X	64/32	40000h–4FFFFh	20000h–27FFFh
SA8	1	0	1	X	X	X	64/32	50000h–5FFFFh	28000h–2FFFFh
SA9	1	1	0	X	X	X	64/32	60000h–6FFFFh	30000h–37FFFh
SA10	1	1	1	X	X	X	64/32	70000h–7FFFFh	38000h–3FFFFh

Note for Tables 2 and 3: *Address range is A17:A-1 in byte mode and A17:A0 in word mode. See "Word/Byte Configuration" section for more information.*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires VID on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 4 on page 12. In addition, when verifying sector protection, the sector address must appear on the appro-

priate highest order address bits (see Table 2 on page 11 and Table 3 on page 11). Table 4 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 5 on page 18. This method does not require VID. See *Command Definitions, on page 18* for details on using the autoselect mode.

Table 4. Am29SL400C Autoselect Codes (High Voltage Method)

Description	Mode	CE#	OE#	WE#	A17 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: AMD		L	L	H	X	X	V_{ID}	X	L	X	L	L	X	01h
Device ID: Am29SL400C (Top Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	70h
	Byte	L	L	H									X	70h
Device ID: Am29SL400C (Bottom Boot Block)	Word	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	F1h
	Byte	L	L	H									X	F1h
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	H	L	X	01h (protected)
													X	00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented via two methods.

Sector protection/unprotection requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2, on page 14 shows the algorithms and Figure 24, on page 37 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See *Autoselect Mode, on page 11* for details.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 3, on page 16 shows the algorithm, and Figure 22 shows the timing diagrams, for this feature.

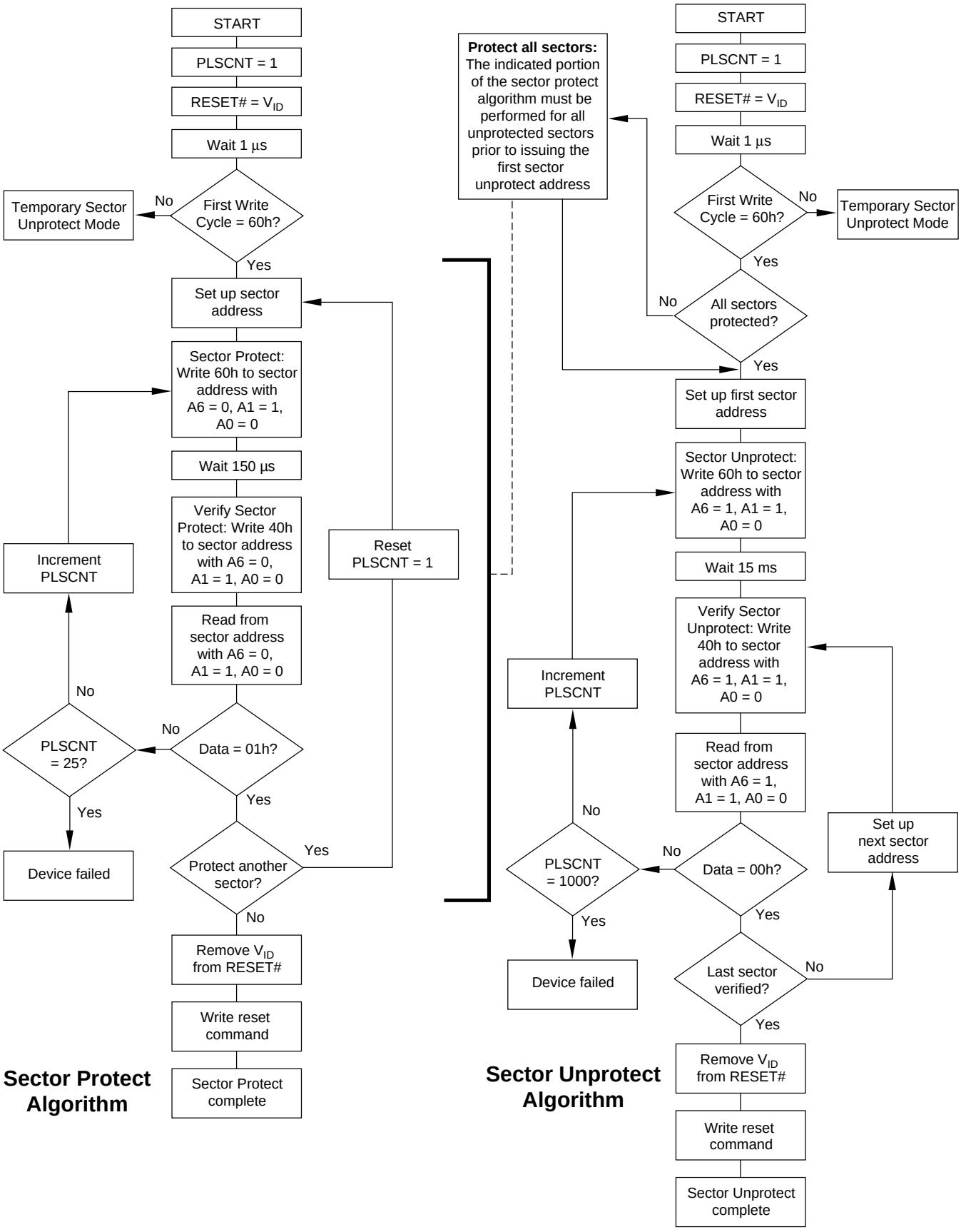
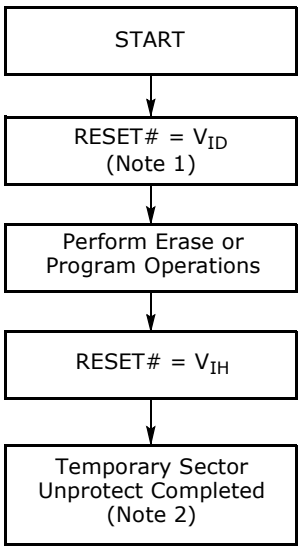


Figure 1. In-System Sector Protect/Unprotect Algorithms



Notes:

1. *All protected sectors unprotected.*
2. *All previously protected sectors are protected once again.*

Figure 2. Temporary Sector Unprotect Operation

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 5 on page 18 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 5 on page 18 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the *AC Characteristics* section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the *Reset Command, on page 14* section, next.

See also *Requirements for Reading Array Data, on page 9* for more information. The Read Operations table provides the read parameters, and Figure 14, on page 28 shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the de-

vice ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 5 on page 18 shows the address and data requirements. This method is an alternative to that shown in Table 4 on page 12, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address 01h in word mode (or 02h in byte mode) returns the device code. A read cycle containing a sector address (SA) and the address 02h in word mode (or 04h in byte mode) returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table 2 on page 11 and Table 3 on page 11 for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Word/Byte Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 5 on page 18 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See *Write Operation Status, on page 18* for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

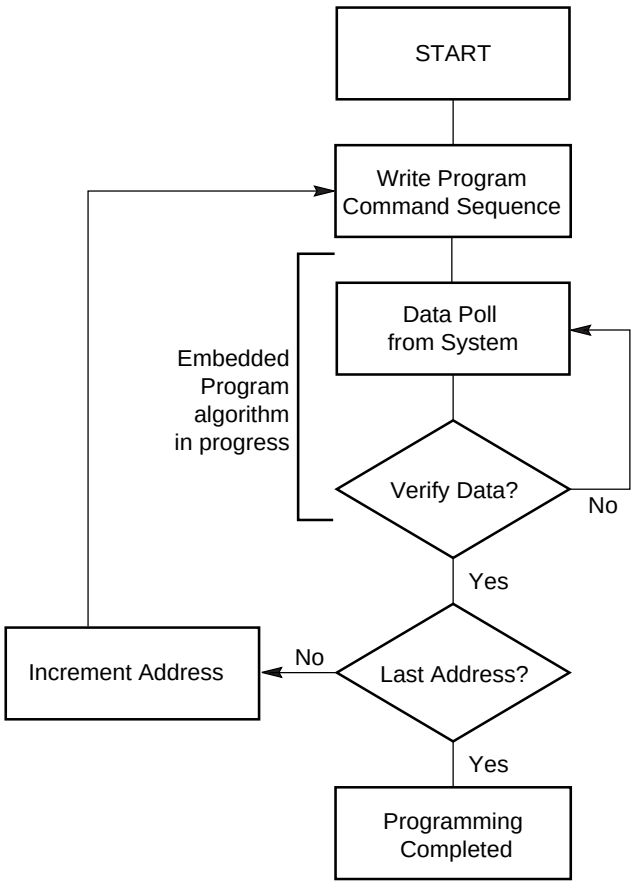
Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a *0* back to a *1*.** Attempting to do so may halt the operation and set DQ5 to *1*, or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still *0*. Only erase operations can convert a *0* to a *1*.

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 5 on page 18 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't cares. The device then returns to reading array data.

Figure 3, on page 16 illustrates the algorithm for the program operation. See *Erase/Program Operations, on page 30* for parameters, and Figure 17, on page 31 for timing diagrams.



Note: *See Table 5 for program command sequence.*

Figure 3. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 5 on page 18 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. Note that a **hardware reset** during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. See *Write Operation Status, on page 18* for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 4, on page 17 illustrates the algorithm for the erase operation. See *Erase/Program Operations, on page 30* for parameters, and to Figure 18 for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table 5 on page 18 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. Note that a **hardware reset** during the sector erase operation immediately terminates the operation. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. (Refer to *Write Operation Status, on page 18* for information on these status bits.)

Figure 4 illustrates the algorithm for the erase operation. Refer to the *Erase/Program Operations, on page 30* for parameters, and to Figure 18, on page 32 for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are *don't-cares* when writing the Erase Suspend command.

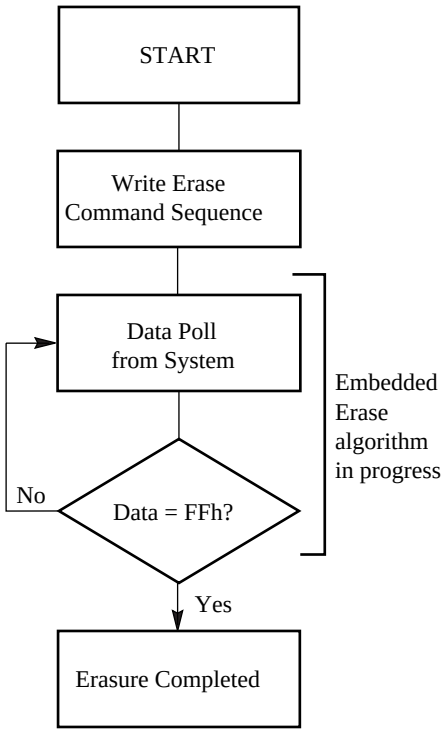
When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device *erase suspends* all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See *Write Operation Status, on page 18* for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See *Write Operation Status, on page 18* for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See *Autoselect Command Sequence, on page 15* for more information.

The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.



Notes:

1. *See Table 5 on page 18 for erase command sequence.*
2. *See DQ3: Sector Erase Timer, on page 21 for more information.*

Figure 4. Erase Operation

Command Definitions

Table 5. Am29SL400C Command Definitions

Command Sequence (Note 1)			Cycles	Bus Cycles (Notes 2-5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	01				
		Byte		AAA		555		AAA							
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	555	90	X01	70h				
		Byte		AAA		555		AAA		X02	70h				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	555	90	X01	FIh				
		Byte		AAA		555		AAA		X02	FIh				
	Sector Protect Verify (Note 9)	Word	4	555	AA	2AA	55	555	90	(SA) X02	XX00				
											XX01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 10)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)			2	XXX	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend (Note 12)			1	XXX	B0										
Erase Resume (Note 13)			1	XXX	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A17–A12 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except when reading array or autoselect data, all bus cycles are write operations.*
4. *Data bits DQ15–DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A17–A11 are don't cares for unlock and command cycles, unless SA or PA required.*
6. *No unlock or command cycles required when reading array data, unless SA or PA required.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth cycle of the autoselect command sequence is a read cycle.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.*
10. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
11. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
12. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
13. *The Erase Resume command is valid only during the Erase Suspend mode.*

Write Operation Status

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 6 on page 22 and the following

subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

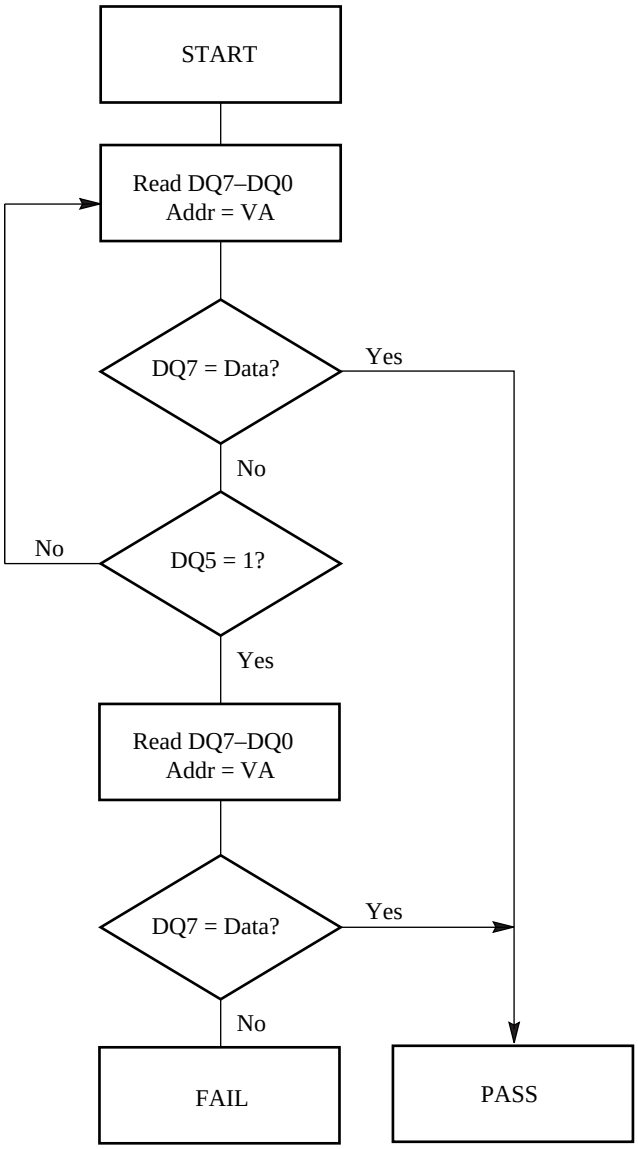
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a *0* on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a *1* on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to *1*; prior to this, the device outputs the *complement*, or *0.* The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. Figure 19, on page 33 Data# Polling Timings (During Embedded Algorithms), illustrates this.

Table 6 on page 22 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.*

Figure 5. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes program-

ming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 6 on page 22 shows the outputs for RY/BY#. Figure 14, on page 28, Figure 17, on page 31, and Figure 18, on page 32 shows RY/BY# for reset, program, and erase operations, respectively.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle (The system may use either OE# or CE# to control the read cycles). When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on *DQ7: Data# Polling, on page 19*).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 6 on page 22 shows the outputs for Toggle Bit I on DQ6. Figure 6, on page 21 shows the toggle bit algorithm. Figure 20, on page 33 shows the toggle bit timing diagrams. Figure 21 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on *DQ2: Toggle Bit II, on page 20*.

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. The device toggles DQ2 with each OE# or CE# read cycle.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 6 on page 22 to compare outputs for DQ2 and DQ6.

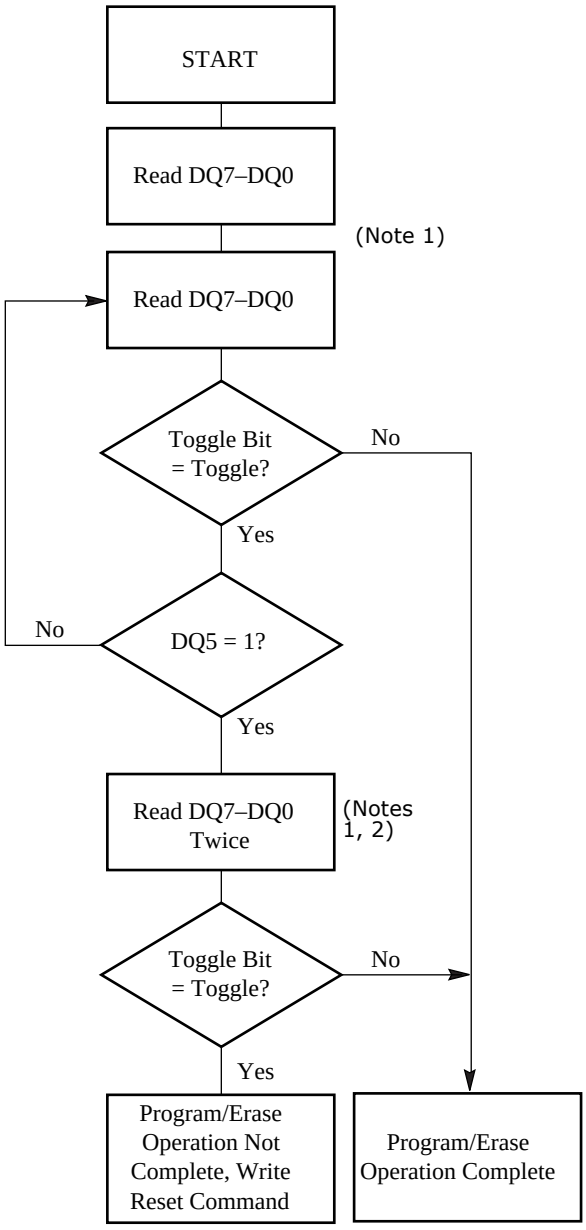
Figure 6, on page 21 shows the toggle bit algorithm in flowchart form, and the section *DQ2: Toggle Bit II, on page 20* explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 20, on page 33 shows the toggle bit timing diagram. Figure 21, on page 34 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 6, on page 21 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6, on page 21).



Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to* 1. *See text.*

Figure 6. Toggle Bit Algorithm

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit.

Under these conditions DQ5 produces a *1*. This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a *1* to a location that is previously programmed to "0." **Only an erase operation can change a *0* back to a *1*.** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a *1*.

Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from *0* to *1*. If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also *Sector Erase Command Sequence, on page 16*.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is *1*, the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is *1*, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 6 on page 22 shows the outputs for DQ3.

Table 6. Write Operation Status

Operation		DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to 1 when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See* *DQ5: Exceeded Timing Limits, on page 21* *for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

Absolute Maximum Ratings

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground
. . . . . V_{CC} (Note 1) –0.5 V to +2.5 V
. . . . . A9, OE#, and RESET# (Note 2) . . . . . –0.5 V to +11.0 V
. . . . . All other pins (Note 1) –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . 100 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is –0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See. Maximum DC input voltage on pin A9 is +11.0 V which may overshoot to 12.5 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

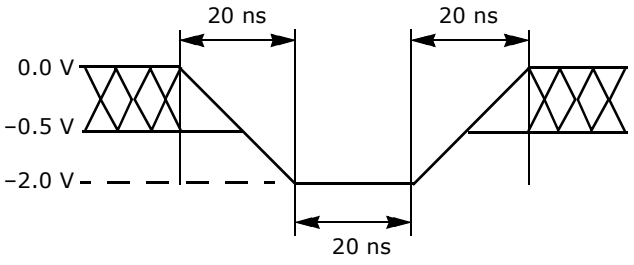


Figure 7. Maximum Negative Overshoot Waveform

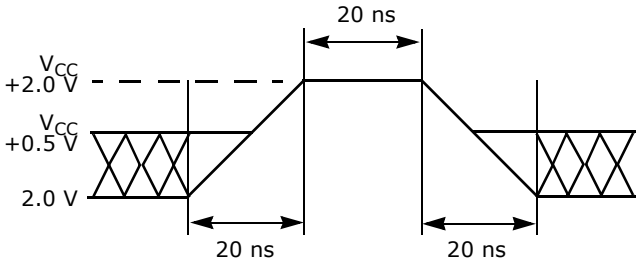


Figure 8. Maximum Positive Overshoot Waveform

Operating Ranges

Commercial (C) Devices

Ambient Temperature (T_A). . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A). . . . . –40°C to +85°C

V_{CC} Supply Voltages

V_{CC} for full voltage range . . . . . +1.65 V to +2.2 V

V_{CC} for regulated voltage range . +1.70 V to +2.2 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics

CMOS Compatible

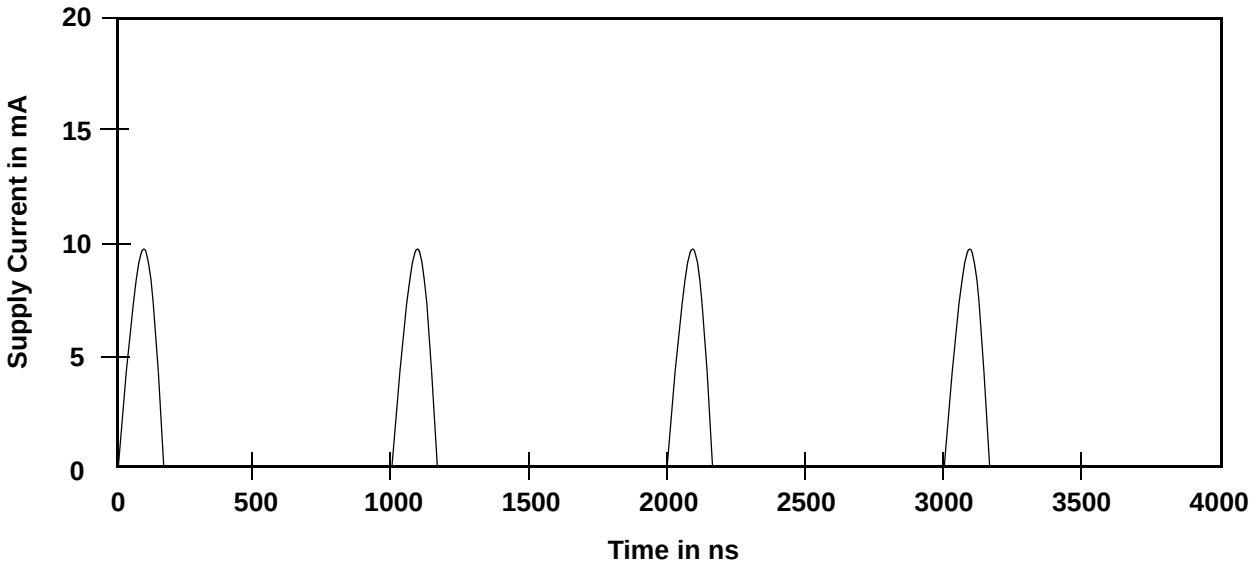
Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 11.0 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		5	10	mA
			1 MHz		1	3	
		CE# = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		5	10	
			1 MHz		1	3	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3, 5)	CE# = V_{IL}, OE# = V_{IH}			20	25	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, RESET# = V_{CC} ± 0.2 V			1	5	µA
I_{CC4}	V_{CC} Reset Current (Note 2)	RESET# = V_{SS} ± 0.2 V			1	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 3)	$V_{IH} = V_{CC}$ ± 0.2 V; $V_{IL} = V_{SS}$ ± 0.2 V			1	5	µA
V_{IL}	Input Low Voltage			–0.5		0.2 x V_{CC}	V
V_{IH}	Input High Voltage			0.8 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 2.0 V		9.0		11.0	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.0 mA, $V_{CC} = V_{CC\ min}$				0.25	V
V_{OL2}		I_{OL} = 100 µA, $V_{CC} = V_{CC\ min}$				0.1	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.7 x V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.1			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 4)			1.2		1.5	V

Notes:

1. *The I_{CC} current listed is typically less than 1 mA/MHz, with OE# at V_{IH}. Typical V_{CC} is 2.0 V.*
2. *The maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 50 ns.*
5. *Not 100% tested.*

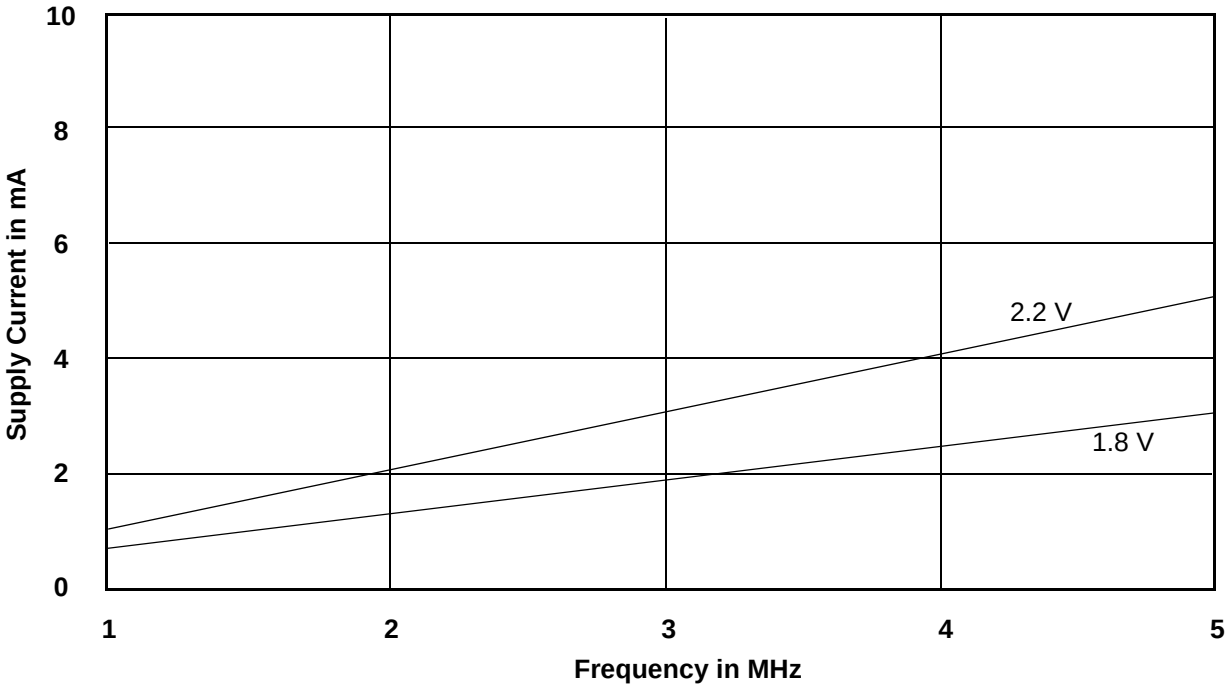
DC Characteristics (Continued)

Zero Power Flash



Note: *Addresses are switching at 1 MHz*

Figure 9. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

Figure 10. Typical I_{CC1} vs. Frequency

Test Conditions

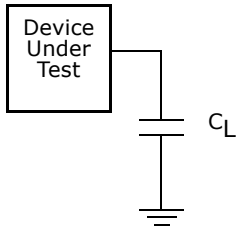


Figure 11. Test Setup

Table 7. Test Specifications

Test Condition	All Speed Options	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–2.0	V
Input timing measurement reference levels	1.0	V
Output timing measurement reference levels	1.0	V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Figure 12. Input Waveforms and Measurement Levels

AC Characteristics

Read Operations

Parameter		Description		Test Setup		Speed Options				Unit
JEDEC	Std					-100R	-110	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	100	110	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	100	110	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	100	110	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	35	45	50	65	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	16				ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	16				ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	30				ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0				ns

Notes:

1. *Not 100% tested.*
2. *See Figure 11, on page 26 and Table 7 on page 26 for test specifications.*

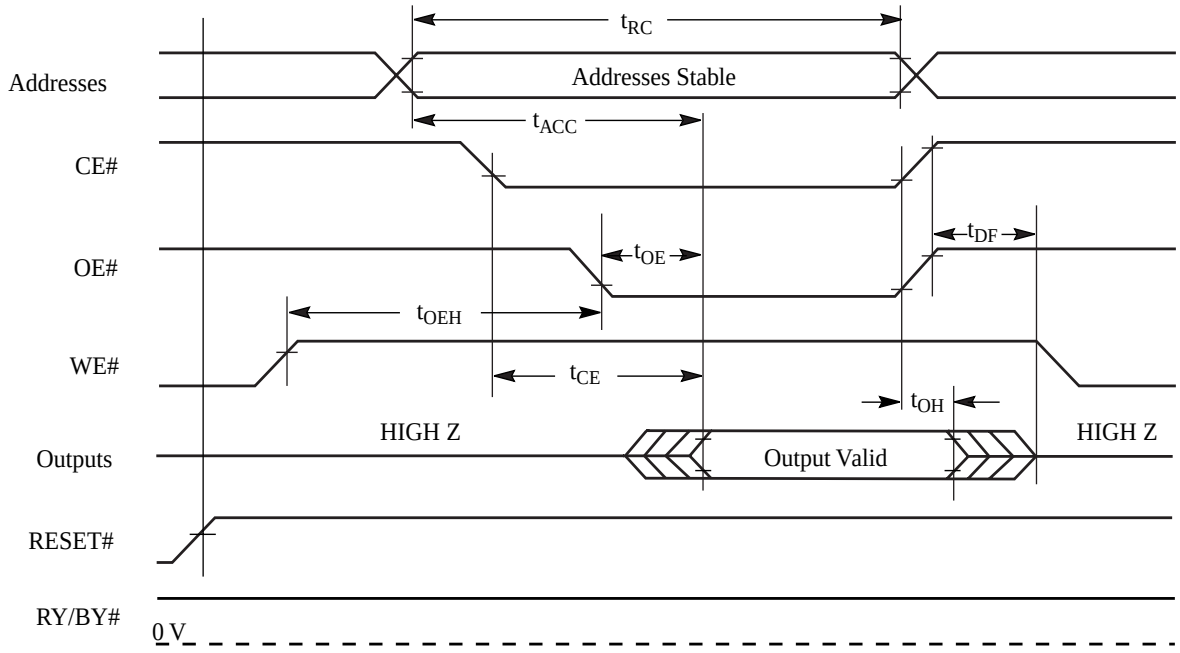


Figure 13. Read Operations Timings

AC Characteristics

Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	200	ns
	t_{RPD}	RESET# Low to Standby Mode		Min	20	µs
	t_{RB}	RY/BY# Recovery Time		Min	0	ns

Note: *Not 100% tested.*

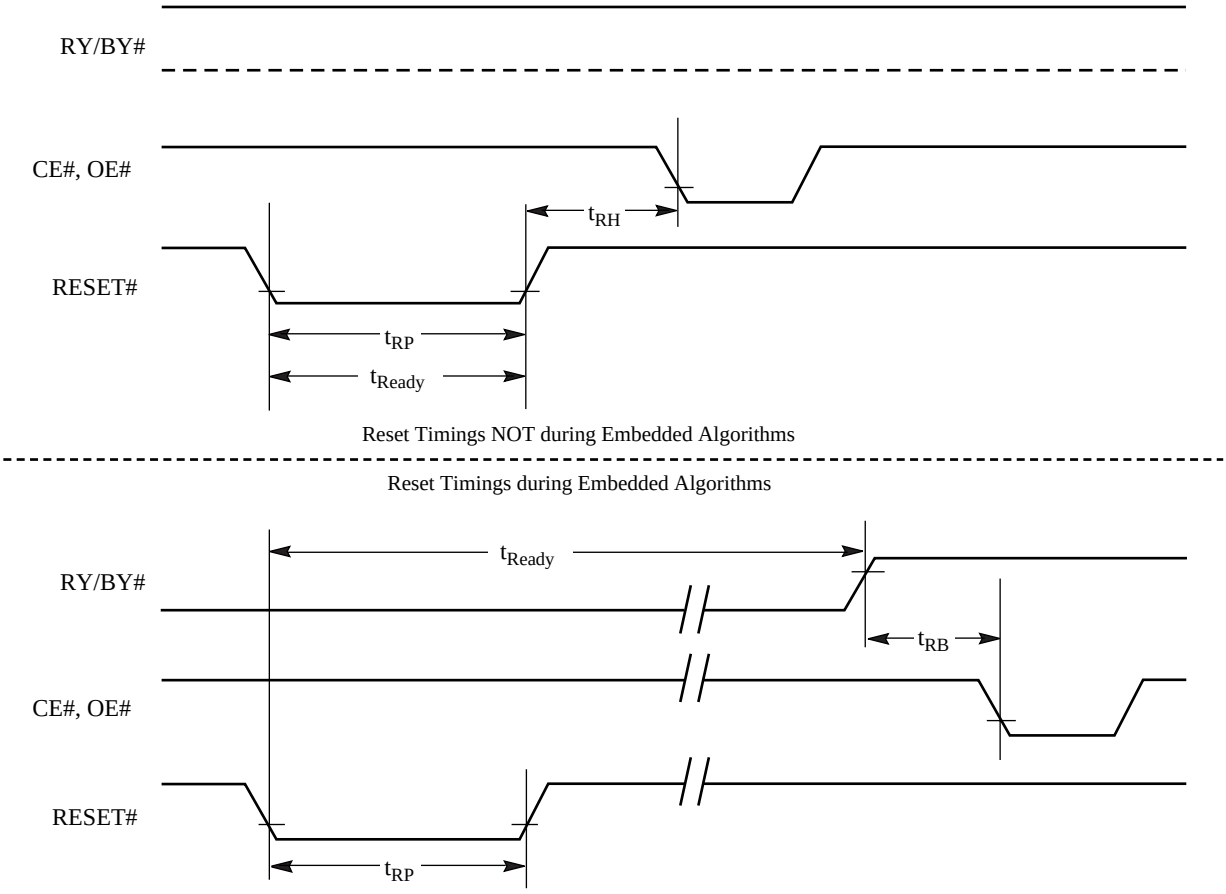


Figure 14. RESET# Timings

AC Characteristics

Word/Byte Configuration (BYTE#)

Parameter		Description		Speed Options				Unit
JEDEC	Std			-100R	-110	-120	-150	
	t_{ELFL}/t_{ELFH}	CE# to BYTE# Switching Low or High	Max	10				ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	50	55	60	60	ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	100	110	120	150	ns

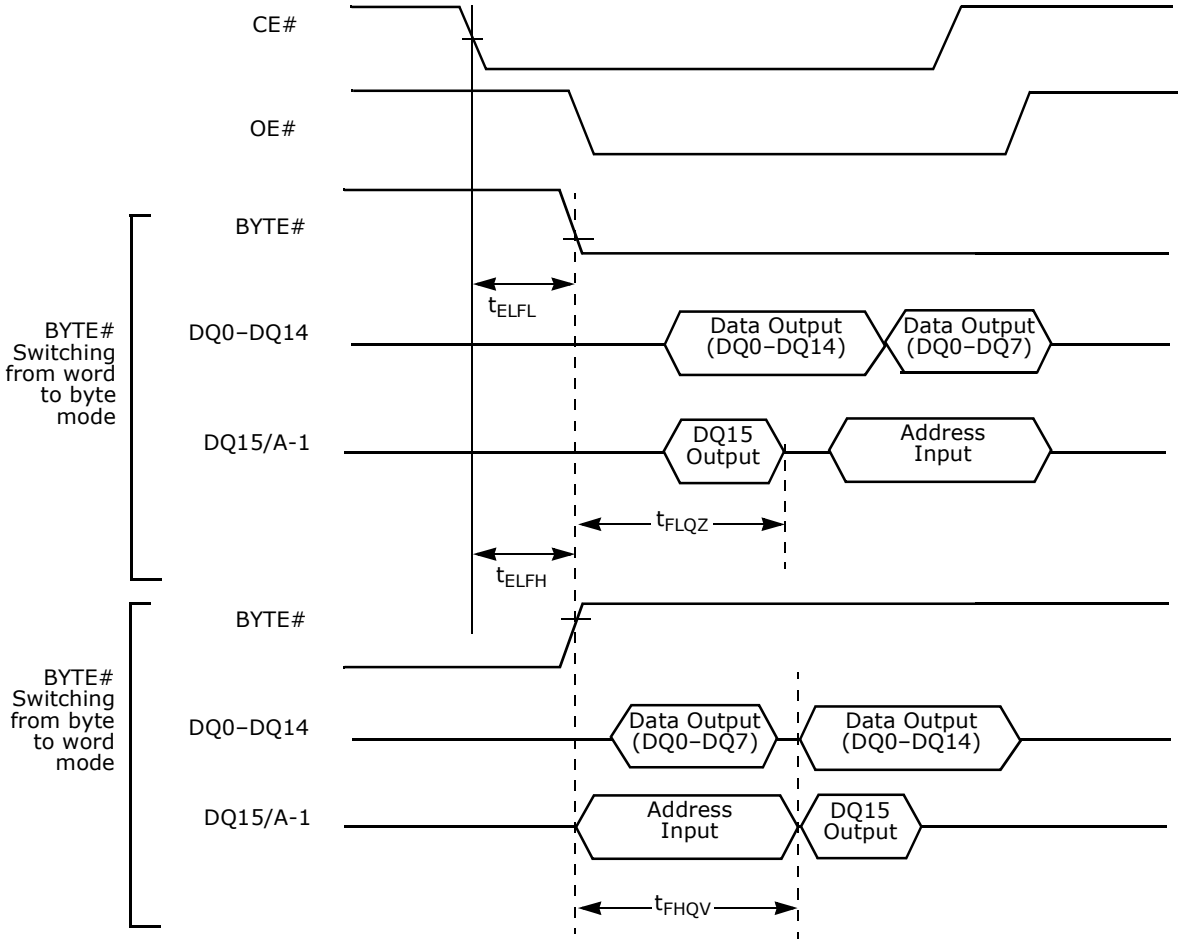
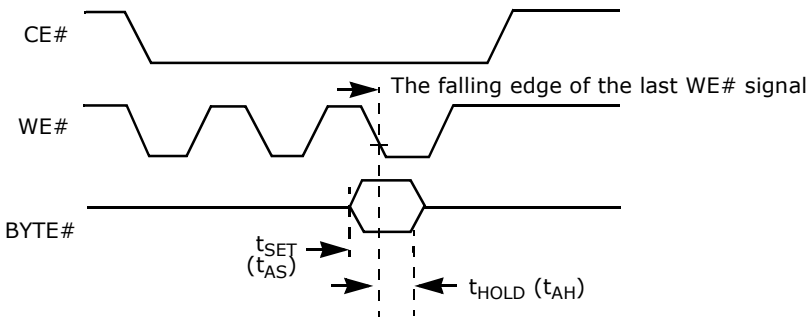


Figure 15. BYTE# Timings for Read Operations



Note: *Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.*

Figure 16. BYTE# Timings for Write Operations

AC Characteristics

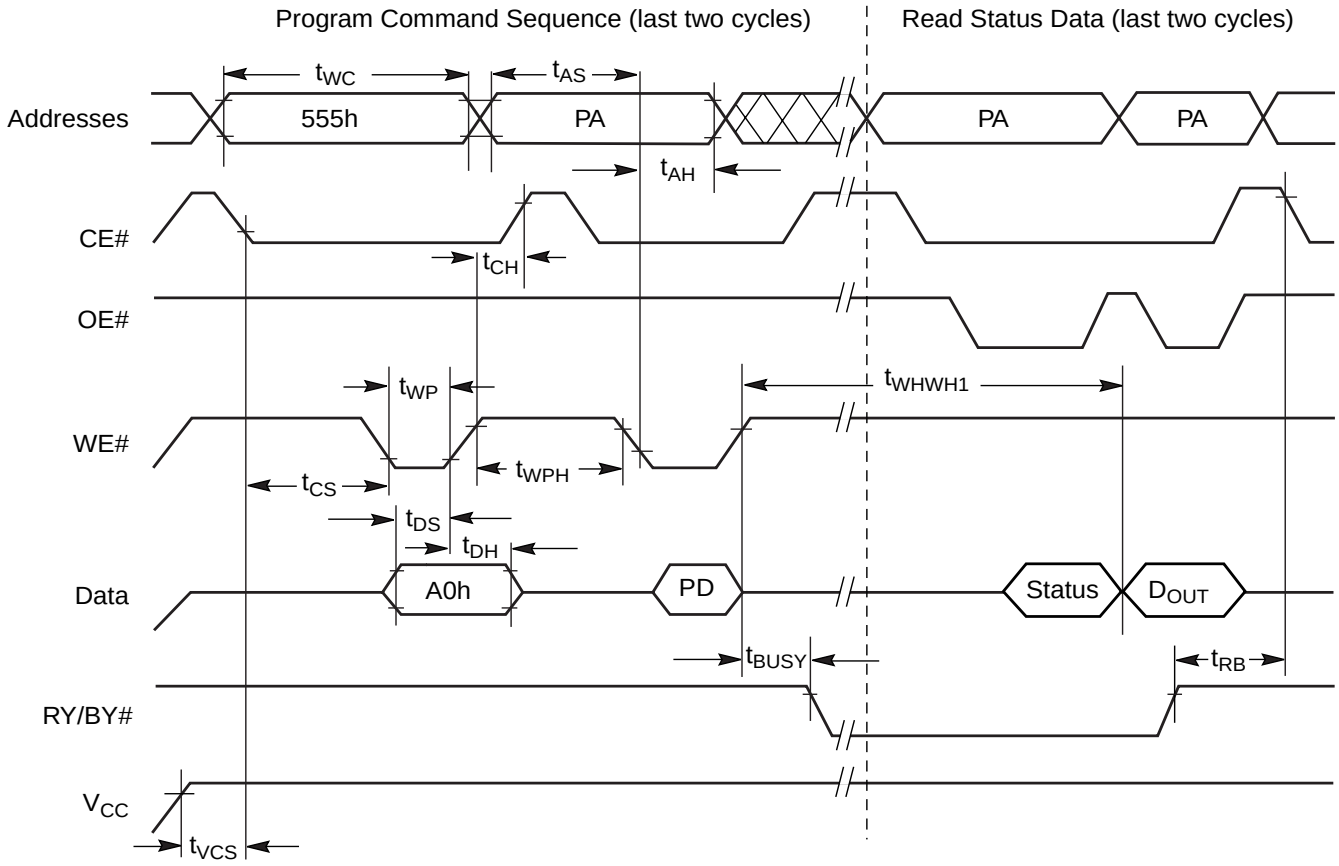
Erase/Program Operations

Parameter		Description			Speed Options				Unit
JEDEC	Std				-100R	-110	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	100	110	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	50	55	60	70	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	50	55	60	70	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OES}	Output Enable Setup Time		Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	50	55	60	70	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Notes 1, 2)	Byte	Typ	10				µs
			Word	Typ	12				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Notes 1, 2)		Typ	2				sec
	t_{VCS}	V_{CC} Setup Time		Min	50				µs
	t_{RB}	Recovery Time from RY/BY#		Min	0				ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Min	200				ns

Notes:

1. *Not 100% tested.*
2. *See the* *Erase and Programming Performance, on page 38* *section for more information.*

AC Characteristics

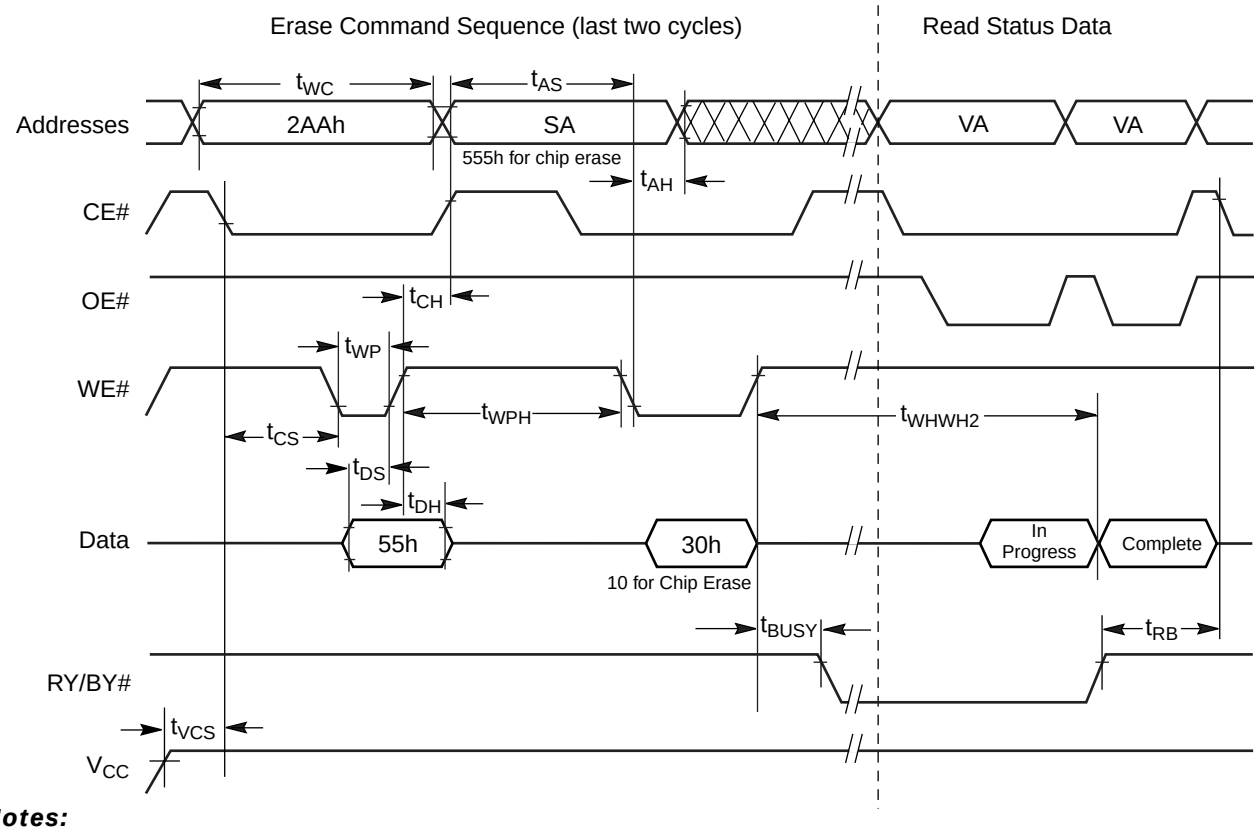


Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 17. Program Operation Timings

AC Characteristics

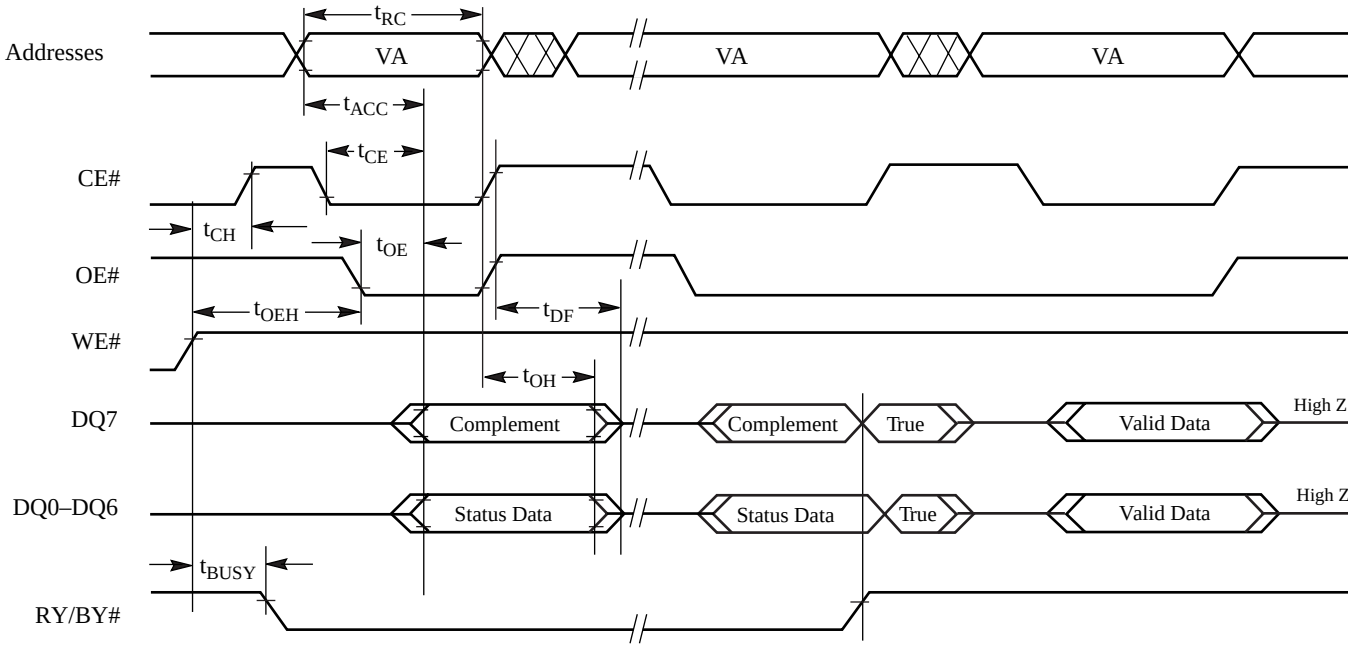


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Write Operation Status, on page 1*
2. *Illustration shows device in word mode.*

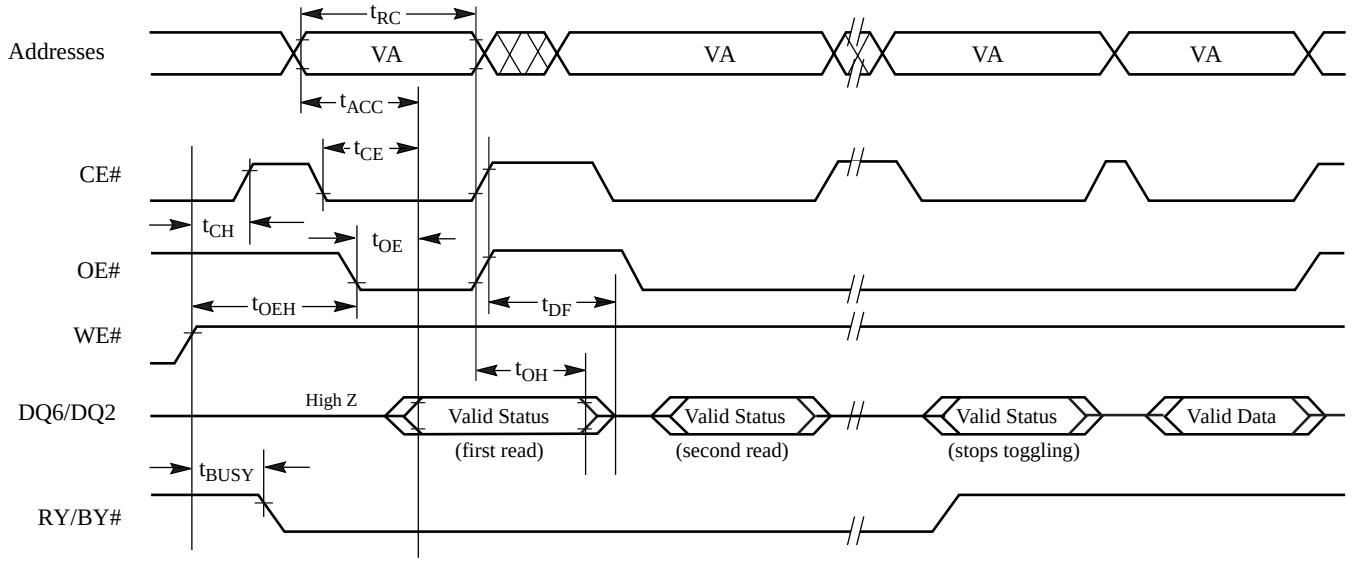
Figure 18. Chip/Sector Erase Operation Timings

AC Characteristics



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

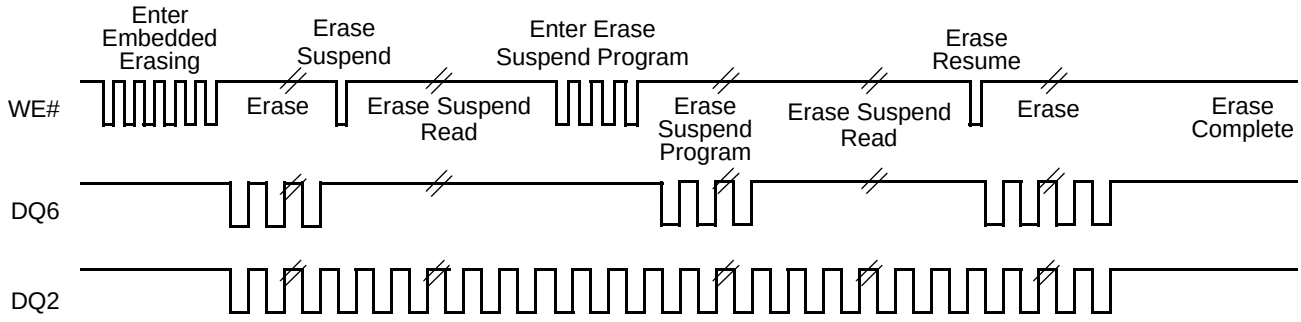
Figure 19. Data# Polling Timings (During Embedded Algorithms)



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 20. Toggle Bit Timings (During Embedded Algorithms)

AC Characteristics



Note: *The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

Figure 21. DQ2 vs. DQ6

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

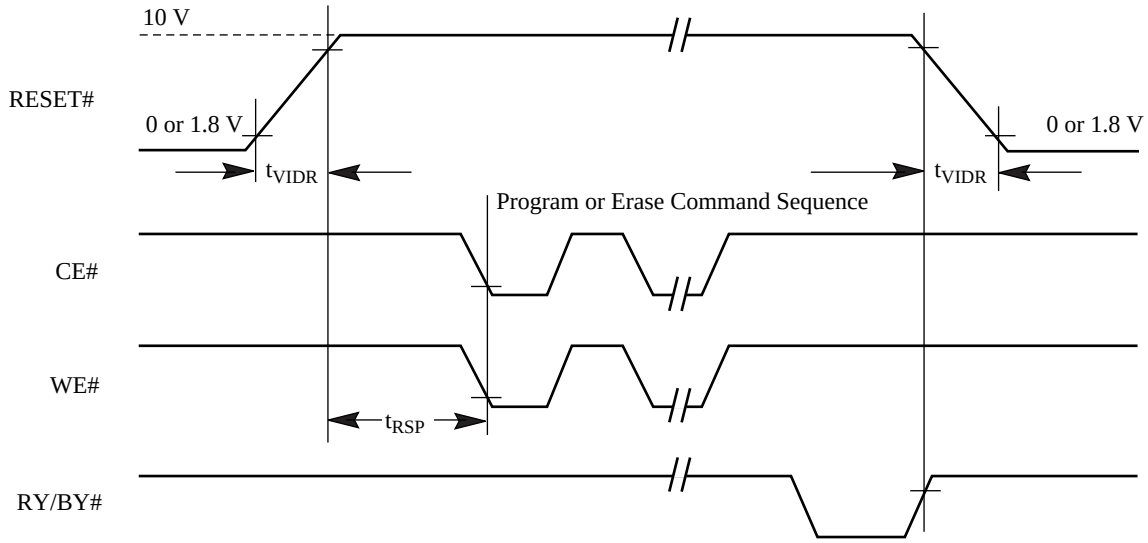
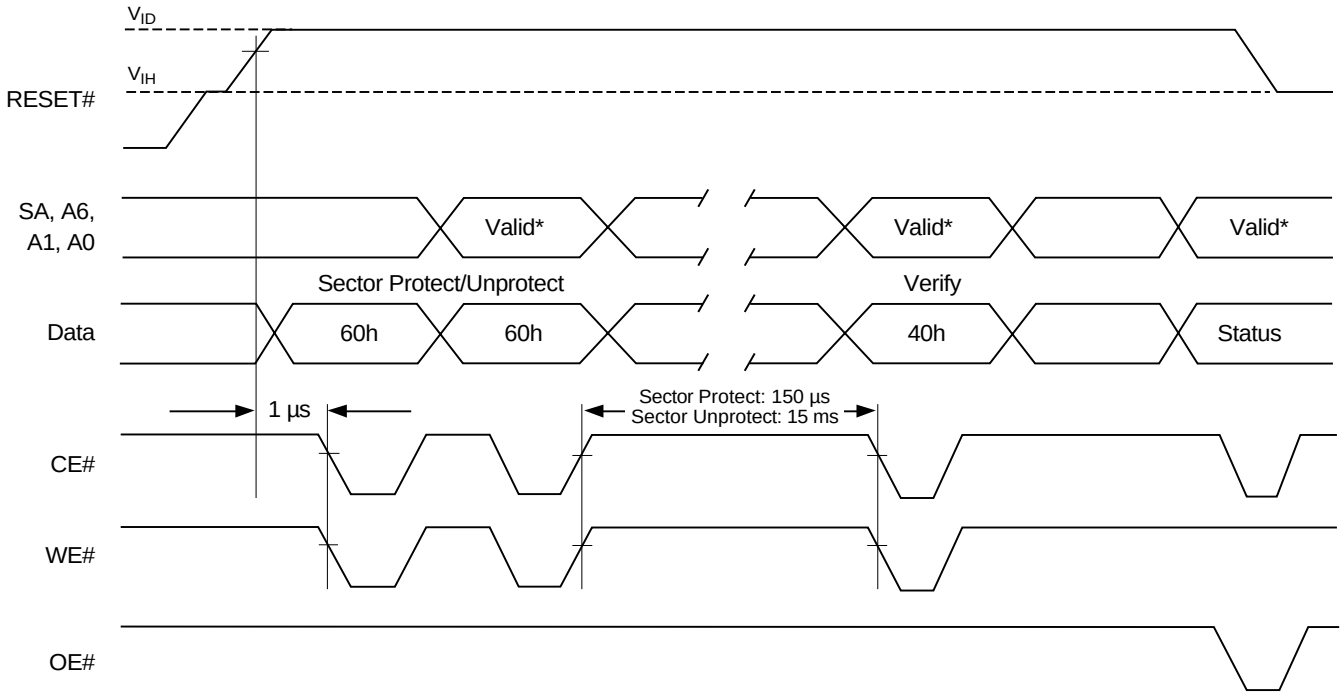


Figure 22. Temporary Sector Unprotect Timing Diagram

AC Characteristics



* *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 23. Sector Protect/Unprotect Timing Diagram

AC Characteristics

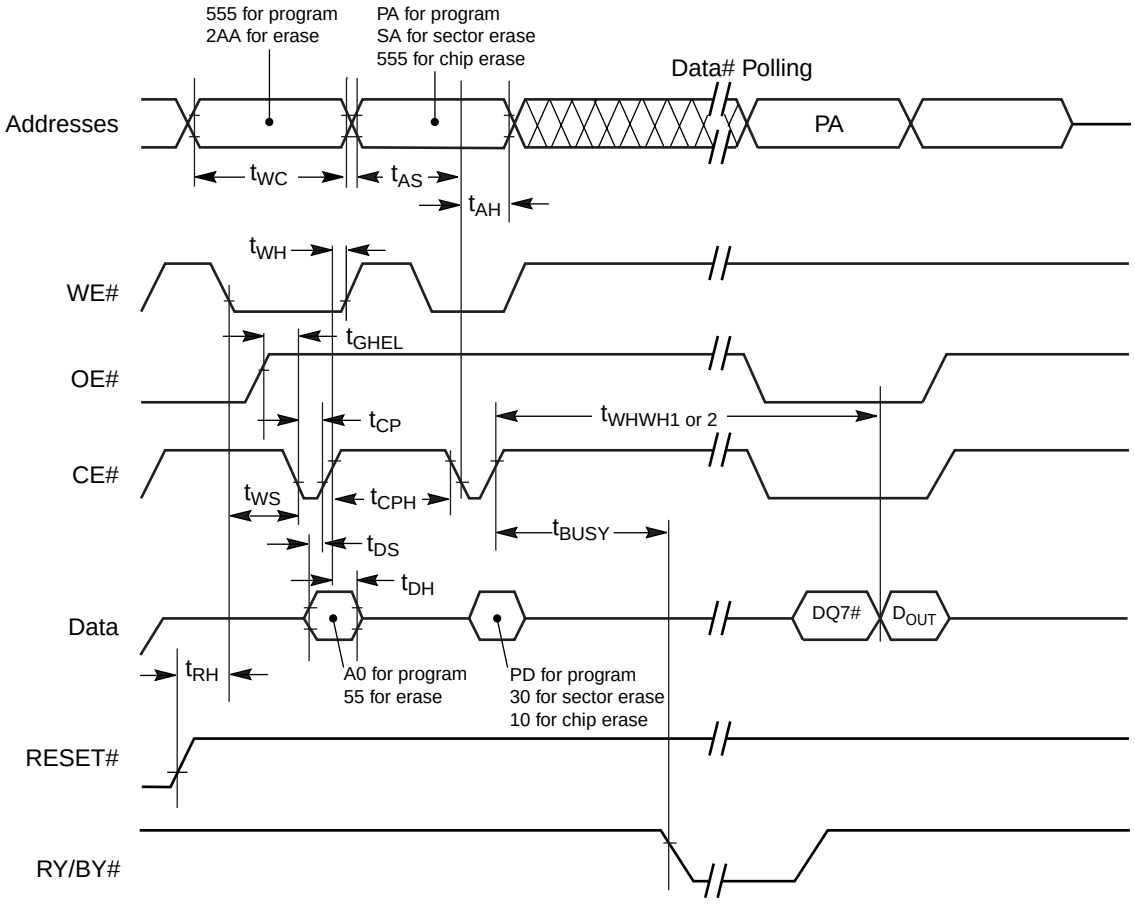
Alternate CE# Controlled Erase/Program Operations

Parameter		Description			Speed Options				Unit
JEDEC	Std				-100R	-110	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	100	110	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	50	55	60	70	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	50	55	60	70	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OES}	Output Enable Setup Time		Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	50	55	60	70	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Notes 1, 2)	Byte	Typ	10				µs
			Word	Typ	12				
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Notes 1, 2)		Typ	2				sec

Notes:

1. *Not 100% tested.*
2. *See the* *Erase and Programming Performance, on page 38* *section for more information.*

AC Characteristics



Notes:

1. *PA = program address, PD = program data, DQ7# = complement of the data written, D_{OUT} = data written*
2. *Figure indicates the last two bus cycles of command sequence.*
3. *Word mode address used as an example.*

Figure 24. Alternate CE# Controlled Write Operation Timings

Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		2	15	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		38		s	
Byte Programming Time		10	300	µs	Excludes system level overhead (Note 5)
Word Programming Time		12	360	µs	
Chip Programming Time (Note 3)	Byte Mode	5	40	s	
	Word Mode	3.5	30	s	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 2.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.8 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 5 on page 18 for further information on command definitions.*
6. *The device has a minimum guaranteed erase and program cycle endurance of 1,000,000 cycles.*

Latchup Characteristics

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	11.0 V
Input voltage with respect to V_{SS} on all I/O pins	–0.5 V	V_{CC} + 0.5 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 1.8 V, one pin at a time.

TSOP Pin and BGA Package Capacitance

Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	7.5	pF
			Fine-pitch BGA	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	8.5	12	pF
			Fine-pitch BGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	7.5	9	pF
			Fine-pitch BGA	3.9	4.7	pF

Notes:

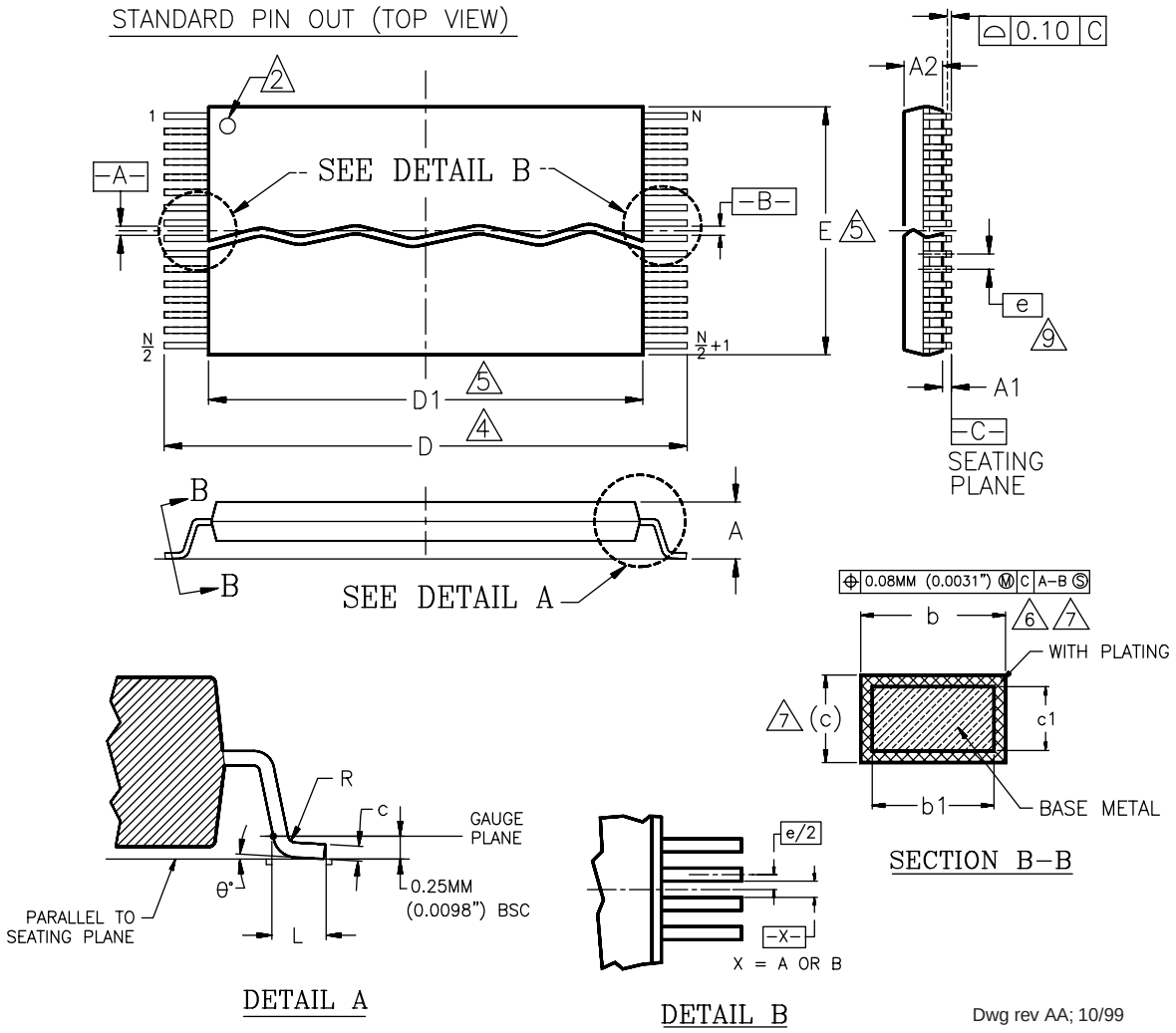
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

Data Retention

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

Physical Dimensions

TS048—48-Pin Standard TSOP



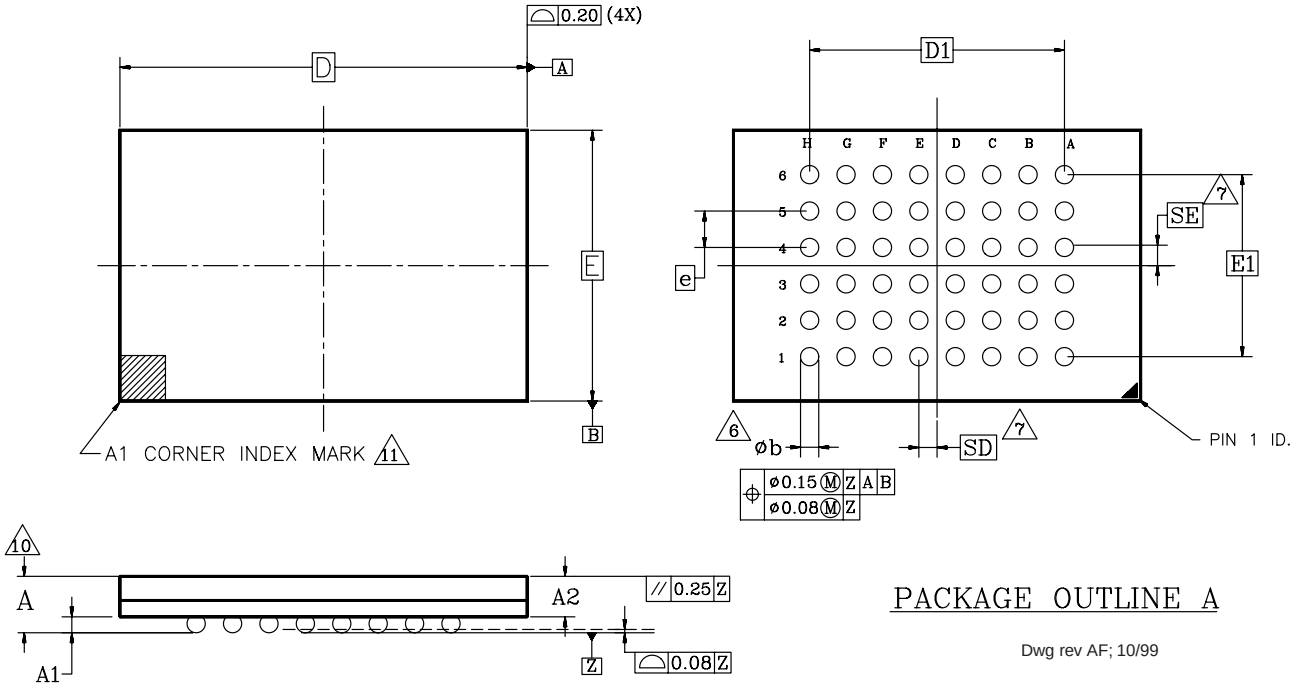
Package	TS 48		
Jedec	MO-142 (B) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	48		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

Physical Dimensions

FBA048—48-Ball Fine-Pitch Ball Grid Array (FBGA) 6 x 8 mm Package



PACKAGE OUTLINE A

Dwg rev AF; 10/99

PACKAGE	xFBA 048			
JEDEC	N/A			
	6.15mmx8.15mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	OVERALL THICKNESS
A1	0.20	—	—	BALL HEIGHT
A2	0.84	—	0.94	BODY THICKNESS
D	8.15 BSC			BODY SIZE
E	6.15 BSC			BODY SIZE
D1	5.60 BSC			BALL FOOTPRINT
E1	4.00 BSC			BALL FOOTPRINT
MD	8			ROW MATRIX SIZE D DIRECTION
ME	6			ROW MATRIX SIZE E DIRECTION
N	48			TOTAL BALL COUNT
b	0.25	0.30	0.35	BALL DIAMETER
e	0.80 BSC			BALL PITCH
SD/SE	0.40 BSC			SOLDER BALL PLACEMENT

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" IN THE PACKAGE DRAWING INDICATE THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. FOR PACKAGE THICKNESS A IS THE CONTROLING DIMENSION.
11. A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTION OR OTHER MEANS.

Revision Summary

Revision A (August 14, 2002)

Initial Release.

Revision A+1 (August 28, 2002)

Sector Protection/Unprotection

Changed beginning of second paragraph from, "The primary method...." to read, "Sector protection/unprotection."

Deleted third paragraph.

FBB048—48-Ball Fine-Pitch Ball Grid Array (FBGA) 6 x 8 mm package

Changed number in row D in table from 9.00 mm to 8.0 mm.

Revision A + 2 (February 5, 2003)

Global

Changed fastest speed option from 103 ns to 100 ns, regulated voltage, added 110 ns speed option standard voltage.

General Description

Changed first sentenced to indicate 48-pin TSOP package option.

Command Definitions, Table 5

Removed TBD markers from device ID, Top Boot Block to 70h.

Removed TBD markers from device ID, Bottom Boot Block to FIh.

Changed address bits A18–A11 to A17–A11.

Physical Dimensions, 48-pin TSOP

Changed from Reverse to Standard TSOP package.

Revision A + 3 (February 26, 2003)

Global

Added 110 ns speed option.

Distinctive Characteristics

Updated Automatic Sleep Mode and standby mode current values.

Pin Configuration

Updated V_{CC} low-end value.

Ordering Information

Changed WB package type to WA.

DC Characteristics, CMOS Compatible

Updated V_{CC} Standby and Reset currents Typ values, and Automatic Sleep Mode Typ value.

Revision A+ 4 (March 18, 2003)

Ordering Information, Valid Combinations

Removed dashes from Order Numbers.

Revision A + 5 (March 3, 2005)

Ordering Information

Added Commercial and Industrial Pb-free Package temperatures.

Valid Combinations for TSOP package

Added two package codes

Valid Combination for FBGA package

Added two package codes

Global

Added Colophon.

Updated Trademark information.

Colophon

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