SHARP

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To ;

SPECIFICATIONS

Product Type 240 Output LCD Segment Driver

Model No. LH1548F

※This specifications contains 26 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

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BY:

PRESENTED

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SHARP CORPORATION ★ IC TENRI GROUP ★ 9.30.97. MAIL DATE

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- ·Instrumentation and measuring equipment
- ·Machine tools
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- ·Home appliances
- ·Communication equipment other than for trunk lines

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- ·Mainframe computers
- ·Traffic control systems
- ·Gas leak detectors and automatic cutoff devices
- ·Rescue and security equipment
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- ·Medical equipment related to life support, etc.

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●Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

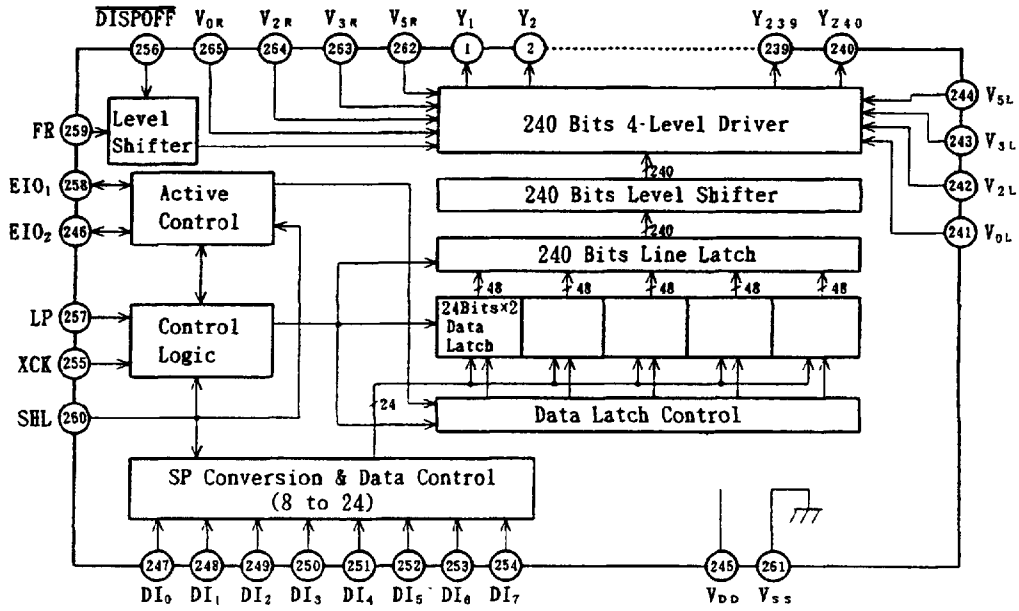
1. Summary

The LH1548F is a 240 output segment driver LSI suitable for driving large scale dot matrix LC panels using as personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LC module. When combined with the LH1530 Common Driver, a low power consuming, high-precision LC panel display can be assembled.
This driver is for 8-bits parallel input exclusive use.

2. Features

- Number of LC drive outputs : 240
- Supply voltage for LC drive : +10.0 to +42.0 V
- Supply voltage for the logic system : +2.5 to +5.5 V
- Shift Clock frequency : 25 MHz (Max.) V_{DD}=+4.5 to +5.5 V
  : 15 MHz (Max.) V_{DD}=+3.0 to +4.5 V
  : 12 MHz (Max.) V_{DD}=+2.5 to +3.0 V
- Low power consumption
- Low output impedance
- Adopts a data bus system
- 8-bits parallel input
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip select mode, causes the internal clock to be stopped by automatically counting 240 of input data
- CMOS silicon gate process (P-type Silicon Substrate)
- Supports high capacity LC panel display when combined with the LH1530 Common Driver
- Package : 265 pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

3. Block Diagram

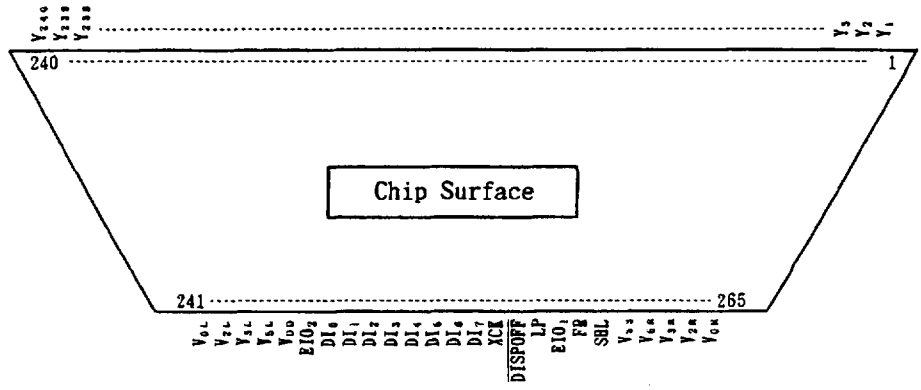


4. Functional Operations of Each Block

Block	Function
Active Control	Controls the selection or deselection of the chip. Following a LP signal input, and after the chip select signal is input, a select signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected.
SP Conversion & Data Control	Keep input data which are 3 clocks of XCK into latch circuit, after that they are put on the internal data bus 24 bits at a time.
Data Latch Control	Selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic, for every 48 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	Latches the data on the data bus. The latch state of each LC driver output pin is controlled by the control logic and the data latch control, 240 bits of data are read in 10 sets of 24 bits.
Line Latch	All 240 bits which have been read into the data latch are simultaneously latched on the falling edge of the LP signal, and output to the level shifter block.

Block	Function
Level Shifter	The logic voltage signal is level-shifted to the LC drive voltage level, and output to the driver block.
4-Level Driver	Drives the LC driver output pins from the latch data, selecting one of 4 levels (V_0, V_2, V_3, V_5) based on the FR and $\overline{\text{DISPOFF}}$ signals.
Control Logic	Controls the operation of each block. When a LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 240 bits of data are read in, and the chip is deselected.

5. Pin Configuration

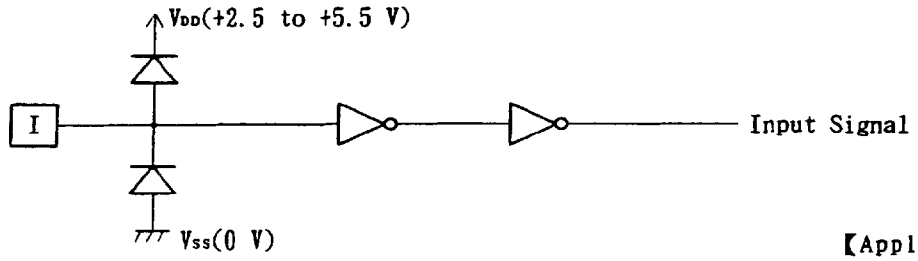


6. Pin Descriptions

6-1. Pin Designations

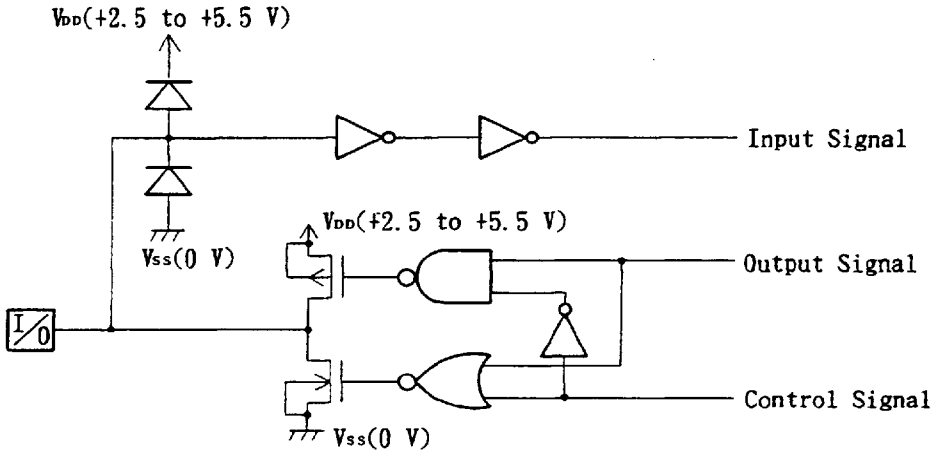
Pin No.	Symbol	I/O	Designation
1 to 240	$Y_1 - Y_{240}$	O	LC drive output
241, 265	V_{0L}, V_{0R}	-	Power supply for LC drive
242, 264	V_{2L}, V_{2R}	-	Power supply for LC drive
243, 263	V_{3L}, V_{3R}	-	Power supply for LC drive
244, 262	V_{5L}, V_{5R}	-	Power supply for LC drive
245	V_{DD}	-	Power supply for logic system(+2.5 to +5.5 V)
260	SHL	I	Display data shift direction selection
246, 258	EIO_2, EIO_1	I/O	Input/Output for chip select
247 to 254	DI_0-DI_7	I	Display data input
255	XCK	I	Display data shift clock input
257	LP	I	Display data latch pulse input
256	$\overline{DISPOFF}$	I	Control input for deselect output level
259	FR	I	AC-converting signal input for LC drive waveform
261	V_{SS}	-	Ground (0 V)

6-2. Input/Output Circuits



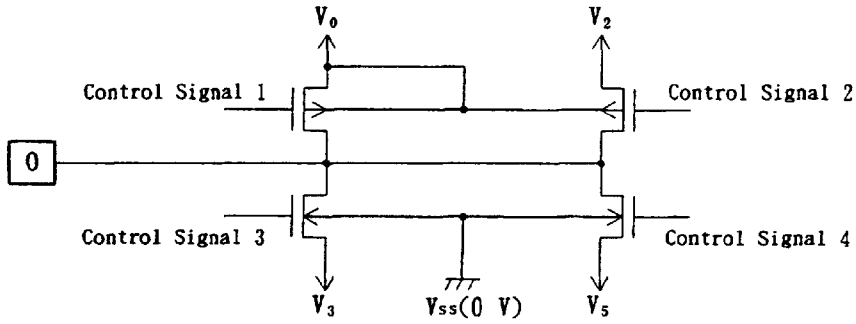
【Applicable pins】
DI_0-DI_7, XCK, LP
$\overline{DISPOFF}$, SHL, FR

Fig.1 Input Circuit



【Applicable pins】
EIO_1, EIO_2

Fig.2 Input/Output Circuit



【Applicable pins】
Y_1-Y_{240}

Fig.3 LC Drive Output Circuit

7. Description of Functional Operations

7-1. Pin Functions

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5 V
V_{SS}	Ground pin connects to 0 V
V_{0L}, V_{0R} V_{2L}, V_{2R} V_{3L}, V_{3R} V_{5L}, V_{5R}	Power supply pin for LC driver voltage bias •V_{iL} and V_{iR}(i=0,2,3,5) aren't connected with inside LSI. Therefore, it is necessary that these terminals connect with an outside power supply. •Normally, the bias voltage used is set by a resistor divider. •Ensure that voltages are set such that $V_{SS} \leqq V_5 < V_3 < V_2 < V_0$.
DI_0-DI_7	Input Pin for display data •Input data into the 8 pins DI_0-DI_7.
XCK	Clock input pin for taking display data •Data is read on the falling edge of the clock pulse.
LP	Latch pulse input pin for display data •Data is latched on the falling edge of the clock pulse.
SHL	Direction selection pin for reading display data •When set to V_{SS} level "L", data is read sequentially from Y_{240} to Y_1. •When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{240}.
$\overline{DISPOFF}$	Control input pin for output deselect level •The input signal is level-shifted from logic voltage level to LC drive voltage level,and controls LC drive circuit. •When set to V_{SS} level "L", the LC drive output pins (Y_1-Y_{240}) are set to level V_5.
FR	AC signal input for LC driving waveform •The input signal is level-shifted from logic voltage level to LC drive voltage level,and controls LC drive circuit. •Normally,inputs a frame inversion signal. •The LC driver output pin's output voltage level can be set using the line latch output signal and the FR signal. Table of truth values is shown in 7-2-1.
EIO_1 EIO_2	Input/Output pin for chip selection •When SHL input is at V_{SS} level "L", EIO_2 is set for input,and EIO_1 is set for output. •When SHL input is at V_{DD} level "H", EIO_2 is set for output,and EIO_1 is set for input. •During output, set to "H" while LP*$\overline{XCK}$ is "H", and after 240 bits of data have been read, set to "L" for one cycle (from rising edge to rising edge of XCK), after which it returns to "H". •During input, after the LP signal is input, the chip is selected while $\overline{EI}$*$\overline{XCK}$ is "H", after 240 bits of data have been read, the chip is deselected.

Symbol	Function
Y_1-Y_{240}	LC driver output pins ·Corresponding directly to each bit of the data latch, one level (V_0, V_2, V_3, or V_5) is selected and output. Table of truth values is shown in 7-2-1.

7-2. Functional Operations

7-2-1. Truth Table

FR	Latch Data	DISPOFF	Driver Output Voltage Level (Y_1-Y_{240})
L	L	H	V_3
L	H	H	V_5
H	L	H	V_2
H	H	H	V_0
x	x	L	V_5

Here, $V_{SS} \leqq V_5 < V_3 < V_2 < V_0$, H : V_{DD} (+2.5 to +5.5 V), L : V_{SS} (0 V), x : Don't care

【Note】 "Don't care" should be fixed to "H" or "L", avoiding floating.
There are two kinds of power supply (logic level voltage,LC drive voltage) for LCD driver. Please supply regular voltage which assigned by specification for each power pin.

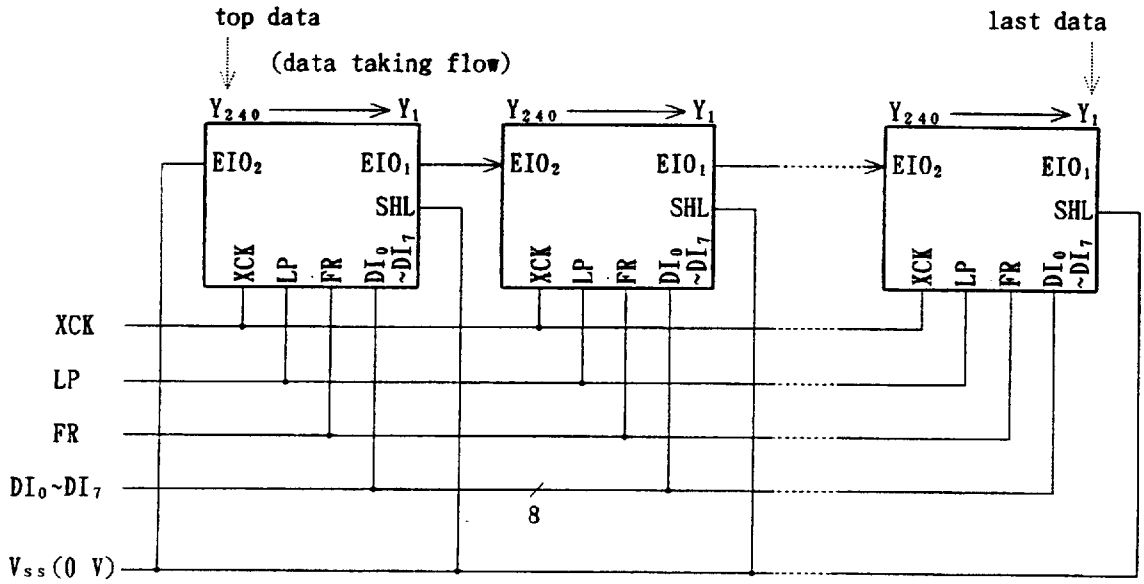
7-2-2. Relationship between the Display Data and Driver Output pins

8-Bits Parallel Mode

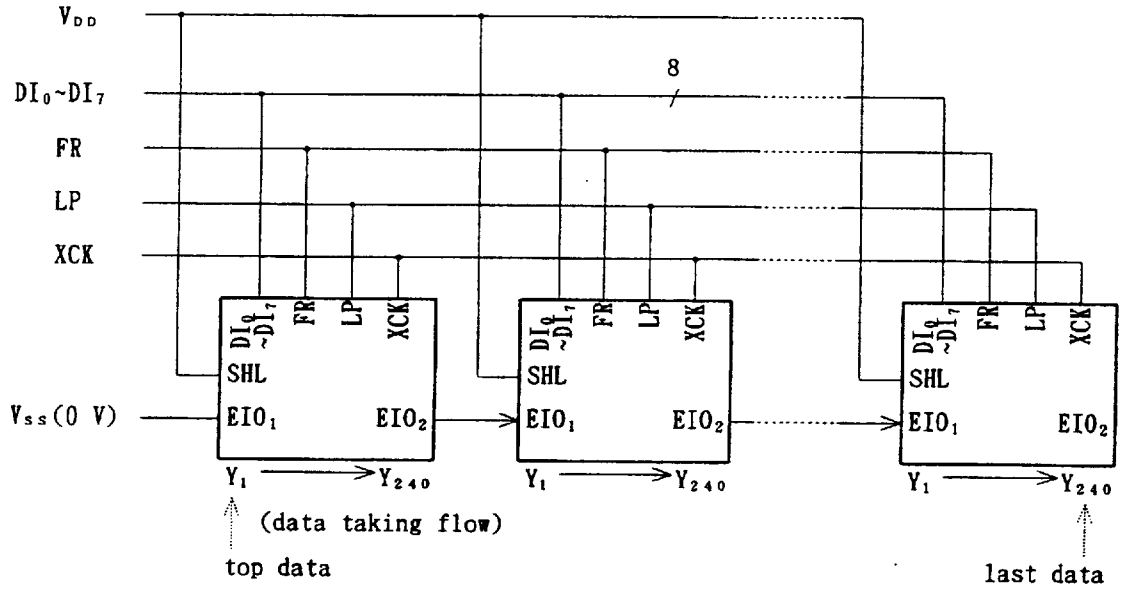
SHL	EIO_1	EIO_2	Data Input	Figure of Clock						
				30clock	29clock	28clock	…	3clock	2clock	1clock
L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	…	Y_{217}	Y_{225}	Y_{233}
			DI_1	Y_2	Y_{10}	Y_{18}	…	Y_{218}	Y_{226}	Y_{234}
			DI_2	Y_3	Y_{11}	Y_{19}	…	Y_{219}	Y_{227}	Y_{235}
			DI_3	Y_4	Y_{12}	Y_{20}	…	Y_{220}	Y_{228}	Y_{236}
			DI_4	Y_5	Y_{13}	Y_{21}	…	Y_{221}	Y_{229}	Y_{237}
			DI_5	Y_6	Y_{14}	Y_{22}	…	Y_{222}	Y_{230}	Y_{238}
			DI_6	Y_7	Y_{15}	Y_{23}	…	Y_{223}	Y_{231}	Y_{239}
			DI_7	Y_8	Y_{16}	Y_{24}	…	Y_{224}	Y_{232}	Y_{240}
H	Input	Output	DI_0	Y_{240}	Y_{232}	Y_{224}	…	Y_{24}	Y_{16}	Y_8
			DI_1	Y_{239}	Y_{231}	Y_{223}	…	Y_{23}	Y_{15}	Y_7
			DI_2	Y_{238}	Y_{230}	Y_{222}	…	Y_{22}	Y_{14}	Y_6
			DI_3	Y_{237}	Y_{229}	Y_{221}	…	Y_{21}	Y_{13}	Y_5
			DI_4	Y_{236}	Y_{228}	Y_{220}	…	Y_{20}	Y_{12}	Y_4
			DI_5	Y_{235}	Y_{227}	Y_{219}	…	Y_{19}	Y_{11}	Y_3
			DI_6	Y_{234}	Y_{226}	Y_{218}	…	Y_{18}	Y_{10}	Y_2
			DI_7	Y_{233}	Y_{225}	Y_{217}	…	Y_{17}	Y_9	Y_1

7-2-3. Connection Example of Plural Segment Drivers

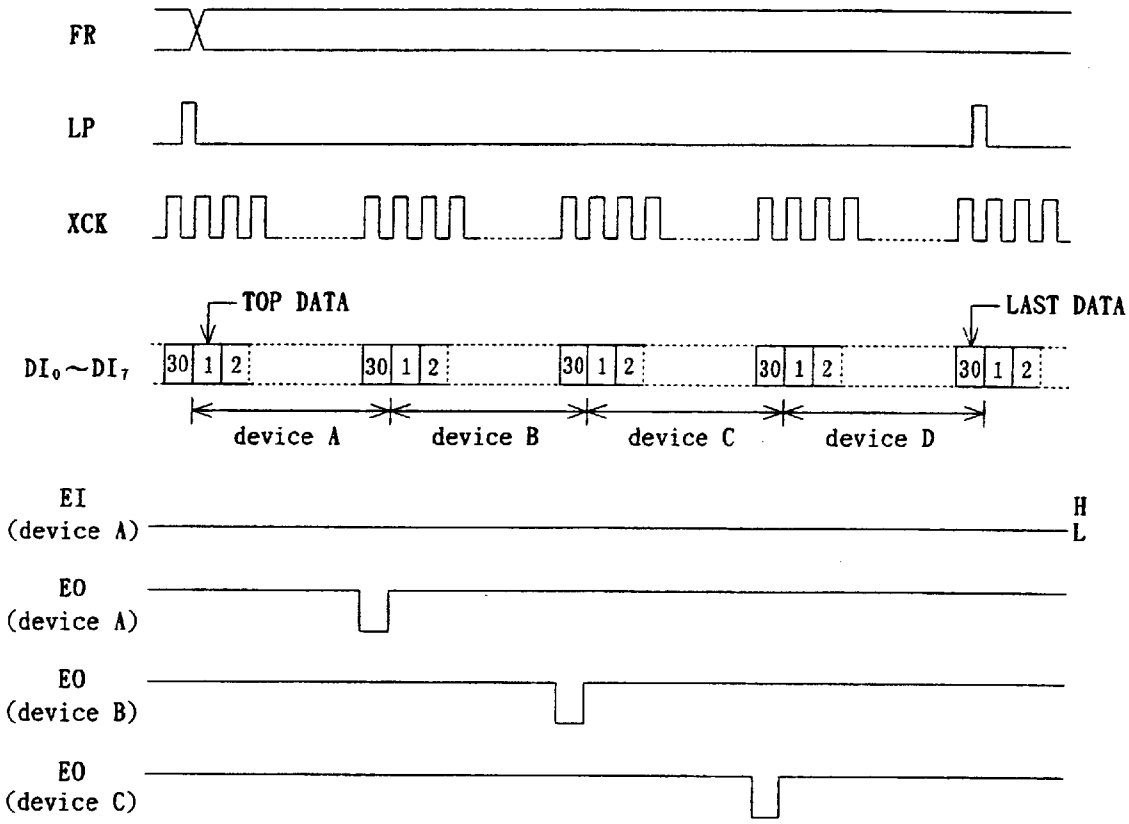
(a) Case of SHL="L"



(b) Case of SHL="H"



7-2-4. Timing Chart of 4-Device cascade Connection

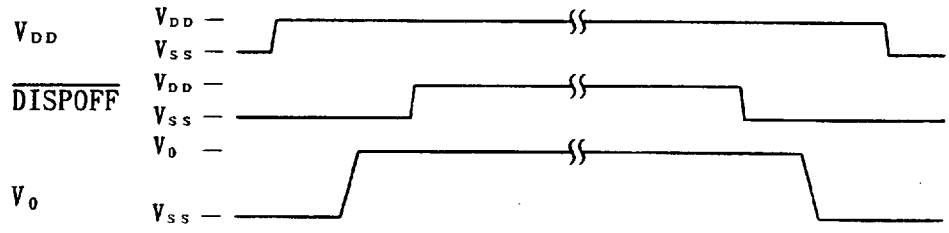


8. Precaution

○Precaution when connecting or disconnecting the power
This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC drive power supply while the logic system power supply is floating.
The detail is as follows.

- When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC drive power.
- We recommend you connecting the serial resistor(50 to 100 Ω) or fuse to the LC drive power V_0 of the system as a current limitter resistor. And set up the suitable value of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LC drive power supply after resetting logic condition of this LSI inside on $\overline{DISPOFF}$ function. After that, cancel the $\overline{DISPOFF}$ function after the LC driver power supply has become stable. Furthermore, when disconnecting the power, set the LC drive output pins to level V_5 on $\overline{DISPOFF}$ function. After that, disconnect the logic system power after disconnecting the LC drive power.
When connecting the power supply, show the following recommend sequence.



9. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable pins	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta=25 ℃	V_{DD}	-0.3 to +7.0	V
Supply voltage (2)	V_0	Referenced	V_{0L}, V_{0R}	-0.3 to +45.0	V
	V_2	to V_{SS}(0 V)	V_{2L}, V_{2R}	-0.3 to V_0+0.3	V
	V_3		V_{3L}, V_{3R}	-0.3 to V_0+0.3	V
	V_5		V_{5L}, V_{5R}	-0.3 to V_0+0.3	V
Input voltage	V_I		DI_{0-7}, XCK, LP, SHL, FR EIO_1, EIO_2, $\overline{DISPOFF}$	-0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}			-45 to +125	℃

10. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{DD}	Referenced	V_{DD}	+2.5		+5.5	V
Supply voltage (2)	V_0	to V_{SS}(0 V)	V_{0L}, V_{0R}	+10.0		+42.0	V
Operating temperature	T_{opr}			-20		+85	℃

【NOTE】 Ensure that voltages are set such that $V_{SS} \leqq V_5 < V_3 < V_2 < V_0$.

11. Electrical Characteristics

11-1. DC Characteristics

(V_{SS}=V_5=0 V, V_{DD}=+2.5 to +5.5 V, V_0=+10.0 to +42.0 V, Ta=-20 to +85 ℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		DI_{0-7}, XCK, LP, SHL, FR	0.7V_{DD}			V
	V_{IL}		EIO_1, EIO_2, $\overline{DISPOFF}$			0.3V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4 mA	EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4 mA				+0.4	V
Input leakage current	I_{LI}	$V_{SS} \leqq V_I \leqq V_{DD}$	All input pins			±10.0	μA
I/O leakage current	$I_{LI/O}$	$V_{SS} \leqq V_I \leqq V_{DD}$	EIO_1, EIO_2			±10.0	μA
Output resistance	R_{ON}	*1 V_0=+40.0 V	Y_1-Y_{240}		1.0	1.5	kΩ
		V_0=+30.0 V			1.5	2.0	
		V_0=+20.0 V			2.0	2.5	
Stand-by current	I_{STB}	*2	V_{SS}			75.0	μA
Consumed current (1) (Deselection)	I_{DD1}	*3	V_{DD}			2.4	mA
Consumed current (2) (Selection)	I_{DD2}	*4	V_{DD}			14.4	mA
Consumed current (3)	I_O	*5	V_{0L}, V_{0R}			2.0	mA

【NOTE】

*1 : $|\Delta V_{ON}|$=0.5 V

*2 : V_{DD}=+5.0 V, V_0=+40.0 V, V_{IH}=V_{DD}, V_{IL}=V_{SS}

*3 : V_{DD}=+5.0 V, V_0=+40.0 V, f_{XCK}=25 MHz, No-load, EI=V_{DD}
The input data is turned over by data taking clock

*4 : V_{DD}=+5.0 V, V_0=+40.0 V, f_{XCK}=25 MHz, No-load, EI=V_{SS}
The input data is turned over by data taking clock

*5 : V_{DD}=+5.0 V, V_0=+40.0 V, f_{XCK}=25 MHz, f_{LP}=38.4 kHz, f_{FR}=80 Hz, No-load
The input data is turned over by data taking clock

11-2. AC Characteristics

(mode 1) $V_{SS}=V_5=0$ V, $V_{DD}=+5.0$ V±10%, $V_0=+10.0$ to $+42.0$ V, Ta=−20 to +85 ℃
Inside of ( ) are : Ta=−20 to +60 ℃

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	*3	40(36)			ns
Shift clock "H" pulse width	t_{WCKH}		12			ns
Shift clock "L" pulse width	t_{WCKL}		14			ns
Data setup time	t_{DS}		5			ns
Data hold time	t_{DH}		15			ns
Latch pulse "H" pulse width	t_{WLPH}		15			ns
Shift clock rise to Latch pulse rise time	t_{LD}		5			ns
Shift clock fall to Latch pulse fall time	t_{SL}		25			ns
Latch pulse rise to Shift clock rise time	t_{LS}		25			ns
Latch pulse fall to Shift clock fall time	t_{LH}		25			ns
Enable setup time	t_S		5(4)			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Output delay time (1) XCK to EIO_1, EIO_2	t_D	C_L=15 pF			28(27)	ns
Output delay time (2) FR to Y_1-Y_{240}	tpd_1	C_L=15 pF			1.2	µs
Output delay time (3) LP to Y_1-Y_{240}	tpd_2	C_L=15 pF			1.2	µs

【Note】
*1 Take the cascade connection into consideration.
*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.
*3 $t_r, t_f \leq 7(5)$ ns

(mode 2) $V_{SS}=V_5=0$ V, $V_{DD}=+3.0$ V to $+4.5$ V, $V_0=+10.0$ to $+42.0$ V, Ta=−20 to +85 ℃
Inside of ( ) are : Ta=−20 to +60 ℃

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	*3	66(60)			ns
Shift clock "H" pulse width	t_{WCKH}		23(20)			ns
Shift clock "L" pulse width	t_{WCXL}		23(20)			ns
Data setup time	t_{DS}		10			ns
Data hold time	t_{DH}		25(20)			ns
Latch pulse "H" pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		10			ns
Shift clock fall to Latch pulse fall time	t_{SL}		30			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift clock fall time	t_{LH}		30			ns
Enable setup time	t_S		12(10)			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Output delay time (1) XCK to EIO_1, EIO_2	t_D	C_L=15 pF			44(40)	ns
Output delay time (2) FR to Y_1-Y_{240}	tpd_1	C_L=15 pF			1.2	µs
Output delay time (3) LP to Y_1-Y_{240}	tpd_2	C_L=15 pF			1.2	µs

【Note】
*1 Take the cascade connection into consideration.
*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.
*3 $t_r, t_f \leq 10$ ns

(mode 3)

$V_{SS}=V_S=0$ V, $V_{DD}=+2.5$ to $+3.0$ V, $V_0=+10.0$ to $+42.0$ V, Ta=-20 to $+85$ ℃

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	*3	82			ns
Shift clock "H" pulse width	t_{WCKH}		28			ns
Shift clock "L" pulse width	t_{WCKL}		28			ns
Data setup time	t_{DS}		10			ns
Data hold time	t_{DH}		30			ns
Latch pulse "H" pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		10			ns
Shift clock fall to Latch pulse fall time	t_{SL}		30			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift clock fall time	t_{LH}		30			ns
Enable setup time	t_S		15			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Output delay time (1) XCK to EIO_1,EIO_2	t_D	C_L=15 pF			57	ns
Output delay time (2) FR to Y_1-Y_{240}	tpd_1	C_L=15 pF			1.2	μs
Output delay time (3) LP to Y_1-Y_{240}	tpd_2	C_L=15 pF			1.2	μs

【Note】

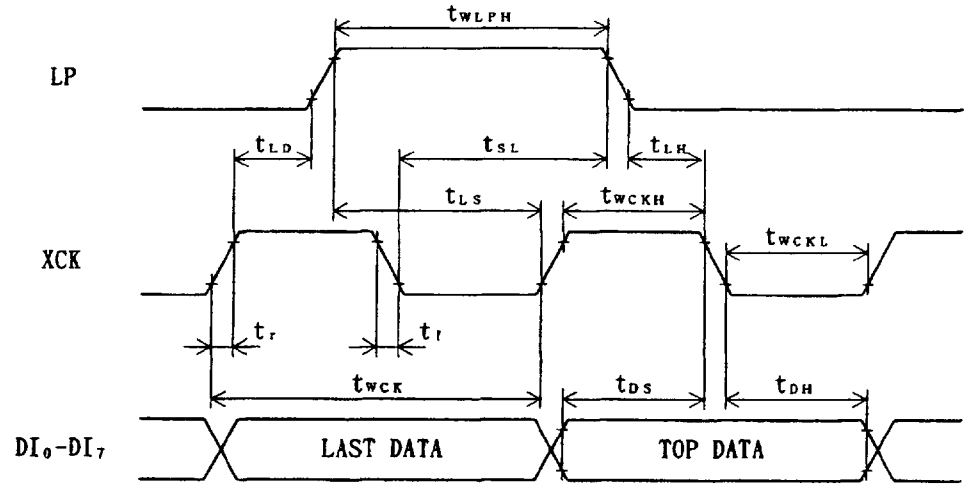
*1 Take the cascade connection into consideration.

*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.

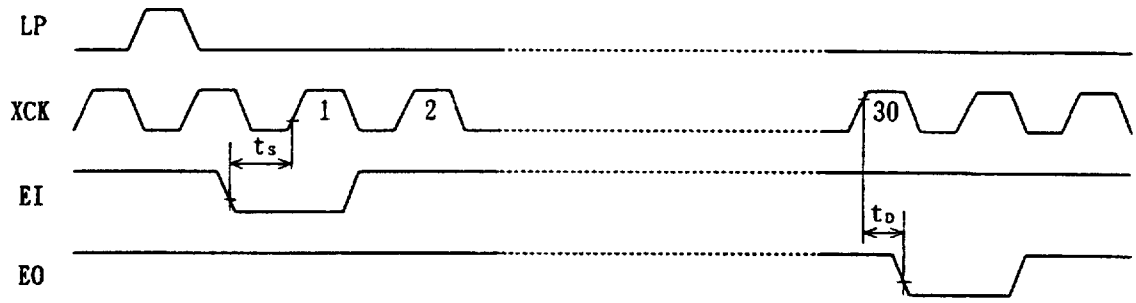
*3 $t_r, t_f \leq 10$ ns

11-3. Timing Diagrams

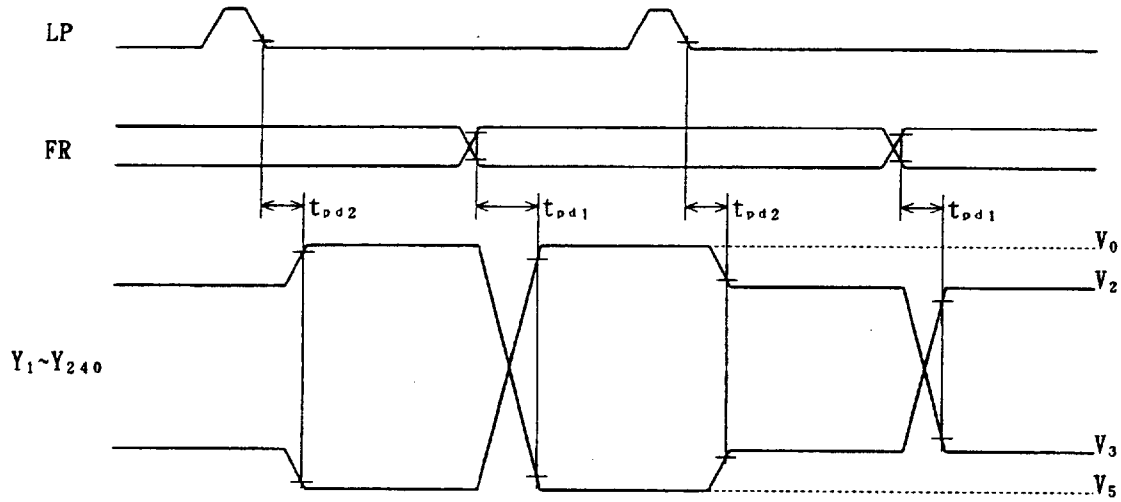
Input Timing Characteristics



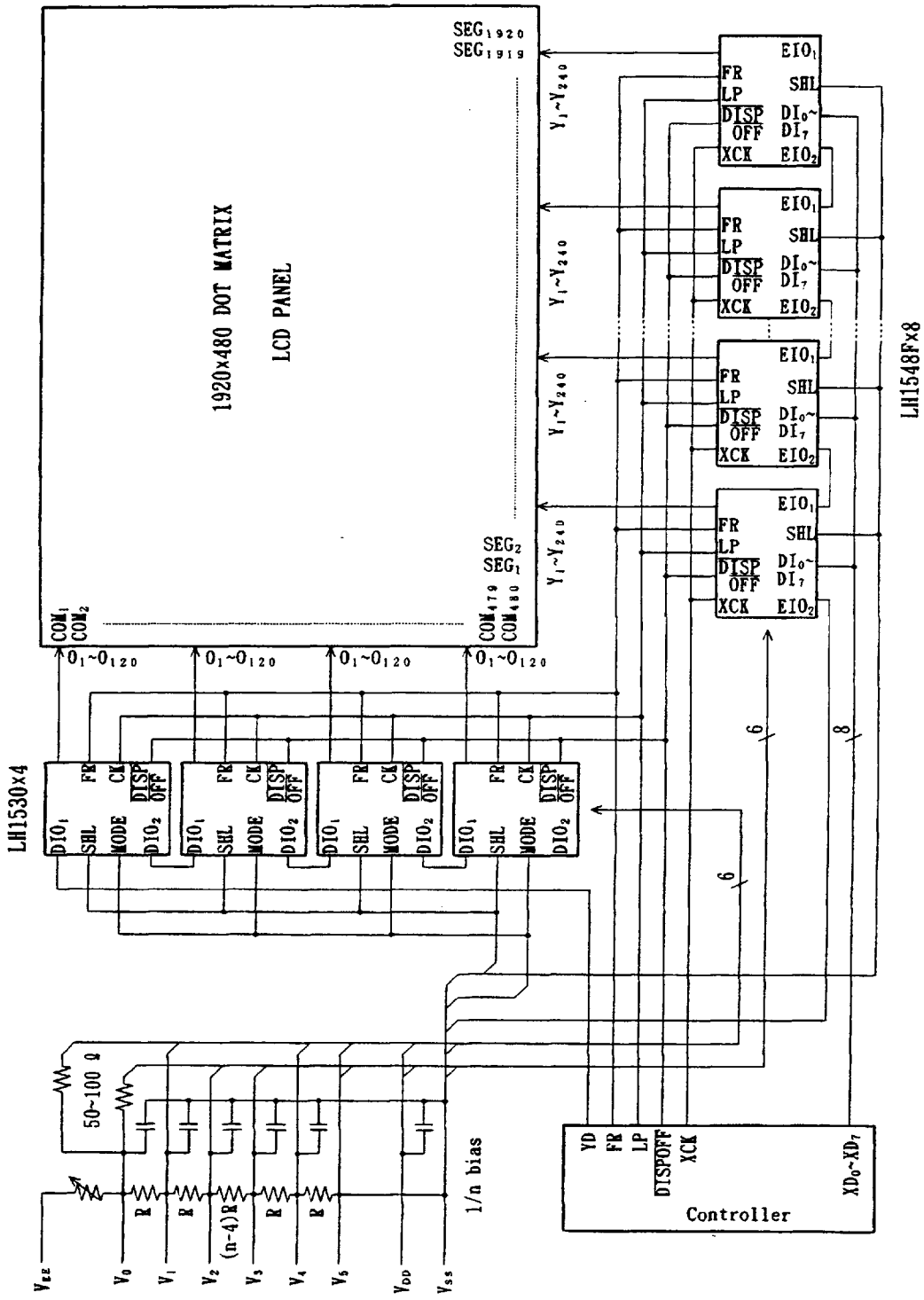
Input/Output Timing Characteristics



Output Timing Characteristics



12. Example of System Configuration



13. Example of Typical Characteristic

Parameter	Conditions	Min.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time	Ta=+25 ℃, V_{SS}=0 V, V_{DD}=+5.0 V		10		ns

14. PACKAGE AND PACKING SPECIFICATION

1. Package Outline Specification
   Refer to drawing No. SPN2251-00
2. Markings
   The meanings of the device code printed on each tape carrier package are as follows.
   (1) Date code (example) : 5 (a) 4 8 (b) D (c) 0 (d)
   a) denotes the last figure of Anno Domini (of production)
   b) denotes the week (of production)
   c) denotes factory code (of production)
   d) denotes the number of times of alteration
3. Packing Specifications
   3-1 Packing Materials

Item	Material	Purpose
Reel	Anti-static treated plastic (405 mm dia.)	Packing of tape carrier package.
Separator	Anti-static treated PET (188 μ mt)	Protects device and prevents ESD (Electro Static Discharge)
Aluminum laminated bag	(520×600 mm)	Moisture proof.
Adhesive tape paper		Fixing of tape carrier package and separator.
Label	Paper	Indicates production name, lot.No., and quantity.
Desiccant	Silica gel	Drying of device
Inner carton	Cardboard(420×420×50mm)	Contains a reel.
Outer carton	Cardboard(445×285×450mm)	Contains 5 inner cartons.

   3-2 Packing Form
   a) Tape carrier package(TCP)is wound on a reel with separator and the ends of them are fixed with adhesive tape.
   b) A label indicating production name, lot number and quantity is stuck on one side of the reel.
   c) The reel and silica gel are put in a laminated aluminum bag. Nitrogen gas is enclosed in the bag and the bag is sealed. The same label(b) is affixed to the bag. The bag is put in a carton and the same label(b) is affixed to one side of the inner carton.
   d) 5 inner cartons are put in an outer carton and the same label(b) is affixed to one side of the outer carton.

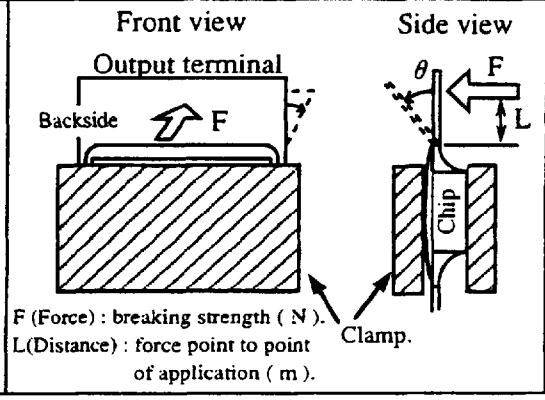
   * Specification of label

TYPE	
	Production name Lot No.
QUANTITY	Quantity
LOT(DATE)	Shipping date

   3-3 Other
   (1) The length of the TCP is typically 40 m per reel, but this may change in accordance with the inventory quantity.
   (2) Faulty devices is completely punched out at the part of the device.
   (3) The maximum number of continuous faulty devices is 16.

ISSUE DATE	AUG.27,1997	DESIGN	M. Fukita	(NOTE)
ISSUE NUMBER	H9801	CHECK	Y. Honda	
S/C NUMBER		APPROVE	I. Hara	

4. Cautions concerning handling.
Although the strength of the device has been verified in accordance with the test method shown below, do not subject the resin parts or the slit terminals to any excessive bending or pressure.

Test	Test method	Rating
Flexure test		Indicate as moment M. $M=F\times L$ (N·m) $M=1.47\times10^{-3}$ N·m MAX. (for both $+\theta$ and $-\theta$)

5. Cautions concerning storage.
- When storing the product, it is recommended that it be left in its shipping package. After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
- Storage conditions

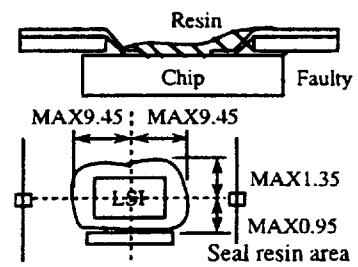
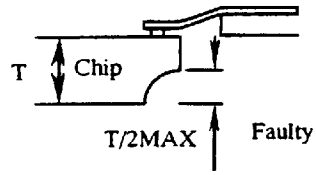
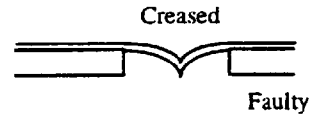
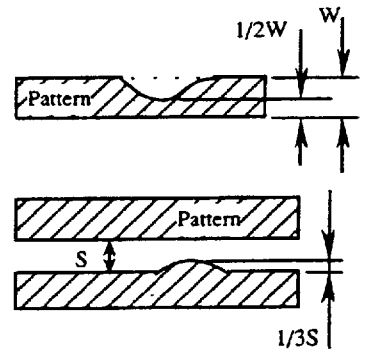
Storage state	Storage conditions
Unopened(less than 60 days)	Temperature: 5 to 30℃; humidity : 80% RH or less.
After seal of broken(less than 30 days)	Temperature: 25℃; humidity : 15% RH or less, dry nitrogen atmosphere.

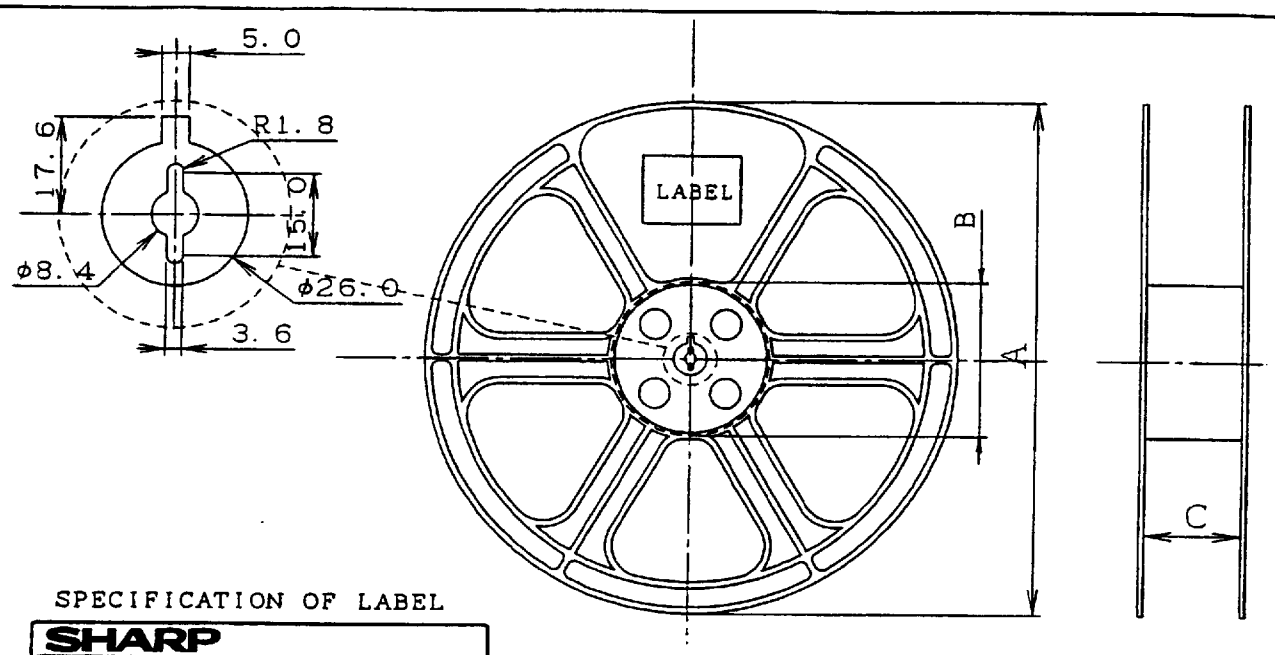
- Don't store in a location exposed to corrosive gas or excessive dust.
- Don't store in a location exposed to direct sunlight or subject to sharp changes in temperature.
- Don't store the product such that it subjected to an excessive load weight, such as by stacking.
- Deterioration of the plating may occur after long-term storage, so special care is required.
It is recommended that the products be inspected before use.

6. Other cautions.
- Immediately after opening the moisture-proof packing, the measurement will shrink slightly. In order to return the measurements to those shown in the drawing, it is necessary to store the product for at least 48 hours at a temperature of 20 to 25℃ and humidity of 50 to 60%.
- When soldering TCP, the TCP wiring pattern may become corroded if unreacted halogen remains within the flux deposited on the TCP. Therefore, avoid applying flux to areas other than the part to be soldered, and ensure that no solvent remains in the flux after mounting.
Avoid using flux containing highly concentrated .

7. External appearance inspection

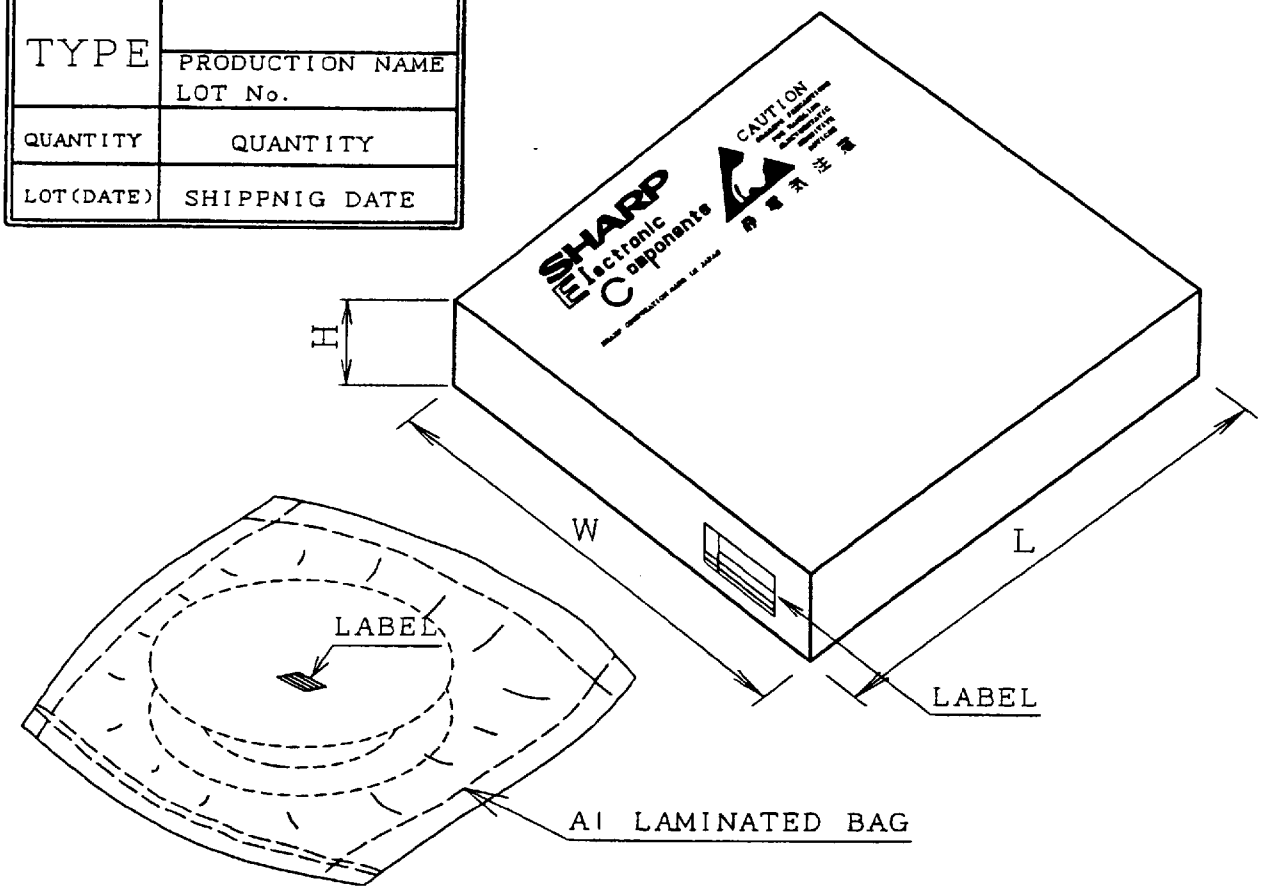
The standards for the inspection of the external appearance of the package are shown below.

Item	Inspection standards	Remarks
1. Exposure of the inner leads and device holes	·Faulty if the chip or inner leads are completely exposed. ·Faulty if the device holes are not completely filled with resin.	
2. Air bubbles	·Faulty if there are air bubbles extending as far as the surface of the chip. ·Faulty if there are air bubbles at the inner leads.	
3. Seal resin area	·Faulty if the area of the seal resin area exceeds the specifications.	Upperside:18.9×2.3mmMAX Underside:18.9×2.3 mmMAX
4. Seal resin thickness	·Faulty if the thickness of the device exceeds the specifications.	Upperside:0.15 mmMAX Underside:0.75 mmMAX Total thickness:1.0 mmMAX
5. Adherence of resin or foreign matter except the seal resin area.	·Faulty if any deposits of foreign matter or resin is allowed to bridge the conductor pattern gaps. However, deposits of foreign matter or resin which can be removed easily can be ignored.	
6. Underside of the chip	·Faulty if there are any cracks in the chip. ·Faulty if there is any chipping in the underside of the chip that is lager than one-half the thickness of the chip. ·Faulty if adherence of the resin to the underside of the chip that causes the thickness of the devices exceed the specifications.	
7. Scratches, cracks and chipping in the tape carrier	·Faulty if there are any scratches exposing the substrate (chip, pattern, or inner leads) at the seal resin. ·Faulty if there are holes or scratches which bridge two conductor patterns at the lower part of the applied solder resist. ·Faulty if there are any cracks or chipping at the perforations.	
8. Pattern deformation	·Faulty if the pattern overhanging the slits is markedly deformed	
9. Discoloration	·Faulty if the tin plating is markedly discolored. ·Faulty if the cover coating is markedly discolored.	
10. Markings	·Faulty if the markings are illegible.	
11. Missing parts of output leads	·Faulty if the width of the output lead is reduced to less than one-half of the standard. ·Faulty if copper foil remnants reduce the clearance between the output leads to less than two-thirds of the standards.	
12. Other	·Faulty if there is any warping, twisting, bending, etc., of the tape that would impair use. ·Faulty if there are no indication holes at the non-effective indication holes.	

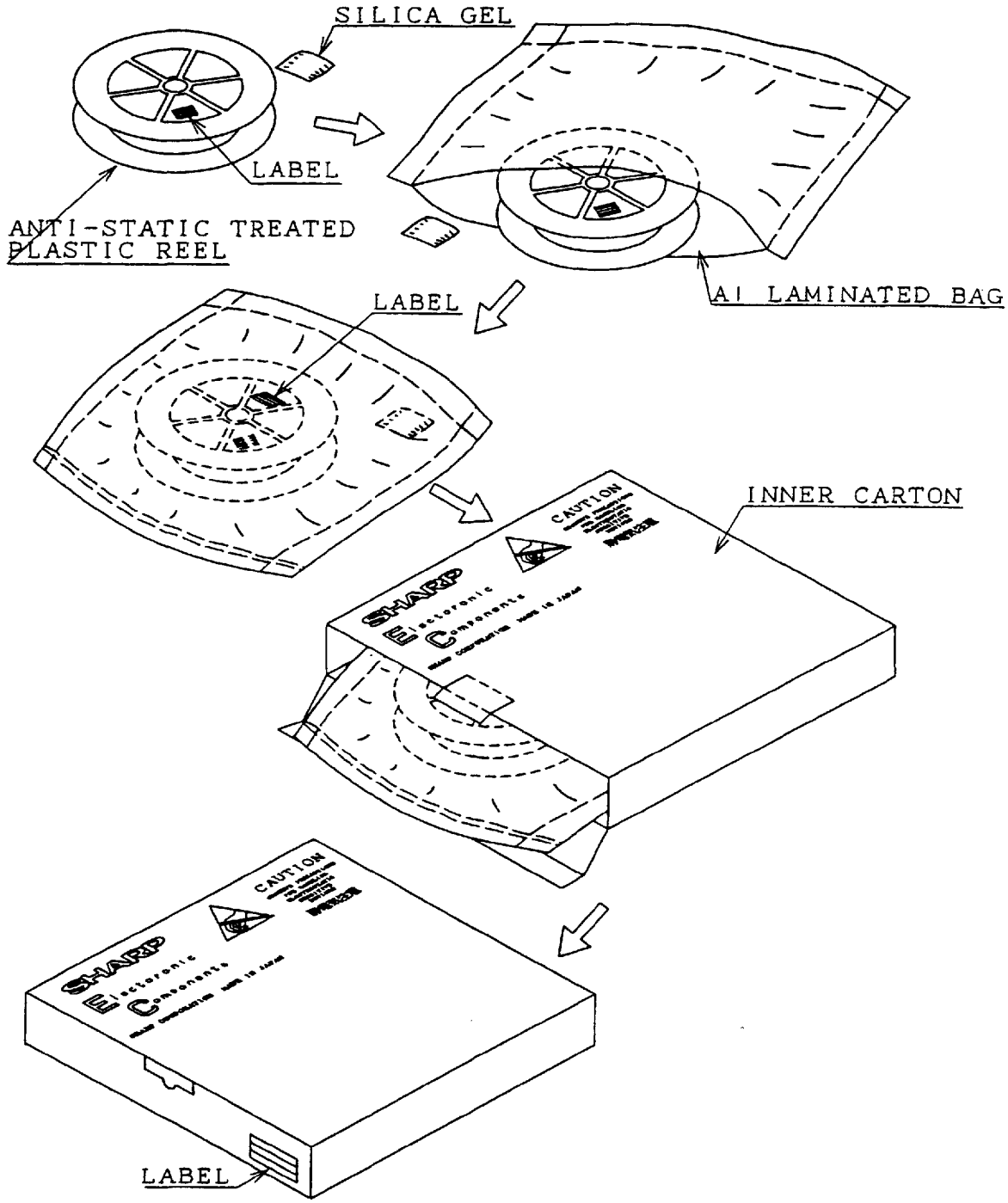


SPECIFICATION OF LABEL

SHARP	
TYPE	
	PRODUCTION NAME LOT No.
QUANTITY	QUANTITY
LOT(DATE)	SHIPPNIG DATE



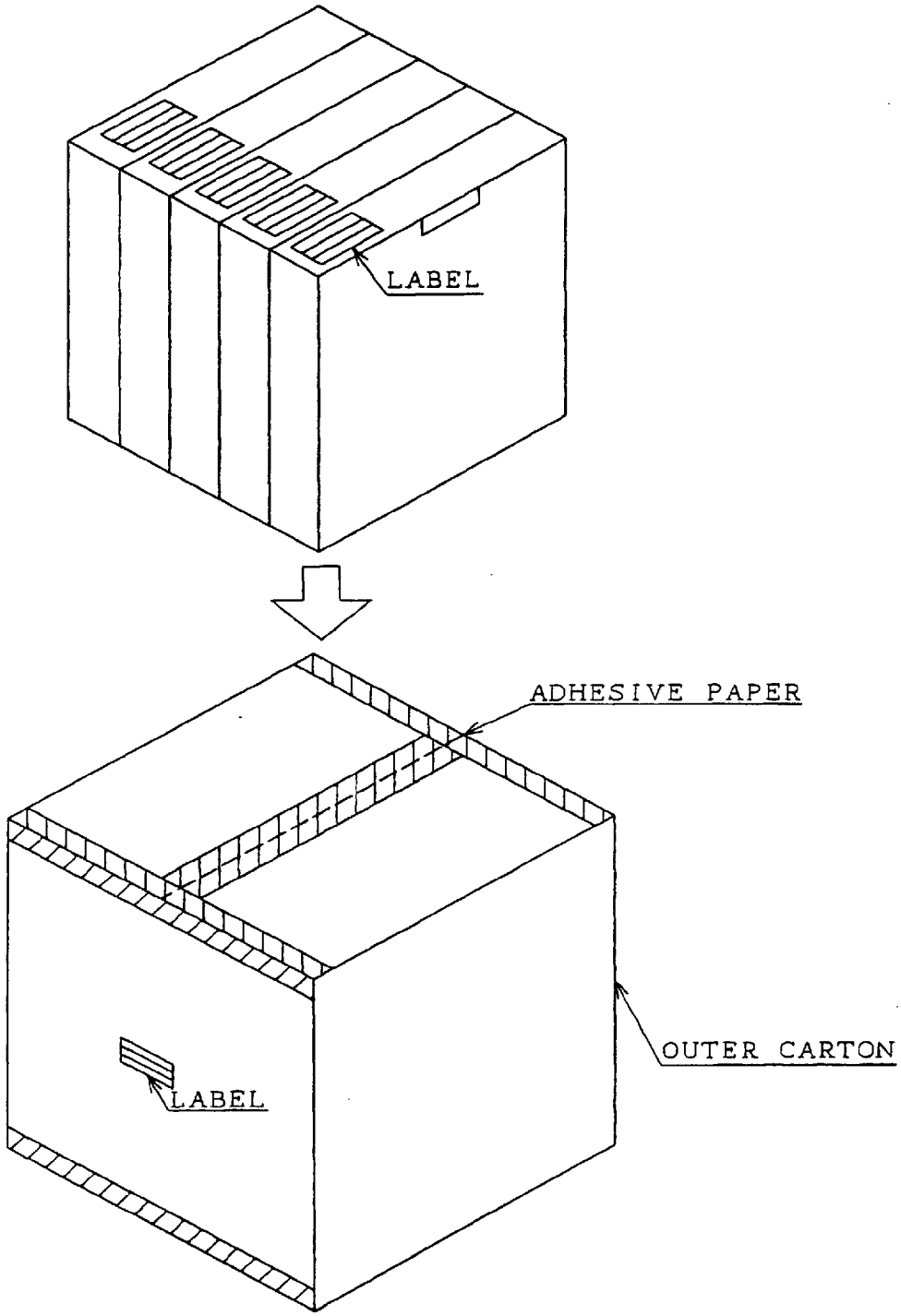
REEL			INNER CARTON			DATE	JAN. 17. 1997	TITLE	REEL AND INNER CARTON OF TCP PACKING
SIZE	A	φ405	SIZE	L	420	UNIT	mm		
	B	φ127		W	420			DRAWING No.	KPN 023
	C	36		H	50	DESIGN	J. Kidoguchi	MODULE ASSEMBLY APPLICATION ENGNEERING DEPT.	
MATERIAL	ANTI-STATIC TREATED PLASTIC		MATERIAL	CARDBOARD		CHECK	H. Honda	IC FUKUYAMA GROUP	



DATE	JANUARY 17, 1997	
ITEM	MATERIAL	NUMBER
ANTI-STATIC TREATED PLASTIC REEL	ANTI-STATIC TREATED PORYSTYLENE	1 REEL
DESICCANT	SILICA GEL	10g
BAG	ALUMINUM	1 PACK
LABEL	PAPER	3 PCS
INNER CARTON	CARDBOARD	1 CASE

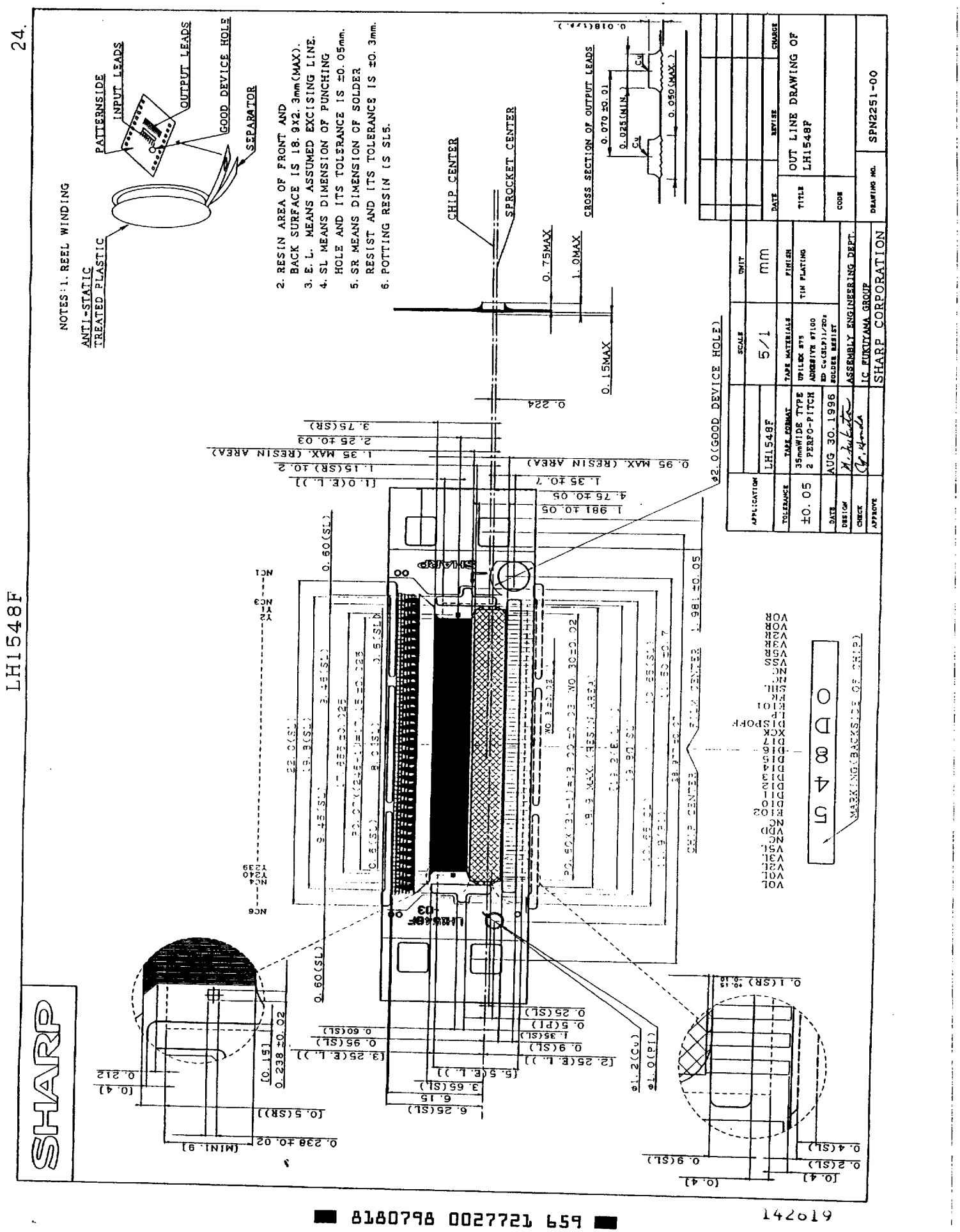
DESIGN	T. Kidoguchi	MODULE ASSEMBLY APPLICATION ENGNEERING DEPT.
CHECK	Y. Honda	IC FUKUYAMA GROUP
APPROVE		SHARP CORPORATION

TITLE	PACKING VIEW OF TCP (1)
CODE	
DRAWING No	



DATE	JANUARY 17. 1997					
ITEM	MATERIAL	NUMBER				
OUTER CARTON	CARDBOARD	1 CASE				
ADHESIVE TAPE	PAPER					
			TITLE	PACKING VIEW OF TCP (2)		
DESIGN	T. Kidoguchi	MODULE ASSEMBLY APPLICATION ENGNEERING DEPT.	CODE			
CHECK	Y. Honda	IC FUKUYAMA GROUP				
APPROVE	R. Tanaka	SHARP CORPORATION	DRAWING No.			

8180798 0027720 712



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