# Highly Intergated 10/100M Dual Speed Hub With Extra 4 Port Switch Built-In

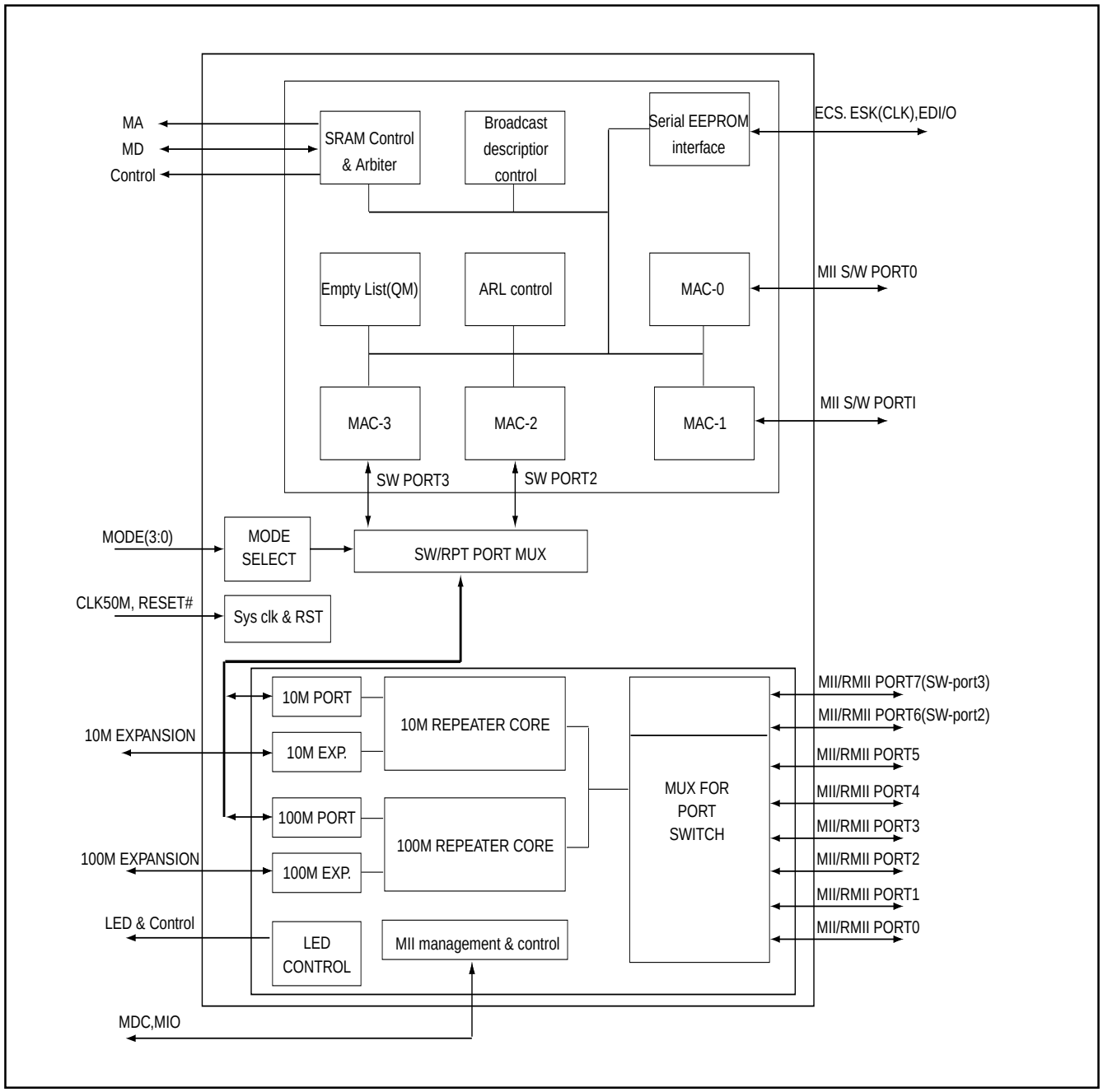
## 1. Features

- Integrate a 4-port switch core and a 12-port dual-speed repeater core.
- Support 0 to 4 MII switch ports and 6 to 8 MII/RMII repeater ports and 10/100M expansion ports. Configure by MODE select.
- Each switch port can operate in 10/100, half/full duplex mode, auto-configured by a N-way PHYceiver.
- Each repeater port auto-sense line speed (10/100M), and operate in half-duplex mode.
- Provide 10M and 100M Expansion Buses for stacking up to 9 Hubs.
- Provide Link/Activity, Partition, Utilization LED display function for diagnostic purpose.
- The embedded switch operates in Store-and-forward mode
- Support up to 2K address entries without external address look-up IC
- Single 64Kx32 SSRAM part used as data buffering and filtering database for the embedded switch.
- IEEE802.3X flow control for full-duplex switch port.
- Backpressure flow control for half-duplex switch port.
- Provide RX-Buffer-Threshold control and TX-Buffer-Threshold control to avoid any port occupying all buffer resource.
- Support serial EEPROM interface for power on configuration

## 2. General Description

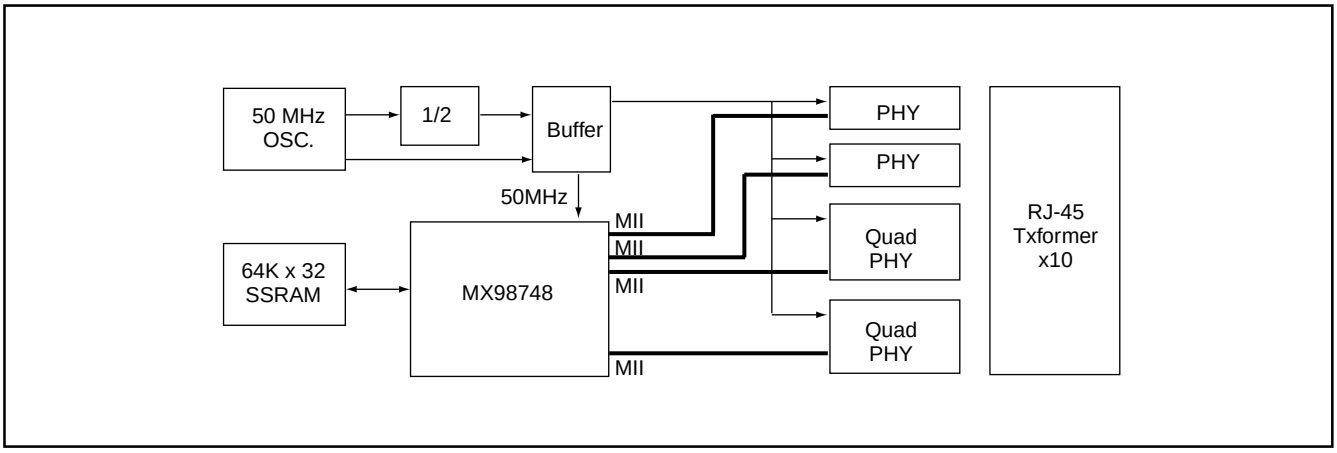
The MX98748 is a Fast Ethernet product with 4 port switch and 8 port repeater hub controller. By MODE select, it can offer different type of switch and hub port configuration such as 2SW/8HUBport, 3SW/7HUB port, 4SW/6HUB port seperately. Combine with MX98747 - 8 Ports dual speed repeater controller, customer can design diverse hibrid hub ( hub with switch function) products such as 16rpt port + 2 switch ports, 24rpt port + 2 switch ports,and etc.(more information on application configuration can be found in application note and MX98748 presentation material.)

## 3.0 Block Diagram

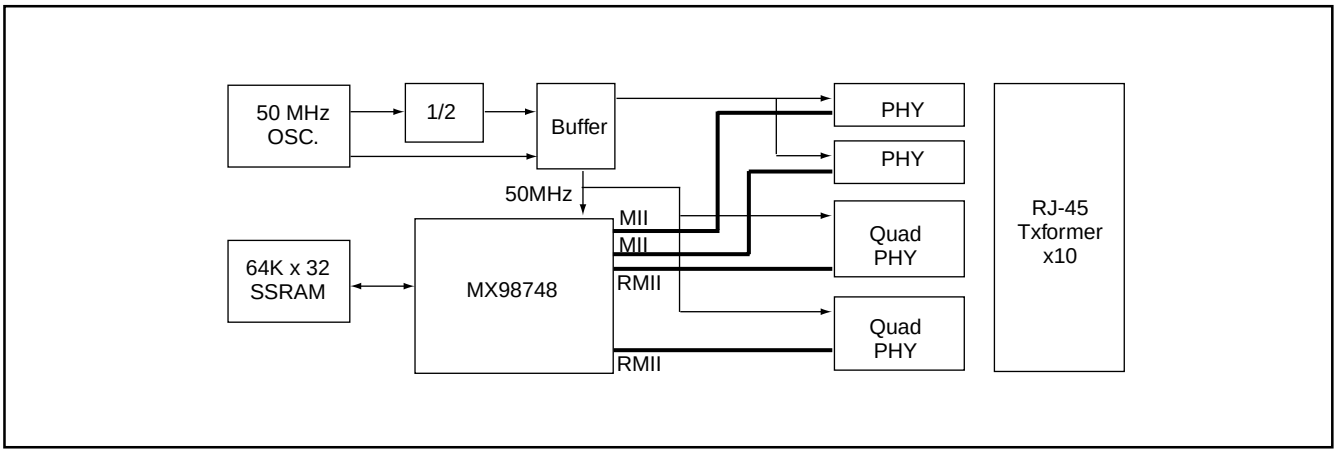


## 3.1 Typical Application

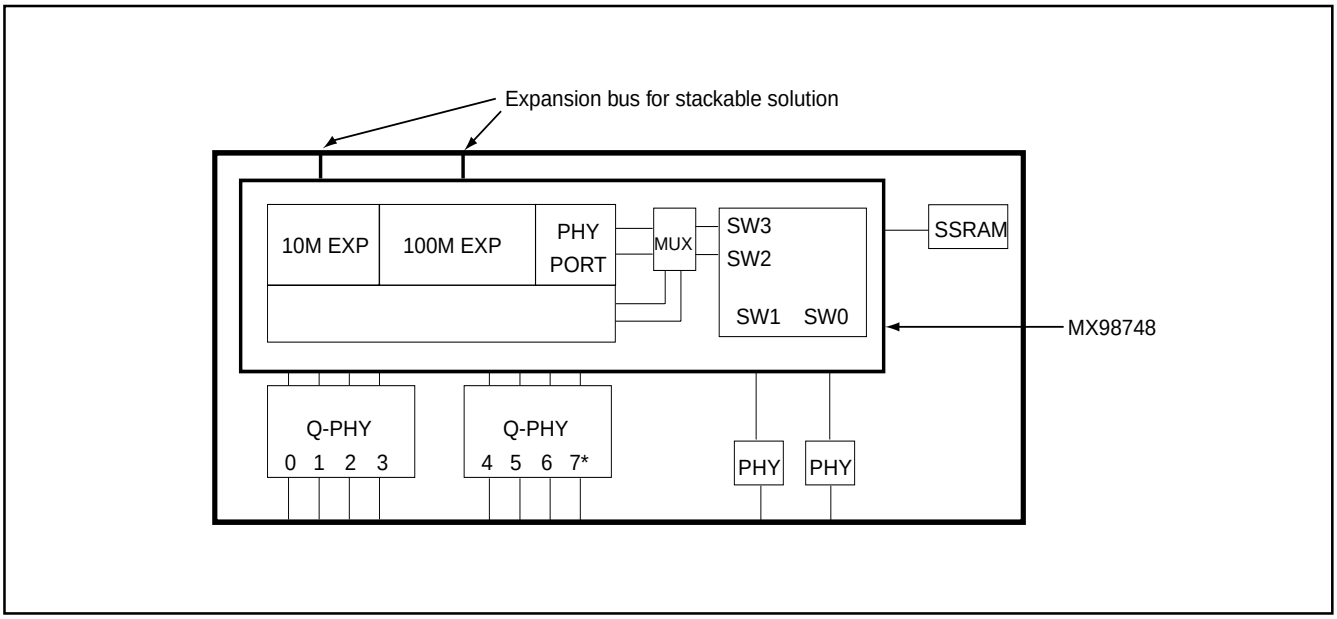
### MII Interface:



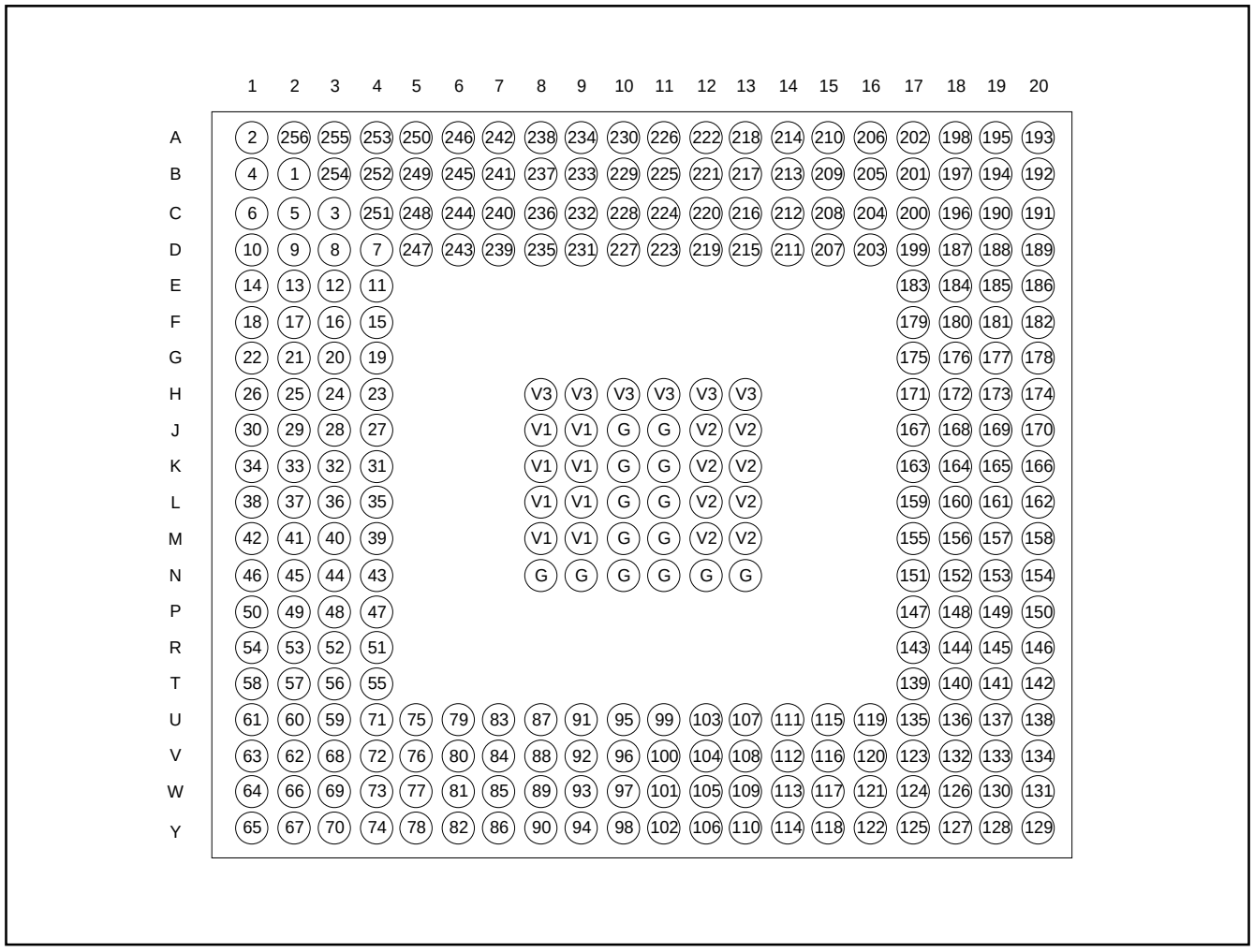

### RMII Interface:



## 4.0 System Implementation Block Diagram



## 5.0 Pin Configuration



## 6.0 Pin description

**A.Switch MII Port, 35 pins**

| Pin NAME | PIN TYPE | BGA # | Description |
|---|---|---|---|
| S1TXD[3:0] | O, 4mA | 159-162 | Switch MII Transmit Data. |
| S2TXD[3:0] | | 95-98 | |
| S1TXEN | O, 4mA | 171 | Switch MII Transmit Enable. |
| S2TXEN | | 106 | |
| S1TXCLK | I, TTL, DN | 172 | Switch MII Transmit Clock. |
| S2TXCLK | | 107 | |
| S1CRS | I, TTL, DN | 157 | Switch MII Carrier Sense. |
| S2CRS | | 93 | |
| S1RXDV | I, TTL, DN | 175 | Switch MII Receive Data Valid. |
| S2RXDV | | 110 | |
| S1COL | I, TTL, DN | 158 | Switch MII Collision Input. High if network has collision. S3COL |
| S2COL | | 94 | input from LINK[6] in mode (1100,1101) |
| S4COL | | 138 | |
| S1RXCLK | I, TTL, DN | 174 | Switch MII Receive Clock. |
| S2RXCLK | | 109 | |
| S1RXD[3:0] | I, TTL, DN | 179-176 | Switch MII 4B Receive Data. |
| S2RXD[3:0] | | 114-111 | |
| S1RXER | I, TTL, DN | 173 | Switch MII Receive Error. |
| S2RXER | | 108 | |
| DUPLEX1 | I, TTL, DN | 140 | Switch MII Duplex Input. High for half duplex, low for full duplex. |
| DUPLEX2 | | 141 | And this polarity can be change by register 0.8. DUPLEX3 input |
| DUPLEX4 | | 139 | from LINK[7] in mode(1100,1101) |
| LSWBUFF | O, 16mA | 126 | Switch SSRAM Buffer Full LED Output. Low active. Active when the buffer is full. |

**B. Switch SSRAM Interface, 50 pins**

| Pin NAME | PIN TYPE | BGA # | Description |
|---|---|---|---|
| MA[15:0] | O, 4mA | 210-217 | Switch SSRAM Address Outputs. |
| | | 225-232 | |
| MD[31:0] | I/O,TTL,4mA | 38-31 | Switch SSRAM Data I/O. |
| | | 26-19 | |
| | | 7-256 | |
| | | 246-240 | |
| GWX | O, 8mA | 202 | Switch SSRAM Write Enable. (Low active) |
| CEX | O, 8mA | 204 | Switch SSRAM Chip Enable. (Low active) |

**C. EEPROM Interface, 6 pins**

| Pin NAME | PIN TYPE | BGA # | Description |
|---|---|---|---|
| ECS/TEST0 | I/O,TTL,4mA | 122 | EEPROM Chip Select. Input for test mode selection when RESETL active. |
| ESK/TEST1 | I/O,TTL,4mA | 123 | EEPROM Clock. Input for test mode selection when RESETL active. |
| EDI/TEST2 | I/O,TTL,4mA | 124 | EEPROM Data In. Input for test mode selection when RESETL active. |
| EDO | I/O,TTL,4mA | 125 | EEPROM Data Output. |
| EEPROM | I,TTL | 203 | High for EEPROM Present. |
| EEMASTER | I,TTL | 163 | EEPROM Master. If high, MX98748 will work as the master of EEPROM interface; if low, it will work in slave mode of EEPROM interface. |

**Note:**(TEST0, TEST1, TEST2)=(0,0,0) in normal operation.

**D. Repeater Hub MII/RMII Port, 120 pins**

| Pin NAME | PIN TYPE | BGA # | Description |
|---|---|---|---|
| TXD0[3:0] | O,4mA | 253-255,8 | Repeater Transmit Data. Port7 ~ Port0 |
| TXD1[3:0] | | 28-30,39 | |
| TXD2[3:0] | | 50-53 | |
| TXD3[3:0] | | 65-68 | |
| TXD4[3:0] | | 80-83 | |
| TXD5[3:0] | | 100-103 | |
| TXD6[3:0] | | 165-168 | |
| TXD7[3:0] | | 189-192 | |
| TXEN[7:0] | O,4mA | 193,169,104, 84, 69, 54, 40, 9 | Repeater Transmit Enable. |
| TXCLK[7:0] | I,TTL | 194,170,105, 85, 70, 55, 41, 10 | Repeater Transmit Clock. |
| LINK[7:0] | I,TTL | 137, 136, 133, 128,78, 56, 127, 18 | Repeater Link Good. Low for link good. If high over 192ms, a link fail will detect. |
| CRS[7:0] | I,TTL | 188, 164, 99, 79, 64, 49, 27, 252 | Repeater Carrier Sense. |
| RXDV[7:0] | I,TTL | 197, 183, 117, 88,73, 59, 44, 13 | Repeater Receive Data Valid. Also speed input in RMII mode, low for speed 100M. |
| RXCLK[7:0] | I,TTL | 196, 182, 116, 87, 72, 58, 43, 12 | Repeater Receive Clock. |
| RXER[7:0] | I,TTL | 195, 181, 115, 86, 71, 57, 42, 11 | Repeater Receive Error. If true, a jam pattern will send out through that packet. |
| RXD0[3:0] | I,TTL | 17-14 | Repeater Receive Data. Port7 ~ Port0 |
| RXD1[3:0] | | 48-45 | |
| RXD2[3:0] | | 63-60 | |
| RXD3[3:0] | | 77-74 | |
| RXD4[3:0] | | 92-89 | |
| RXD5[3:0] | | 121-118 | |
| RXD6[3:0] | | 150-147 | |
| RXD7[3:0] | | 165-162 | |

**E. Repeater Hub LED & Control, 14 pins**

| Pin NAME | PIN TYPE | BGA # | Description |
|---|---|---|---|
| LEDINF[7:0] | I/O,TTL,16mA | 142-150 | Repeater LED Information Output (Normal Mode).In SCAN mode, LEDINF output 10/100M core state information. In power on jumper mode, set each port control register.<br>LNKACTSEL PARSEL<br>0 0 ----Normal<br>0 1 ----Partition Disable<br>1 0 ----Jabber Disable<br>1 1 ----Speed Set |
| LED10COL | O,16mA | 135 | Repeater 10M Collision LED Output. Low active Also it is 10M core state jam or quiet indicator in SCAN mode. |
| LED100COL | O,16mA | 134 | Repeater 100M Collision LED Output. Low active.Also it is 100M core state jam or quiet indicator in SCAN mode. |
| LNKACTSEL | I/O,TTL,4mA | 132 | Repeater LEDINF Link/Act Rising Latch Clock (Normal Mode) Also power on jumper mode setting, see LEDINF. |
| PARSEL | I/O,TTL,4mA | 131 | Repeater LEDINF Partition Rising Latch Clock (Normal Mode). Also power on jumper mode setting, see LEDINF. |
| UTL10SEL | I/O,TTL,4mA | 130 | Repeater LEDINF 10M Utilization Rising Latch Clock (Normal Mode). In SCAN mode, 10M state output Error/Idle indicator. Power on jam extension jumper mode setting. |
| UTL100SEL | I/O, TTL, 4mA | 129 | Repeater LEDINF 100M Utilization Rising Latch Clock (Normal Mode). In SCAN mode, 100M state output Error/Idle indicator. Power on jam extension jumper mode setting. |

**F. 10/100M Expansion Port, 22 pins**

| Pin NAME | PIN TYPE | BGA # | Description |
|---|---|---|---|
| JAMO10<br>JAMO100 | O, 8mA | 235<br>207 | Forced Jam Out. Active High. The pin is asserted upon collision detected or receive error. |
| JAMI10<br>JAMI100 | I,TTL,Schm | 236<br>208 | Forced Jam Input. Active High. Assert when other stacked hub detected a collision. |
| EPCLK10<br>EPCLK100 | I/O,TTL,DN,8mA | 238<br>219 | Expansion port Data Clock. Use as receive or transmit expansion port clock. |
| ERXDV10<br>ERXDV100 | I/O,TTL,DN,8mA | 239<br>220 | Expansion Port Data Valid. |
| E10DAT[3:0]<br>E100DAT[3:0] | I/O,TTL,DN,8mA | 224-221<br>251-248 | Expansion Port 4B Data. |
| ANYACT10<br>ANYACT100 | O,8mA | 234<br>206 | Any Activity. Active high. A OR function result of CRS[7:0]. to tell other stacked hubs there are activities. To other stacked hub's EDCRS. |
| EDCRS10<br>EDCRS100 | I,TTL,Schm | 237<br>218 | Expansion Data Carrier Sense. Active high, other stacked hubs' activities will pass on this pin. |
| EDACT10<br>EDACT100 | O,8mA | 233<br>205 | Expansion Data Activity. System application use this pin to control data flow of EDAT, ERXDV, EPCLK. |

**G. Management Interface & Miscellaneous, 9 pins**

| Pin NAME | PIN TYPE | BGA # | Desvription |
|---|---|---|---|
| MDC | I/O,TTL,DN,4mA | 151 | Management Data Clock. |
| MDIO | I/O,TTL,UP,4mA | 150 | Management Data Input/Output. |
| MODE[3:0] | I,TTL,DN | 155-152 | MODE Select. Define MX98748 function<br>0000 NORMAL - 2SW + 8MII Hub Ports<br>0001 SCAN - Hub Scan for Debug Use<br>0010 SW2RMII - 2SW + 8RMII Hub Ports<br>0011 FMODE - Hub High Speed Test Mode<br>0110 SW4D10R- 3SW + 7RMII Hub Ports, internal 10M link disable<br>0111 SW4D10- 3SW + 7MII Hub Ports, internal 10M link disable<br>1010 SW3D100R - 3SW + 7RMII Hub Ports, internal 100M link disable<br>1011 SW3D100 - 3SW + 7RMII Hub Ports, internal 100M link disable<br>1100 SW4 - 4SW \| 6MII Hub Ports with no internal link<br>1101 SW4R - 4SW \| 6RMII Hub Ports with no internal link<br>1110 - Test only<br>1111 - Test only |
| RESETL | I,TTL,Schm | 156 | Reset Bar Input. Low active. Must last more than 160ns. |
| CLK50M | I,TTL,Schm | 180 | Chip 50MHz Clock Input. |
| ALL100 | Tri-state | 209 | If any repeater port in the Hub is connected to 10 Base, the pin will assert low, otherwise it will keep in High-Z state. |

**H. Power & Ground, 34 pins**

| Pin NAME | PIN TYPE | BGA # | Desvription |
|---|---|---|---|
| VDD = 3.3V | I | In Center V1 Ball | Power. |
| GND | I | In Center G Ball | Ground. |

## 7.0 FUNCTIONAL DESCRIPTION

The MX98748 is operating by a single 50MHz clock frequency.
The MX98748 is a chip integrated with the 4-port switch and the 12-port repeater. MODE[3:0] determines the major chip function whether it is a 2SW/8Hub, 3SW/7Hub, 4SW/6 Hub Ports. MODE[3:0] also determines MII or RMII interface functions.

Each switch port can operate in 10/100M, half/full duplex mode. auto-configured by N-Way PHYceiver.
Each repeater port auto-detect line speed (10/100M), operate in half-duplex mode.
The repeater also equiped with 10/100M expansion port for stackable solution. 9 hubs can be stacked through the expansion bus architecture.

The MII management interface can program Seeq 84225 Quad PHY into half duplex repeater mode after power on for hub application. One can also force The MX98748 internal register for each repeater port to control port behavior.
The LED interface provide Link/Activity, Partition, Utilization function diaplay of repeater hub.

### 7.1 Mode seting

The MX98748 function is determined by MODE[3:0] as shown table below:

| Mode Name | MODE[3:0] | Function Description |
|---|---|---|
| NORMAL | 0000 | Normal mode, 2 SW + 8 MII Hub Ports |
| SCAN | 0001 | Test only |
| SW2RMII | 0010 | 2 SW + 8 RMII Hub ports |
| FMODE | 0011 | Test only |
| - | 0100 | Reserve |
| - | 0101 | Reserve |
| SW4D10R | 0110 | 3 SW + 7 RMII Hub port, Hub port 7 = SW4,internal 10M Link disable |
| SW4D10 | 0111 | 3 SW + 7 MII Hub port, Hub port 7 = SW4,internal 10M Link disable |
| - | 1000 | Reserve |
| - | 1001 | Reserve |
| SW3D100R | 1010 | 3 SW + 7 RMII Hub port, Hub port 6 = SW3,internal 100M Link disable |
| SW3D100 | 1011 | 3 SW + 7 MII Hub port, Hub port 6 = SW3,internal 100M Link disable |
| SEPERATE | 1100 | Seperate 4 SW and 6 MII Hub Ports |
| SEP_RMII | 1101 | Seperate 4 SW and 6 RMII Hub Ports |
| TEST | 1110 | Test only |
| TEST | 1111 | Test only |

When chip is under normal mode operation, there are extra 2 SW ports and 8 MII repeater ports from the application view point.
Under SW2RMII, same as NORMAL except hub port is RMII interface.
SW4D10R: Disable10M phy mode link between switch and hub core internally. Hub port 7 becomes Swtich port 4. Hub port 0-6 are RMII interface.
SW4D10: The same as SW4D10R except Hub port 0-6 are MII interface.

SW3D100R: Disable100M phy mode link between switch and hub core internally. Hub port 6 becomes Swtich port 3. Hub port 0-5, 7 are RMII interface.
SW3D100: The same as SW3D100R except Hub port 0-5, 7 are MII interface.
SEPERATE mode, there is no data link between switch and hub core. Hub port 6, 7 become SW3 & SW4. The chip functions 4 switch ports and 6 hub ports. LINK[6] is S3COL, LINK[7] is DUPLEX3.
SEP_RMII: The same as SEPERATE, except 6 hub ports are RMII interface.

### 7.2 EEPROM pin function description

EEPROM = true means EEPROM device present.

### 7.3 Port function jumper mode description

Each port will set its port behavior depends on two control pin by power on latch.

| LNKACTSEL | PARSEL | Function Description |
|---|---|---|
| 0 | 0 | Normal |
| 0 | 1 | Partition Disable |
| 1 | 0 | Jabber Disable |
| 1 | 1 | Speed Set. True=100M |

### 7.4 End of Jam extension jumper mode description

End of jam extension can be alter by power on jumper setting.

| UTL10SEL | UTL100SEL | Function Description |
|---|---|---|
| 0 | 0 | Extend 15 nibbles |
| 0 | 1 | Extend 0 nibbles |
| 1 | 0 | Extend 10 nibbles |
| 1 | 1 | Extend 20 nibbles |

### 7.5 Switch function description

Four ports switch are built-in on the MX98748. The unique features make the MX98748 can be easily used in dual speed HUB application. Two of the 4-PORTS switch are used internally to connect 10M segment and 100M segment. Another extra two switch ports make the application of the chip diversely.

Four ported fast ethernet switch controller is embedded. The switchcore includes MAC protocal, address resolution logic, buffer management and SSRAM controller.

The MAC block supports store-and-forward mode. Both Full Duples Flow Control 802.3x and JAM based flow control are supported. The transmit and receive beffer's threshold is programmable to avid only port occupying all buffer resource.

The Address Resolution Logic functions for Address look up, learning, and aging. The address table is in external SSRAM and contains four layer of hash table.

The buffer management includes Broadcast descriptor and Empty List(QM). Each has several discriptors for management.

The SSRAM controller functions as follows. Buffer memory is a 64K*32 SSRAM. The higher memory is used for address resolution table. The others are partitioned into 256 bytes/page for data and descriptor. Each packet may use 1~6 page depends on packet size. Each descriptor page includes 16 descriptors.

| memory size | page size | ARL | No. of page |
|---|---|---|---|
| 64K*32 | 256Byte | 2K entries | 960 |

### 7.5 Internal Register Function Description

The internal register are addressed by the following address:

0x10 * (~EEMASTER) + offset

offset is between 0x0 and oxf.

#### 7.5.1 Internal Register Format

| Offset | Description | Default |
|---|---|---|
| 0000(0x0) | Configuration Register | 0x1c00 |
| 0001(0x1) | Aging Time. 10sec/per count | 0x001e |
| 0010(0x2) | Flow Control Pause Counter | 0x01ff |
| 0011(0x3) | MAC ID [15:0] for Flow Control | 0x0000 |
| 0100(0x4) | MAC ID [31:16] for Flow Control | 0x0000 |
| 0101(0x5) | MAC ID [47:32] for Flow Control | 0x0000 |
| 0110(0x6) | Port 0 Receive Buffer threshold | 0x0200 |
| 0111(0x7) | Port 1 Receive Buffer threshold | 0x0200 |
| 1000(0x8) | Port 2 Receive Buffer threshold | 0x0200 |
| 1001(0x9) | Port 3 Receive Buffer threshold | 0x0200 |
| 1010(0xa) | TxThresh Enable / Port 0 Transmit Buffer threshold | 0x2300 |
| 1011(0xb) | TxThresh Enable / Port 1 Transmit Buffer threshold | 0x2300 |
| 1100(0xc) | TxThresh Enable / Port 2 Transmit Buffer threshold | 0x2300 |
| 1101(0xd) | TxThresh Enable / Port 3 Transmit Buffer threshold0 | 0x2300 |
| 1110(0xe) | Multicast Buffer threshold | 0x2300 |

#### 7.5.2 Internal Register Description

##### 7.5.2.1 Configuration Register

| 15 | 14 | 13 | 12 | 11 10 | 9 | 8 | 7 6 | 5 4 | 3 2 1 0 |
|---|---|---|---|---|---|---|---|---|---|
| R | MIM | C16D | FCE | Hash | R | DP | BPN | AbortCnt | MBZ |

Default: 0x1c00

Bit 3:0 : MBZ : Must Be Zero "0000"

Bit 5:4 : AbortCnt : Define the packets may be received after recive threshold is over.

00 : Can Receive 8 good Packets after Receive threshold over

01 : Can Receive 16 good packets after Receive threshold over

10 : Can Receive 32 good packets after Receive threshold over

11 : All good packets will be Received after Receive threshold over

Bit 7:6 : BPN : Define the Back-Pressure-Number of jamming the coming packets.

00 : Back Pressure Count = 8

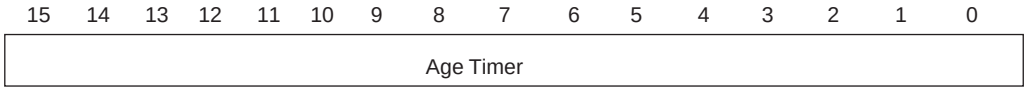
01 : Back Pressure Count = 16

10 : Back Pressure Count = 32

11 : Back Pressure Count = Infinite

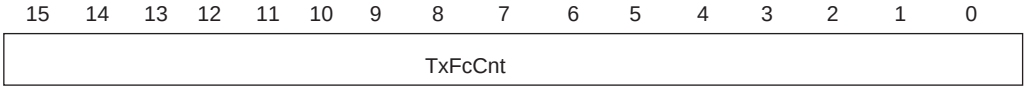
Bit 8 : Duplex polarity : 1 : Input pin Duplex High -> Full, Low -> Half
0 : Input pin Duplex Low -> Full, High -> Half
Bit 9 : Reserved
Bit 11:10 : Hash bits select. 0 : Hash bits = CRC bit 12:4
1 : Hash bits = CRC bit 18:10
2 : Hash bits = CRC bit 25:17
3 : Hash bits = CRC bit 31:23
Bit 12 : Full Duplex Flow Control Enable, high active.
Bit 13 : Collision-16 Disable, high active.
Bit 14 : Management Interface Master Enable, high active.
Bit 15 : Reserved

#### 7.5.2.2 Ageing timer



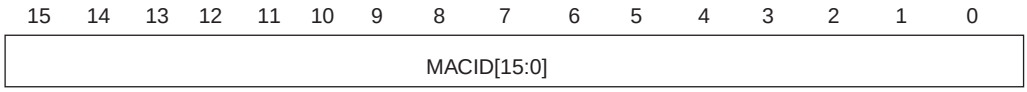

Default : 0x001e
Bit 0:15 : AgeTimer : Ageing Timer 10 sec/per count

#### 7.5.2.3 Flow Control Pause Time



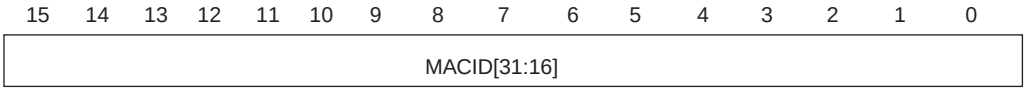

Default: 0x01ff
Bit 0:15: TxFcCnt : Flow Control Pause Time

#### 7.5.2.4 MAC ID [15:0] for Flow Control



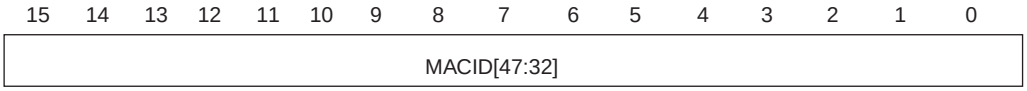

Default: 0x0000
Bit 0:15: MACID[15:0] : MAC ID for Flow Control

#### 7.5.2.5 MAC ID [31:16] for Flow Control



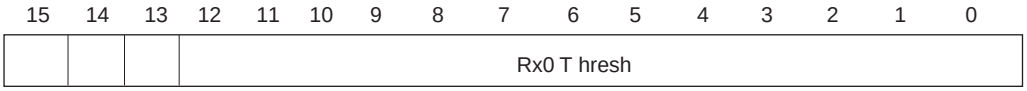

Default: 0x0000
Bit 0:15: MACID[31:16] : MAC ID for Flow Control

#### 7.5.2.6 MAC ID [47:32] for Flow Control



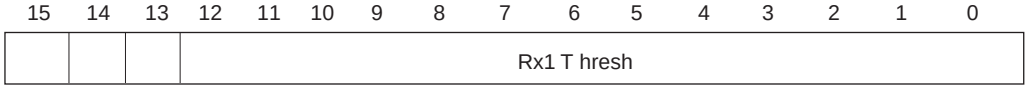

Default: 0x0000
Bit 0:15: MACID[47:32] : MAC ID for Flow Control

#### 7.5.2.7 Port 0 Receive buffer threshold



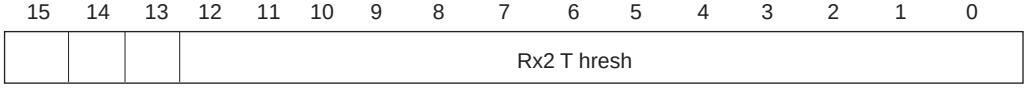

Default: 0x0200
Bit 0:12 : Rx0Thresh : Port 0 Receive buffer threshold.

#### 7.5.2.8 Port 1 Receive buffer threshold



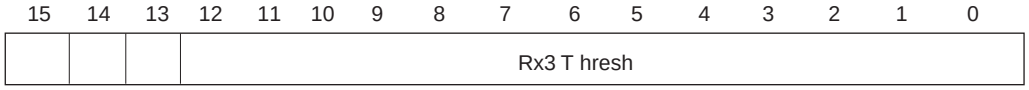

Default: 0x0200
Bit 0:12 : Rx1Thresh : Port 1 Receive buffer threshold.

#### 7.5.2.9 Port 2 Receive buffer threshold



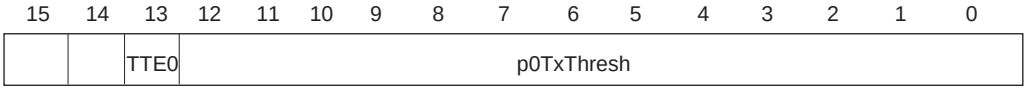

Default: 0x0200
Bit 0:12 : Rx2Thresh : Port 2 Receive buffer threshold.

#### 7.5.2.10 Port 3 Receive buffer threshold



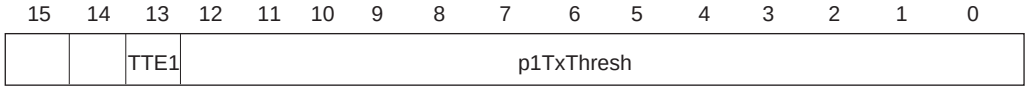

Default: 0x0200
Bit 0:12 : Rx3Thresh : Port 3 Receive buffer threshold.

#### 7.5.2.11 Port 0 Transmit buffer Threshold and transmit threshold enable



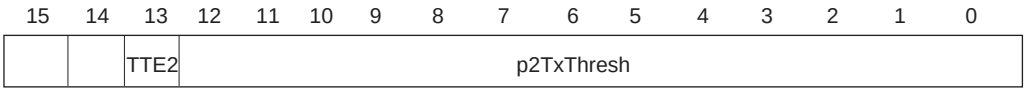

Default: 0x2300
Bit 0:12 : p0TxThresh : Port 0 Transmit buffer Thresh.
Bit 13 : TTE0 : Port 0 Transmit Threshold Enable

#### 7.5.2.12 Port 1 Transmit buffer Threshold and transmit threshold enable



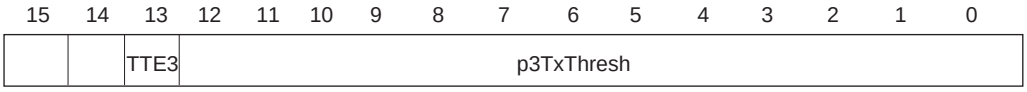

Default: 0x2300
Bit 0:12 : p1TxThresh : Port 1 Transmit buffer Thresh.
Bit 13 : TTE1 : Port 1 Transmit Threshold Enable

#### 7.5.2.13 Port 2Transmit buffer Threshold and transmit threshold enable



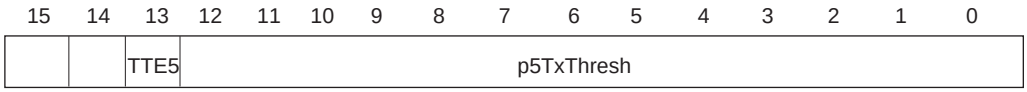

Default: 0x2300
Bit 0:12 : p2TxThresh : Port 2 Transmit buffer Thresh.
Bit 13 : TTE2 : Port 2 Transmit Threshold Enable

#### 7.5.2.14 Port 3 Transmit buffer Threshold and transmit threshold enable




Bit 0:12 : p3TxThresh : Port 3 Transmit buffer Thresh.
Bit 13 : TTE3 : Port 3 Transmit Threshold Enable

#### 7.5.2.15 Port 4 Transmit buffer Threshold and transmit threshold enable




Bit 0:12 : mTxThresh : Multicast Transmit buffer Thresh.
Bit 13 : TTE5 : Multicast Transmit Threshold Enable

## 8.0 ABSOLUTE MAXIMUM OPERATION RATING

| RATING | VALUE |
|---|---|
| Supply Volatge(VCC) | 3.0V to 4.0V |
| DC Input Voltage(Vin) | -0.3V to VCC+0.3V |
| DC Output Voltage (Vout) | -0.3V to VCC+0.3V |
| Storage Temperature Range(TSTG) | -55℃ to 150℃ |
| Power Dissipation(PD) | 800mW |
| ESD rating(Rzap=1.5K, Czap=100pF) | 2000V |

Absolute Maximum Rating for MX98748

Notice:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cauase permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

## 9.0 AC/DC CHARACTERISTIC

A.Supply Current

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| ICC | Average Active(TXing/RXing) Supply Current | X1=50MHz<br>VIN=Switching | - | - | mA |
| ICCIDLE | Average Idle Supply Current | X1=50MHz<br>VIN=VCC/GND | - | - | mA |
| IDD | Static IDD Current | X1=Undriven | - | - | mA |

### 9.1 DC CHARACTERISTIC

B.TTL Inputs, Outputs Tri-States

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| Vil | Input Low Voltage | - | - | 0.8 | V |
| Vih | Input High Voltage | | 2.0 | VCC+0.3 | V |
| Iin | Input Current | VI=VCC/GND | -1.0 | 1.0 | V |
| Voh | Minimum High Level<br>Output Voltage<br>(others/MII/Expansion) | Ioh=-2mA/<br>-4mA/<br>-8mA | 2.4 | - | V |
| Vol | Maximum Low Level<br>Output Voltage<br>(others/MII/Expansion) | Iol=2mA/<br>4mA/<br>8mA | - | 0.4 | V |
| Ioz | Maximum TRI-STATE<br>Output Leakage Current | VOUT=VCC/<br>GND | -10.0 | 10.0 | uA |

### 9.2 AC Characterisitics

#### A.MII Management Interface

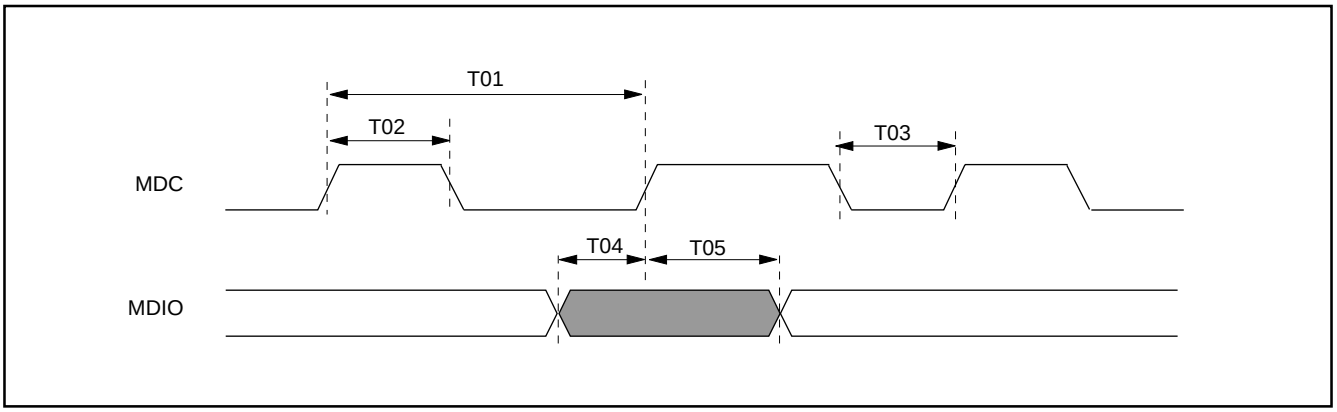



Figure 6-1 MDIO Timing Relationship to MDC

| Symbol | Description | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| T01 | Period MDC | 400 | - | ns |
| T02 | High Time for MDC | 160 | - | ns |
| T03 | Low Time for MDC | 160 | - | ns |
| T04 | MDIO Setup to MDC rising edge(sourced by STA) | 10 | - | ns |
| T05 | MDIO Hold to MDC rising edge(sourced by STA) | 10 | - | ns |
| T05 | MDIO to MDC rising edge (source by MX98748) | 200 | - | ns |

**B.MII/RMII Interface**

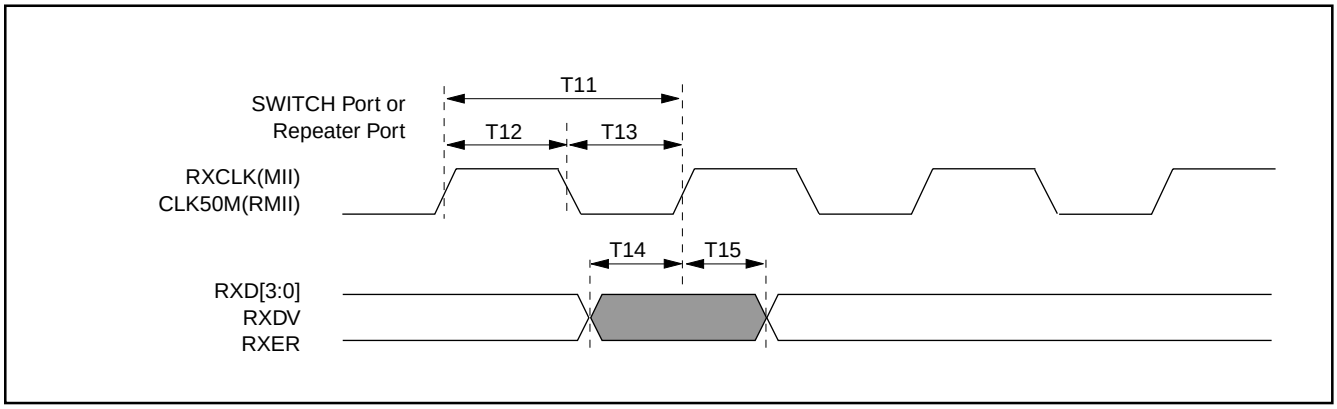



Figure 6-2 Receive Signal Timing Relationships at the MII/RMII

| Symbol | Description(Include SWITCH & REPEATER Port) | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| T11 | RECEIVE CLOCK Period in 100M(Note1) | 39.998 | 40 | 40.002 | ns |
| T11 | RECEIVE CLOCK Period in 10M(Note1) | 399.98 | 40 | 400.02 | ns |
| T11 | CLK50M Period(Note1) | 19.999 | 20 | 20.001 | ns |
| T12 | RECEIVE CLOCK High Time | 0.35*T11 | - | - | ns |
| T13 | RECEIVE CLOCK Low Time | 0.35*T11 | - | - | ns |
| T14 | RXD[3:0]/RXDV/RXER Setup Time (MII Interface) | 5 | - | - | ns |
| T14 | RXD[3:0]/RXDV/RXER Setup Time (RMII Interface Repeater Only) | 2 | - | - | ns |
| T15 | RXD[3:0]/RXDV/RXER Hold Time(MII Interface) | 5 | - | - | ns |
| T15 | RXD[3:0]/RXDV/RXER Hold Time (RMII Interface Repeater Only) | 4 | - | - | ns |

Note 1: The accurate RECEIVE CLOCK frequency shall be 25MHz+/- 50ppm.
CLK50M should be 50MHz+/-50ppm.

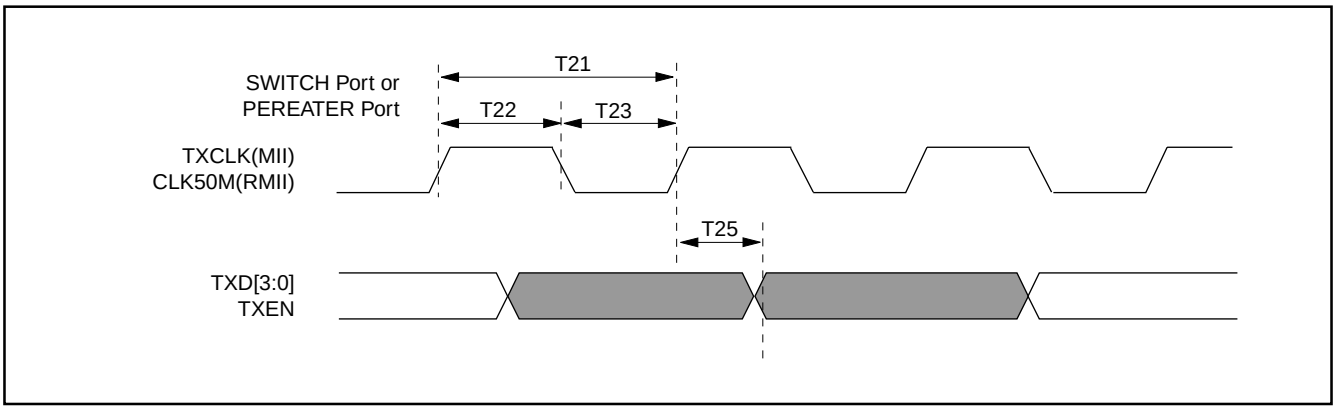



Figure 6-3Transmit Signal Timing Relationships at the MII/RMII

| Symbol | Description(Include SWITCH & REPEATER Port) | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| T21 | TRANSMIT CLOCK Period in 100M(Note1) | 39.998 | 40 | 40.002 | ns |
| T21 | TRANSMIT CLOCK Period in 10M(Note1) | 39.998 | 40 | 40.002 | ns |
| T21 | CLK50M Period (Note1) | 19.999 | 20 | 20.001 | ns |
| T22 | TRANSMIT CLOCK High Time | 0.3*T21 | - | - | ns |
| T23 | TRANSMIT CLOCK Low Time | 0.3*T21 | - | - | ns |
| T24 | TRANSMIT CLOCK to TXD[3:0]/TXEN Delay (MII Interface) | 4 | - | 11 | ns |
| T24 | CLK50M to TXD[3:0]/TXEN Delay (RMII Interface Repeater Only) | 4 | - | 11 | ns |

Note 1: The accurate TRANSMIT CLOCK frequency shall be 25MHz+/- 50ppm.
CLK50M should be 50MHz +/- 50ppm.

### C.Power on Reset

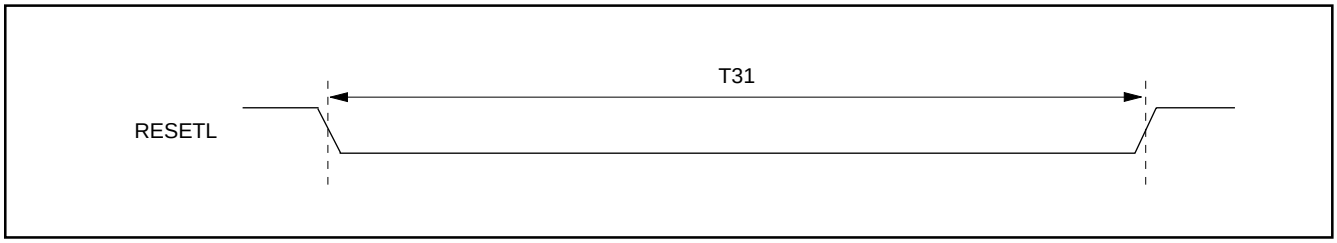



Figure 6-6 Timing Constraint RESETL

| Symbol | Description | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| T31 | Pulse Width for RESETL | 1000 | - | ns |

### D.Expansion Port

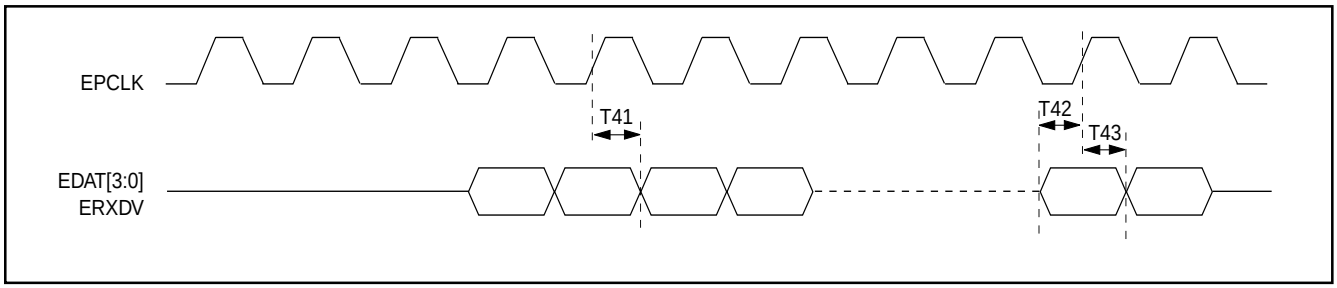



Figure 6-11 EPCLK and EDAT Timing Relationship

| Symbol | Description | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| T41 | EPCLK to EDAT delay time (100M bps)<br>(EPCLK and EDAT outputed from MX98748) | 19 | 21 | ns |
| T41 | EPCLK to EDAT delay time(10M bps)<br>(EPCLK and EDAT outputed from MX98748) | 199 | 201 | ns |
| T42 | EDAT/ERXDV Sepup Time (Input to MX98748) | 5 | - | ns |
| T43 | EDAT/ERXDV Hold Time (Input to MX98748) | 5 | - | ns |

## E.LED Display

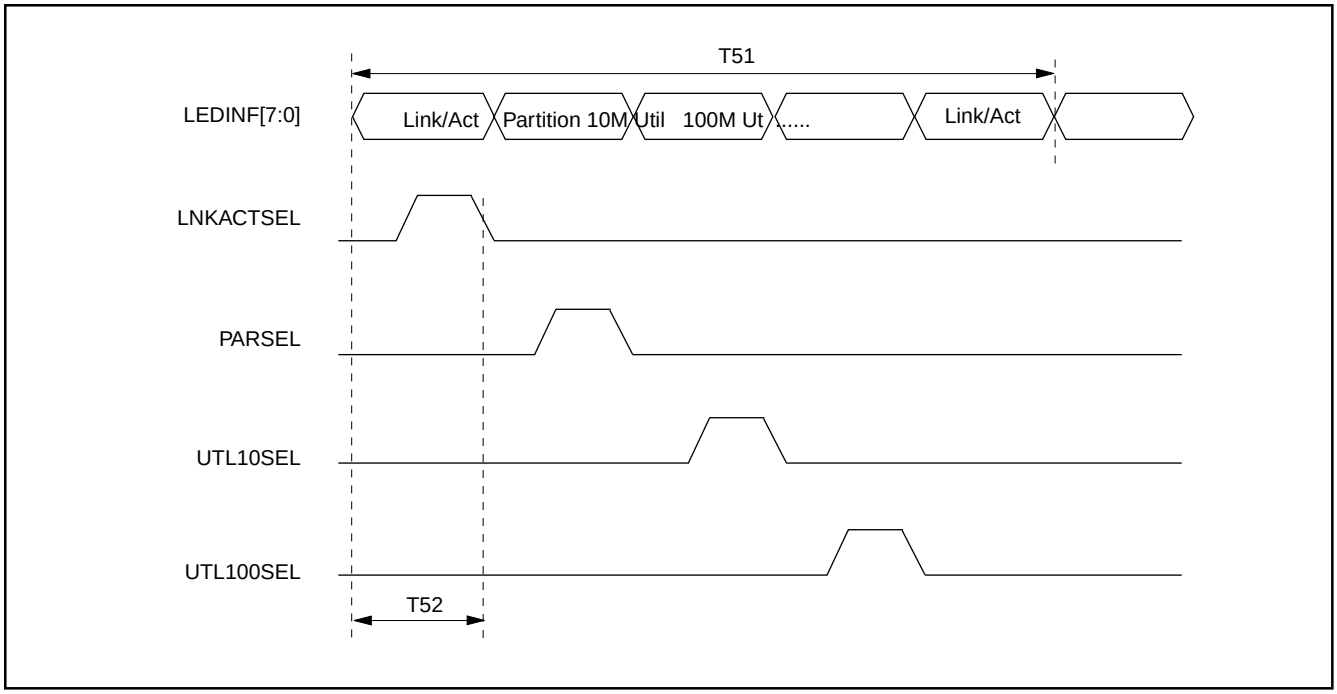



Figure 6-12 Timing Relationship for LED Display

| Symbol | Description | Typ. | UNIT |
|---|---|---|---|
| T51 | Multiplexed LEDINF Period | 40 | ms |
| T52 | Latch Clock Period | 8 | ms |

### F.SSRAM Interface

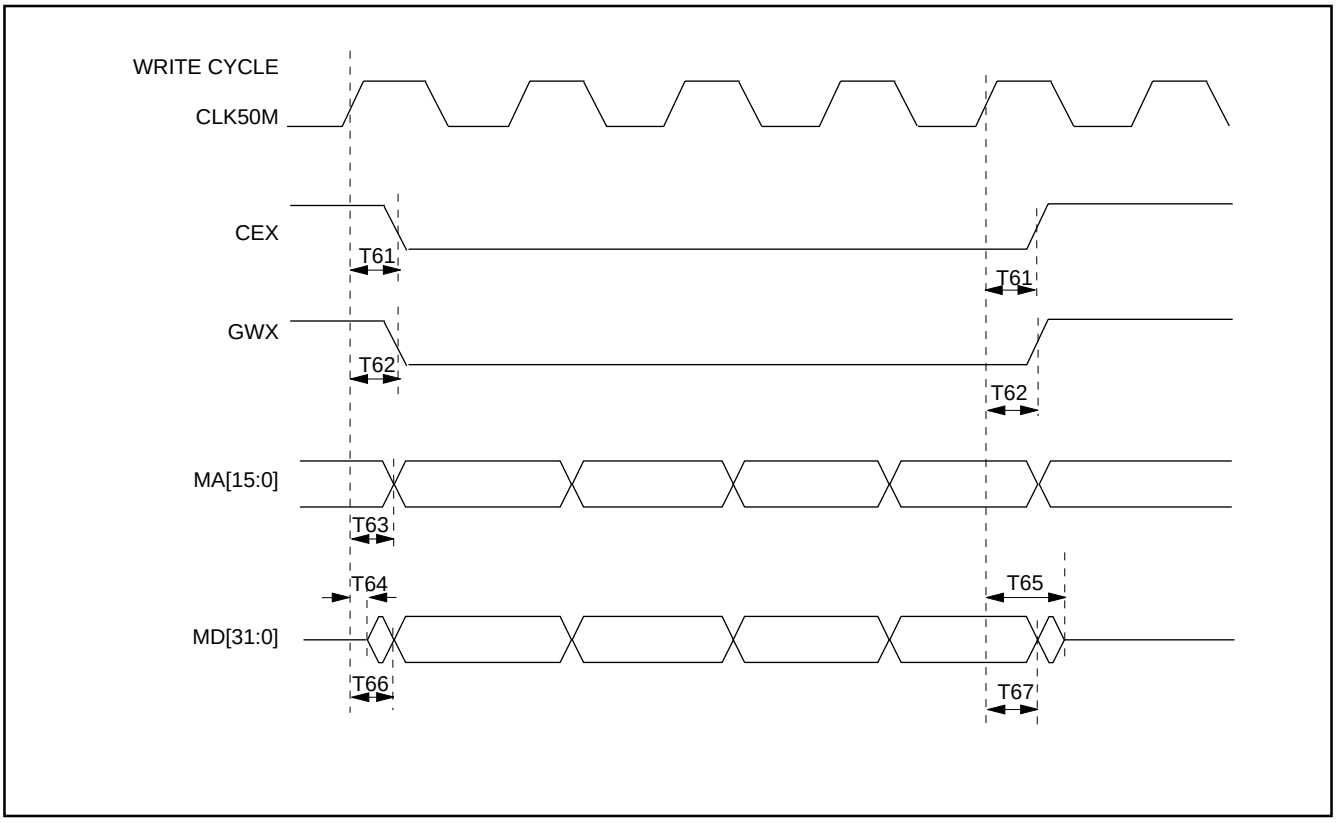



Figure 6-12 Timing Relationship for SSRAM Interface(WRITE Cycle)

| Symbol | Description | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| T61 | CLK50M to CEX Change | 3.5 | 10.5 | ns |
| T62 | CLK50M to GWX Change | 3.5 | 10.5 | ns |
| T63 | CLK50M to MA Valid | 2.5 | 12.5 | ns |
| T64 | CLK50M to MD Low Z | 3.5 | 8 | ns |
| T65 | CLK50M to MD High Z | 3.5 | 8 | ns |
| T66 | CLK50M to MD Valid | 3.5 | 15 | ns |
| T67 | CLK50M to MD Invalid | 3.5 | - | ns |

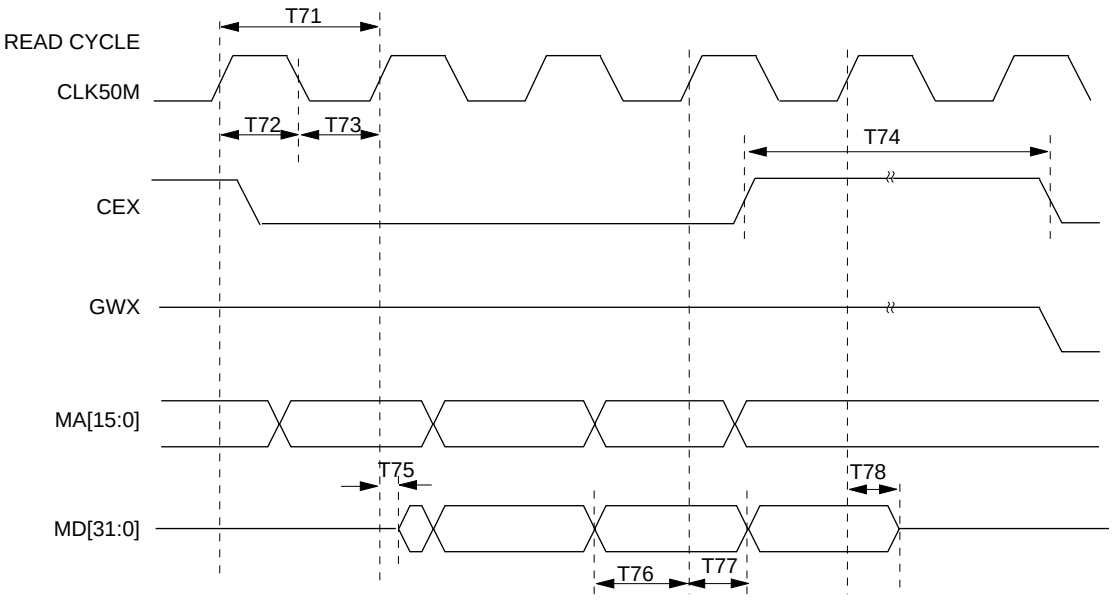



Figure 6-12 Timing Relationship for SSRAM Interface(READ Cycle)

| Symbol | Description | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| T71 | CLK50M Cycle Time | 20 | - | ns |
| T72 | CLK50M High Pulse Width | 7 | - | ns |
| T73 | CLK50M Low Pulse Width | 7 | - | ns |
| T74 | RAED to WRITE Width | 40 | - | ns |
| T75 | CLK50M to MD Low Z | 0 | - | ns |
| T76 | MD Setup Time | 0 | - | ns |
| T77 | MD Hold Time | 1.5 | - | ns |
| T78 | CLK50M to MD High Z | - | 23 | ns |

### G. EEPROM Interface

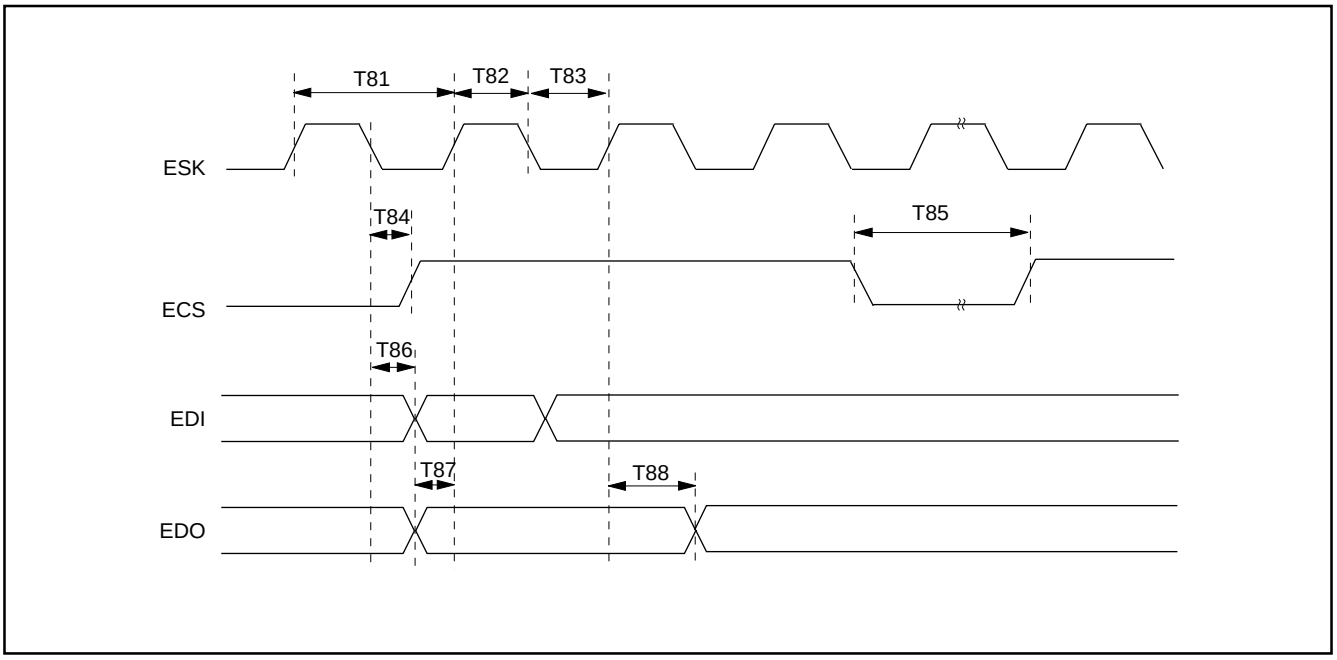
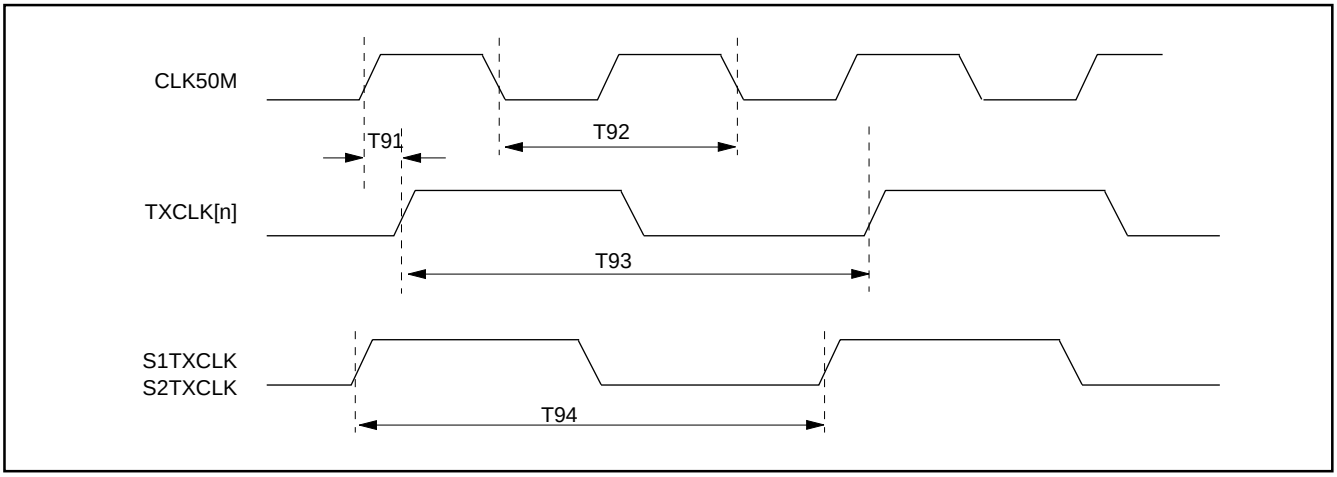



Figure 6-12 Timing Relationship for EEPROM Interface

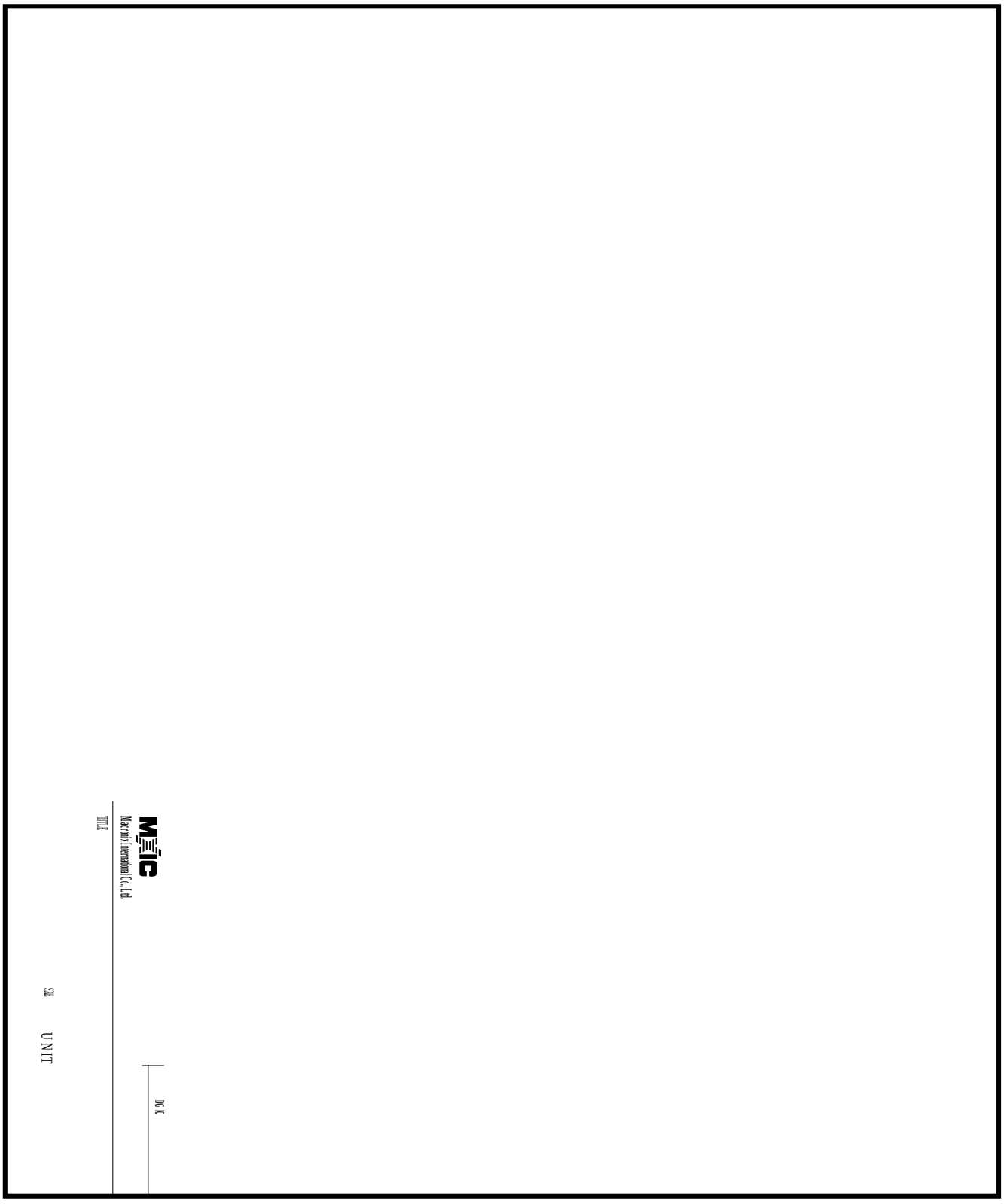
| Symbol | Description | MIN. | Typ. | MAX. | UNIT |
|---|---|---|---|---|---|
| T81 | ESK Cycle Time | - | 1280 | - | ns |
| T82 | ESK High Pulse Width | - | 640 | - | ns |
| T83 | ESK Low Pulse Width | - | 640 | - | ns |
| T84 | ESK Low to ECS Change | - | - | 3 | ns |
| T85 | ECS Low Width | 2560 | - | - | ns |
| T86 | ESK Low to EDI Change | - | - | 4 | ns |
| T87 | EDO Setup Time | 5 | - | - | ns |
| T88 | EDO Hold Time | 1 | - | - | ns |

**H. CLOCK Input**




| Symbol | Description | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| T91 | CLK50M to TXCLK[n] Time Interval in MII Mode | 6 | - | - | ns |
| T92 | CLK50M Period | 19.999 | 20 | 20.001 | ns |
| T93 | TXCLK[n] Period in 100M | 39.998 | 40 | 40.002 | ns |
| T93 | TXCLK[n] Period in 10M | 399.98 | 400 | 400.02 | ns |
| T94 | S1TXCLK, S2TXCLK Period in 100M | 39.998 | 40 | 40.002 | ns |
| T94 | S1TXCLK, S2TXCLK Period in 10M | 399.98 | 400 | 400.02 | ns |

## 10.PACKAGE INFORMATION



## REVISION HISTORY

| Revision | Description | Page | Date |
|---|---|---|---|
| 0.1 | Correct mistyping<br>Modify A/C waveform | | JUN/22/1999 |
| 0.2 | Add Typical Application<br>Update MII management interface<br>Update MII/RMII interface(receive Transmit)<br>Add clock input waveform | P2<br>P21<br>P22<br>P29 | JUN/17/1999 |
| 0.3 | Correct mistyping<br>Add Package Information<br>Modify EEPROM Interface T81:1024-->1280;T82:512-->640;<br>T83:512-->640;T85:2048-->2560 | P1,6-16<br>P30<br>P28 | AUG/20/1999 |

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