

4 M-BIT DYNAMIC RAM
1 M-WORD BY 4-BIT, FAST PAGE MODE

DESCRIPTION

The μPD424400 is a 1 048 576 words by 4 bits dynamic CMOS RAM. The fast page mode capability realize high speed access and low power consumption.

These are packed in 26-pin plastic TSOP, 26-pin plastic SOJ and 20-pin plastic ZIP.

FEATURES

- 1 048 576 words by 4 bits organization
- Single +5.0 V±10 % power supply
- Fast access and cycle time

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μPD424400-60	660.0 mW	5.5 mW (CMOS level input)	60 ns	120 ns	40 ns
μPD424400-70	550.0 mW		70 ns	140 ns	45 ns
μPD424400-80	495.0 mW		80 ns	160 ns	50 ns
μPD424400-10	440.0 mW		100 ns	190 ns	60 ns

- 1 024 refresh cycles/16 ms
- CAS before RAS refresh, RAS only refresh, Hidden refresh
- Multiplexed address inputs Row address : A0 to A9, Column address : A0 to A9

The information in this document is subject to change without notice.

★ ORDERING INFORMATION

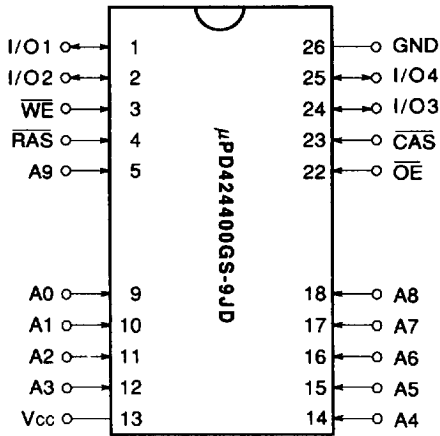
Part number	Access time (MAX.)	Package	Quality grade
μPD424400GS-60-9JD	60 ns	26-pin Plastic TSOP (300 mil)	Standard
μPD424400GS-70-9JD	70 ns		
μPD424400GS-80-9JD	80 ns		
μPD424400GS-10-9JD	100 ns		
μPD424400GS-60-9KD	60 ns	26-pin Plastic TSOP Reverse bent (300 mil)	
μPD424400GS-70-9KD	70 ns		
μPD424400GS-80-9KD	80 ns		
μPD424400GS-10-9KD	100 ns		
μPD424400LA-60	60 ns	26-pin Plastic SOJ (300 mil)	
μPD424400LA-70	70 ns		
μPD424400LA-80	80 ns		
μPD424400LA-10	100 ns		
μPD424400V-60	60 ns	20-pin Plastic ZIP (400 mil)	
μPD424400V-70	70 ns		
μPD424400V-80	80 ns		
μPD424400V-10	100 ns		

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

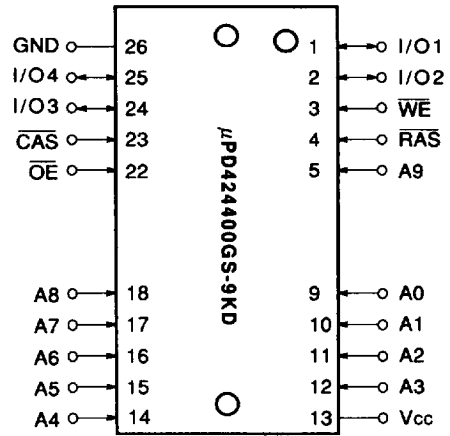
PIN CONFIGURATIONS (Marking Side)



26-pin Plastic TSOP (300 mil)

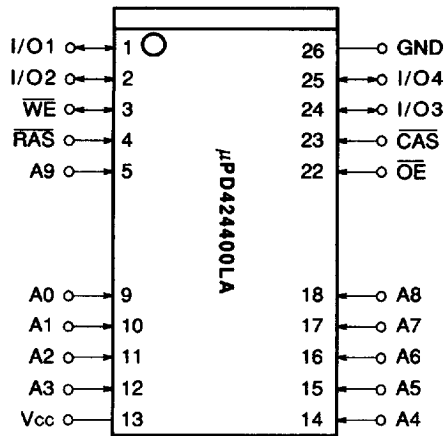


Reverse bent

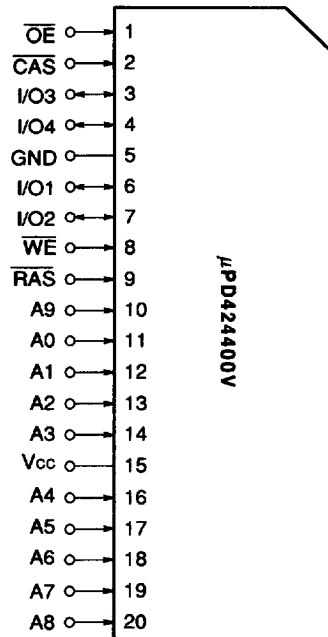


- A0 to A9 : Address Inputs
- I/O1 to I/O4 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$: Column Address Strobe
- $\overline{\text{WE}}$: Write Enable
- $\overline{\text{OE}}$: Output Enable
- Vcc : Supply Voltage
- GND : Ground

26-pin Plastic SOJ (300 mil)

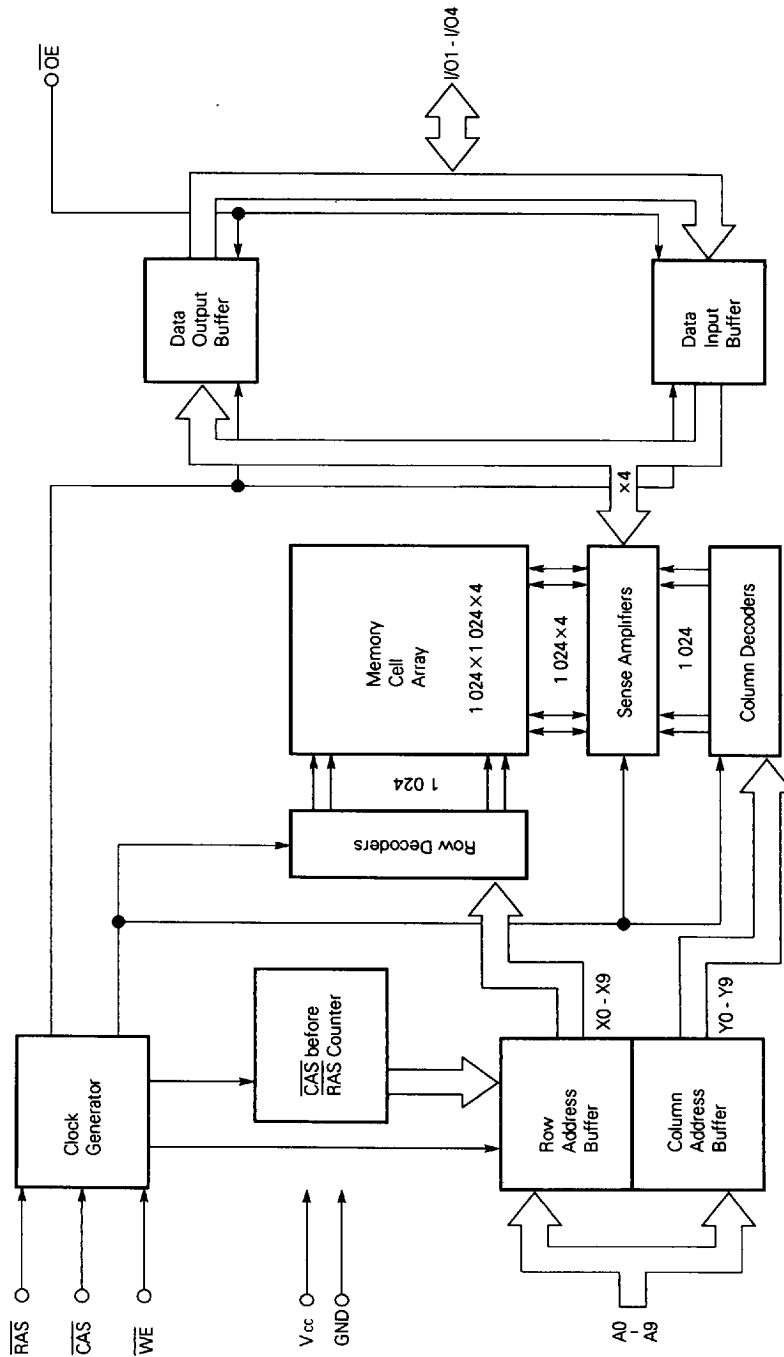


20-pin Plastic ZIP (400 mil)



- A0 to A9 : Address Inputs
- I/O1 to I/O4 : Data Inputs/Outputs
- \overline{RAS} : Row Address Strobe
- \overline{CAS} : Column Address Strobe
- \overline{WE} : Write Enable
- \overline{OE} : Output Enable
- Vcc : Supply Voltage
- GND : Ground

BLOCK DIAGRAM



★ INPUT/OUTPUT PIN FUNCTIONS

The μPD424400 has input pins \overline{RAS} , \overline{CAS} , \overline{WE} , \overline{OE} , A0 to A9 and input/output pins I/O1 to I/O4.

Pin name	Input/output	Function
\overline{RAS} (Row address strobe)	Input	\overline{RAS} activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • \overline{CAS} before \overline{RAS} refresh.
\overline{CAS} (Column address strobe)		\overline{CAS} activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A9 (Address input)		Address bus. Input total 20-bit of address signal, upper 10-bit and lower 10-bit in sequence (address multiplex method). Therefore, one word is selected from 1 048 576-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating \overline{RAS} . Then, switch the address bus to column address and activate \overline{CAS} . Each address is taken into the device when \overline{RAS} and \overline{CAS} are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of \overline{RAS} and \overline{CAS} .
\overline{WE} (Write enable)		Write control signal. Write operation is executed by activating \overline{RAS} , \overline{CAS} and \overline{WE} .
\overline{OE} (Output enable)		Read control signal. Read operation can be executed by activating \overline{RAS} , \overline{CAS} and \overline{OE} . If \overline{WE} is activated during read operation, \overline{OE} is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data input/output)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

ELECTRICAL SPECIFICATIONS Notes 1, 2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V _T		-1.0 to +7.0	V
Supply voltage	V _{CC}		-1.0 to +7.0	V
Output current	I _O		50	mA
Power dissipation	P _D		1	W
Operating temperature	T _{opt}		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		4.5	5.0	5.5	V
High level input voltage	V _{IH}		2.4		V _{CC} +1.0	V
Low level input voltage	V _{IL}		-1.0		+0.8	V
Ambient temperature	T _a		0		70	°C

CAPACITANCE (T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 to A9			5	pF
	C _{I2}	RAS, CAS, WE, OE			7	pF
Data Input/Output capacitance	C _D	I/O1 to I/O4			7	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}(\text{MIN})}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	120	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	100		
			$t_{\text{RAC}} = 80 \text{ ns}$	90		
			$t_{\text{RAC}} = 100 \text{ ns}$	80		
Standby current	I _{CC2}	$V_{\text{IH}(\text{MIN})} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $V_{\text{CC}} - 0.2 \text{ V} \leq \overline{\text{RAS}}, \overline{\text{CAS}}$ $I_o = 0 \text{ mA}$	$I_o = 0 \text{ mA}$	2	mA	
			$I_o = 0 \text{ mA}$	1		
$\overline{\text{RAS}}$ only refresh current	I _{CC3}	$\overline{\text{RAS}}$ Cycling $V_{\text{IH}(\text{MIN})} \leq \overline{\text{CAS}}$ $t_{\text{RC}} = t_{\text{RC}(\text{MIN})}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	120	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	100		
			$t_{\text{RAC}} = 80 \text{ ns}$	90		
			$t_{\text{RAC}} = 100 \text{ ns}$	80		
Operating current (Fast page mode)	I _{CC4}	$\overline{\text{CAS}}$ Cycling $\overline{\text{RAS}} \leq V_{\text{IL}(\text{MAX})}$ $t_{\text{PC}} = t_{\text{PC}(\text{MIN})}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	90	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	80		
			$t_{\text{RAC}} = 80 \text{ ns}$	70		
			$t_{\text{RAC}} = 100 \text{ ns}$	60		
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh current	I _{CC5}	$\overline{\text{RAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}(\text{MIN})}$ $I_o = 0 \text{ mA}$	$t_{\text{RAC}} = 60 \text{ ns}$	120	mA	3,4
			$t_{\text{RAC}} = 70 \text{ ns}$	100		
			$t_{\text{RAC}} = 80 \text{ ns}$	90		
			$t_{\text{RAC}} = 100 \text{ ns}$	80		
Input leakage current	I _{I(L)}	$V_i = 0 \text{ to } 5.5 \text{ V}$ all other pins except for testing pin = 0 V	-10	+10	μA	
Output leakage current	I _{O(L)}	Outputs are disabled (Hi-Z) $V_o = 0 \text{ to } 5.5 \text{ V}$	-10	+10	μA	
High level output voltage	V _{OH}	$I_o = -5.0 \text{ mA}$	2.4		V	
Low level output voltage	V _{OL}	$I_o = +4.2 \text{ mA}$		0.4	V	



AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted) Notes 5, 6

(1/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t _{RC}	120		140		160		190		ns	7
Read Write Cycle Time	t _{RWC}	165		185		210		250		ns	7
Fast Page Mode Cycle Time (Read or Write)	t _{PC}	40		45		50		60		ns	7
Read Modify Write Cycle Time (Fast Page Mode)	t _{PRWC}	85		90		100		120		ns	7
Access Time from RAS	t _{RAC}		60		70		80		100	ns	8, 9
Access Time from CAS (Falling Edge)	t _{CAC}		15		20		20		25	ns	8, 9
Access Time from Column Address	t _{AA}		30		35		40		50	ns	8, 9
Access Time from CAS Precharge	t _{ACP}		35		40		45		55	ns	9
Access Time from OE	t _{OEa}		20		20		20		25	ns	9
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	17	40	17	50	ns	8
CAS to Data Setup Time	t _{CLZ}	0		0		0		0		ns	9
OE to Data Setup Time	t _{OLZ}	0		0		0		0		ns	9
Output Buffer Turn-off Delay Time (CAS)	t _{OFF}	0	15	0	15	0	20	0	25	ns	10
OE to Data Delay Time	t _{oED}	15		15		20		25		ns	
Output Buffer Turn-off Delay Time (OE)	t _{oEZ}	0	15	0	15	0	20	0	25	ns	
OE Command Hold Time	t _{oEH}	0		0		0		0		ns	
OE to RAS inactive Setup Time	t _{oES}	0		0		0		0		ns	
Transition Time (Rise and Fall)	t _T	3	50	3	50	3	50	3	50	ns	
RAS Precharge Time	t _{RP}	50		60		70		80		ns	
RAS Pulse Width (Random Read, Write Cycle)	t _{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
RAS Pulse Width (Fast Page Mode)	t _{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
RAS Hold Time	t _{RSH}	20		20		20		25		ns	
CAS Pulse Width	t _{CAS}	15	10 000	20	10 000	20	10 000	25	10 000	ns	
CAS Hold Time	t _{CSH}	60		70		80		100		ns	
RAS to CAS Delay Time	t _{RCD}	20	40	20	50	25	60	25	90	ns	8
CAS to RAS Precharge Time	t _{CRP}	10		10		10		10		ns	11
CAS Precharge Time	t _{CPN}	10		10		10		10		ns	
CAS Precharge Time (Fast Page Mode)	t _{CP}	10		10		10		10		ns	
RAS Precharge CAS Hold Time	t _{RPC}	10		10		10		10		ns	
RAS Hold Time from CAS Precharge	t _{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t _{ASR}	0		0		0		0		ns	
Row Address Hold Time	t _{RAH}	10		10		12		12		ns	
Column Address Setup Time	t _{ASC}	0		0		0		0		ns	
Column Address Hold Time	t _{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to RAS	t _{RAL}	30		35		40		50		ns	
Read Command Setup Time	t _{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to RAS	t _{RRH}	10		10		10		10		ns	12
Read Command Hold Time Referenced to CAS	t _{RCH}	0		0		0		0		ns	12

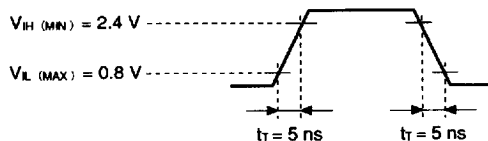
(2/2)

Parameter	Symbol	t _{RAC} = 60 ns		t _{RAC} = 70 ns		t _{RAC} = 80 ns		t _{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write Command Hold Time Referenced to $\overline{\text{CAS}}$	t _{WCH}	15		15		15		20		ns	13
Write Command Pulse Width	t _{WP}	15		15		15		20		ns	13
Data-in Setup Time	t _{DS}	0		0		0		0		ns	14
Data-in Hold Time	t _{DH}	15		15		15		20		ns	14
$\overline{\text{WE}}$ Command Setup Time	t _{WCS}	0		0		0		0		ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	40		40		45		55		ns	15
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	80		90		105		130		ns	15
$\overline{\text{CAS}}$ Precharge Delay Time Referenced to $\overline{\text{WE}}$ (Fast Page Mode)	t _{CPWD}	55		60		70		85		ns	15
Column Address Delay Time Referenced to $\overline{\text{WE}}$	t _{AWD}	50		55		65		80		ns	15
Write Command Lead Time Referenced to $\overline{\text{RAS}}$	t _{RWL}	20		20		20		25		ns	
Write Command Lead Time Referenced to $\overline{\text{CAS}}$	t _{CWL}	15		15		15		20		ns	
$\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	t _{CSR}	10		10		10		10		ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh	t _{CHR}	15		15		15		20		ns	
$\overline{\text{WE}}$ Setup Time	t _{WSR}	10		10		10		10		ns	
$\overline{\text{WE}}$ Hold Time	t _{WHR}	15		15		15		20		ns	
Refresh Time	t _{REF}		16		16		16		16	ms	

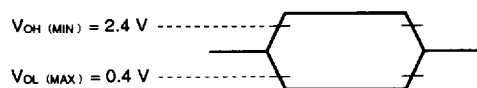
Notes

1. All voltages are referenced to GND.
2. An initial pause of 100 μs is required after power up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 CAS before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles are required.
3. t_{CC1} , t_{CC3} , t_{CC4} and t_{CC5} depend on t_{AC} and t_{PC} . Specified values are obtained with outputs open.
4. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$ and $\overline{\text{CAS}} = V_{IH}$.
5. AC measurements assume $t_r = 5$ ns.
6. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



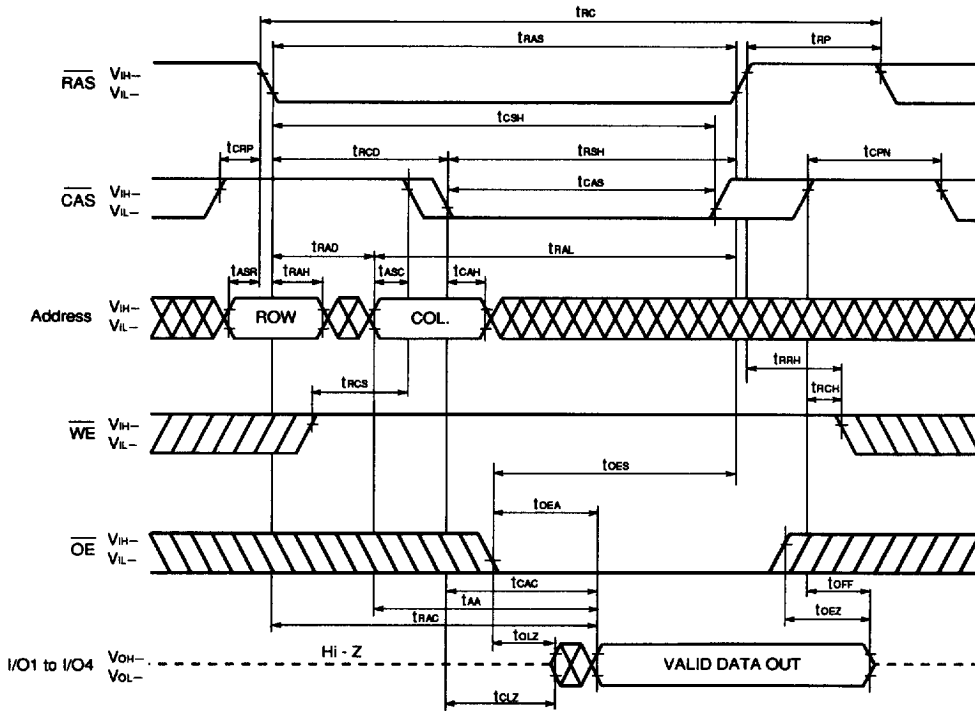
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_a = 0$ to 70 °C) is assured.
8. In random read cycle, the access time is changed by the conditions of t_{RAD} and t_{RCD} as follows.

CONDITION	ACCESS TIME
$t_{RAD} \leq t_{RAD}(\text{MAX.})$ and $t_{RCD} \leq t_{RCD}(\text{MAX.})$	$t_{RAC}(\text{MAX.})$
$t_{RAD}(\text{MAX.}) \leq t_{RAD}$ and $t_{RCD} \leq t_{RCD}(\text{MAX.})$	$t_{AA}(\text{MAX.})$
$t_{RCD}(\text{MAX.}) \leq t_{RCD}$	$t_{CAC}(\text{MAX.})$

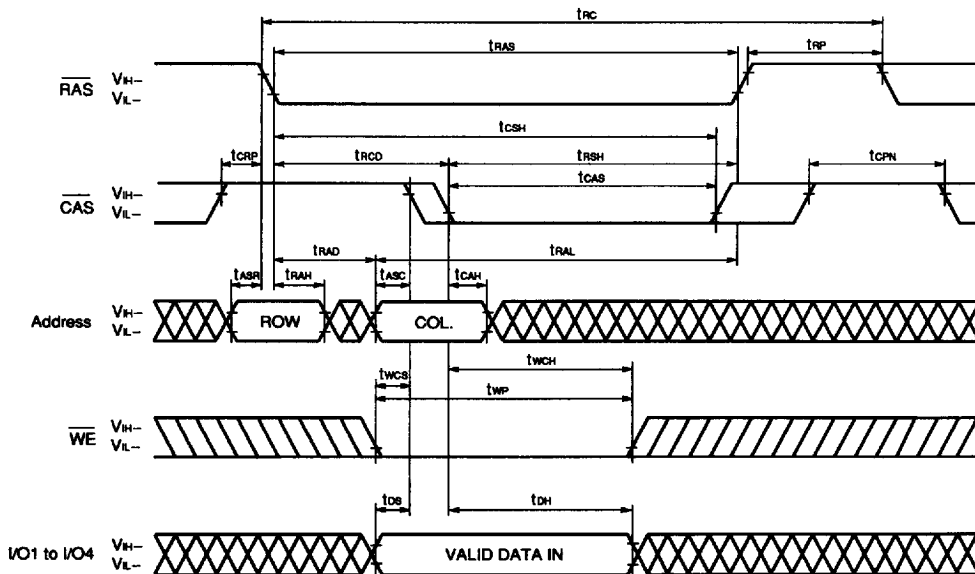
$t_{RAD}(\text{MAX.})$ and $t_{RCD}(\text{MAX.})$ indicate the points which the access time changes and are not the limits of operation.

9. Loading conditions are 2 TTL and 100 pF.
10. $t_{OFF}(\text{MAX.})$ and $t_{OEZ}(\text{MAX.})$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL} .
11. $t_{CRP}(\text{MIN.})$ requirement should be applicable for $\overline{\text{RAS}} / \overline{\text{CAS}}$ cycles preceded by any cycles.
12. Either $t_{RCH}(\text{MIN.})$ or $t_{RRH}(\text{MIN.})$ must be satisfied for a read cycle.
13. $t_{WP}(\text{MIN.})$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH}(\text{MIN.})$ should be satisfied.
14. This specification is referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{WE}}$ falling edge in late write or read modify write cycles.
15. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS}(\text{MIN.}) \leq t_{WCS}$, the cycle is an early write cycle and the data out pins will remain Hi-Z through the entire cycle. If $t_{RWD}(\text{MIN.}) \leq t_{RWD}$, $t_{CWD}(\text{MIN.}) \leq t_{CWD}$, $t_{AWD}(\text{MIN.}) \leq t_{AWD}$ and $t_{CPWD}(\text{MIN.}) \leq t_{CPWD}$, the cycle is a read modify write cycle and condition of the data out (at access time) is indeterminate.

READ CYCLE

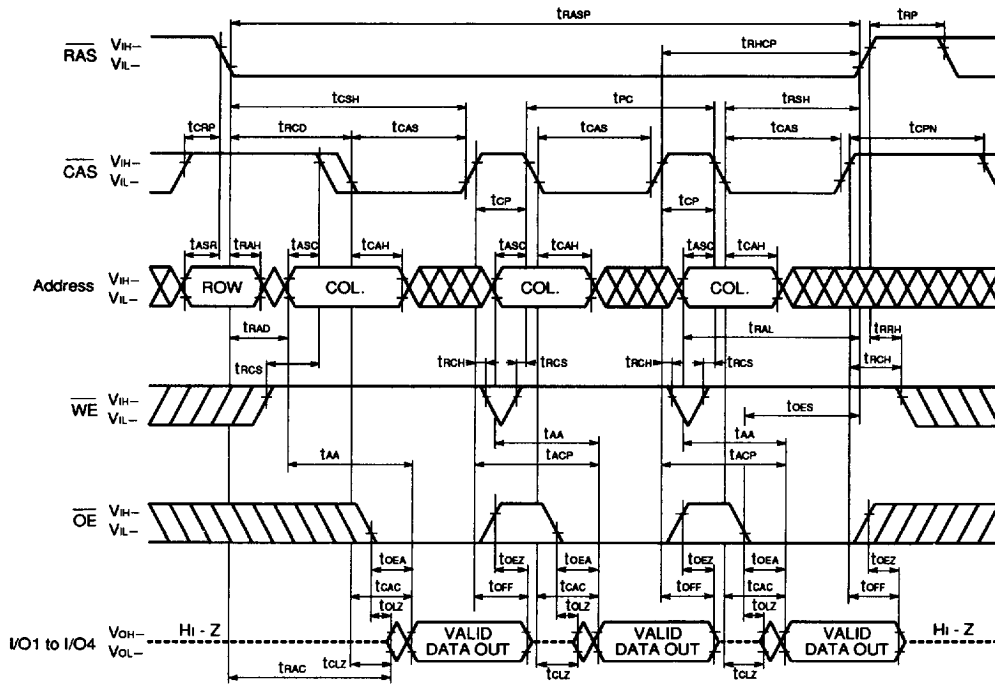


EARLY WRITE CYCLE



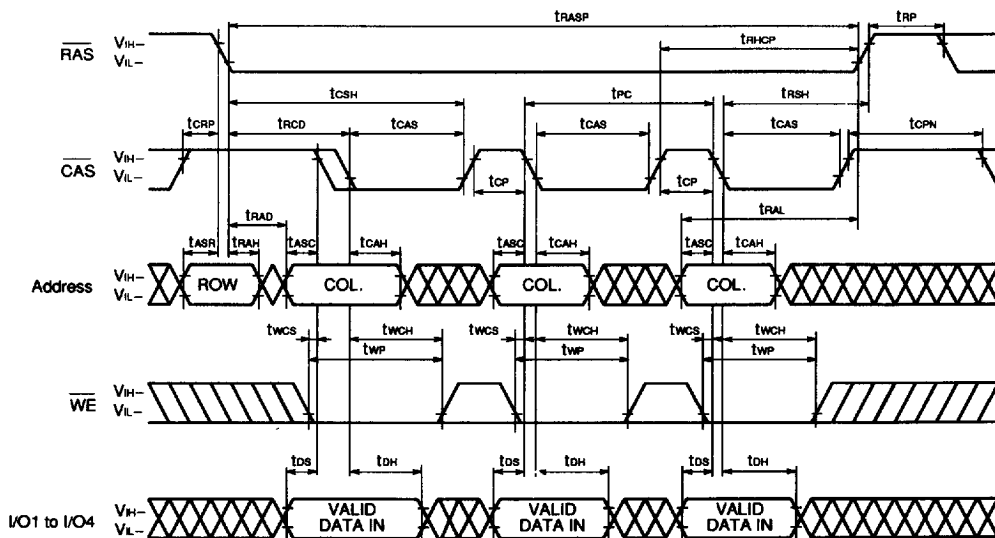
Remark \overline{OE} = Don't Care

FAST PAGE MODE READ CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

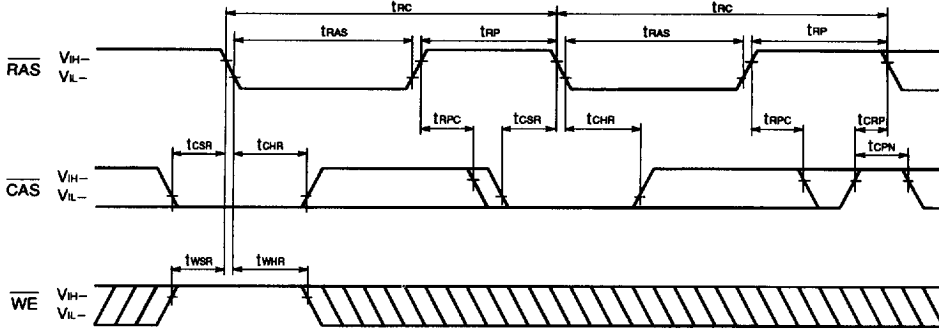
FAST PAGE MODE EARLY WRITE CYCLE



Remark \overline{OE} = Don't Care

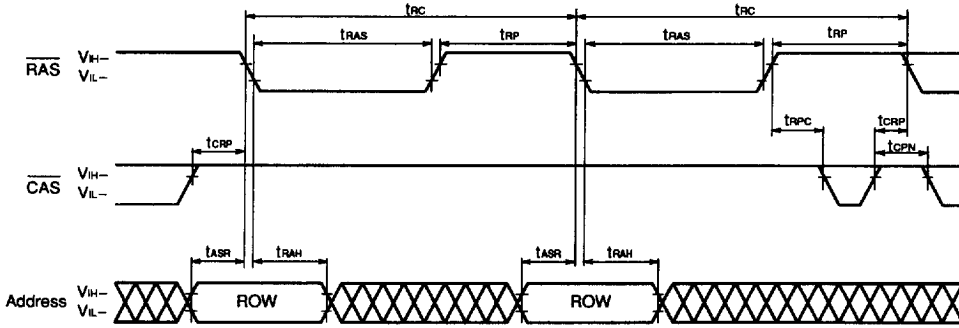
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive CAS cycles within the same RAS cycle.

★ CAS BEFORE RAS REFRESH CYCLE



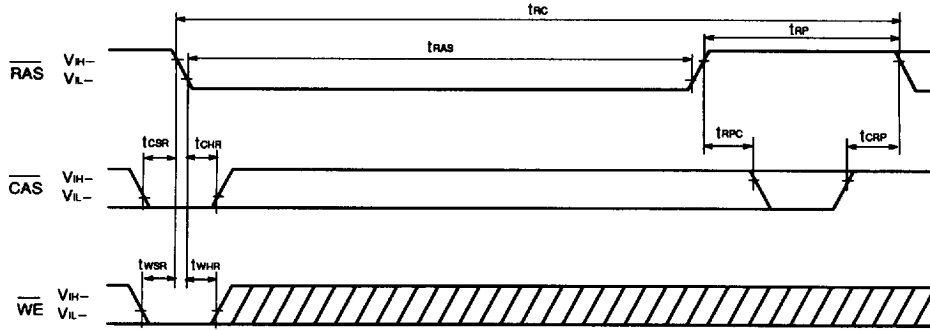
Remark Address, \overline{OE} = Don't care I/O1 to I/O4 = Hi-Z

★ RAS ONLY REFRESH CYCLE



Remark \overline{WE} , \overline{OE} = Don't care I/O1 to I/O4 = Hi-Z

TEST MODE SET CYCLE ($\overline{\text{WE}}$ AND $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE)



Remark Address, $\overline{\text{OE}}$ = Don't care I/O1 to I/O4 = Hi - Z

TEST MODE

TEST MODE is fast test function. On using this mode, test time is reduced to 1/2. In this TEST MODE, internal organization is 512 K words by 8 bits apparently. Don't care about the input levels of the $\overline{\text{CAS}}$ input A0.

1. How to enter TEST MODE

Through TEST MODE SET CYCLE ($\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle), the device enters TEST MODE.

2. Write / Read in TEST MODE

Write data of "1" or "0" through I/O1 to I/O4 by controlling address except for above-mentioned address. Each input data through each I/O write 2 bits at once. And read through I/O1 to I/O4 to check written data. If each 2 bits are written rightly, each I/O data is "1". But wrong, the data is "0".

3. Refresh in TEST MODE

Use normal read cycle or $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

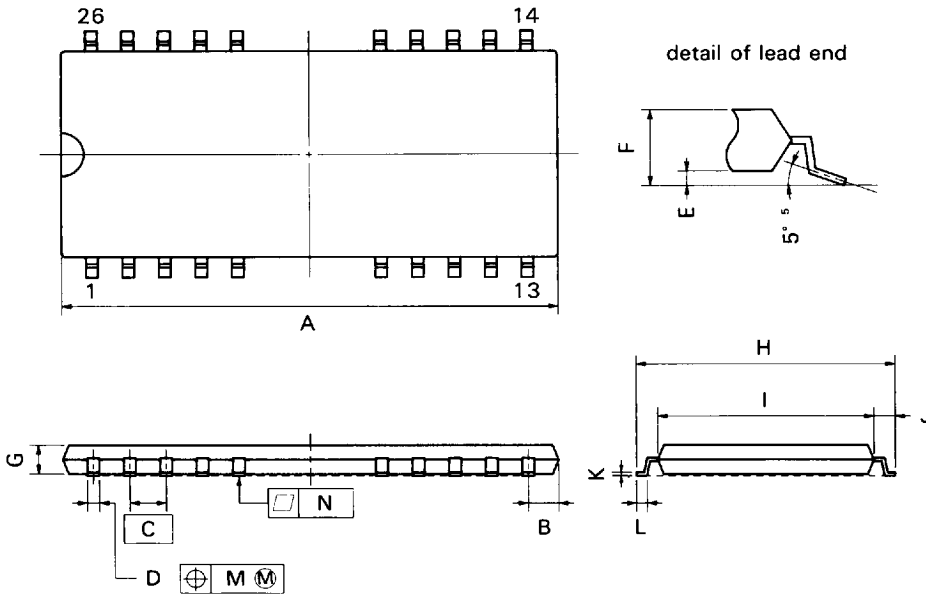
4. How to exit from TEST MODE

Through $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle, the device exits from TEST MODE.

PACKAGE DRAWINGS



26 PIN PLASTIC TSOP (300mil)



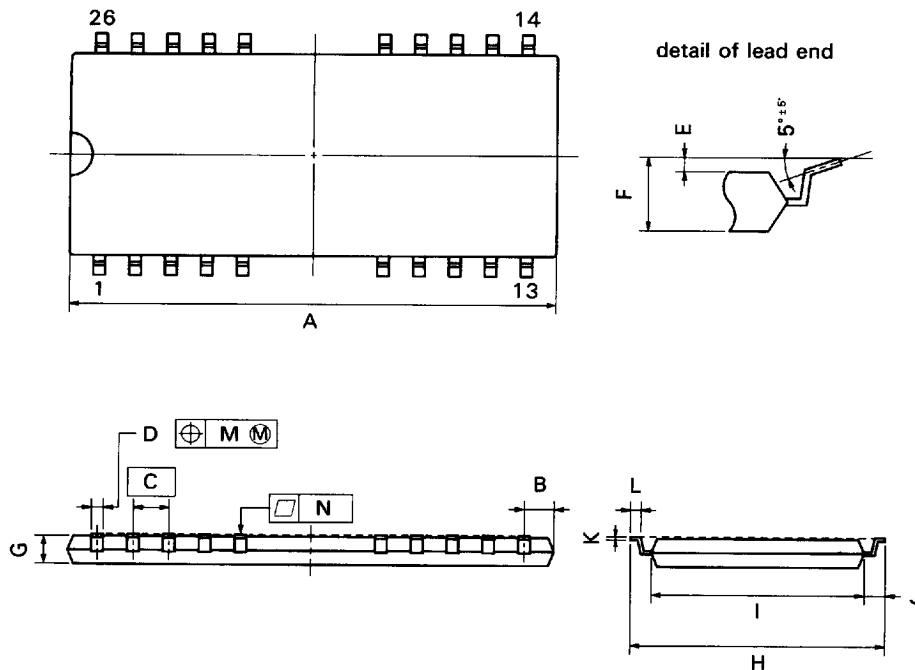
S26GS 50 9JD 1

NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.54 MAX.	0.691 MAX.
B	1.18 MAX.	0.047 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10}	0.016 ^{+0.004}
E	0.05 ^{+0.05}	0.002 ^{+0.002}
F	1.13 MAX.	0.045 MAX.
G	1.0	0.039
H	9.22 ^{±0.2}	0.363 ^{±0.008}
I	7.62 ^{±0.1}	0.300 ^{±0.004}
J	0.8 ^{±0.2}	0.031 ^{+0.008}
K	0.125 ^{+0.10}	0.005 ^{+0.004}
L	0.5 ^{±0.1}	0.020 ^{+0.005}
M	0.21	0.009
N	0.10	0.004

26 PIN PLASTIC TSOP (300mil)



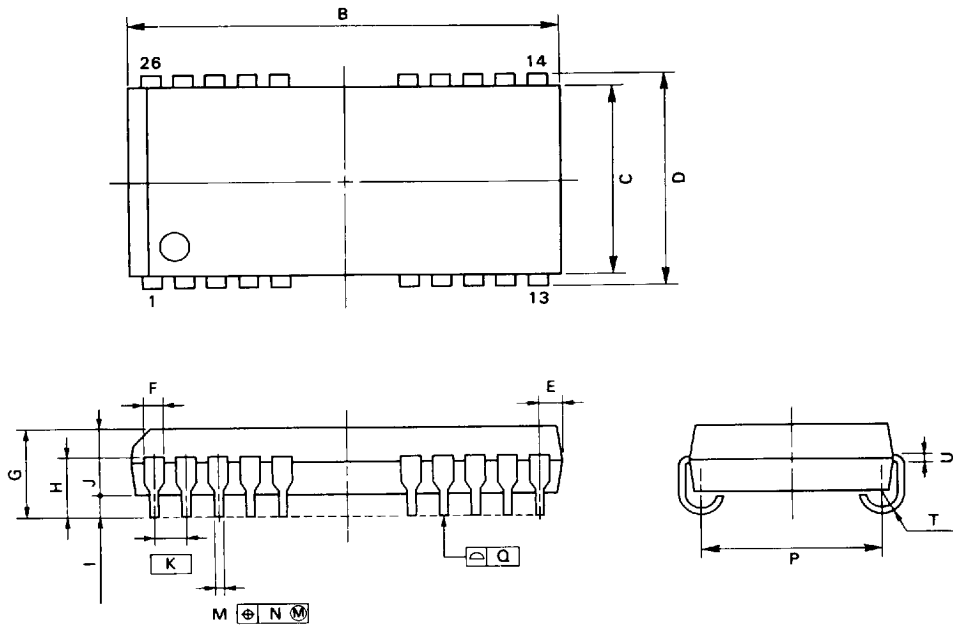
S26GS-50-9KD-1

NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.54 MAX.	0.691 MAX.
B	1.18 MAX.	0.047 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{±0.10}	0.016 ^{+0.004} _{-0.005}
E	0.05 ^{±0.05}	0.002 ^{±0.002}
F	1.13 MAX.	0.045 MAX.
G	1.0	0.039
H	9.22 ^{±0.2}	0.363 ^{±0.008}
I	7.62 ^{±0.1}	0.300 ^{±0.004}
J	0.8 ^{±0.2}	0.031 ^{+0.003} _{-0.002}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5 ^{±0.1}	0.020 ^{+0.004} _{-0.002}
M	0.21	0.009
N	0.10	0.004

26PIN PLASTIC SOJ (300 mil)



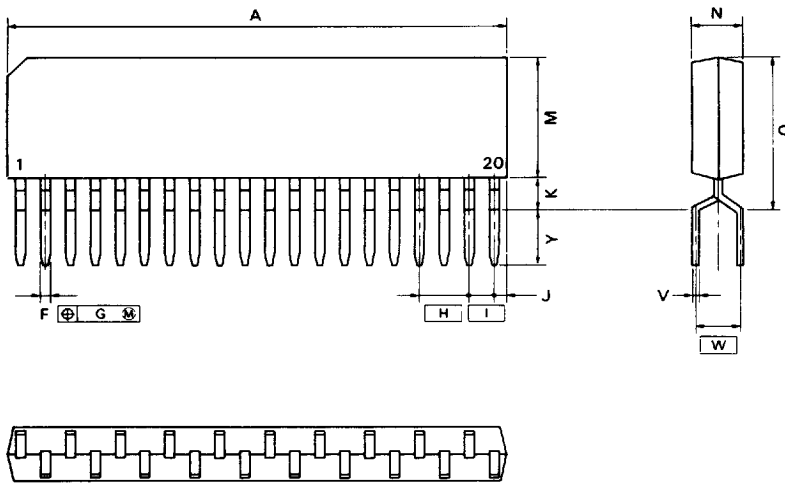
P26LA-50A-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition

ITEM	MILLIMETERS	INCHES
B	17.4 ^{+0.2} _{-0.35}	0.685 ^{+0.008} _{-0.013}
C	7.57	0.298
D	8.47 ^{±0.2}	0.333 ^{+0.008} _{-0.008}
E	1.08 ^{±0.15}	0.043 ^{+0.006} _{-0.007}
F	0.6	0.024
G	3.5 ^{±0.2}	0.138 ^{±0.008}
H	2.4 ^{±0.2}	0.094 ^{+0.009} _{-0.008}
I	0.8 MIN	0.031 MIN
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40 ^{±0.10}	0.016 ^{+0.004} _{-0.005}
N	0.12	0.005
P	6.73 ^{±0.20}	0.265 ^{±0.008}
Q	0.15	0.006
T	R 0.85	R 0.033
U	0.20 ^{+0.10} _{-0.06}	0.008 ^{+0.004} _{-0.002}

20PIN PLASTIC ZIP (400 mil)



NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P20V-254-400A-1

ITEM	MILLIMETERS	INCHES
A	26.67 MAX	1.050 MAX.
F	0.5 ^{±0.1}	0.020 ^{+0.004} _{-0.004}
G	φ0.25	φ0.010
H	2.54	0.100
I	1.27	0.050
J	1.27 MAX	0.050 MAX
K	1.0 MIN.	0.039 MIN.
M	8.9 MAX.	0.350 MAX
N	2.8 ^{±0.2}	0.110 ^{+0.008} _{-0.008}
Q	10.16 MAX.	0.400 MAX.
V	0.25 ^{+0.08} _{-0.08}	0.010 ^{+0.004} _{-0.004}
W	2.54	0.100
Y	3.3 ^{±0.5}	0.130 ^{±0.02}

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD424400.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case other soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

μPD424400GS : 26-pin plastic TSOP (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	IR35-107-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (10 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD424400LA : 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit ^{Note} : 7 days (20 hours pre-baking is required at 125 °C afterwards) [Remark] (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or below, Time : 3 seconds or below (Per one side of the device).	_____

Note Exposure limit before soldering after dry-pack package is opened.
 Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

TYPE OF THROUGH HOLE MOUNT DEVICE

μPD424400V : 20-pin plastic ZIP (400 mil)

Please consult with our sales offices for soldering conditions of the μPD424400V.