Very High-Speed Precision Sample-and-Hold Amplifiers

AD681/AD683

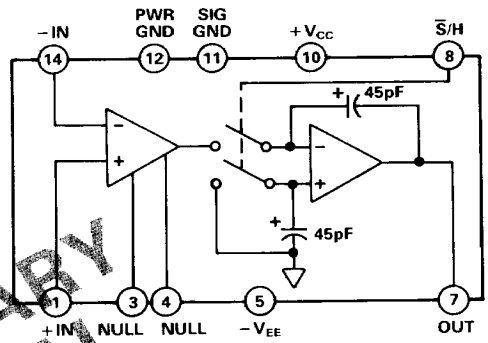
FEATURES

Fast Acquisition Time: 500ns max to 0.01% (AD683)
900ns max to 0.01% (AD681)
Monolithic with On-Board Hold Capacitor
Low Droop Rate: 0.01μV/μs
Low Output Noise: 35μV rms (dc to 10MHz)
Industrial and Military Temperature Ranges
Operation with ±12V or ±15V Supplies

APPLICATIONS

Data Acquisition Systems
Data Distribution Systems
Analog Delay and Storage
Peak Amplitude Measurements
Deglitching D/As

AD681/AD683 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD681 and AD683 are monolithic sample-and-hold amplifiers that set new standards in terms of speed and accuracy. They are manufactured on a complementary bipolar process which provides a medium for wideband circuitry with extremely low noise characteristics.

The AD683 has an acquisition time of 500ns maximum to 0.01% for a 10V step. The maximum power dissipation of the AD683 is 660mW. The AD681 has an acquisition time of 900ns and a maximum power dissipation of 240mW. All other operating features are equivalent with both having on-board hold capacitors. The AD681 and the AD683 have identical pinouts.

The performance of the AD681/AD683 makes it ideal for 12- and 14- bit data acquisition systems. The droop rate of the AD681/AD683 is typically 0.01μV/μs. An aperture jitter of only 20ps allows full-scale frequencies up to to 1.9MHz to be sampled.

The AD681/AD683 can be configured with a user-defined feedback network to provide any desired gain in the sample mode. The output impedance is sufficiently low in the hold mode to maintain output accuracy under the dynamic loading conditions of a successive approximation A/D converter. The sample/hold control signal is compatible with TTL and CMOS.

The devices are available in "A" and "S" grades. The "A" is specified for the −40°C to +85°C industrial temperature range, and the "S" is specified for the extended −55°C to +125°C temperature range. The "S" grade is available with 883B processing. All versions are available in a 14-pin cerdip package.

PRODUCT HIGHLIGHTS

1. The low droop rate (0.01μV/μs) allows long hold times without sacrificing accuracy.
2. The output noise is extremely low with a typical value of 35μV rms (to 10MHz) in the sample mode and 100μV rms (to 36MHz) in the hold mode.
3. The AD681/AD683 is recommended for use with 10-, 12- and 14-bit successive approximation A/D converters. It is the first choice for high-speed converters like the AD674 and the AD7572.
4. The AD681/AD683 can source 35mA and has output short circuit protection.

SPECIFICATIONS (typical @ 25°C and V_S = ±12V andr ±15V unless otherwise specified)

PARAMETER	AD681A	AD681S	AD683A	AD683S	Units
SAMPLE/HOLD CHARACTERISTICS					
Acquisition Time (T_{min} to T_{max})					
10V Step to 0.01%	900	900	500	500	ns max
20V Step to 0.01%	1000	1000	600	600	ns max
10V step to 0.003%	1000	1000	600	600	ns max
Aperture Delay	2.5	*	*	*	ns
Aperture Jitter	20	*	*	*	ps
Droop Rate	0.01	*	*	*	μV/μs
Hold Step Error	0.5	*	*	*	mV
Hold Mode Settling Time (to 0.01%)	80	*	*	*	ns
Feedthrough (fin = 100kHz)	−100	*	*	*	dB
TRANSFER CHARACTERISTICS					
Open Loop Gain	140	*	*	*	dB
Unity Gain Crossover	10	*	*	*	MHz
Full Power Bandwidth	1.6	*	*	*	MHz
Common-Mode Rejection (V_{CM} = ±10V)[1]	100	*	*	*	dB
Slew Rate	130	*	*	*	V/μs
Overshoot	10	*	*	*	%
Rise Time	20	*	*	*	ns
OUTPUT CHARACTERISTICS					
Output Current	±35	*	*		mA max
Output Resistance					
Hold	10	*	*	*	Ω
Sample	10	*	*	*	Ω
Output Noise					
Sample (dc to 10MHz)	35	*	*	*	μV rms
Hold (dc to 36MHz)	10	*	*	*	μV rms
ANALOG CHARACTERISTICS					
Offset Voltage	1		*	*	mV
Offset Voltage Temp Coefficient	1		*	*	μV/°C
Bias Current	700	*	*	*	nA
Offset Current	35	*	*	*	nA
Input Capacitance	3	*	*	*	pF
Input Resistance	10	*	*	*	MΩ
Input Voltage Differential	±20	*	*	*	V max
DIGITAL INPUT CHARACTERISTICS					
(T_{min} to T_{max})					
Input Voltage High, V_{IH}	2.0	*	*	*	V min
Input Voltage Low, V_{IL}	0.8	*	*	*	V max
Input Current (V_{IN} = 0V)	25	*	*	*	μA max
Input Current (V_{IN} = 5V)	1	*	*	*	μA max
POWER SUPPLY CHARACTERISTICS					
Positive Supply Current (T_{min} to T_{max})	9	10	24	27	mA max
Negative Supply Current (T_{min} to T_{max})	9	10	24	27	mA max
Power Supply Rejection					
V_{CC} = +12V (±10%) or +15V (±10%)	100	*	*	*	dB
V_{EE} = −12V (±10%) or −15V (±10%)	100	*	*	*	dB
Power Consumption (±V_S = ±15V)	270	300	720	810	mW max
PACKAGE OPTION[2]					
Cerdip (Q-14)	AD681AQ	AD681SQ	AD683AQ	AD683SQ	

NOTES
*Same as AD681A
[1]Maximum input step is the minimum supply voltage being used minus a headroom voltage of 3V
[2]See Section 13 for package outline information.

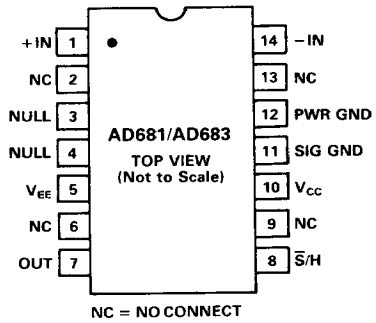


Figure 1. Pinout

ABSOLUTE MAXIMUM RATINGS[1]

Supplies (V_{CC},V_{EE})	±18V
Analog Inputs	±V_S
Logic Input	±V_S
Analog Common to Digital Common	±1V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering)	+300°C
Output Short Circuit to Ground	Indefinite
Power Dissipation	960mW

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditons above those indicated in the operational section of this specification is not implied.

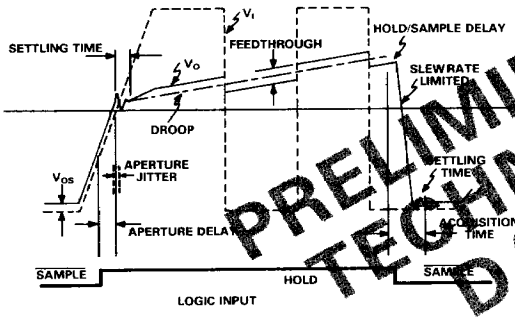


Figure 2. Sample/Hold Characteristics

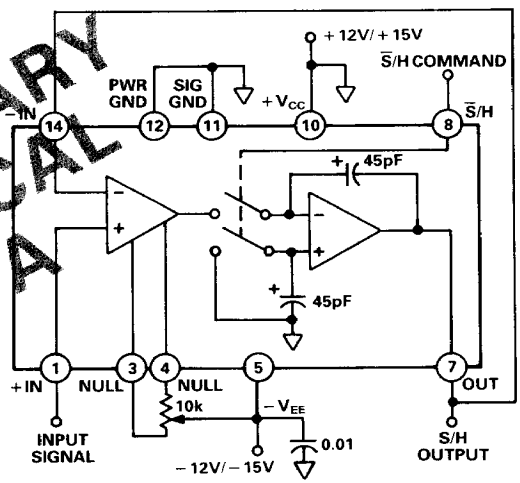


Figure 3. Connection Diagram, Gain = 1

DEFINITIONS OF SPECIFICATIONS
(see Figure 2)

SAMPLE-TO-HOLD-TRANSITION

Aperture Delay:
Aperture delay is the time required for the sample-and-hold amplifier to switch from sample to hold. The effect of aperture delay can be eliminated as an error source by advancing the hold command with respect to the input signal.

Aperture Jitter:
Aperture jitter is the variation in aperture delay for successive samples. The error which results from this variation is directly related to the dV/dT of the analog input.

In a system where a time-varying signal is being digitized, the maximum signal frequency can be calculated from the jitter and the resolution of the N-bit converter being used. The formula is:

$$F_{max} = \frac{2^{-(N+1)}}{\pi(\text{aperture jitter})}$$

Using this formula, we can derive the maximum input frequency of the AD681/AD683 in an application using a 12-bit A/D converter with a 10V full scale and a maximum error of 1/2LSB:

$$F_{max} = \frac{2^{-(12+1)}}{\pi\ (20\ \text{ps})} = 1.94\text{MHz}$$

Hold Step Error:
Hold step error is an output shift or step caused by charge injection into the hold capacitor as the device is switched from sample to hold. This error is also referred to as "sample-to-hold offset" or "pedestal."

HOLD MODE

Droop Rate:
Droop rate is the constant drift of the output per unit of time. It is the direct result of leakage from the hold capacitor. The main contributors to the droop rate are switch leakage and the bias current of the integrating amplifier.

Feedthrough:
Feedthrough is an attenuated version of the input signal which appears at the output. This error is created mainly by capacitive coupling of the switch and is particularly important when the sample and hold follows an analog multiplexer that switches among many different channels.

HOLD-TO-SAMPLE TRANSITION

Acquisition Time:
Acquisition time is the length of time which the sample-and-hold must remain in sample mode in order for the hold capacitor to acquire a full-scale input to a given accuracy. It is made up of the delay time of the switch in addition to the small signal settling time of the input amplifier.

GROUNDING

Data acquisition components often have two or more ground pins (analog/digital) which are not connected together within the device. The grounds must be tied together at a single point to eliminate voltage drops between the individual component grounds and the system grounding point.

The connection in Figure 3 shows the AD681/AD683 connected in a gain of +1. Separate ground lines should be connected to the power and signal grounds (analog and digital), to eliminate the problem of voltage drops along these points. Each ground should be terminated at the system grounding point.