MV1812

TELETEXT DATA ACQUISITION

The MV1812 is a high speed CMOS circuit capable of decoding any World System 625 line teletext transmissions.

The circuit operates on serial teletext data provided by the Plessey SL9100 Data Slicer and provides parallel words of data if the transmitted data matches the selection criteria set in the internal registers.

The circuit will be of particular use in teletext systems where the transmitted data is not intended for immediate display, where its high data throughput rate will allow large volumes of data to be received at the highest transmission rates possible. The design of the MV1812 will allow data in paged format or other formats to be equally well received.

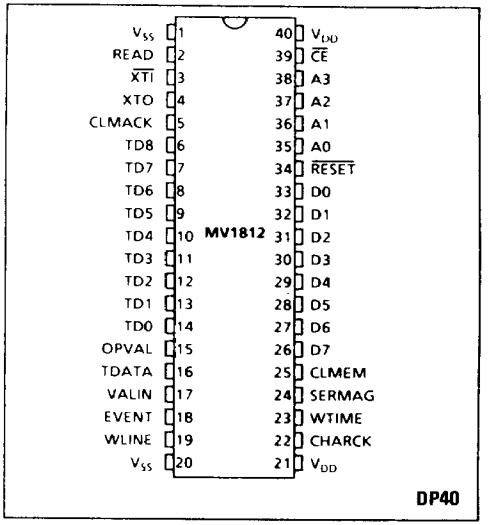

Fig 1 Pin Connections (top view)

FEATURES

- Interfaces with standard 8-bit data bus
- Nine internal registers giving complete acquisition control
- Data checking ensures minimal reception of errors
- Data purity counter for optimal electronic tuning
- Programmable Framing Code
- All teletext packets received
- 16,777,216 unique teletext pages may be specified

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.3V to 7V
Input voltage (all pins)	-0.3V to V_{DD} + 0.3V
Operating temperature range	0°C to + 70°C
Storage temperature range	-40°C to + 125°C
Relative Humidity	85%

APPLICATIONS

- Datacast and other 'Subscription User Group' service receivers
- Teletext/Telesoftware receivers for personal computers
- World System Level 1 to 5 teletext receivers
- Aerial and TV tuning equipment
- Advanced multi-media teletext service transceivers
- Hand held low power teletext receivers
- Video programming of VCRs (VPX)
- Specialist teletext receivers for cable TV systems

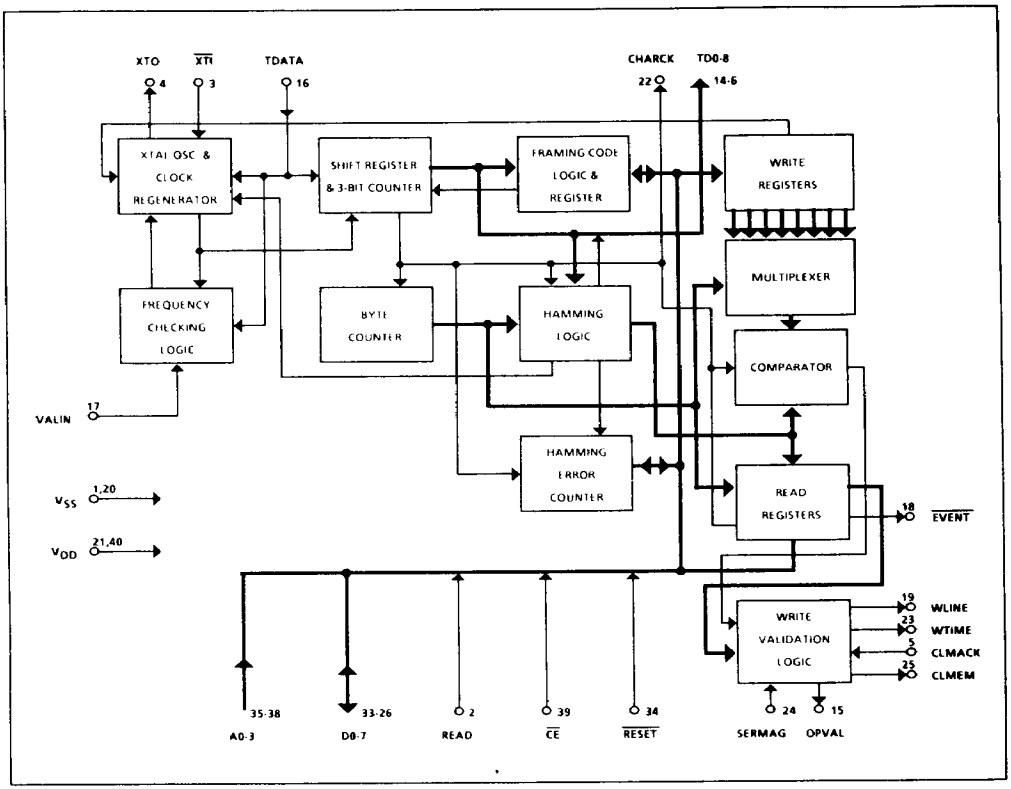

Fig 2 MV1812 Block Diagram

DEVICE DESCRIPTION

The MV1812 is a single chip teletext data acquisition circuit capable of receiving all current and proposed future teletext services. A block diagram of the device is shown in fig.2.

The device is controlled via a standard 8-bit data bus allowing a simple interface to most microprocessors. Complete control of the acquisition of data is provided via nine internal registers. A data purity counter is included to show the error rate of incoming data, which allows systems with electronic tuning to tune for optimum teletext reception and also has potential for aerial tuning. Page selection is achieved by specifying the magazine number, page number and page sub-code of the desired teletext page. The digits of each of these page selection codes may individually be specified as "don't care" or, alternatively, data acquisition may be disabled completely. The framing code is also programmable such that any 8-bit code may be specified for byte synchronisation at the start of each line. The default framing code for World System teletext transmissions is 27_{16}.

The MV1812 receives a teletext data stream from a data slicer such as the SL9100. An on chip oscillator provides a clock against which the frequency of the incoming data is compared. A data clock is recovered and used to shift the teletext data into an 8-bit shift register. The data is checked for the framing code which is used to byte synchronise the data and to initialise a character clock. A byte counter counts the character clock for subsequent enabling of data latches in the read registers. After any Hamming Code checking and correction, the data is latched into the appropriate registers and compared with the internal programmable registers, as set up by the controlling microprocessor, to check for the desired magazine page. Parallel 8-bit page data is output from the device together with a parity check bit for enabling or disabling writing of the data to memory.

PIN DESCRIPTIONS

V_{DD} & V_{SS} (pins 21 & 40, and 1 & 20 respectively).
The 5 volt ±0.5v supply is applied on any convenient pair of these pins. However, if large bus loads are to be driven from either of the data output buses, it is recommended that all four supply pins are used.

TDATA (Teletext Data, pin 16).
Sliced teletext data from the SL9100 circuit is input to the chip on this pin. (see fig. 3)

XTI & XTO (XTAL in & XTAL out, pins 3 & 4).
This pair of pins is designed to drive a 27.75000 MHz fundamental or third overtone quartz crystal. If a third overtone type is used, two external components are required to ensure operation at the correct frequency. Typical external components are, a 33nF capacitor and a 1µH inductor in series and in parallel with the crystal (see fig.4). A nominal 1 MΩ resistor is included on chip between XTI and XTO to bias the input to its correct operating region. The crystal should be within ± 100 p.p.m. of the nominal frequency over the operating temperature range.

VALIN (Valid Line, pin 17).
This input must be high during any TV line that may contain teletext data. It must return low (for at least the minimum period) prior to the next TV line in order to reset the acquisition circuits ready for the next clock run-in. The Sync Output from the SL9100 may be used, though for maximum data security, it should be gated off during the picture transmission lines if full field teletext transmissions are not being received.

RESET (pin 34).
The active low reset input. This input has a nominal 150KΩ resistor coupled to V_{DD}, and a Schmitt input buffer, allowing a simple external circuit consisting of a 1µF capacitor to ground, to perform a power-on reset pulse of sufficient duration to allow the crystal oscillator to stabilize. When held low, this input resets all registers to default settings, and initialises counters.

CE (Chip Enable, pin 39).
The active low chip enable input. When low, this input enables a read or write operation of the registers via the D0-D7 tri-state I/O's and A0-A3 address inputs.

READ (pin 2).
When READ is high with CE low, this input forces the D0-D7 pins to an active state, outputting the contents of the register addressed by the An inputs. If READ is low when CE is low, the addressed register is written with the data input on the Dn pins.

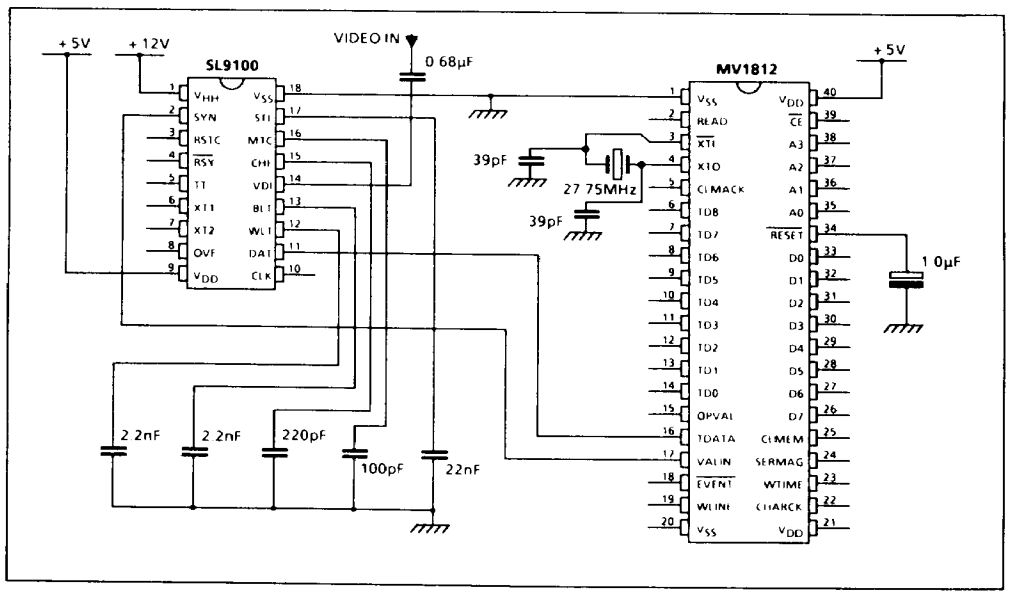

Fig 3 Interface to SL9100

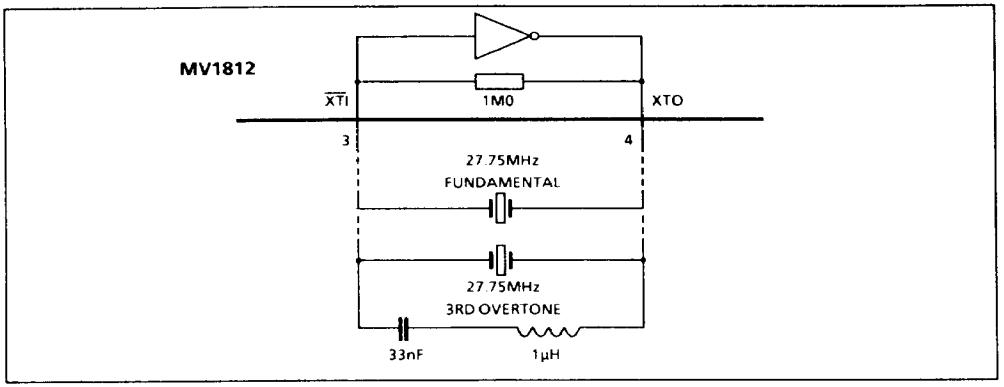

Fig 4 Crystal Oscillator Options

A0 - A3 (Address Inputs, pins 35 - 38).
The register address inputs. There are nine 8-bit registers to control the circuit as shown in Table 1. All other register addresses are absent. If written to, no action is taken, if read, FF_{16} is output. Details of the register contents and actions are described later.

TD8 - TD0 (Teletext Data Outputs, pins 6 - 14).
These nine outputs transmit the checked teletext data. Bits 7 to 0 are the data, bit 8 is a "write enable" bit for the word. It is controlled by the setting of the 'PAR' (Parity check inhibit) bit in the RECON register as shown below.

PAR	TD8
0	1 = PARITY CHECK CORRECT 0 = PARITY CHECK FAILED
1	ALWAYS 1

CHARCK (Character Clock, pin 22).
This output signal is used to 'clock' the TDn outputs. The TDn outputs are stable when this output is high.

D7 - D0 (Data Inputs/Outputs, pins 26 - 33).
The register data inputs/outputs. These pins are high impedance inputs at all times except when CE is low and READ is high, when they become outputs.

EVENT. (pin 18).
An active low open drain output intended for interrupting a microprocessor when an important event has occurred. The 'EVENT' register bits uniquely describe which type of event has occurred.

WLINE (Write this Line, pin 19).
This output is set near the beginning of every line to indicate to the external system whether the data appearing on TD0-TD8 is to be used or not. The time at which it is set in any particular line may vary depending on the packet number being received, but it is unconditionally stable when the OPVAL output goes high on each line.

WTIME (Write Time only, pin 23).
This output will only be set high during a line if the packet being received is a header (pkt. #0) and:-
i) the magazine number compares with that set in register bits MG2,1 & 0, or,
ii) the SERMAG input is high.
The data contained on such lines can be used for updating a real time clock display. As with WLINE, this output is not valid until OPVAL goes high.

ADDRESS				HEX	REGISTER NAME	REGISTER CONTENTS							
A3	A2	A1	A0			D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	EVENT	NPR	C10	C8	C4	VHR	NDP2	NDP1	NDP0
0	0	0	1	1	CBITS	C14	C13	C12	C11	C9	C7	C6	C5
0	1	0	0	4	SELCON	ACQ	MC	PBC	PAC	SDC	SCC	SBC	SAC
0	1	0	1	5	PGREQ1	SC3	SC2	SC1	SC0	SA3	SA2	SA1	SA0
0	1	1	0	6	PGREQ2	MG2	MG1	MG0	SD1	SD0	SB2	SB1	SB0
0	1	1	1	7	PGREQ3	PB3	PB2	PB1	PB0	PA3	PA2	PA1	PA0
1	0	0	0	8	RECON	CA	WI0	WI24	WI25	PAR	MV	MPX	RLH
1	0	1	1	B	HAMMC	H7	H6	H5	H4	H3	H2	H1	H0
1	1	1	1	F	FCODE	F7	F6	F5	F4	F3	F2	F1	F0

Table 1 Register Contents

SERMAG (Serial Magazine Reception, pin 24).

An input that controls the writing of header packets in conjunction with the above two outputs. The C11 control bit, as read from the CBITS register, defines whether or not serial magazine transmission is being used. The table below shows which headers are flagged by the WTIME and WLINE outputs for all combinations of the SERMAG input and the RLH (roll headers) bit in the RECON register. Note that the RLH bit enables WTIME and WLINE to only flag headers in which the C9 bit is not set.

INPUTS		OUTPUTS	
SERMAG	RLH.$\overline{C9}$	WTIME	WLINE
0	0	MH	PH
0	1	MH	MH
1	0	AH	PH
1	1	AH	AH

KEY:

PH - Headers for the requested page only
MH - Headers for requested magazine only
AH - All headers

OPVAL (Output Valid, pin 15).

WLINE & WTIME outputs are always valid when this output goes high. At the start of every line this output is reset low by the VALIN input and will go high as the fifteenth byte of data is being received by the circuit, unless a byte with an uncorrectable Hamming error is received, in which case it will stay low to the end of the line.

CLMEM (Clear Memory, pin 25).

Clear memory output. This output goes high if the first header received for a requested page has the C4 bit set. Subsequent headers for the same page do not affect this output.

CLMACK (Clear Memory Acknowledge, pin 5).

Clear memory acknowledge input. To reset the CLMEM output to the normally low state, this input must go high momentarily. A full chip reset will also clear CLMEM.

REGISTER DESCRIPTIONS

EVENT Register (Address 0)

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
NPR	C10	C8	C4	VHR	NDP2	NDP1	NDP0
CONDITION ON RESET							
0	ud	ud	ud	0	0	0	0

ud = undefined

This register is read only, if written to, no action is taken. The register can be read at any time by the controlling microprocessor, but if an interrupt condition has been set, the condition will be cleared by the reading of this register and the EVENT output will return to a high impedance state.

There are eight possible events which set the EVENT output low. They are:-

i) a valid header (pkt. #0) has been received for the requested page,

ii) the complete requested page has been received, or

iii) one of six different non-display packets has been received.

The VHR bit, read via D3, indicates the "Valid Header Received" condition and the NPR bit, read via D7, indicates the "New Page Received" condition. These two bits are cleared by reading this register, as are NDP0-2, but bits C4, C8 & C10 remain as set by the last event to change them.

The three NDP bits in D2, D1 & D0, indicate which of the six "Non-Display Packets" has most recently been received. These bits are the three least significant bits of the packet number (or row address) as received in bytes four and five. They uniquely describe the packet number as in the table below:-

Received Packet No.	NDP Bits		
	2	1	0
26	0	1	0
27	0	1	1
28	1	0	0
29	1	0	1
30	1	1	0
31	1	1	1

The other three bits in positions D4, D5 & D6 are the control bits C4, C8 & C10 respectively from the most recently received header (pkt. #0). Their respective functions are Erase Page, Update Page and Inhibit Display. These three bits cannot set the EVENT output.

Header packets passing through the MV1812 for the purpose of updating displays etc.(eg WTIME), have no effect on the bits in this register.

CBITS (Control Bits) Register (Address 1)

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
C14	C13	C12	C11	C9	C7	C6	C5
CONDITION ON RESET							
ud	ud	ud	ud	ud	ud	ud	ud

ud = undefined

This register is also read only. Its contents are as shown in the table above. They are the remaining control bits from the most recently received header (pkt. #0) which matched the acquisition requirements in the PGREQ registers.

The bit functions are:-
C5 - Newsflash
C6 - Subtitle
C7 - Suppress header
C9 - Out of sequence page
C11 - Serial magazines
C12, C13 & C14 - Language control bits

SELCON (Select Acquisition Control) Register (Address 4)

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
ACQ	MC	PBC	PAC	SDC	SCC	SBC	SAC
CONDITION ON RESET							
1	1	1	1	0	0	0	0

The SELCON register has full read and write capability. Its control bits govern which digits of the incoming headers (pkts. #0) are compared with the register contents for page acceptance. The read data is normally identical to that most recently written to this register (see note under PGREQ registers). The individual bits have the following functions:-

ACQ -Acquisition on. When set high, Teletext acquisition is enabled. When low, acquisition is disabled. It is recommended that acquisition is disabled when changing channel, to minimise the possibility of data errors and to reset the internal "Page Being Received" flag to avoid a lock-up situation, where a page has started being received, then no suitable terminating header is received, due to a channel change.

MC -Magazine Compare. When set, this bit allows comparison of the received magazine bits with the register bits. Not set implies don't care.

PBC, PAC -Page Number Digits Compare. When set, these bits allow comparison of the respective received page number bits with the register bits (PA = least significant digit).

SDC, SCC, SBC, SAC -Page Sub-code Digits Compare. When set, these bits allow comparison of the respective received sub-code bits with the register bits (SA = least significant digit).

PGREQ1, 2 & 3 (Page Request) Registers (Addresses 5, 6 & 7) (see Table 2)

These registers define the magazine, page number and sub-code (formerly time-code) which the MV1812 compares with the incoming headers (pkts. #0) to establish if the following page related packets (pkt. nos. 1-28) are to be received or not. The default setting after reset is magazine 1, page 00, sub-code 0000, though the sub-code digits are ignored by the default state of the SELCON register.

The bit functions are:
MGn -Magazine select bits
PBn, PAn -Page no. select bits
SDn, SCn, SBn, SAn -Sub-code select bits

The read sections of these registers are completely separate to the write sections. Initially they are undefined, but after reception of the first valid header, they contain the magazine no., page no. and sub-code of the page being received, irrespective of any "don't care" settings in the SELCON register. This feature allows the microprocessor to read the page number as soon as the "Valid Header Received" interrupt has occurred, so that it may decide in advance of receiving the data, where the data is to be stored. This is particularly useful in the case of rolling pages (multi-page sequences with the same page no.), as each received page can (if sub-coded) be stored in separate areas of memory and updated as required.

NOTE: The PGREQ registers are double buffered by the internal "Page Being Received" signal. This prevents data from different pages being accepted erroneously as the original page. If a new page number is written to the PGREQ registers during reception of a page, the new data is held internally until the current page has been completed (defined by the reception of another header which does not compare with the current SELCON/PGREQ settings). The new page number is then transferred to the comparison registers.

The SELCON register is also double buffered, but by the VALIN signal, such that any data written to the SELCON register while VALIN is high, is not transferred to the active part of the register until VALIN returns low. If the SELCON register is set such that all digits except the magazine number are "don't care", all headers for the specified magazine will compare and the "Page Being Received" signal may be permanently on. In this case, writing a new value to PGREQ2 to select a different magazine will not take effect unless the ACQ bit in SELCON is set low temporarily, to reset the "Page Being Received" signal.

ADDR	REGISTER NAME	REGISTER CONTENTS							
		D7	D6	D5	D4	D3	D2	D1	D0
5	PGREQ1	SC3	SC2	SC1	SC0	SA3	SA2	SA1	SA0
6	PGREQ2	MG2	MG1	MG0	SD1	SD0	SB2	SB1	SB0
7	PGREQ3	PB3	PB2	PB1	PB0	PA3	PA2	PA1	PA0
		CONDITION ON RESET							
5	PGREQ1	0	0	0	0	0	0	0	0
6	PGREQ2	0	0	1	0	0	0	0	0
7	PGREQ3	0	0	0	0	0	0	0	0

Table 2 Page Request Register Contents

RECON (Receive Control) Register (Address 8)

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
CA	WI0	WI24	WI25	PAR	MV	MPX	RLH
CONDITION ON RESET							
0	0	0	0	0	0	0	0

This register controls various aspects of the reception of teletext information within the MV1812. With the exception of the MPX bit (read via D1), the written and read information are identical. The bit functions are:-

CA -This bit is for future requirements.

WI0 -Write Inhibit packet #0. Setting this bit inhibits the appearance of WLINE and WTIME if they would otherwise have been set high by a received header (packet #0). It does not inhibit writing of any internal registers by such headers or reception of data related to any such headers.

WI24 & WI25 -Write Inhibit of packets #24 and #25. These bits inhibit the setting of WLINE during reception of either packets #24 or #25 during reception of page related data

PAR -Parity check disable when set. See also the description of TD8 (pin 6) output.

MV -Majority Voting enable bit. When set high, this bit enables any seven of the eight bits of the framing code word to be matched for word synchronization, otherwise all eight have to match exactly. Synchronization will always be correct with seven bit matching of the default framing code (27_{16}), since during the clock run in, the best match will be of five bits. Majority voting therefore allows synchronization in the presence of errors that might otherwise cause the line to be rejected.

MPX -Non-multiplexed data bit. This bit has no effect when written to. When read, this is the first message bit (L.S.B.) of byte six of the most recently received packet 8/30, or Broadcast Service Data packet. This indicates whether the teletext transmissions are full field (MPX = 1) or field-blanking interval only (MPX = 0).

RLH -Roll Headers bit. When set, this bit allows all sequentially numbered headers to be written to store in conjunction with the WLINE output. Normally, only headers (packets #0) pertaining to the requested page would be signalled by WLINE, but when RLH is high and SERMAG (pin 24) is low, all headers of the selected magazine (MG2,1 & 0) are signalled. When SERMAG is also high, all magazines headers are signalled. Any header though, with the C9 (out of sequence) bit set, will not be signalled with WLINE. The register contents will not be affected by such headers, and interrupts will not be generated by them.

HAMMC (Hamming Error Counter) Register (Address B_{16})

This register shows the number of errors in the Hamming encoded words checked by the MV1812. Any recognisable Hamming error*, correctable or not, causes the count to be incremented by one. The counter overflows at 255 (FF_{16}) and restarts. The Hamming encoded words checked (and internally corrected) by the MV1812 are:-

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
H7	H6	H5	H4	H3	H2	H1	H0
CONDITION ON RESET							
0	0	0	0	0	0	0	0

Packet no.	Byte nos. checked
0	4 - 13 inc.
1 - 25	4 & 5
26 - 31	4,5 & 6

The counter is reset to zero by a hardware reset (pin 34) or by writing zero to it. Writing any other number has no effect.

This counter is primarily intended to allow an electronic system to tune for optimum teletext reception. It should be noted that intervals between broadcasts of particular teletext page numbers may be erratic, giving erratic short term count rates for a given average level of errors. This can be overcome either by enabling reception of all pages by setting all SELCON register bits (except ACQ) low to receive all pages, or to disable page based data reception, as described in the SELCON register description. The former technique is probably preferable as it will give a far higher count rate for any given level of errors, allowing more rapid tuning. The latter would only give the error rates of packets such as 8/30 which may not be broadcast by all authorities.

* 3,5,7 & 8 bit errors in Hamming encoded words are not recognisable.

FCODE (Framing Code) Register (Address F_{16})

REGISTER CONTENTS							
D7	D6	D5	D4	D3	D2	D1	D0
F7	F6	F5	F4	F3	F2	F1	F0
CONDITION ON RESET							
0	0	1	0	0	1	1	1

This register establishes the byte used for comparison with the incoming data for the purpose of establishing byte synchronization. For normal World System Teletext this will be 27_{16}, so this is the default. However any other byte may be used. The read data is identical to that written.

APPLICATION NOTES

The following notes assume that the MV1812 is to operate in a system which conforms to the principles of teletext transmissions as described in the "World System Teletext Specification".

DATA INPUT

Prior to any data being presented to the MV1812, the RESET and VALIN inputs must be held low for at least the minimum period, and preferably for about 250ms from power up, if a crystal is used as the clock source, to avoid erroneous clocking as the crystal starts oscillating.

After VALIN is released (goes high), the clock regeneration section (see fig 2) searches for the first negative going edge of the incoming data stream on TDATA and synchronises to this. The frequency of the clock run-in is compared with the bit clock derived from the 27.75MHz clock. If the clock run-in is not within + 16/-10% of the correct frequency, the acquisition circuits are locked to prevent any further action until VALIN returns low.

If the frequency check is good, the fifth negative going edge of the clock run-in is used to resynchronise the bit clock, which is then used to clock the incoming data into the main shift register. The contents of this shift register are compared after each shift with the programmed framing code. If an exact match of all eight bits occurs (or seven bits, see RECON register description), a three bit (divide-by-eight) counter is started, to generate a byte synchronised clock. If no match is found in the first 24 received bits, the acquisition circuits are locked until VALIN returns low.

As the subsequent bytes (nos. 4, 5, etc.) are received, they are latched and presented on outputs TD0 to TD7 (with parity check output on TD8) with the byte synchronised clock, CHARCK. On all received teletext lines, bytes four and five are checked for correct Hamming protection. If possible and necessary, the four message bits are corrected internally, prior to being latched into the appropriate registers. Bytes four and five contain the magazine number (3 bits) and the packet number (5 bits). If the packet number is in the range 26-31, byte six is also checked for good Hamming protection. If the packet number is zero, a page header, bytes six to thirteen are checked by the Hamming circuits. If any of the Hamming checked bytes fails and cannot be corrected, the acquisition circuits are locked until VALIN returns low. The data output on pins TD0 to TD7 is as received, without any Hamming correction, therefore the user must also do the Hamming correction on these and any subsequent bytes so protected, prior to using the data.

DATA OUTPUT

In the event of an uncorrectable Hamming failure, it is likely that some data may already have been latched into external circuits by CHARCK. To avoid the possibility of this data being used erroneously, it is suggested that the output data is buffered before being transferred to system memory. One method of achieving this is to use the MV1830 as shown in fig.5. The MV1830 is a high speed CMOS teletext data buffer organised as 64 by 9 bit words. The first device stores data from one TV line until OPVAL goes high. If WLINE is high, data is gated into the next data buffer in sequence until VALIN goes low at the end of the line. If WLINE is not high when OPVAL goes high, or if OPVAL does not go high, any data in the first MV1830 will be reset by VALIN at the end of that line. Once the teletext data has been transferred to the second data buffer, the host processor may read the data during the remainder of the current line and part of the subsequent line, bearing in mind that a further 42 bytes of data may be transferred when OPVAL goes high during the

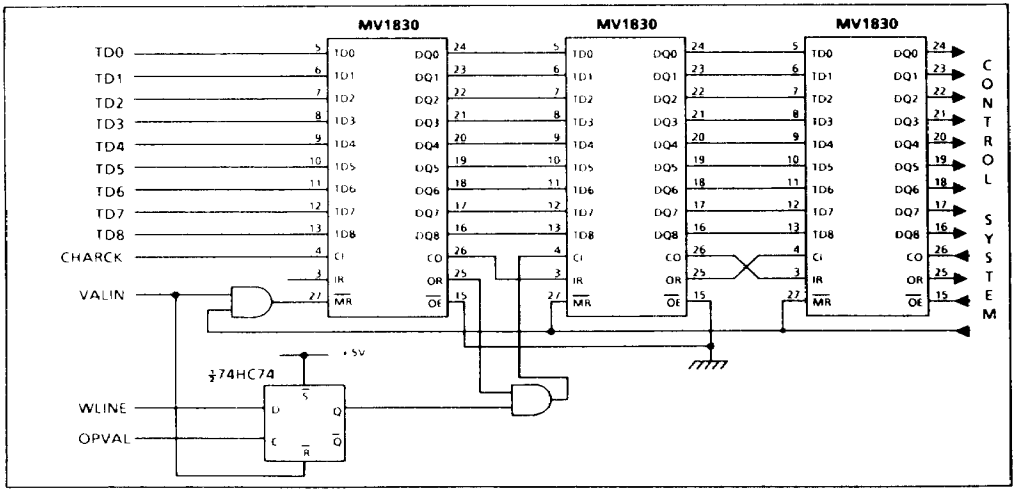

Fig 5 Data Buffering Using MV1830

Channel	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Magazine	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Packet	30	30	30	30	30	30	30	30	31	31	31	31	31	31	31	31
Received?	Y	N	N	N	N	N	N	N	Y	Y	Y	Y	Y	Y	Y	Y

Table 3 Independent Data Service Packets

NOTE:
Received? indicates whether or not reception of packets belonging to a particular channel is indicated by WLINE. Channels marked 'N' are received and passed through the MV1812, but do not set WLINE or generate an EVENT. At the present time, only channels 0, 8, 9, 10 & 11 have defined purposes within the World System Teletext Specification.

next TV line. If a total of four MV1830s are added in cascade after the first device, the data from up to six TV lines may be stored during the vertical blanking interval, allowing a slow system to read the data during the rest of the TV frame period.

An alternative arrangement is to use DMA to transfer the data directly from the MV1830 into system memory. One possible DMA interface is shown in Fig. 6. Teletext data is stored in the MV1830 until the end of the current line. If WLINE and OPVAL are not both high when VALIN goes low, the data buffer is reset. If WLINE and OPVAL are both high, however, a DMA request is generated. The DMA controller should be programmed to transfer 42 bytes of data only, after which the DMA request must be reset before VALIN goes low again after the next TV line.

ACQUISITION CONTROL

Teletext packets related to a particular page are those that follow a given page header (pkt. #0) if they are of the same magazine, and if their packet numbers are in the range 1-28 inclusive. Such packets are signalled by the MV1812 using WLINE, assuming that the selection criteria within registers SELCON and PGREQ1, 2 & 3 have been fulfilled for the page header in question.

Packet numbers 29, 30 & 31 have no relation to any particular page and may be transmitted at any time. The MV1812 will signal with WLINE the reception of X/29, 0/30 and X/31, where 'X' is the magazine number defined in PGREQ2 and SELCON.

Packets X/29 are defined as 'magazine related', containing information relating to all pages within that magazine.

Packets #30 and #31 are referred to as an 'Independent Data Service' facility within the teletext transmission service. Instead of referring to packets and magazines, bytes four and five are re-labelled as:-

Byte 4 -parallel data channel number

Byte 5 -all data bits = 1 indicating Independent Data Service packet

The four bits of byte four thus define one of 16 parallel data channels, which correspond to magazines/packets as shown in Table 3.

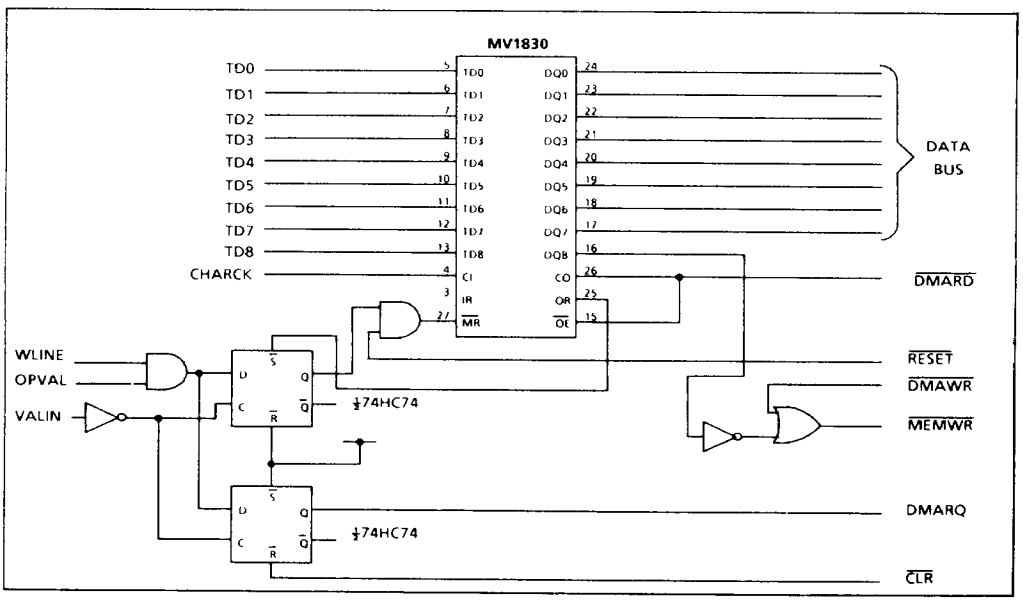

Fig 6 Data Buffering for DMA Interface

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 0°C to 70°C, V_{DD} = + 5V ± 0.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
All Inputs (except XTI)						
Input low current (source)		-10	-33	-100	µA	All inputs have 150KΩ pull-
Input high current (sink)				± 1	µA	up resistor to V_{DD}
XTI input	3					
Input low current (source)				-10	µA	
Input high current (sink)				+ 10	µA	
All Inputs (except RESET, VALIN & TDATA)						
Input low voltage		-0.3		1.5	V	
Input high voltage		3.5		5.3	V	$V_{IH_{MAX}} = V_{DD} + 0.3V$
VALIN & TDATA	17,16					
Input low voltage		-0.3		0.8	V	
Input high voltage		2.0		5.3	V	$V_{IH_{MAX}} = V_{DD} + 0.3V$
RESET input (Schmitt input)	34					
Input low voltage		-0.3		1.0	V	
Input high voltage		2.0		5.3	V	$V_{IH_{MAX}} = V_{DD} + 0.3V$
Threshold voltage (rising)			1.85		V	V_{DD} = 5V
(falling)			1.05		V	V_{DD} = 5V
All outputs (except CHARCK, XTO & EVENT)						
Output low (sink)		13.8	26		mA	V_{OL} = 0.4V
Output high (source)		-21.7	-46		mA	V_{OH} = 2.4V
CHARCK, XTO & EVENT	4,18,22					
Output low (sink)		6.9	13		mA	V_{OL} = 0.4V
CHARCK,& XTO	4,22					
Output high (source)		-10.8	-23		mA	V_{OH} = 2.4V
Supply Current	21,40			10	µA	F_{IN} (XTI) = 0Hz
			10		mA	F_{IN} (XTI) = 27.75MHz
Max Input Frequency, $F_{IN_{MAX}}$	3	27.75			MHz	

DYNAMIC CHARACTERISTICS (see Fig 7)

Test conditions (unless otherwise stated)

T_{amb} = 0°C to 70°C, V_{DD} = +5V ±0.5V

Characteristic	Sym	Value			Units	Conditions
		Min	Typ	Max		
Reset low time	T_{RL}	75			nS	
Address to data valid	T_{ADV}			70	nS	
Read enable to data valid	T_{EDV}			80	nS	Note 1
Read disable to data bus free	T_{DF}			30	nS	Note 1
Data setup before address change or write disable	T_{DAS}			30	nS	Note 2
Data hold after address change or write disable	T_{DAH}			30	nS	Note 2
VALIN low time	T_{VL}	75			nS	
VALIN high to first negative TDATA clock edge	T_{VC}	50			nS	
Clock run in	$T_{CR_{MIN}}$	10			bits	Note 3
	$T_{CR_{MAX}}$			16	bits	Note 3
Data setup before CHARCK	T_{DS}	100			nS	
Data hold after CHARCK	T_{DH}	400			nS	
CHARCK high time	T_{CH}	4	4	4	bits	Note 3
CHARCK low time	T_{CL}	4	4	4	bits	Note 3
Write outputs setup time before OPVAL high	T_{WS}	1.08			µS	Outputs WLINE & WTIME
OPVAL low after VALIN low	T_{OPL}			80	nS	
OPVAL high after first CHARCK positive edge	T_{OPH}	87	87	87	bits	Note 3
EVENT low after VALIN low	T_{EN}			40	nS	Note 4
EVENT low after first CHARCK positive edge	T_{EP}	80	80	80	bits	Note 5

Note 1 -Read enable/disable is from the leading/trailing edge of the logical AND of READ high and CE low
Note 2 -Write enable/disable is from the leading/trailing edge of the logical AND of READ low and CE low
Note 3 -One bit period = 4 x XTI period
Note 4 -All events other than NPR or VHR
Note 5 -Events due to NPR or VHR bits being set

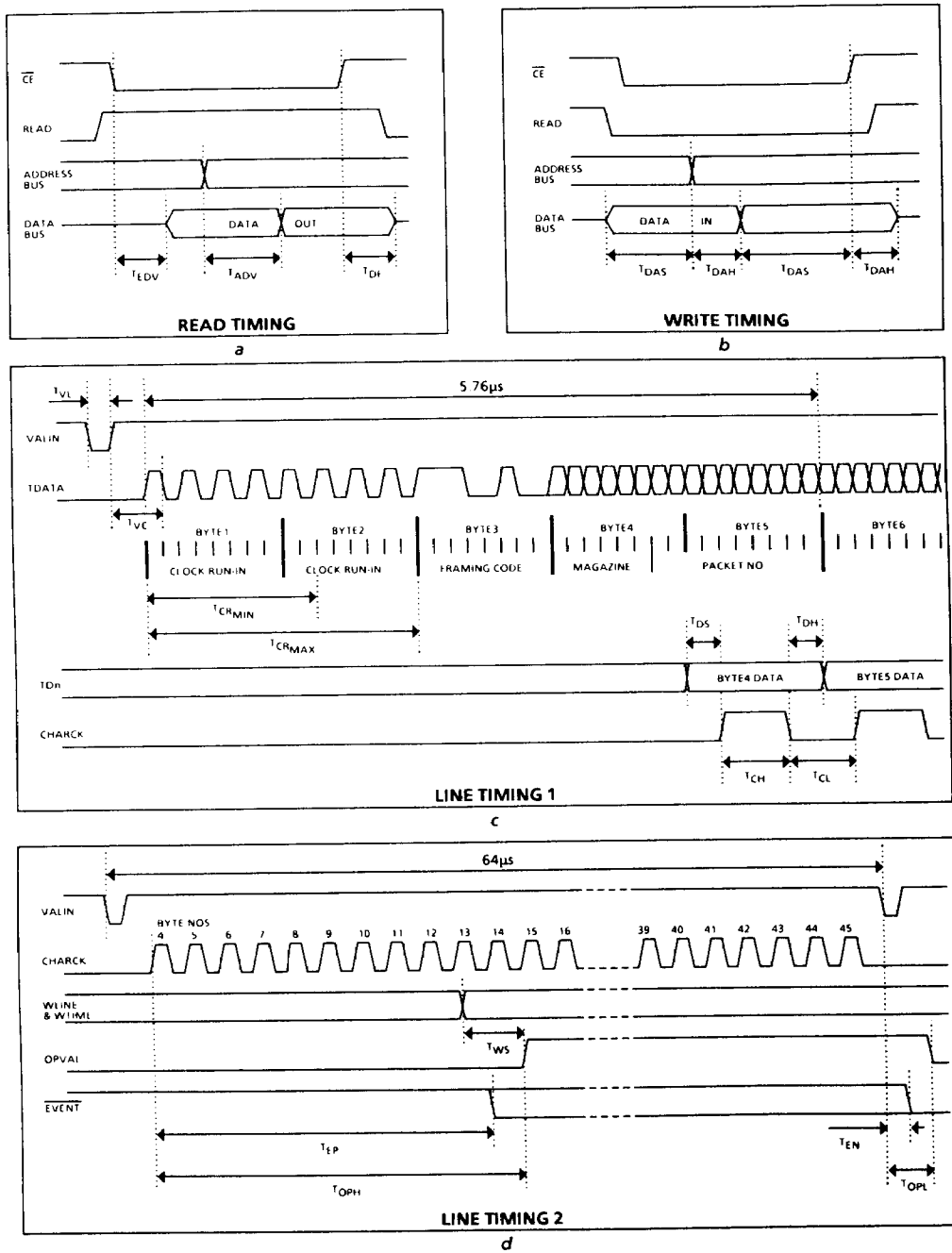

Fig 7 MV1812 Timing Diagrams