MV1830

TELETEXT DATA BUFFER

The MV1830 is a 64 x 9 sequential data buffer designed to be used with the MV1812 Teletext Data Acquisition Circuit. The MV1830 can be used singly, or can be cascaded so that the data from multiple VBI lines may be stored, allowing time for a slow system to read the data during the rest of the frame period.

FEATURES

- 10MHz Guaranteed Cascade Rate
- <150mW Power Dissipation at 10MHz
- <55mW Standby
- Single +5V Supply
- Tri-state Outputs

ASSOCIATED PRODUCTS

MV1812 Teletext Data Acquisition circuit
SL9100 Teletext Data Slicer and Clock

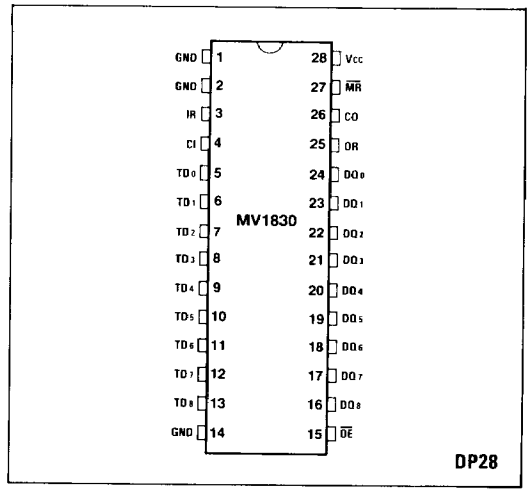

Fig.1 Pin connections - top view

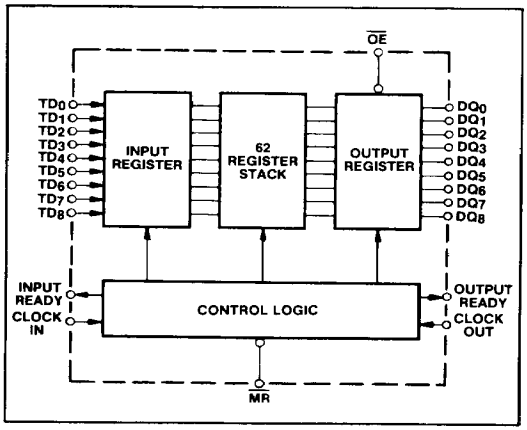

Fig.2 Block diagram

BUFFER OPERATION

The MV1830 data buffer contains 64 nine-bit data registers. Data is initially loaded from the data inputs TD0-TD8 by applying a low to high transition on the Clock In (CI) input. Input Ready (IR) goes low indicating that data has been entered into the first register and the input is unable to accept more data. When CI goes low again, the fall through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second and IR goes high indicating that the buffer is ready to accept new data.

Data falling through the registers stacks up at the output end. A high level on OR indicates that there is valid data waiting on DQ0-8. A Clock Out (CO) can then be used to shift data out of the buffer. The low to high transition on CO causes Output Ready (OR) to go low indicating that the data on the outputs may no longer be valid. When CO goes low, the data in the next to last register moves into the last register and OR goes high again.

The depth of the buffer can be extended by connecting the data outputs of one device to the inputs of the next, as shown in Fig.10. The Input Ready pin of the receiving device is connected to the Clock Out pin of the sending device. Similarly the Output Ready pin of the sending device is connected to the Clock In pin of the receiving device.

Master Reset ($\overline{MR}$) is used to reset the control logic and remove the data from the outputs (i.e. resets to all zeros).

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V

DC Characteristics

Characteristic	Symbol	Value		Unit	Conditions
		Min.	Max.		
Output high level	V_{OH}	2.4		V	V_{IN} = V_{IH} or V_{IL}, I_{OH} = -1mA
Output low level	V_{OL}		0.5	V	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8mA
Input high level	V_{IH}	2		V	
Input low level	V_{IL}		0.8	V	
Input leakage	I_{IN}	-10	+10	μA	V_{IN} = V_{IH} or V_{IL}
Output leakage GND ≤ V_{OUT} ≤ V_{CC}	I_{OZ}	-50	+50	μA	V_{CC} = +5.5V
Short circuit current	I_{OS}		80	mA	Note 8
Supply current	I_{CC}		30	mA	V_{CC} = +5.5V T_{amb} = 70°C I_{LOAD} = 0mA
Standby current			10	mA	V_{CC} = +5.5V I_{LOAD} = 0mA All inputs at V_{IL}

AC Characteristics - Using test circuit

Characteristic	Symbol	Value		Unit	Conditions
		Min.	Max.		
Maximum operating frequency	f_O	10		MHz	Note 1
CI HIGH time	t_{PHCI}	30		ns	
CI LOW time	t_{PLCI}	40		ns	
Data setup to CI	t_{SCI}	0		ns	Note 2
Data hold from CI	$t_{HCI\ (a)}$	50		ns	Note 2 and 3
	$t_{HCI\ (b)}$	t_{PHCI} - 5		ns	
Delay, CI HIGH to IR LOW	t_{DLIR}		30	ns	
Delay, CI LOW to IR HIGH	t_{DHIR}		40	ns	
CO HIGH time	t_{PHCO}	30		ns	
CO LOW time	t_{PLCO}	40		ns	
Delay, CO HIGH to OR LOW	t_{DLOR}		30	ns	
Delay, CO LOW to OR HIGH	t_{DHOR}		40	ns	
Data setup to OR HIGH	t_{SOR}	-20		ns	
Data hold from CO LOW	t_{HCO}	10		ns	
IR pulse HIGH	t_{PIR}	9		ns	
OR pulse HIGH	t_{POR}	10		ns	
Data setup to IR	t_{SIR}	0		ns	Note 5
Data hold from IR	t_{HIR}	50		ns	Note 5
Bubble through time	t_{BT}		2400	ns	
$\overline{MR}$ pulse width	t_{PMR}	60		ns	Note 6
$\overline{MR}$ HIGH to CI HIGH	t_{DCI}	60		ns	
$\overline{MR}$ LOW to OR LOW	t_{DOR}		60	ns	
$\overline{MR}$ LOW to IR HIGH	t_{DIR}		60	ns	
$\overline{MR}$ LOW to output LOW	t_{LZMR}		60	ns	Note 4
Output valid from $\overline{OE}$ LOW	t_{OOE}		60	ns	
Output HIGH-Z from $\overline{OE}$ HIGH	t_{HZOE}		60	ns	

NOTES
1. $1/f_O > t_{PHCI} + t_{DHIR}$, $1/f_O > t_{PHCO} + t_{DHOR}$.
2. t_{SCI} and t_{HCI} apply when memory is not full.
3. Hold time is the lesser of the two parameters (a) and (b).
4. All data outputs will be at LOW level after reset goes high until data is entered into the buffer.
5. These times apply when the device is full and CI is held high.
6. For cascade applications, t_{PMR} must be double that specified above.

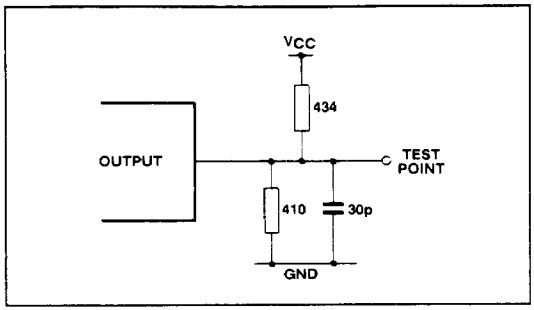

Fig.3 Test circuit

ABSOLUTE MAXIMUM RATINGS (Note 7)

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN} (see Note 9)	-0.9V to V_{CC} +0.9V
DC voltage applied to output when high impedance	-0.5V to 7.0V
Clamp diode current per pin (see Note 8)	+18mA
Storage temperature Ts	-65°C to +150°C

NOTES
7. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
8. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
9. Input voltages more negative than —0.9V cause clamp diode current to flow. The maximum negative voltage depends on the source impedance.

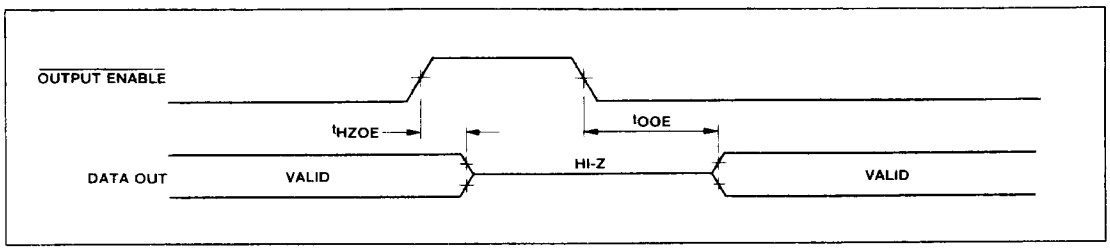

Fig.4 Output enable timing

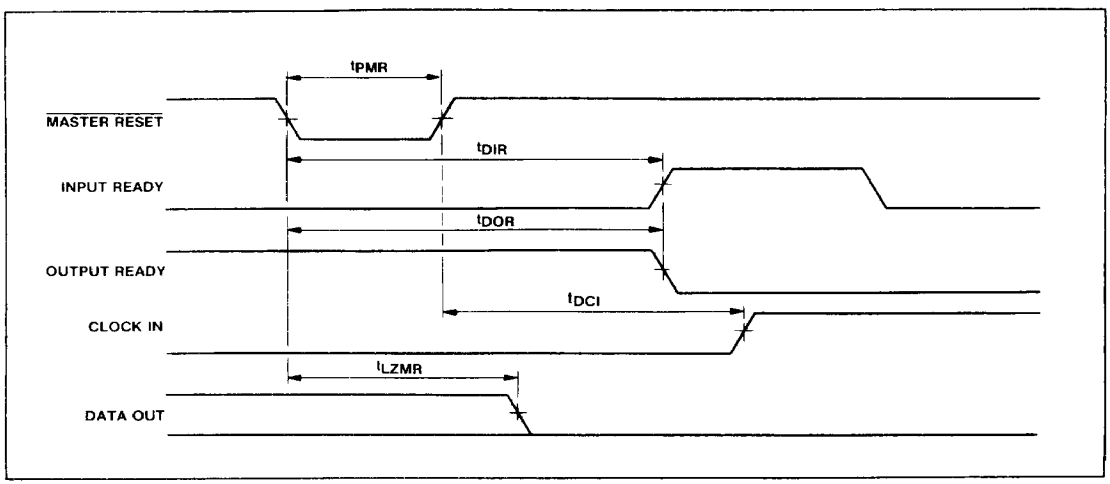

Fig.5 Master reset timing

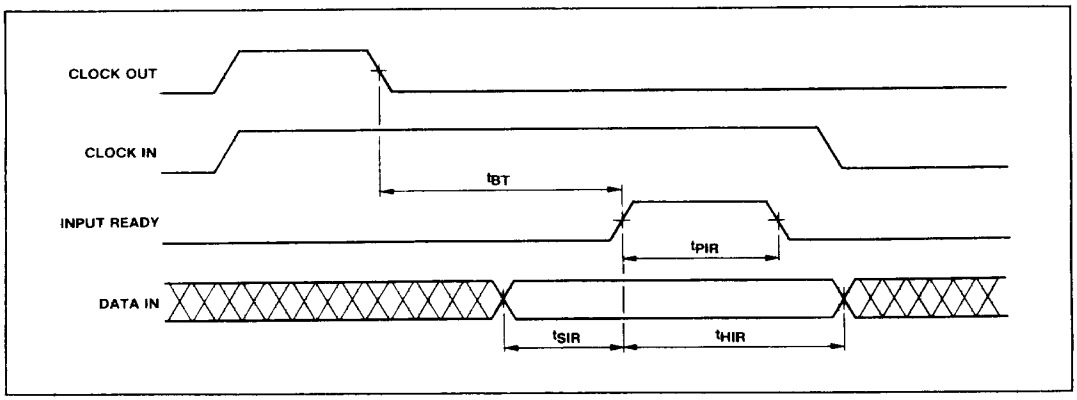

Fig.6 Data Out to Data In bubble through time

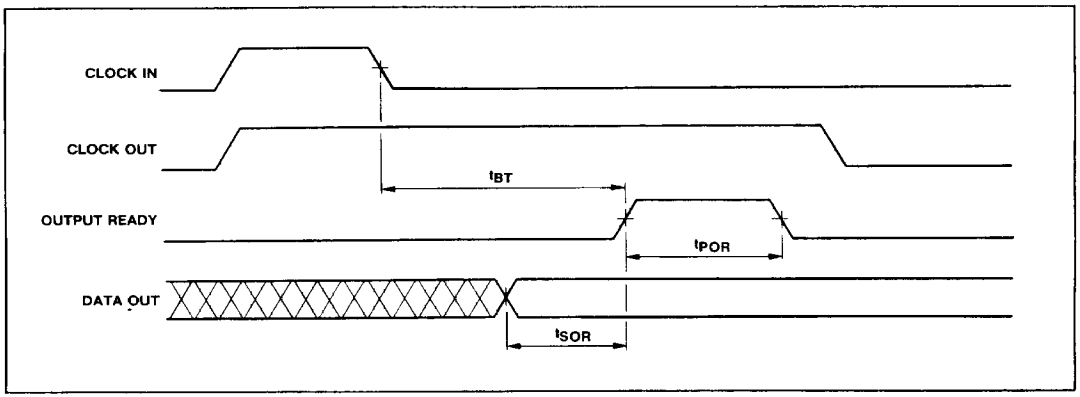

Fig.7 Data In to Data Out bubble through time

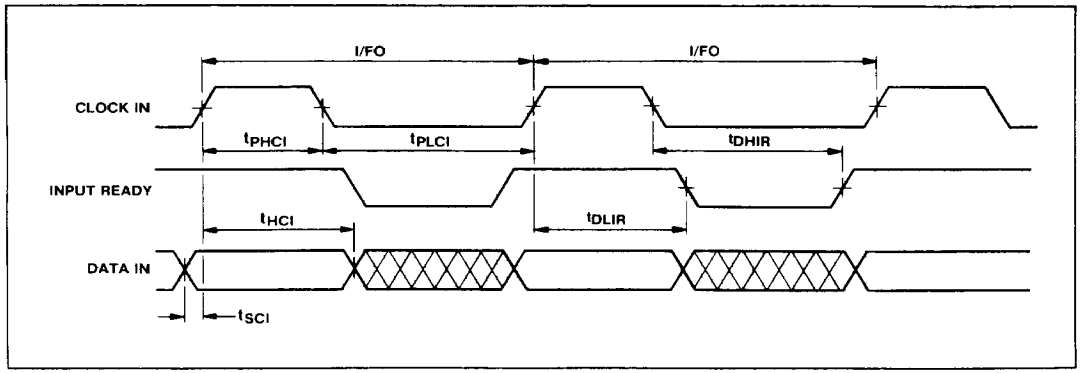

Fig.8 Switching waveforms - Data In timing

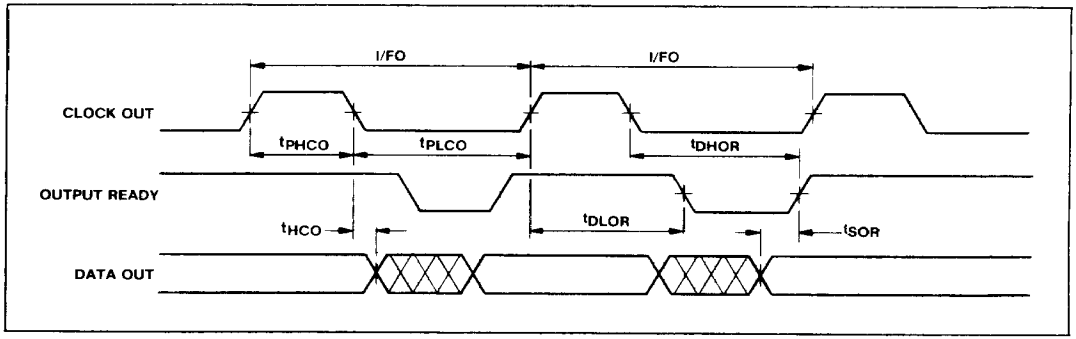

Fig.9 Switching waveforms - Data Out timing

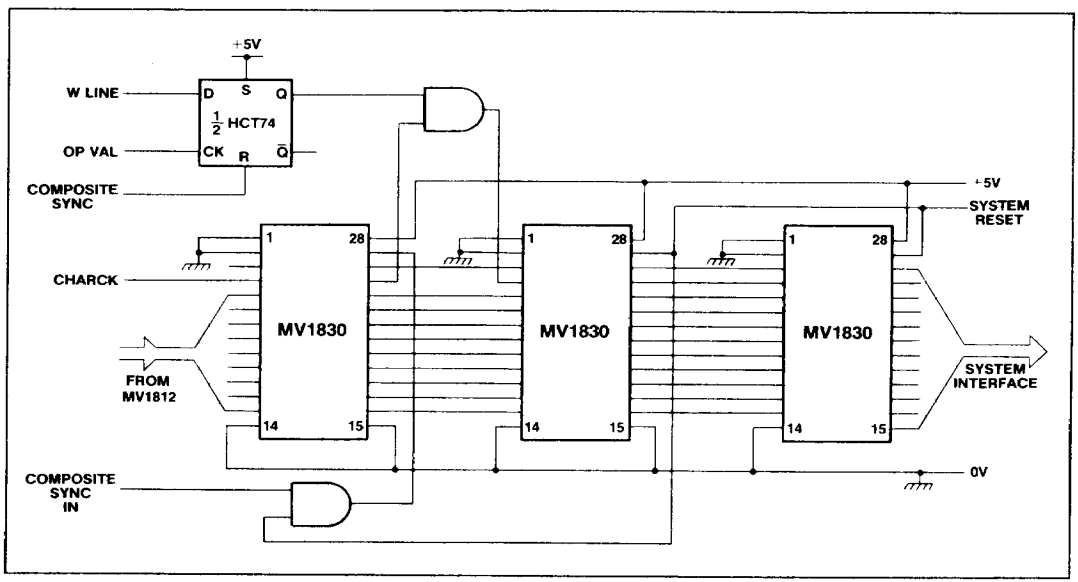

Fig.10 Interface to MV1812

USER NOTES

1. When the buffer is *empty the last word read will remain on the outputs* until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output changes as a result of a pulse on CO, the OR signal always goes LOW before there is any change in output data.
3. If CO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the buffer to the output. OR will go HIGH for one internal cycle (t_{POR}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the buffer, they will line up behind the first word and will not appear on the outputs until CO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If CI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the buffer and IR will return to the LOW state until CI is brought LOW. If CI is LOW when the master reset is ended, the IR will go HIGH, but the data on the inputs will not enter the buffer until CI goes HIGH.