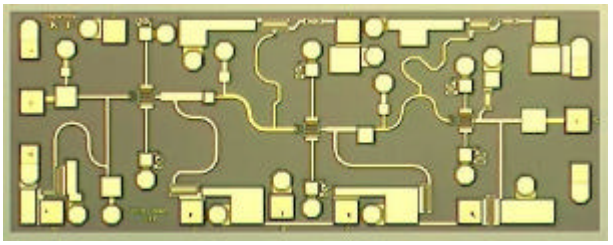
# HEMT MMIC LNA

# 20 - 32GHz



## Features

- Typical 2.1dB Noise Figure @24GHz &28GHz
- Self Biased Design
- 2.36 x 0.94mm Die Size

## Description

The P35-5113-000-200 is a 20-32GHz Gallium Arsenide Self-Biased low noise amplifier. This product is intended for use in fixed-point and point to point microwave systems.

The die is fabricated using Caswell Technology's 0.20µm gate length, pHEMT process and is fully protected using Silicon Nitride passivation for excellent performance and reliability.

## Electrical Performance

Ambient Temperature = 22±3° C, $Z_O$ = 50Ω, Vd = 2V

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Small Signal Gain | 20-32GHz | - | 23 | - | dB |
| Input Return Loss | 20-32GHz | - | 9 | - | dB |
| Output Return Loss | 20-32GHz | - | 12 | - | dB |
| Noise Figure | 20-32GHz | - | 2.5 | - | dB |
| P1dB | 20-32GHz | - | 4 | - | dBm |
| Supply current, Idd | | - | 48 | - | mA |
| Supply Voltage; Vdd | | - | 2 | - | V |

## Notes

1. All parameters measured on wafer

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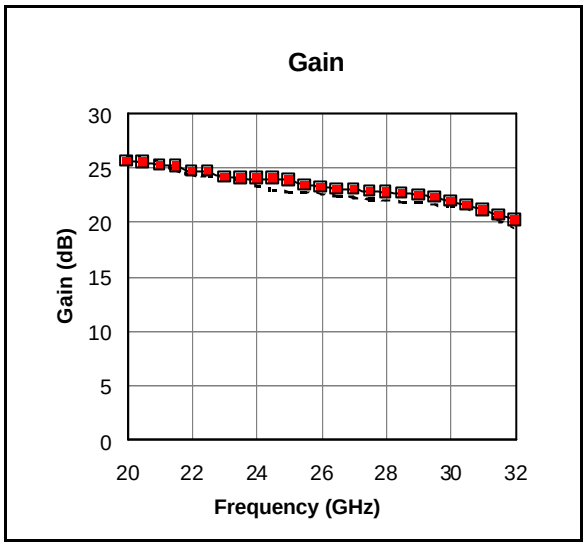
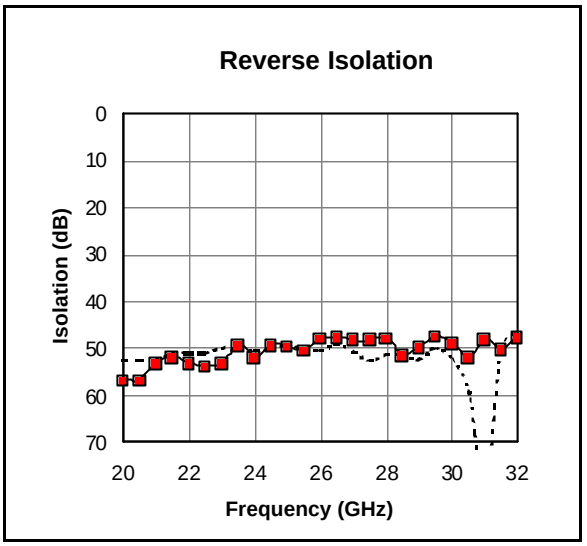
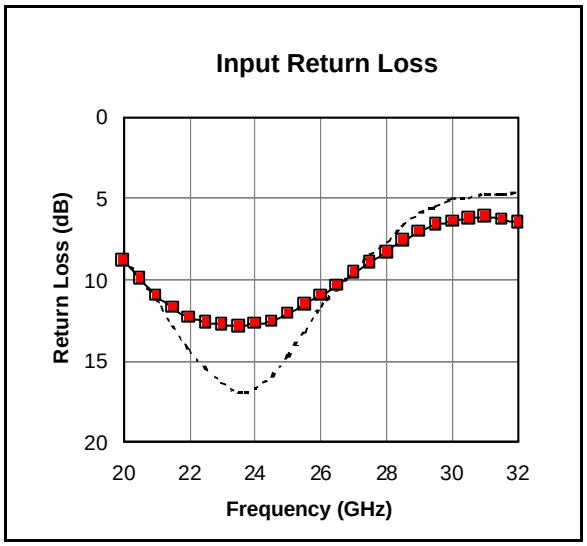
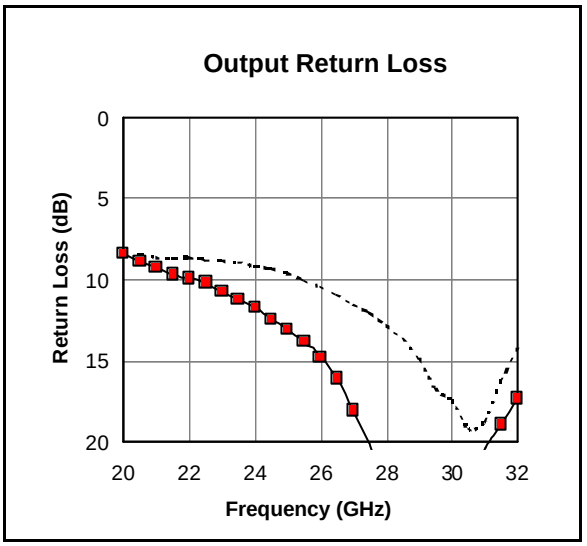
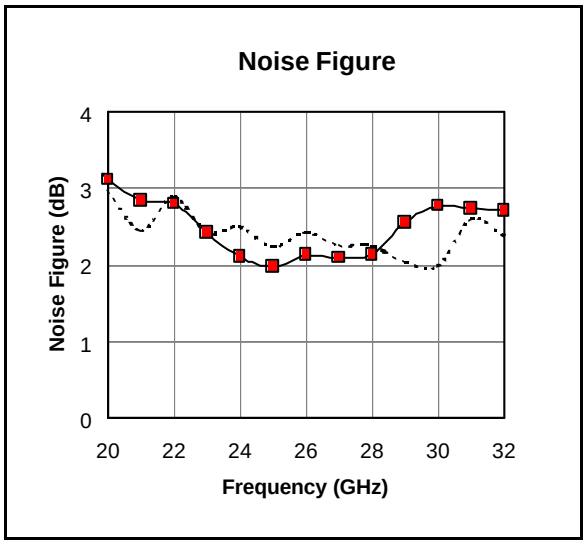
## Typical RFOW Performance ( ----- Jig Measurement )

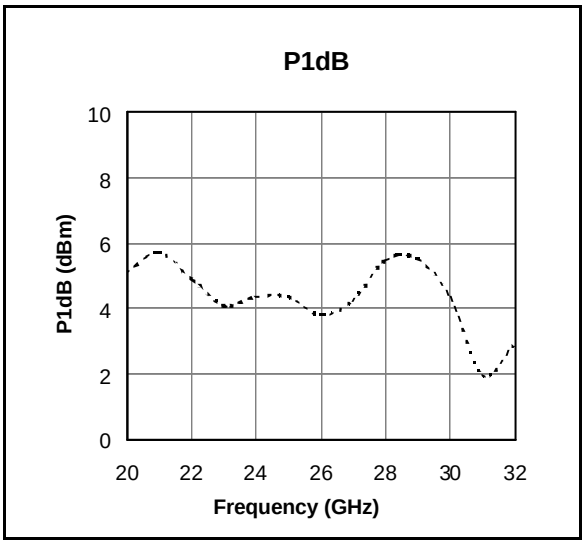
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## Typical S-parameters (RFOW)

| Frequency | S11 | | S21 | | S12 | | S22 | |
|---|---|---|---|---|---|---|---|---|
| (GHz) | Mag | Angle | Mag | Angle | Mag | Angle | Mag | Angle |
| 20 | 0.36 | -20.2 | 19.04 | 14.8 | 0.0014 | -174.4 | 0.38 | 172.5 |
| 20.5 | 0.32 | -26.7 | 18.84 | -3.5 | 0.0014 | -164.5 | 0.36 | 170 |
| 21 | 0.28 | -33.4 | 18.35 | -21.3 | 0.0021 | -153.6 | 0.34 | 167.4 |
| 21.5 | 0.26 | -39.9 | 17.99 | -37.6 | 0.0025 | 158.7 | 0.33 | 164.3 |
| 22 | 0.24 | -48.9 | 17.12 | -54.4 | 0.0021 | 174.1 | 0.32 | 161.4 |
| 22.5 | 0.23 | -59.6 | 17.15 | -69.2 | 0.002 | 154.3 | 0.31 | 156.9 |
| 23 | 0.23 | -70.2 | 16.11 | -85.3 | 0.0021 | 144.4 | 0.29 | 152.2 |
| 23.5 | 0.23 | -82.7 | 15.99 | -99.8 | 0.0033 | 135.3 | 0.28 | 147.8 |
| 24 | 0.23 | -96.2 | 15.84 | -113.2 | 0.0025 | 135.8 | 0.26 | 143.1 |
| 24.5 | 0.24 | -109.5 | 15.84 | -127 | 0.0033 | 117.3 | 0.24 | 136.8 |
| 25 | 0.25 | -123.2 | 15.66 | -140.9 | 0.0032 | 110.2 | 0.22 | 131.8 |
| 25.5 | 0.27 | -135.1 | 14.79 | -156.6 | 0.0029 | 110.3 | 0.20 | 126.3 |
| 26 | 0.28 | -147.9 | 14.56 | -170.4 | 0.0039 | 91.3 | 0.18 | 119.8 |
| 26.5 | 0.30 | -160 | 14.23 | 175.3 | 0.004 | 79.2 | 0.16 | 112.1 |
| 27 | 0.33 | -170.8 | 14.15 | 161.8 | 0.0038 | 56.4 | 0.12 | 106.1 |
| 27.5 | 0.36 | 177.4 | 13.87 | 147.8 | 0.0038 | 65.6 | 0.10 | 104.8 |
| 28 | 0.38 | 167.4 | 13.74 | 134.9 | 0.0039 | 51 | 0.07 | 108.8 |
| 28.5 | 0.41 | 155.2 | 13.60 | 120.9 | 0.0026 | 40 | 0.05 | 114.8 |
| 29 | 0.44 | 143.9 | 13.32 | 106.3 | 0.0031 | 41.3 | 0.04 | 140.9 |
| 29.5 | 0.47 | 132.7 | 13.09 | 92 | 0.0041 | 30.1 | 0.04 | 169.6 |
| 30 | 0.48 | 121.9 | 12.48 | 77.1 | 0.0035 | 13.7 | 0.05 | -167.7 |
| 30.5 | 0.49 | 111 | 11.95 | 63.1 | 0.0025 | 10.7 | 0.07 | -166.8 |
| 31 | 0.49 | 100.9 | 11.35 | 49.2 | 0.0038 | -3.3 | 0.10 | -165.6 |
| 31.5 | 0.48 | 90.8 | 10.76 | 36.3 | 0.003 | -3 | 0.11 | -168.4 |
| 32 | 0.47 | 82.5 | 10.22 | 23.6 | 0.004 | -5.8 | 0.14 | -169.6 |

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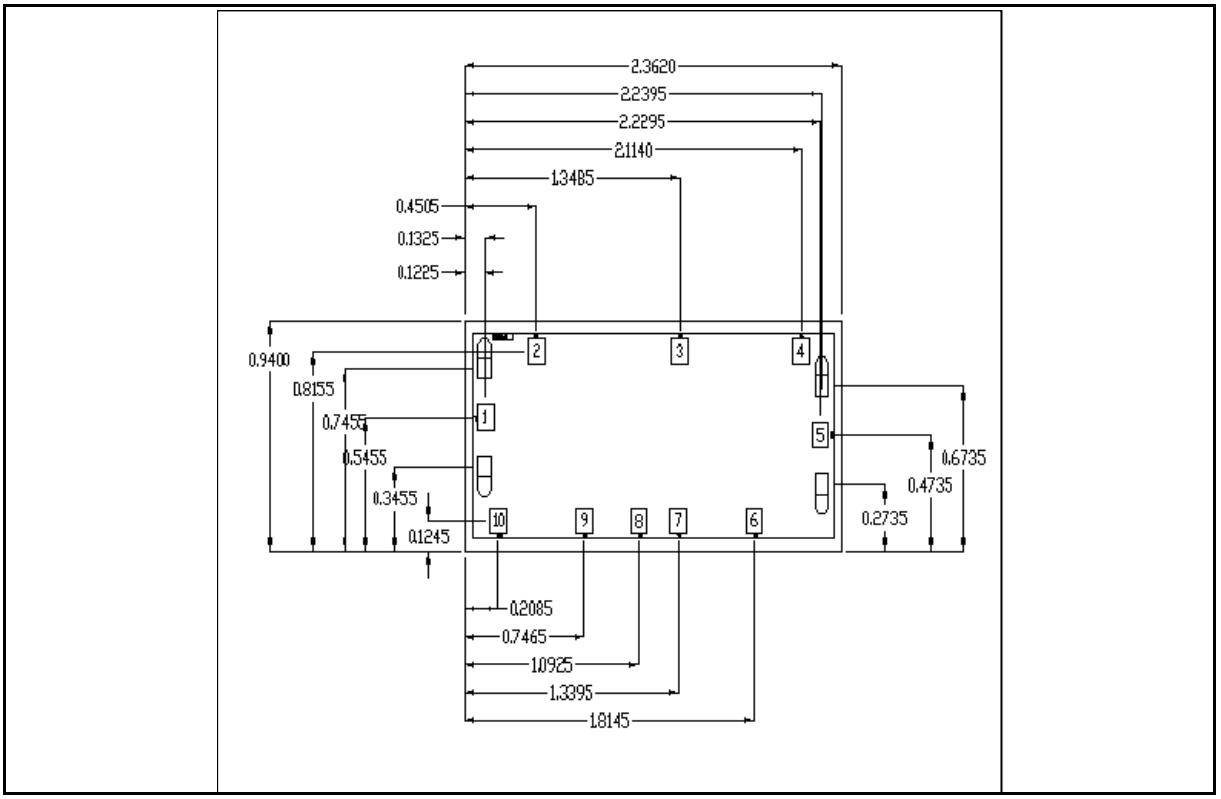
## Chip Outline




| | |
|---|---|
| Die size: | 2.36 x 0.94mm |
| RF bond pads (1 & 5): | 120µm x 120µm |
| All other bond pads: | 120µm x 120µm |
| Die Thickness: | 100µm |

## Pad Details

| Pad | Function |
|---|---|
| 1 | RF Input |
| 2 | N/C |
| 3 | N/C |
| 4 | N/C |
| 5 | RF Output |
| 6 | Vdd |
| 7 | N/C |
| 8 | N/C |
| 9 | N/C |
| 10 | N/C |

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## Handling and Assembly Information

Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Dice are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded anti-static workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

GaAs Products from Caswell Technology's pHEMT Foundry process are 100µm thick and have through GaAs vias to enable grounding to the circuit. Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die.

The surface to which the die are to be attached should be cleaned with a proprietary de-greasing cleaner.

Conductive epoxy mounting is recommended. Recommended epoxies are Ablestick 84-1LMI or 84-1LMIT cured at 150°C for 1 hour in a nitrogen atmosphere. The epoxy should be applied sparingly to avoid encroachment of the epoxy on to the top surface of the die. An epoxy fillet should be visible around the total die periphery.

Eutectic mounting can be used and entails the use of a gold-tin (AuSn) preform, approximately 0.001″ thick, placed between the die and the attachment surface. The preferred method of mounting is the use of a machine such as a Mullins 8-140 die bonder. This utilises a heated collet and workstation with a facility for applying a scrubbing action to ensure total wetting and avoid the formation of voids. Dry nitrogen gas is directed across the work piece.

The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280°C (Note: Gold Germanium with a higher melting temperature should be avoided, in particular for MMICs). The work station temperature should be 310°C ± 10°C. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. The strength of the bonding formed by this method will result in fracture of the die, rather than the bond under die strength testing.

The P35-5113-000-200 amplifier die has gold bond pads. The recommended wire bonding procedure uses 25µm (0.001") 99.99% pure gold wire with 0.5-2% elongation. Thermo-compression wedge bonding is preferred though thermosonic wire bonding may be used providing the ultrasonic content of the bond is minimised. A work station temperature of 260°C ± 10°C with a wedge tip temperature of 120°C ± 10°C is recommended. The wedge force should be 45 ± 5 grams. Bonds should be made from the bond pads on the die to the package or substrate.

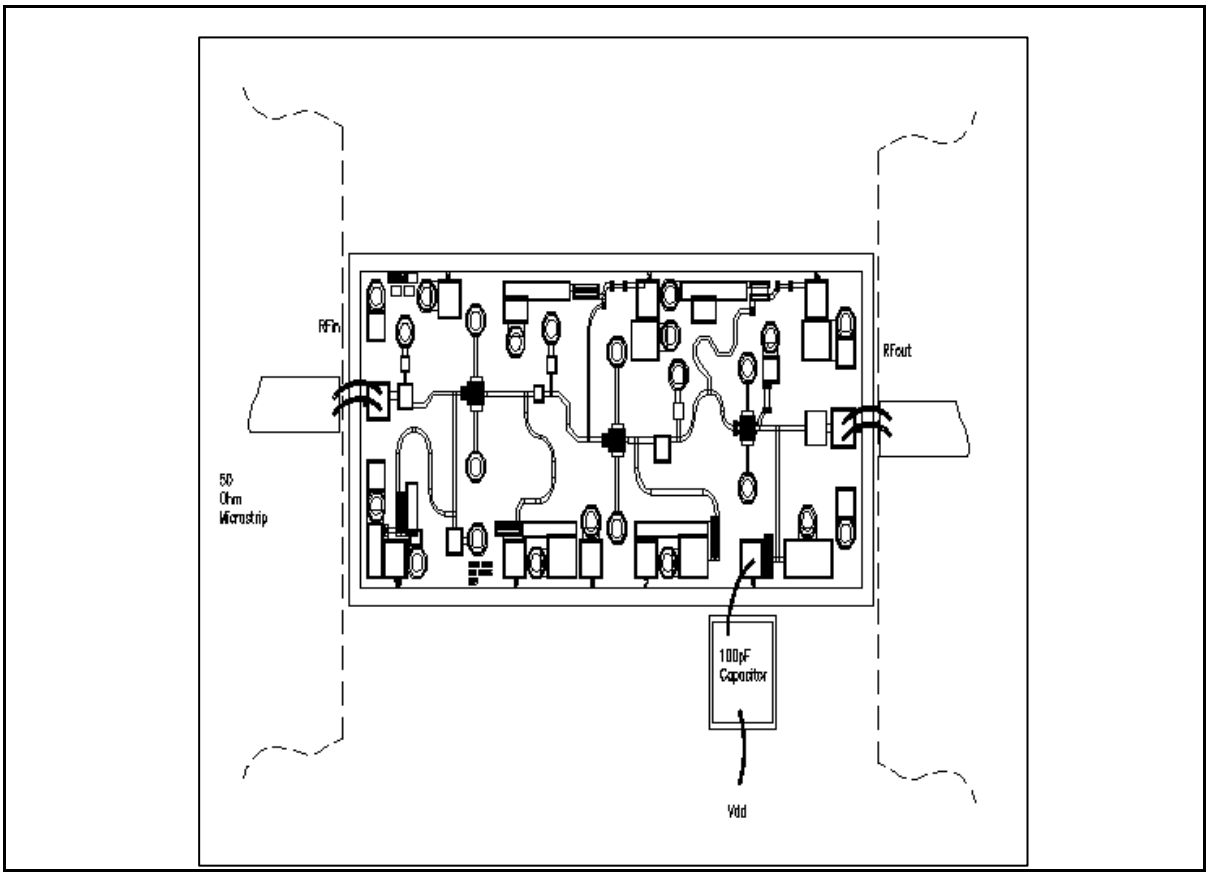
The RF bond pads at the input and output are 120µm x 120µm; all other bond pads are 120µm x 120µm.

The P35-5113-000-200 has been designed to include the inductance of two 25µm bond wires at both the input and output, facilitating the integration of the die into a 50Ω environment, these should be kept to a minimum length.

## Operating and Biasing of the P35-5113-000-200

The P35-5113-000-200 is a three-stage self-biased low noise amplifier. A drain bias of 2V should be applied at pad 6 (Vdd) and should be decoupled to ground using a 100pF chip capacitor placed close to the chip with short bondwires to the amplifier bond pad.

## Typical bonding detail




## Absolute maximum Ratings

| | |
|---|---|
| Max Vdd | +5V |
| Max Vgg | -2V |
| Max channel temperature | 150°C |
| Storage temperature | -65°C to +150°C |

## Ordering Information

*P35-5113-000-200*

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