

DATA SHEET



TDA8961 ATSC Digital Terrestrial TV demodulator/decoder

Objective specification
File under Integrated Circuits, IC02

2000 May 19

ATSC Digital Terrestrial TV demodulator/decoder

TDA8961

FEATURES

General features

- One-chip ATSC-compliant demodulator and concatenated trellis (Viterbi)/Reed Solomon decoder with de-interleaver and de-randomizer
- 0.35 μm process
- 3.3 V device
- QFP80 package
- Boundary Scan Test (BST)
- 12 MHz external clock
- 36 MHz output for external D/A converter
- Parallel or serial MPEG-2 transport stream output.

8-Vestigial Side Band (VSB) demodulator

- Accepts 10-bit IF data sampled at 36 MHz
- 6 MHz wide IF signal, centered at 4 MHz
- On-chip digital circuitry for tuner AGC
- Square-root raised-cosine filter with 11.5% roll-off factor
- Fully internal carrier recovery loop
- No need for external voltage controlled crystal oscillator due to internal sample rate converter
- Fully internal symbol timing recovery with programmable loop filters
- Technology to handle dynamic multipath conditions.

Adaptive equalizer

- Including feed forward and feedback sections with Decision Feedback Equalizer (DFE) structure
- Range of -2.3 to $+22.5 \mu\text{s}$ by default (in conjunction with external software, -2.3 to $+80 \mu\text{s}$)
- Adaptation based on ATSC field sync (trained) and/or 8-VSB data (blind).

NTSC co-channel interference filter

Patented NTSC co-channel interference technology with low noise penalty.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8961	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body $14 \times 20 \times 2.8$ mm	SOT318-2



On-chip forward error correction

- Trellis (Viterbi) decoder
- Rate $\frac{2}{3}$ (Rate $\frac{1}{2}$ Ungerboeck code based)
- (207, 187, T = 10) Reed Solomon code
- Internal convolutional de-interleaving (l = 52; using internal memory)
- External indication of uncorrectable error; transport_error_indicator bit in MPEG packet header is also set
- De-randomizer based on ATSC standard
- Segment error rate readable through I²C.

I²C interface

I²C-bus interface to initialize and monitor the demodulator and Forward Error Correction (FEC) decoder. An operation without I²C-bus is possible (default).

System interfaces

- 8-bit wide or serial MPEG-2 transport stream interface
- ITU656 bypass mode
- MPEG-2 serial transport stream input to reduce external components when the IC is combined in a system with a Quadrature Amplitude Modulation (QAM), Quadrature Phase Shift Keying (QPSK) or Orthogonal Frequency Division Multiplexing (OFDM) channel decoder.

APPLICATIONS

- Digital ATSC compliant TV receiver
- Personal computers with digital television capabilities
- Set top-boxes.

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GENERAL DESCRIPTION

The TDA8961 is an Advanced Television Systems Committee (ATSC)-compliant demodulator and FEC decoder for reception of 8-VSB modulated signals for terrestrial and cable applications:

- **Terrestrial:** reception of 8-VSB modulated signals via standard 6 MHz VHF/UHF terrestrial TV channels (TV channels 2 to 69 in the United States).
- **Cable:** reception of 8-VSB modulated signals via standard 6 MHz VHF/UHF cable TV channels.

An application using the TDA8961 and the TDA8980 NTSC/ATSC TV input processor for TV and Multi-Media is shown in Fig.1. A tuner converts the incoming RF signal to a fixed IF centered at 44 MHz. The output signal from the tuner is filtered and fed to the TDA8980 which performs the following functions:

- Decodes the analog NTSC signals: The audio signals are digitized, using on-chip audio stereo A/D converters, into an I²S-bus stream; the video information is digitized, using on-chip video A/D converters, into an ITU656 stream.

- Down converts the incoming 6 MHz wide 8-VSB IF signal to a low-IF signal centered at 4 MHz: The low-IF signal is then digitized, using an on-chip 10-bit A/D converter, and fed to the TDA8961 for further processing. In this application, AGC is also managed by the TDA8980 so that no other external components, such as an operational amplifier loop integrator, are required.

Although the TDA8980 has an internal 2-D comb filter, external filters such as a 3-D comb filter and other picture improvement devices can easily be connected. Sound can be decoded using an external device such as the TDA9851 I²C-bus controlled economic BTSC stereo decoder. This IC has an internal switch allowing it to process either analog NTSC IF or digital 8-VSB IF signals.

A 12 MHz clock signal is generated using a 12 MHz crystal connected to the TDA8980. The TDA8961 also uses this clock signal which is fed from the TDA8980 to pin XTALI of the TDA8961.

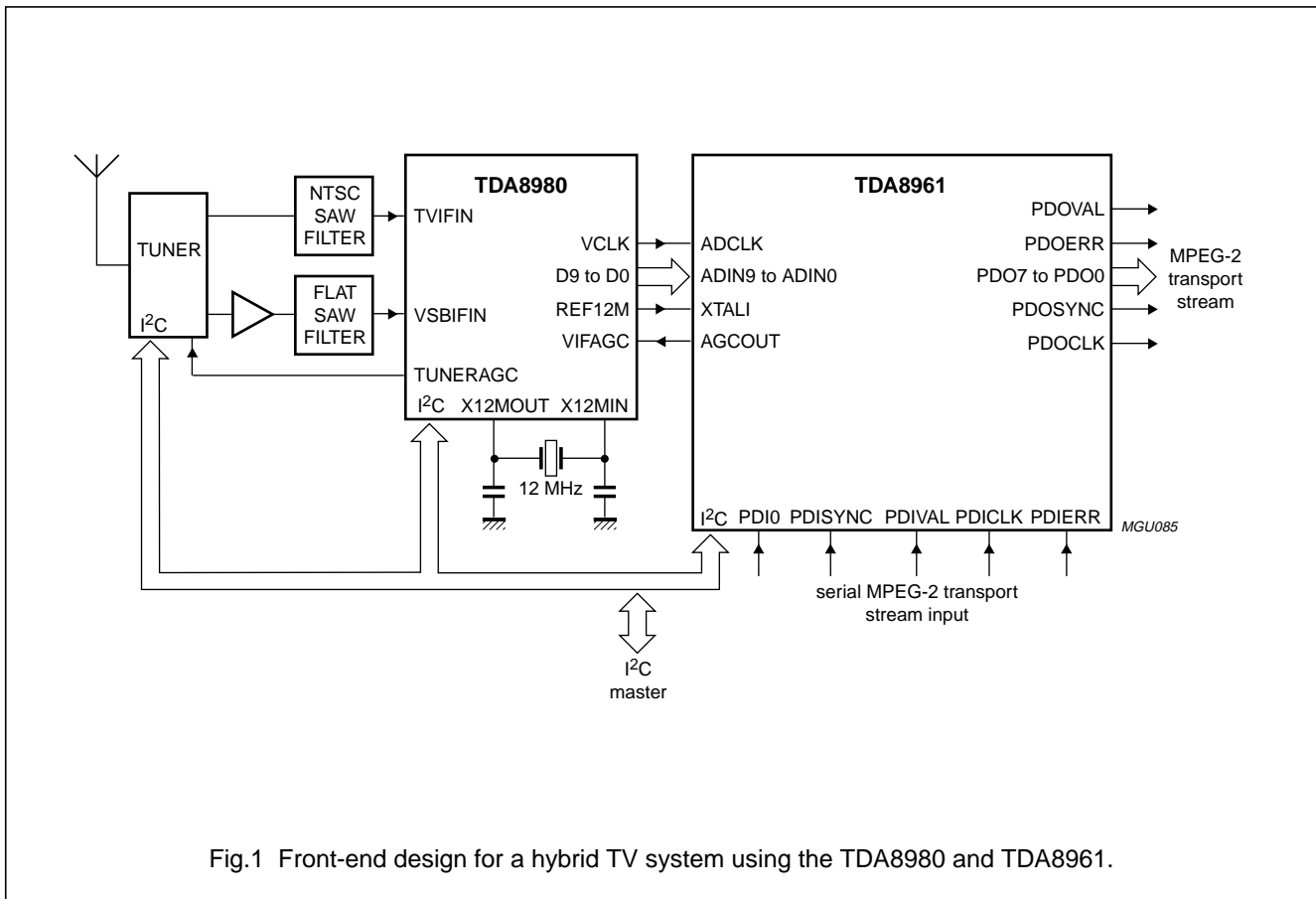


Fig.1 Front-end design for a hybrid TV system using the TDA8980 and TDA8961.

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The incoming data has a sample rate of 36 MHz. This is internally converted to a sample rate of 21.52 MHz which is twice the 8-VSB symbol rate. This patented Philips Semiconductors' technology eliminates the need for external symbol timing recovery loop components. When the TDA8980 is decoding analog NTSC, the TDA8961 can be set to a ITU656 bypass mode which allows the 8-bit ITU656 data output from the TDA8980 to appear at the TDA8961 Moving Pictures Expert Group (MPEG-2) transport stream output, from where it can be fed to the main graphics display device in the system.

The recovery of the carrier is performed entirely within the TDA8961. This function consists of a digital frequency and Frequency Phase-Locked Loop (FPLL).

Data shaping is performed by a square-root raised-cosine (half Nyquist) filter having a roll-off factor of 11.5%.

After the TDA8961 has performed carrier recovery, Nyquist filtering and symbol timing recovery, it then performs adaptive equalization. The adaptive equalizer uses a DFE structure with equalization based on the ATSC field sync (trained equalization) and/or the 8-VSB data itself (blind equalization).

The equalizer is followed by a patented NTSC co-channel interference filter which removes any unwanted NTSC signal interference from the 8-VSB terrestrial DTV signal.

After trellis decoding, the stream is de-interleaved to a depth of 52 by a convolutional de-interleaver whose memory is provided on-chip. The Reed Solomon decoder is ATSC-compliant, with a length of 207, and able to

correct up to 10 bytes. The decoded stream is then de-randomized using a pseudo-random binary sequence (PRBS) and the data passed to a FIFO which prevents the appearance of irregular gaps in the output data.

The output of the TDA8961 is a clock signal and an ATSC-compliant MPEG-2 packetized data stream. Signal flag outputs are provided to indicate the occurrence of sync bytes, valid data bytes and uncorrected Reed Solomon blocks. The packetized data stream is available in either an 8-bit parallel, or a 1-bit serial format for connection to an MPEG-2 transport stream demultiplexer.

An application using the TDA8961 and a stand-alone TDA9829 Downconverter for DVB (Digital Video Broadcast) with an A/D converter is shown in Fig.2. A tuner converts the incoming RF signal to a fixed IF centered at 44 MHz. The output signal from the tuner is filtered using two Surface Acoustical Wave (SAW) filters and then down converted to an IF of 4 MHz by the TDA9829. The signal is then digitized by an A/D converter at a sample rate of 36 MHz using the clock signal output from the TDA8961.

The full input range of the A/D converter is utilized by placing it within what is effectively a fine-AGC loop integrator circuit which has a variable gain stage at the output of the IF downmixer section. However, it is also possible to apply the AGC control output of the TDA8961 to the tuner via the integrator. The peak level of the input signals to the TDA8961 is determined by the AGC output detector which is located just after the A/D.

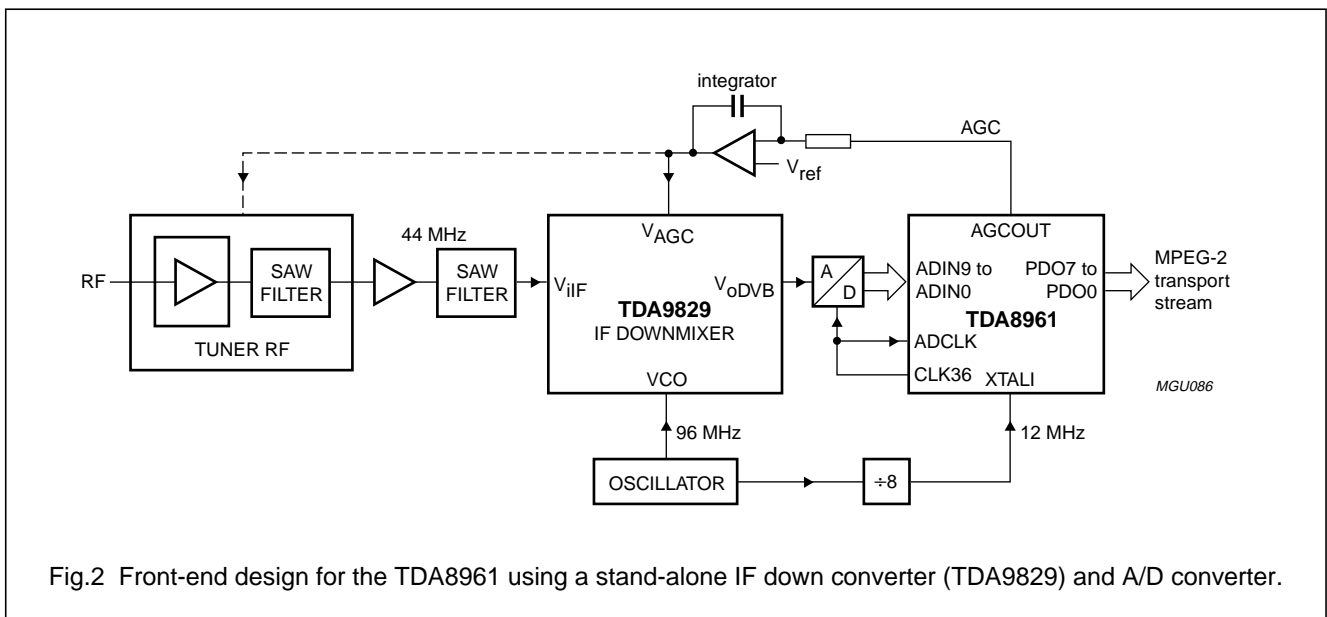


Fig.2 Front-end design for the TDA8961 using a stand-alone IF down converter (TDA9829) and A/D converter.

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.7	3.3	3.6	V
I_{DD}	supply current	$V_{DD} = 3.3\text{ V}$	–	390	–	mA
f_{clk}	clock frequency		–	12	–	MHz
f_{sym}	symbol frequency		–	10.76	–	Msymbols/s
f_s	sample frequency		–	36	–	MHz
$f_{c(IF2)}$	second IF centre frequency		–	4	–	MHz
IL	implementation loss		–	–	–	dB
α_{ro}	half Nyquist filter roll-off factor		–	11.5	–	%
t_{acq}	acquisition time	note 1	–	–	290	ms
T_{amb}	ambient temperature		–20	–	+70	°C
P_{tot}	total power dissipation		–	1.3	–	W

Note

1. Corresponds to 12 training sequences.

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BLOCK DIAGRAM

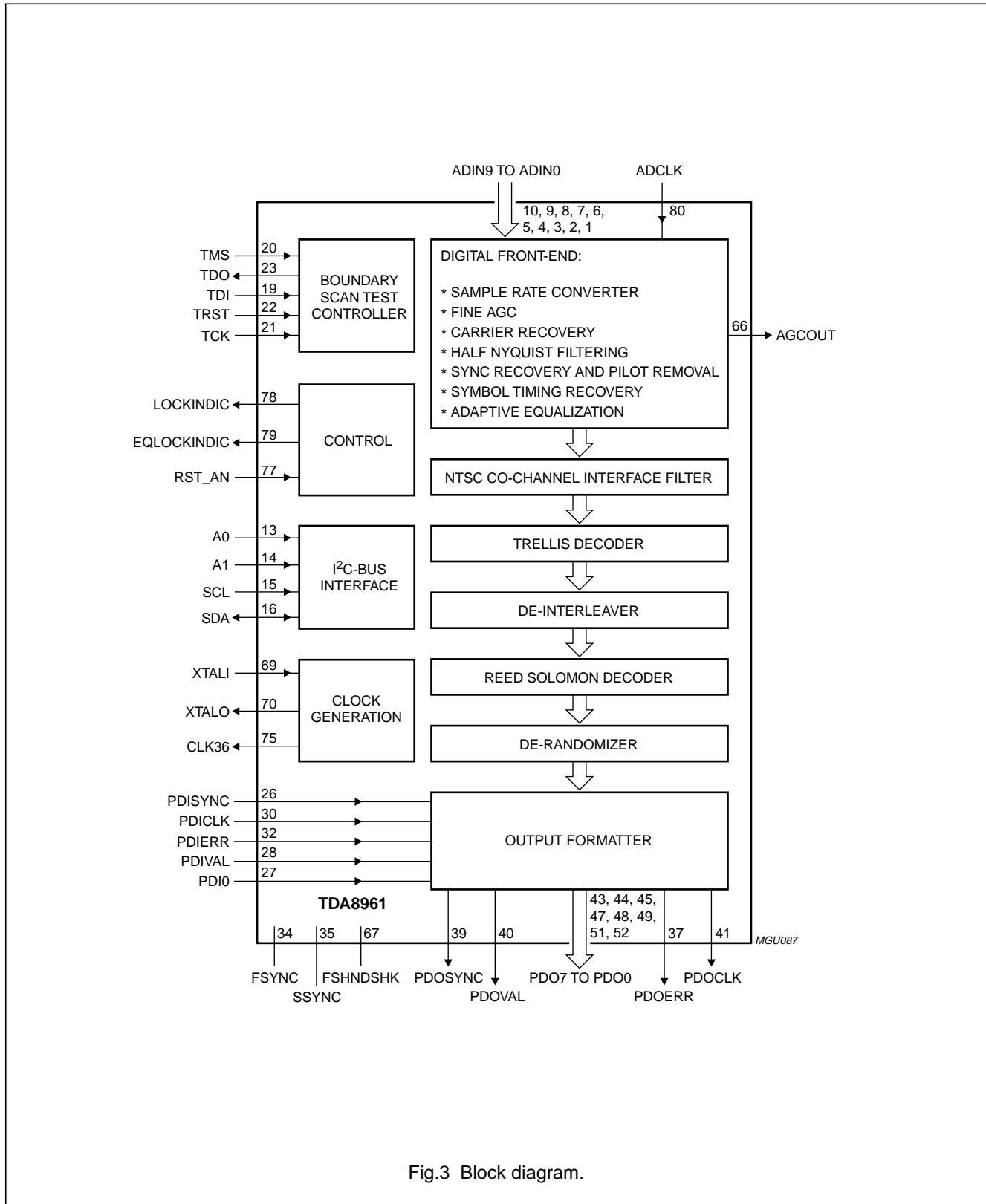


Fig.3 Block diagram.

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PINNING

SYMBOL	PIN	I/O	DESCRIPTION
ADIN0	1	I	data input bit 0 (LSB)
ADIN1	2	I	data input bit 1
ADIN2	3	I	data input bit 2
ADIN3	4	I	data input bit 3
ADIN4	5	I	data input bit 4
ADIN5	6	I	data input bit 5
ADIN6	7	I	data input bit 6
ADIN7	8	I	data input bit 7
ADIN8	9	I	data input bit 8
ADIN9	10	I	data input bit 9 (MSB)
V _{DDD1}	11	–	digital core supply voltage 1 (3.3 V)
V _{SSD1}	12	–	digital core ground 1
A0	13	I	I ² C-bus slave address bit 0
A1	14	I	I ² C-bus slave address bit 1
SCL	15	I	I ² C-bus clock
SDA	16	I/O	I ² C-bus serial data
V _{DDD2}	17	–	I/O supply (3.3 V)
V _{SSD2}	18	–	digital core ground 2
TDI	19	I	TAP controller data input; note 1
TMS	20	I	TAP controller test mode select; note 1
TCK	21	I	TAP controller test clock; note 1
TRST	22	I	TAP controller asynchronous reset (active LOW); notes 1 and 2
TDO	23	O	TAP controller test data (3-state); note 1
V _{DDD3}	24	–	digital core supply voltage 3 (3.3 V)
V _{SSD3}	25	–	digital core ground 3
PDISYNC	26	I	transport stream interface packet sync indicator
PDI0	27	I	transport stream interface packet data bit 0
PDIVAL	28	I	transport stream interface packet data valid signal
V _{DDD4}	29	–	digital core supply voltage 4 (3.3 V)
PDICLK	30	I	transport stream interface packet data clock signal
V _{SSD4}	31	–	digital core ground 4
PDIERR	32	I	transport stream interface packet error signal
V _{DDD5}	33	–	digital core supply voltage 5 (3.3 V)
FSYNC	34	I	field sync strobe (for debug modes)
SSYNC	35	I	segment sync strobe (for debug modes)
V _{SSD5}	36	–	digital core ground 5
PDOERR	37	O	transport stream interface packet error signal (3-state)
V _{DDQ1}	38	–	I/O supply voltage 1 (3.3 V)
PDOSYNC	39	O	transport stream interface packet sync indicator signal (3-state)
PDOVAL	40	O	transport stream interface packet data valid indicator signal (3-state)

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SYMBOL	PIN	I/O	DESCRIPTION
PDOCLK	41	O	transport stream interface packet data clock signal (3-state)
V _{SSQ1}	42	–	I/O ground 1
PDO7	43	O	transport stream interface packet data bit 7 (3-state)
PDO6	44	O	transport stream interface packet data bit 6 (3-state)
PDO5	45	O	transport stream interface packet data bit 5 (3-state)
V _{DDQ2}	46	–	I/O supply voltage 2 (3.3 V)
PDO4	47	O	transport stream interface packet data bit 4 (3-state)
PDO3	48	O	transport stream interface packet data bit 3 (3-state)
PDO2	49	O	transport stream interface packet data bit 2 (3-state)
V _{SSQ2}	50	–	I/O ground 2
PDO1	51	O	transport stream interface packet data bit 1(3-state)
PDO0	52	O	transport stream interface packet data bit 0 (3-state)
V _{DDQ3}	53	–	I/O supply 3 (3.3 V)
n.c.	54		not connected
n.c.	55		not connected
V _{SSQ3}	56	–	I/O ground 3
n.c.	57		not connected
n.c.	58		not connected
n.c.	59		not connected
V _{DDQ4}	60	–	I/O supply 4 (3.3 V)
n.c.	61		not connected
n.c.	62		not connected
n.c.	63		not connected
V _{SSQ4}	64	–	I/O ground 4
n.c.	65		not connected
AGCOUT	66	O	AGC control (3-state)
FSHNDSHK	67	O	field sync strobe or symbol capture memory handshake signal
V _{DDA1}	68	–	analog supply voltage (3.3 V)
XTALI	69	I	external crystal
XTALO	70	O	external crystal
V _{SSA1}	71	–	analog ground 1
V _{DDA2}	72	–	analog supply 2 (3.3 V)
n.c.	73		not connected
V _{DDQ5}	74	–	I/O supply 5 (3.3 V)
CLK36	75	O	36 MHz clock signal
V _{SSQ5}	76	–	I/O ground 5
RST_AN	77	I	asynchronous reset (active LOW)
LOCKINDIC	78	O	front-end lock indicator
EQLOCKINDIC	79	O	equalizer lock indicator
ADCLK	80	I	incoming data sampling clock signal (36 MHz)

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TDA8961**Notes**

1. Input pins TCK, TDI, TMS and TRST have an internal pull-up transistor and must be connected to ground when not used; pin TDO is a 3-state output in accordance with IEEE 1149.1.
2. Pin TRST is active LOW. It can be used to immediately force the Test Access Port (TAP) controller to the test logic reset state (normal operation) in accordance with IEEE 1149.1.

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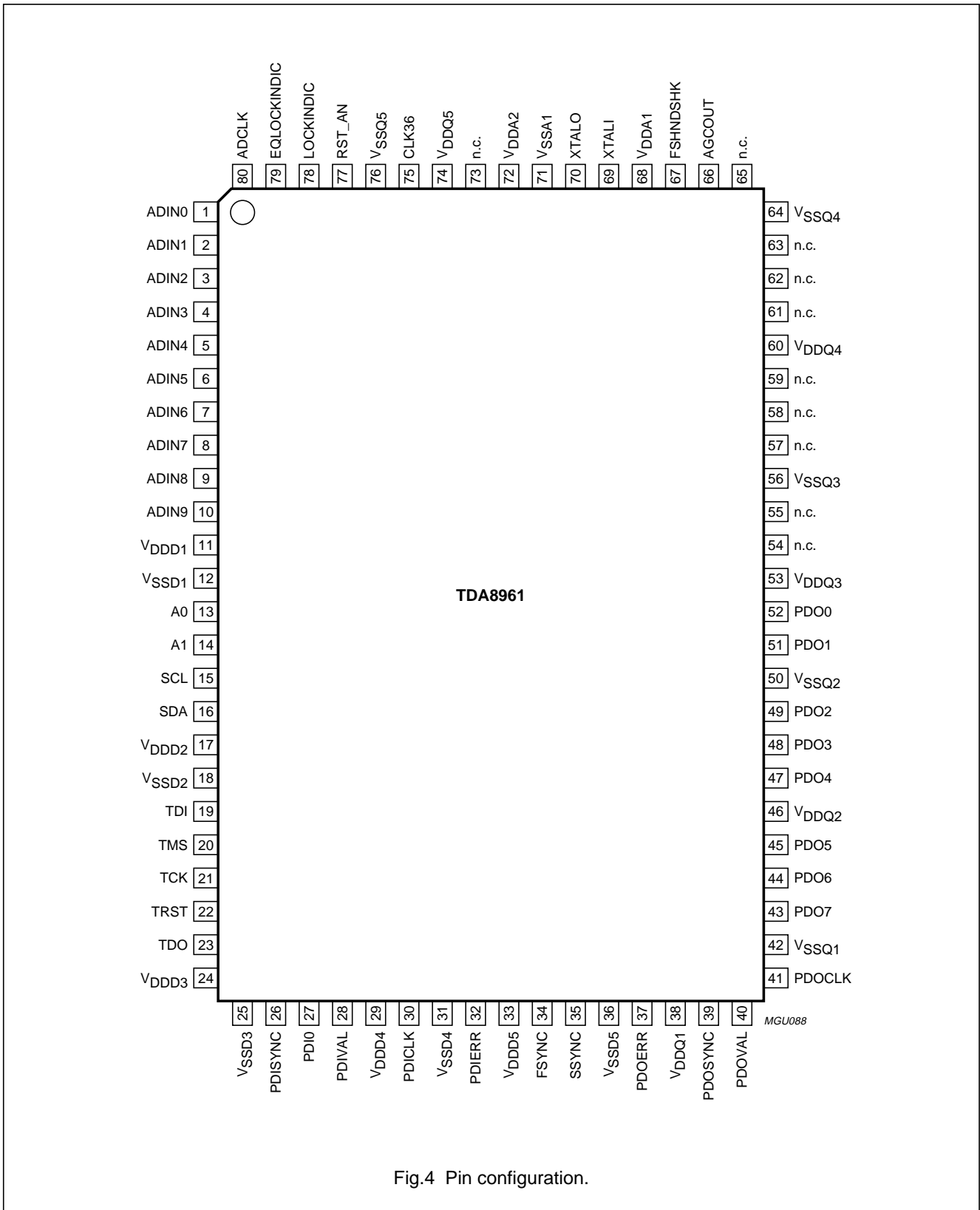


Fig.4 Pin configuration.

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FUNCTIONAL DESCRIPTION

The internal architecture of the TDA8961 basically comprises two parts:

- **The front-end:** containing the AGC, carrier recovery, half Nyquist filter, symbol timing recovery, sync recovery and adaptive equalization sections.
- **The back-end:** containing the NTSC co-channel rejection filter, trellis decoder, de-interleaver, the Reed Solomon decoder and de-randomizer sections.

Sample rate converter

INTRODUCTION

The sample rate converter section changes the incoming data frequency of 36 MHz to an internal sampling frequency of twice the symbol rate.

The 10-bit wide data from either the TDA8980 or a stand-alone A/D converter (TDA8763A is recommended) arrives at the sample rate converter input of the TDA8961 via inputs ADIN9 to ADIN0. The format of the incoming samples can be programmed by the status of I²C-bus bit AD_FMT (see Table 9). The format can be either two's complement or binary. The default setting is binary to comply with the TDA8980.

PINNING

The functions of the input interface pins are given in Table 1. If a stand-alone A/D converter is used, pin CLK36 is connected externally to pin ADCLK.

Table 1 Input interface

NAME	FUNCTION
ADIN9 to ADIN0	10-bit data input (from external A/D converter)
ADCLK	36 MHz clock signal input
CLK36	clock signal output for sampling incoming data (to external A/D converter)

Table 2 AGC

FILTER OUTPUT LEVEL	COMPARATOR OUTPUT	I ² C-bus bit AGC_DIR	Pin AGCOUT
Above threshold	1	0	1
Below threshold	0	0	0
Above threshold	1	1	0
Below threshold	0	1	1
Equal to threshold	Z	0	Z

Fine AGC

The fine AGC section controls the gain of analog signals over a range of ± 20 dB.

The level of the signal at pins ADIN9 to ADIN0 is monitored and an average level from several samples is acquired. The default number of samples is 64, but this value can be set to 256 by setting I²C-bus bit AGC_SAMPLES (see Table 10). A comparator compares the level of the filtered signal with a threshold level represented by a signed four-bit value set by I²C-bus bits AGC_TR_LOW. The comparator output determines the level at pin AGCOUT which is used to either charge or discharge an off-chip ideal integrator, which in turn, controls the gain of the tuner front-end module.

To make the level at pin AGCOUT compatible with the AGC circuits in other devices, the comparator output can be inverted by setting I²C-bus bit AGC_DIR (see Table 10). The default value of bit AGC_DIR is 0 making the output at pin AGCOUT compatible with the AGC circuit in the TDA8980. The levels at pin AGCOUT with respect to the value of bit AGC_DIR are shown in Table 2.

The AGC section can be reset by setting I²C-bus bit AGC_RESET (see Table 8).

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Carrier recovery

The carrier recovery circuit recovers the frequency and phase of the pilot carrier signal. If, as in some cases, the pilot signal is present at the higher edge of the VSB spectrum, the I²C-bus bit CR_INV can be set to ensure that when the frequency is shifted, the pilot signal is DC.

Half Nyquist filtering

The half Nyquist filtering section is a square-root raised-cosine filter with 11.5% roll-off.

Sync recovery

The sync recovery section performs several functions including the recovery of segment sync and field sync. When this section detects the data segment sync signal, pin LOCKINDIC goes HIGH. The status of pin LOCKINDIC can also be read via the I²C-bus bit LOCK_INDICATOR (see Table 16).

Timing recovery

The timing recovery section takes signals from the half Nyquist filter and forms part of a closed loop in order to acquire and maintain a constant sampling rate and clock frequency for the complete system.

Adaptive equalizer

The adaptive equalizer comprises a forward filter and a feedback filter section. At every symbol period, it receives demodulated symbols from the sync recovery section. The equalizer filters these symbols in an attempt to eliminate the effects of multipath conditions on the symbol stream during transmission. The coefficients of the filters are updated every symbol period using the training sequence and/or using blind equalization if required.

The equalizer is designed to correct a maximum pre-echo of 2.32 μ s and a maximum post-echo of 22.5 μ s. The equalizer has an optimized typical acquisition time of 12 training sequences, which corresponds to about 290 ms. It is defined that acquisition occurs when the output signal-to-noise ratio reaches the Threshold Of Visibility (TOV). For 8-VSB, the ATSC defines a TOV of 14.9 dB.

A Mean Square Error (MSE) signal is generated based on the training signal and on the output of the equalizer. The error signal represents a 16-bit value which is read via the I²C-bus bit MSE (see Table 18) and used to monitor the channel adaptation process.

It is possible to use software control to extend the range of the feedback filter to a maximum of 80 μ s.

CONTROL

An integrated sophisticated finite state machine controls the sequence of operations that must be performed to correctly decode a valid VSB data signal into an MPEG-2 packetized transport stream.

After a reset has been applied, the finite state machine is in state 0. When a valid VSB data signal is detected, the finite state machine ensures that the following three states occur.

State 1: channel acquisition

In this state there is either no channel signal present or a channel signal is in the process of being acquired. Before the channel signal can be acquired, the AGC, timing recovery and carrier recovery loops must first lock onto it. If segment sync lock is lost, either pin LOCKINDIC goes LOW, or a hardware reset is applied to the TDA8961 and the finite state machine returns to state 0.

State 2: equalizer training

The finite state machine remains in state 1 until the MSE of the equalized training sequence falls between two specific threshold values. It should be noted that in state 1, the back-end section of the TDA8961 is continuously reset to make sure that after its demodulator has locked onto a signal, the trellis decoder and the following sections begin processing at the start of the next complete data field. The value of I²C-bus bit MSE can be used for applications such as antenna pointing.

State 3: normal operation

Normally the finite state machine remains in state 2 unless a synchronization error occurs. If the MSE of the equalized training sequence exceeds 100 ms, the equalizer is reset for one symbol period and the adaptation process restarts.

If the demodulator synchronization and equalization are both locked, pin EQLOCKINDIC goes HIGH and I²C-bus bit LOCK_INDICATOR is set to 11 (see Table 16).

The filtered output signal is then routed to the NTSC co-channel interference filter.

NTSC co-channel interference filter

The NTSC co-channel interference filter uses patented Philips' technology making its performance considerably better than the ATSC specified comb filter. The filter can be bypassed by setting I²C-bus bit FLT_BYPASS (see Table 13).

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Transport stream interface

INTRODUCTION

The transport stream interface performs the following functions:

- Buffers the data from the Reed Solomon decoder and de-randomizer section
- Inserts the MPEG sync byte at the start of every packet
- Indicates error conditions using a `transport_error_indicator` bit in the packet header and the error signal output PDOERR.
- Outputs either a serial or a parallel output format.

PINNING

The functions of the transport stream interface outputs are summarized in Table 3. It should be noted that different source decoder devices may have different uses for the PDOERR output; its polarity is programmable using I²C-bus bit FPBP (see Table 14).

PARALLEL OUTPUT FORMAT

Figure 5 shows the timing diagram for the parallel output format. The PDOSYNC signal indicates the occurrence of the sync byte in the packet and is only HIGH for one clock period. The polarity of the PDOVAL and PDOERR signals is programmable via I²C-bus bits FDVP and FPBP respectively; Fig.5 shows their default polarities.

The PDOVAL signal is active for the duration of the 188 bytes of the transport stream packet. When the 188 bytes have been transferred, the PDOVAL signal goes LOW for at least ten PDOCLK cycles during which,

when used with DVB devices, the parity bytes are transferred; when used with non-DVB devices, zeroed parity bytes and field sync data are transferred.

The period when the PDOVAL signal is LOW can vary, but will be a minimum of ten PDOCLK cycles. Due to the averaging operation of the FIFO, the number of parity bytes transferred can vary slightly. The PDOCLK signal runs continuously and is not affected by a reset. In parallel output format, it has a frequency of 3 MHz.

When the TDA8961 is trying to acquire a channel, the PDOERR signal goes HIGH (I²C-bus bit FPBP = 1). If this occurs, the PDOVAL signal stays LOW.

SERIAL OUTPUT FORMAT

Figure 6 shows the timing diagram for the serial output format. The LSB of the 8-bit PDO data bus is used to output the MPEG-2 transport stream packets.

The PDOSYNC signal indicates the occurrence of the sync byte in the packet and is only HIGH during 8 PDOCLK cycles. The polarity of the PDOVAL and PDOERR signals is programmable via I²C-bus bits FDVP and FPBP respectively; Fig.6 shows their default polarities.

The PDOVAL signal is active for the duration of the 188 bytes of the transport stream packet. When the 188 bytes have been transferred, the PDOVAL signal goes LOW for a period corresponding to the duration of the parity and field sync information. Figure 6 shows the PDOERR signal is HIGH for the whole packet length indicating that the packet contains errors. The PDOCLK signal has a frequency of 27 MHz.

Table 3 Transport stream interface outputs

All pins are 3-state outputs.

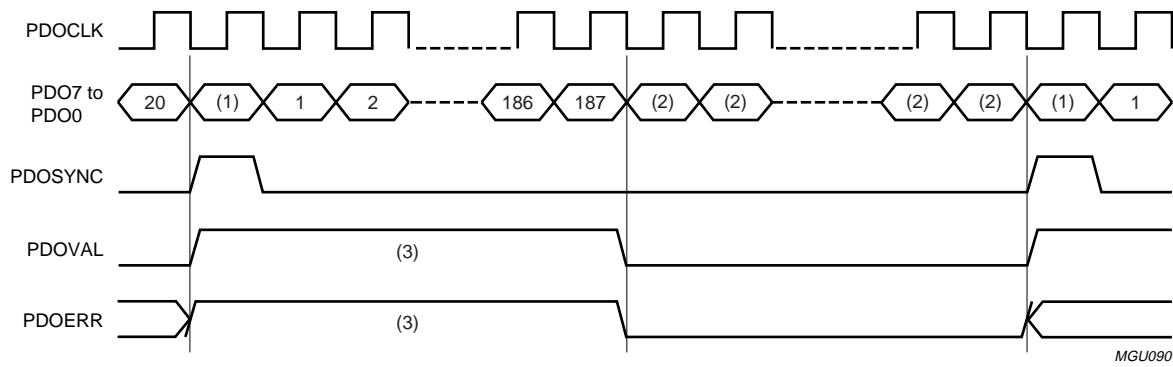
SYMBOL	FUNCTION
PDOCLK	clock signal for MPEG-2 packet data bytes (parallel and serial)
PDOVAL	indicates a valid data signal
PDO7 to PDO0	packet data bits 7 to 0 (8-bit wide output bus) ⁽¹⁾
PDOSYNC	indicates the start of a packet; goes HIGH at the start of a packet and stays HIGH during the first byte, otherwise known as the sync byte
PDOERR	indicates packet error; goes HIGH (I ² C-bus bit FPBP = 1) for every packet (188 bytes) in which the Reed Solomon decoder found more errors than it could correct

Note

1. In serial output format, only pin PDO0 (LSB) is used to output the data.

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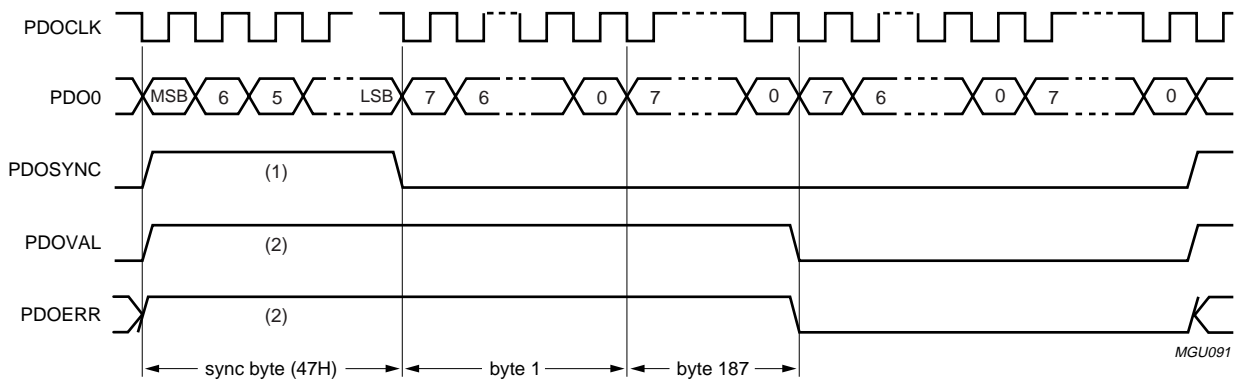
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MGU090

- (1) Sync byte.
- (2) Parity byte; contents set to 00H.
- (3) The polarity of these signals is programmable.

Fig.5 Parallel output format.



MGU091

- (1) Sync byte.
- (2) The polarity of these signals is programmable.

Fig.6 Serial output format.

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SYNC BYTE AND TRANSPORT STREAM ERROR INDICATOR

Figure 7 shows the structure of the so-called transport stream packet header of which only the first two bytes are significant to the TDA8961. The first byte in each header is the sync byte which must have the same value for all packets in accordance with the MPEG-2 standard specification. The TDA8961 sets the sync byte for each outgoing transport stream packet to 47H. The MSB of the second byte in the header is the transport_error_indicator bit. It is asserted when the Reed Solomon decoder is unable to correct all errors in the transport stream packet and indicates that the packet contains invalid data.

To perform bit error rate (BER) measurements, the external channel decoder generates a pseudo-random bit sequence (PRBS) in the last 187 bytes of each transport stream packet. The same PRBS signal is generated within the BER tester which compares it with the PRBS in each transport packet and records any mismatch as an error. It should be noted that during BER measurements, the TDA8961 must not be allowed to set the transport_error_indicator bit. This option is possible using I²C-bus bit FTEI (see Table 14). If bit FTEI is not set, the transport error interface bit is not allowed to indicate an error. If bit FTEI is set, the Reed Solomon decoder is allowed to set the transport_error_indicator bit according to the result of the error correction process. This is the default setting.

SERIAL TRANSPORT STREAM INPUT

The TDA8961 can be used with another channel decoder without requiring the transport stream outputs from either decoder to be selected by an external switch. This configuration requires the serial transport stream output from the other channel decoder to be connected to the serial transport stream input of the TDA8961. When the system requires the transport stream from the other channel decoder, the TDA8961 internally connects PDIERR to PDOERR, PDIVAL to PDOVAL, PDICLK to PDOCLK, PDISYNC to PDOSYNC and PDI0 to PDO0 allowing the transport stream from the other channel decoder to pass through the TDA8961. This pass-through mode is enabled by setting the value of I²C-bus TSMODE bits to 11 (see Table 14).

ITU656 BYPASS MODE

Figure 1 shows the tuner output connected to the TDA8980 which processes the IF and then outputs an 8-bit wide MPEG-2 transport stream to the TDA8961 where it is further processed before it is output to the video processor. This arrangement allows one system to receive both analog and digital broadcasts. When analog signals are received, the TDA8980 supplies an ITU656 format video stream to the TDA8961 input interface comprising pins ADIN9 to ADIN0 and ADCLK. The ITU656 format uses 8-bit data and a 27 MHz clock signal.

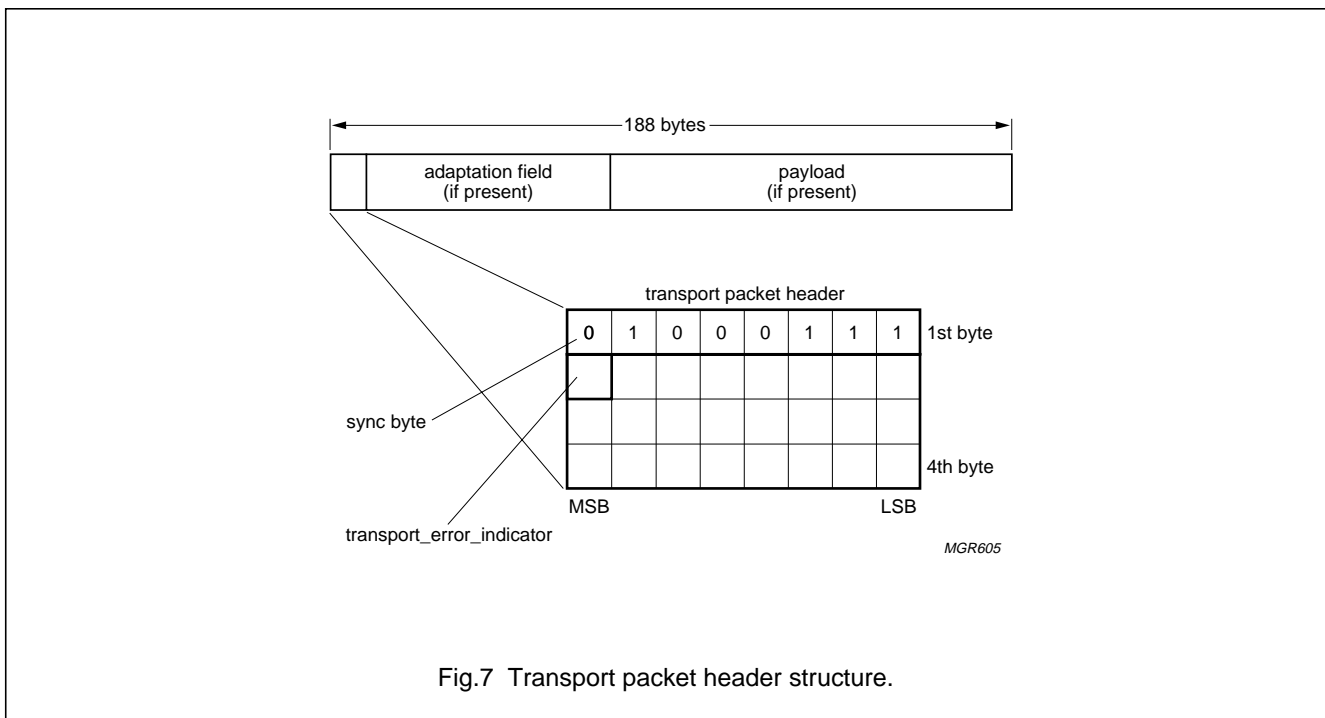


Fig.7 Transport packet header structure.

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Pins PDO0 to PDO7 and PDOCLK are normally part of the transport stream output interface. The signals to these pins are normally routed via an internal multiplexer. However, in the ITU656 bypass mode, these pins connect directly to the lower 8 bits of ADIN9 to ADIN0 and ADCLK. In this mode, PDOSYNC and PDOVAL are kept LOW and the polarity of PDOERR depends on the setting of I²C-bus bit FPBP. If required, these transport stream interface outputs can be forced to 3-state mode by making I²C-bus bit TSO = 0 (see Table 14).

ITU656 bypass mode is enabled by setting the I²C-bus TSMODE bits to 10.

SEGMENT ERROR COUNTER

The TDA8961 transport stream output interface is able to calculate the Segment Error, or packet error, Rate (SER) over a certain time period. The time period can be set to either 1, 4, 8 or 16 seconds by the I²C-bus bits SERTM (see Table 14). The IC counts any packet errors occurring in the set time period. At the end of the time period, the 16-bit value representing the counted number of packet errors can be read via I²C-bus bit SER (see Table 19).

After a reset, the register value is set to 12935 (3287H) which is equivalent to an infinite SER. The TDA8961 is able to automatically reset itself when the SER exceeds a preset threshold value. The SER threshold is a 14-bit value programmable in the range 3 to 13000 represented by I²C-bus bits SER_THRES (see Table 14).

It should be noted that the time period set by the SERTM bits should be long enough to allow this threshold to be reached. This reset function is enabled by setting I²C-bus bit SER_RST (see Table 14). The reset function is disabled by default.

Boundary scan interface

The TDA8961 TAP conforms to the IEEE 1149.1 (JTAG) standard. It is used for board-level testing and for internally testing integrated circuits. The JTAG standard defines the on-chip test logic which comprises an instruction register, a group of test data registers including a bypass register and a boundary scan register, four dedicated pins comprising the TAP, and a TAP controller.

EXTERNAL INTERFACE

The TAP external interface has five pins whose functions are described in Table 4.

Table 4 TAP external interface

SIGNAL	DESCRIPTION
TMS	Test mode select input
TCK	Test clock signal input
TDI	Test data input
TDO	Test data output
TRST	Test asynchronous reset input

I²C-bus interface

The I²C-bus interface writes control information to, and reads low-speed diagnostic information from the TDA8961. The key features of the I²C-bus interface are:

- I²C-bus data rate of up to 400 kbits/s
- Support for only 7-bit addressing and the ability to externally modify the slave address.

A typical system using the I²C-bus interface is shown in Fig.8. The TDA8961 is acting as a slave and is connected to a master via the I²C-bus lines SCL and SDA. It should be noted that the SCL and SDA lines are connected to separate pull-up resistors.

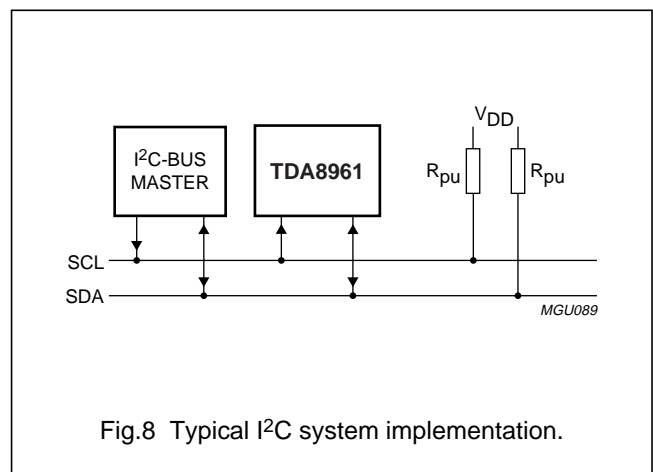


Fig.8 Typical I²C system implementation.

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EXTERNAL INTERFACE

The I²C-bus external interface has three pins whose functions are described in Table 5.

Table 5 I²C-bus external interface

SIGNAL	DESCRIPTION
SDA	I ² C-bus serial data input/output
SCL	I ² C-bus clock input
A0	I ² C-bus slave address input bit 0
A1	I ² C-bus slave address input bit 1

The TDA8961 I/O and I²C-bus signals range between ground and 3.3 V. Systems that have devices which operate at different supply voltages may require special circuitry to allow these devices to communicate and to be controlled. Circuit requirements are described in "Application Report AN97055" (issued Aug. 04, 1997) available from Philips Semiconductors.

ADDRESSING THE DEVICE

The TDA8961 must be addressed by its 7-bit (A6-A0) slave address sent via the system I²C-bus in accordance with the correct protocols, and with bit R/W set to either 1 (write data) or 0 (read data).

The slave address of the TDA8961 is given in Table 6. Bits A6 to A2 are preset, but bits A1 and A0 can be set via their corresponding external pins.

Table 6 TDA8961 slave address

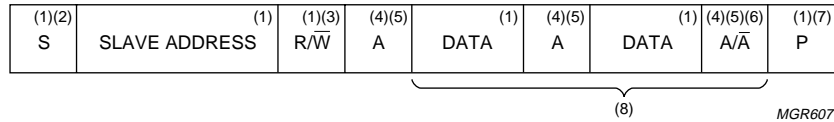
A6	A5	A4	A3	A2	A1	A0	R/W
0	0	0	1	1	A1	A0	0 = write 1 = read

A write operation is shown in Fig.9. The master transmitter sends a START condition followed by the 7-bit slave address which is followed by bit R/W set to 0. The slave receiver (TDA8961) responds by sending an acknowledge. The master then sends write data starting at address zero. If the master sends more than one byte of write data, the TDA8961 automatically increments to the next address. The TDA8961 sends an acknowledge after it receives each byte. If the TDA8961 does not acknowledge the data transfer and/or the master sends a STOP condition, the data transfer stops. It should be noted that the TDA8961 does not support I²C-bus sub-addressing. Therefore, each I²C-bus transfer starting with the transmission of the slave address and bit R/W, starts at address zero.

A read operation is shown in Fig.10. The master transmitter sends a START condition followed by the 7-bit slave address which is followed by bit R/W set to 1. The slave receiver (TDA8961) responds by sending an acknowledge and the value at address zero. The master responds by sending an acknowledge. If the master follows the acknowledge with a STOP condition, the data transfer stops, otherwise the slave is allowed to transfer more bytes. The slave TDA8961 automatically increments to the next address of read data to be sent to the master.

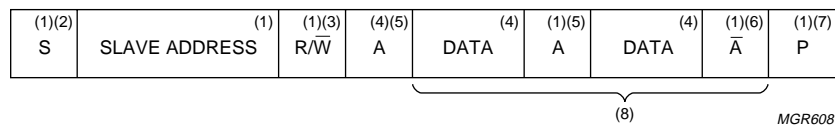
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- (1) From master to slave
- (2) S = START condition
- (3) Logic 0 (write)
- (4) From slave to master
- (5) A = acknowledge (SDA LOW)
- (6) \bar{A} = not acknowledge (SDA HIGH)
- (7) P = STOP condition
- (8) Data transferred (n bytes + acknowledge).

Fig.9 Master transmitter addressing a slave receiver with a 7-bit address (write mode).



- (1) From master to slave.
- (2) S = START condition.
- (3) Logic 1 (read).
- (4) From slave to master.
- (5) A = acknowledge (SDA LOW).
- (6) \bar{A} = not acknowledge (SDA HIGH).
- (7) P = STOP condition.
- (8) Data transferred (n bytes + acknowledge).

Fig.10 Master transmitter addressing a slave receiver with a 7-bit address (read mode).

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I²C-BUS REGISTER MAP
Table 7 I²C-bus write register overview

FUNCTION	ADDRESS (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
General settings	00			EQ_RST_DISABLE	EQ_FREEZE	EQ_RESET	BE_RESET	GNRL_RESET	INITIAL_RESET
	01					AGC_RESET	CR_RESET	TR_RESET	SR_RESET
	02								
	03								
	04								
SRC	05								AD_FMT
AGC/ Carrier recovery	06	AGC_SAMPLES				AGC_TR_LOW			
	07	AGC_DIR						CR_INV	
	08								
	09								
	0A								
	0B								
	0C								
	0D								
	0E								
	0F								
	10								
Equalizer	11	MSE_THR_1[15 to 8]							
	12	MSE_THR_1[7 to 0]							
	13	MSE_THR_2[15 to 8]							
	14	MSE_THR_2[7 to 0]							
	15								
	16								
	17								
	18								
	19								
	1A								

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FUNCTION	ADDRESS (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
	1B								
	1C								
	1D								
	1E								
	1F								
	20								
	21								
	22								
	23								
	24								
	25								
	26								
	27								
	28								
	29								
	2A								
	2B								
	2C								
NTSC co-channel interference filter	2D						FLT_BYPASS		
	2E								
	2F								
Transport stream interface	30		FTEI	FPBP	FDVP	TSO	PMSM		
	31				SER_RST	TSMODE		SERTM	
	32	SER_THRES[13 to 8]							
	32	SER_THRES[7 to 0]							
	33								
	34								

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Table 8 General settings (write)

BIT NAME	BIT VALUE	DESCRIPTION
INITIAL_RESET	0	normal operation (default)
	1	initial reset; note 1
GNRL_RESET	0	normal operation (default)
	1	general reset; note 2
BE_RESET	0	normal operation (default)
	1	backend reset
EQ_RESET	0	normal operation (default)
	1	equalizer reset
EQ_FREEZE	0	normal operation (default)
	1	equalizer adaptation freeze
EQ_RST_DISABLE	0	normal operation (default)
	1	equalizer reset disable
FE_RST_DISABLE	0	normal operation (default)
	1	front-end reset disable
SR_RESET	0	normal operation (default)
	1	reset sync recovery section
AGC_RESET	0	normal operation (default)
	1	reset input AGC
TR_RESET	0	normal operation (default)
	1	reset the timing recovery
CR_RESET	0	normal operation (default)
	1	carrier recovery reset enable

Notes

1. Operating modes and control parameters of all sections in the TDA8961 are not affected.
2. Operating modes and control parameters of all sections in the TDA8961 are reset to their initial values.

Table 9 Sample rate converter settings (write)

BIT NAME	BIT VALUE	DESCRIPTION
AD_FMT	0	two's complement
	1	binary (default)

Table 10 AGC settings (write)

BIT NAME	BIT VALUE	DESCRIPTION
AGC_SAMPLES	0	average over 64 samples (default)
	1	average over 256 samples
AGC_DIR	0	AGC operation compatible with TDA8980 (default)
	1	AGC operation compatible with TDA9819/9829
AGC_TR_LOW	–	AGC threshold value

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Table 11 Carrier recovery settings (write)

BIT NAME	BIT VALUE	DESCRIPTION
CR_INV	0	selects non-inverted spectrum; carrier at lower band-edge
	1	selects inverted spectrum; carrier at higher band-edge (default)

Table 12 Equalizer settings (write)

BIT NAME	BIT VALUE	DESCRIPTION
MSE_THR_1	–	MSE loss-of-convergence threshold value 1
MSE_THR_2	–	MSE loss-of-convergence threshold value 2

Table 13 NTSC co-channel interference filter settings (write)

BIT NAME	BIT VALUE	DESCRIPTION
FLT_BYPASS	0	normal operation (default)
	1	bypass NTSC co-channel interference filter

Table 14 Transport stream interface settings (write)

BIT NAME	BIT VALUE	DESCRIPTION
PMSM	0	parallel format (default)
	1	serial format
TSO	0	transport stream outputs in 3-state mode
	1	transport stream outputs active (default)
FDVP	0	polarity of PDOVAL is LOW during the packet length of 188 data bytes
	1	polarity of PDOVAL is HIGH during the packet length of 188 data bytes (default)
FPBP	0	polarity of PDOERR goes LOW if block cannot be corrected
	1	polarity of PDOERR goes HIGH if block cannot be corrected (default)
FTEI	0	transport_error_indicator bit is not allowed to indicate any errors detected in the transport stream
	1	transport_error_indicator bit is allowed to indicate errors in the transport stream which could not be corrected by the Reed Solomon decoder (default)
TSMODE	00	normal operation (default)
	01	reserved
	10	ITU656 bypass mode
	11	serialized transport input (pass-through mode)
SERTM	00	SER is calculated over a 1 second period (default)
	01	SER is calculated over a 4 second period
	10	SER is calculated over a 8 second period
	11	SER is calculated over a 16 second period
SER_THRES		SER threshold value (used if SER_RST is set to 1)
SER_RST	0	normal operation (default)
	1	TDA8961 is reset when the SER exceeds 2.5

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Table 15 I²C-bus read registers overview

FUNCTION	ADDRESS (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
Basic operation	00						LOCK_INDICATOR	STATE	
Carrier recovery	01	CR_OFFSET[7 to 0]							
	02								
	03								
Equalizer	04	MSE[15 to 8]							
	05	MSE[7 to 0]							
	06								
	07								
	08								
	09								
	0A								
Transport stream interface	0B	SER[15 to 8]							
	0C	SER[7 to 0]							
IC version ⁽¹⁾	0D	TYPE[3 to 0]				VERSION[3 to 0]			

Note

1. This register allows the type and version of the TDA8961 to be read by the controlling host. The TYPE[3 to 0] field contains 1H corresponding to the TDA8961. The VERSION[3 to 0] field contains EH corresponding to the TDA8961 version N1E. Philips Semiconductors reserves the right to change the values in this register for future versions of the TDA8961.

Table 16 General (read)

BIT NAME	BIT VALUE	DESCRIPTION
STATE	01	state 1 (channel acquisition)
	10	state 2 (equalizer training)
	11	state 3 (normal operation)
LOCK_INDICATOR	01	channel acquisition: no synchronization; equalization locked
	10	equalizer training: synchronization locked; no equalization
	11	normal operation: synchronization locked; equalization locked

Table 17 Carrier recovery (read)

BIT NAME	BIT VALUE	DESCRIPTION
CR_OFFSET	–	Carrier recovery offset value

Table 18 Equalizer (read)

BIT NAME	BIT VALUE	DESCRIPTION
MSE	–	Equalizer mean square error value

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Table 19 Transport stream interface (read)

BIT NAME	BIT VALUE	DESCRIPTION
SER	–	segment error rate value

Table 20 TDA8961 version (read)

BIT NAME	BIT VALUE	DESCRIPTION
TYPE	0001	1H = TDA8961
VERSION	1110	EH = TDA8961 version N1E

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		3.0	3.6	V
V_I	input voltage on any pin with respect to ground (V_{SS})		-0.5	$V_{DD} + 0.5$	V
I_I	DC current into any input		–	tbf	mA
I_O	DC current out of any output		–	tbf	mA
T_j	junction temperature		0	125	°C
T_{stg}	storage temperature		–	–	°C
T_{amb}	ambient temperature		-20	+70	°C
P_{tot}	total power dissipation		–	–	W
V_{es}	electrostatic handling	note 1	±2000	±4000	V
		note 2	±200	±400	V

Notes

- Human body model: 2000 V (typical); C = 100 pF; R = 1.5 kΩ; 3 zaps positive and 3 zaps negative.
- Machine model: 200 V (typical); C = 200 pF; L = 0.5 μH; R = 10 Ω; 3 zaps positive and 3 zaps negative.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	43	K/W

QUALITY SPECIFICATION

In accordance with quality specification: "SNW-FQ-611W".

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DC CHARACTERISTICS

$V_{DD} = 3.3\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	3.3	3.6	V
I_{DD}	supply current		–	390	–	mA
Inputs						
V_{IL}	LOW-level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH-level input voltage		2.0	–	–	V
I_{LI}	input leakage current		–	–	1	μA
C_i	input capacitance		–	–	25	pF
Outputs						
V_{OL}	LOW-level output voltage		–	–	$0.4V_{DD}$	V
V_{OH}	HIGH-level input voltage		$0.85V_{DD}$	–	–	V
I_{OL}	LOW-level output current		–	–	4	mA
3-state outputs (pins AGCOUT, PDO7 to 0, PDOCLK, PDOSYNC, PDOVAL and PDOERR)						
$I_{O(Z)}$	high-impedance output current		–	–	1	μA
$C_{O(Z)}$	high-impedance output capacitance		–	–	25	pF
I²C-bus (pins SDA and SCL)						
V_{IL}	LOW-level input voltage		–0.5	–	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.5$	V
V_{OL}	LOW-level output voltage		0	–	0.4	V
V_{OH}	HIGH-level output voltage	note 2	–	–	V_{DD}	V
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	–	–	mA
I_L	leakage current	$V_I = V_{SS}$ or V_{DD}	–	–	± 10	μA
C_i	input capacitance	$V_I = V_{SS}$	–	–	8	pF

Notes

- All supply connections must be made to the same external power supply unit.
- Open drain output, determined by V_{DD} via an external pull-up resistor.

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AC CHARACTERISTICS

$V_{DD} = 3.3\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock (pin XTALI)						
$f_{clk(sys)}$	system clock frequency	note 1	–	12	–	MHz
$\delta_{clk(sys)}$	system clock duty factor	note 1	–	50	–	%
A/D interface (pins ADIN[9 to 0] and ADCLK); see Fig.11						
$t_{su(A/D)}$	A/D interface set-up time		5	–	–	ns
$t_{h(A/D)}$	A/D interface hold time		5	–	–	ns
$T_{cy(ADCLK)}$	ADCLK cycle time		27.8	–	–	ns
Transport stream interface (pins PDOCLK, PDO[7 to 0], PDOSYNC, PDOERR and PDOVAL)						
$t_{PDOCLKL(par)}$	transport stream interface PDOCLK LOW time; parallel format	notes 2 and 3	166.7	–	–	ns
$t_{PDOCLKH(par)}$	transport stream interface PDOCLK HIGH time; parallel format	notes 2 and 3	166.7	–	–	ns
$T_{cy(PDOCLK)(par)}$	transport stream interface PDOCLK cycle time; parallel format	notes 2 and 3	333.3	–	–	ns
$t_{PDOVALH(par)}$	transport stream interface PDOVAL HIGH time; parallel format	notes 3 and 4	62666.7	–	–	ns
$t_{PDOVALL(par)}$	transport stream interface PDOVAL LOW time; parallel format	note 3	–	–	–	ns
$ t_{d(o)(par)} $	delay between transport stream interface outputs PDO to PDOVAL, PDOERR and PDOSYNC; parallel format	note 3	0	–	–	ns
$t_{PDOCLKL(ser)}$	transport stream interface PDOCLK LOW time; serial format	notes 5 and 6	18.5	–	–	ns
$t_{PDOCLKH(ser)}$	transport stream interface PDOCLK HIGH time; serial format	notes 5 and 6	18.5	–	–	ns
$T_{cy(PDOCLK)(ser)}$	transport stream interface PDOCLK cycle time; serial format	notes 5 and 6	37.0	–	–	ns
$t_{PDOSYNCH(ser)}$	transport stream interface PDOSYNC HIGH time; serial format	note 5	296.3	–	–	ns
$t_{PDOVALH(ser)}$	transport stream interface PDOVAL HIGH; serial format	notes 5 and 7	55703.7	–	–	ns
$t_{PDOVALL(ser)}$	transport stream interface PDOVAL LOW; serial format	note 5	–	–	–	ns
$ t_{d(o)(ser)} $	delay between transport stream interface outputs PDO to PDOVAL, PDOERR and PDOSYNC; serial format	note 5	0	–	–	ns

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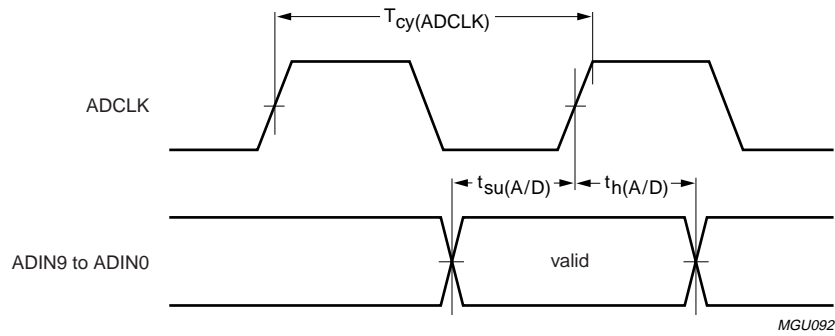
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus (pins SDA and SCL); see Fig.15						
f _{SCL}	SCL clock frequency		0	–	400	kHz
t _{BUF}	bus free time between a STOP and START condition		1.3	–	–	ms
t _{HD;STA}	hold time for a repeated START condition; after this period the first clock pulse is generated		0.6	–	–	ms
t _{LOW}	LOW period of the SCL clock		1.3	–	–	ms
t _{HIGH}	HIGH period of the SCL clock		0.6	–	–	ms
t _{SU;STA}	set-up time for a repeated START condition		0.6	–	–	ms
t _{SU;STO}	set-up time for STOP condition		0.6	–	–	ms
t _{HD;DAT}	data hold time		0	–	0.9	ms
t _{SU;DAT}	data set-up time		100	–	–	ns
t _{SP}	pulse width of spikes which must be suppressed by the input filter		tbf	–	tbf	ns
t _r	rise time of both SDA and SCL signals	note 8	20 + 0.1C _b	–	300	ns
t _f	fall time of both SDA and SCL signals		20 + 0.1C _b	–	300	ns
C _b	capacitive load for each bus line		–	–	400	pF
JTAG interface (pins TDO, TDI, TCK, TMS and TRST); see Fig.14						
t _{d(TCK-TDO)}	pin TCK to TDO valid delay		2	–	10	ns
t _{su(i)(TCK)}	input set-up time to TCK		10	–	–	ns
t _{h(i)(TCK)}	input hold time from TCK		2	–	–	ns
Reset (pin RST_AN)						
t _{su(PO)L}	power-on set-up time LOW		23	–	–	ns

Notes

1. The system clock signal is supplied by either an external 12 MHz crystal or another device such as the TDA8980 generating a stable 12 MHz clock signal.
2. When used for parallel format, the frequency of PDOCLK is 3 MHz.
3. See the timing measurement conditions in Fig.12.
4. This is calculated by multiplying 188 bytes (the length of a packet) by the PDOCLK clock cycle period.
5. See the timing measurement conditions in Fig.13.
6. When used for serial format, the frequency of PDOCLK is 27 MHz.
7. This is calculated by multiplying 188 bytes (the length of a packet) by the PDOCLK clock cycle period, multiplied by 8.
8. C_b = total capacitance of one bus line in pF.

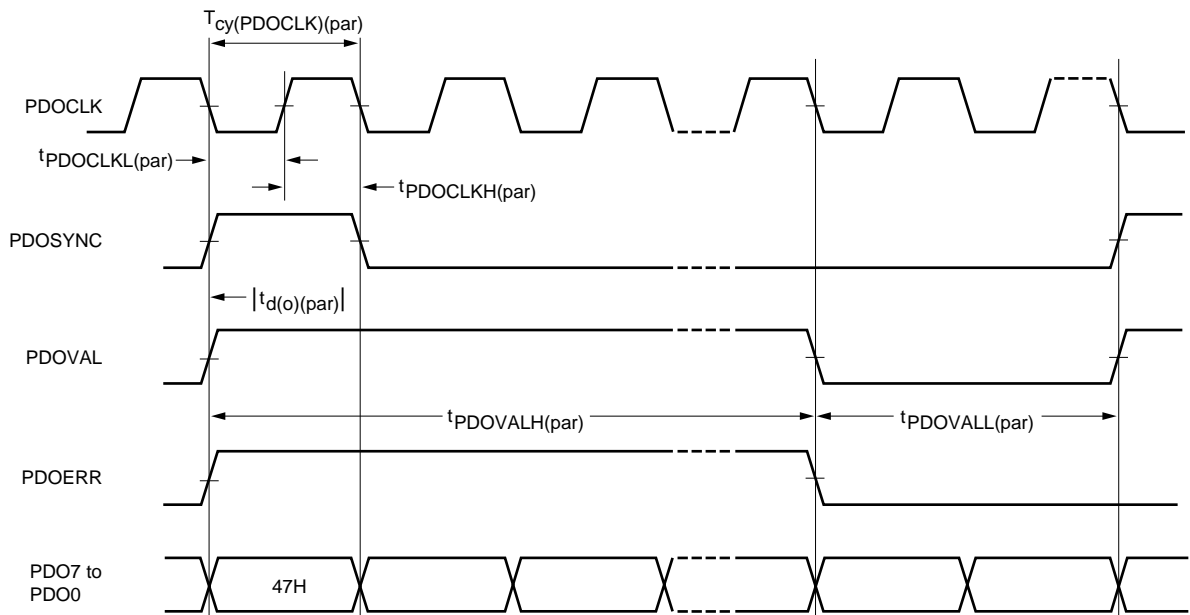
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MGU092

Fig.11 A/D interface timing.



MGU093

Fig.12 Transport stream interface timing (parallel output format).

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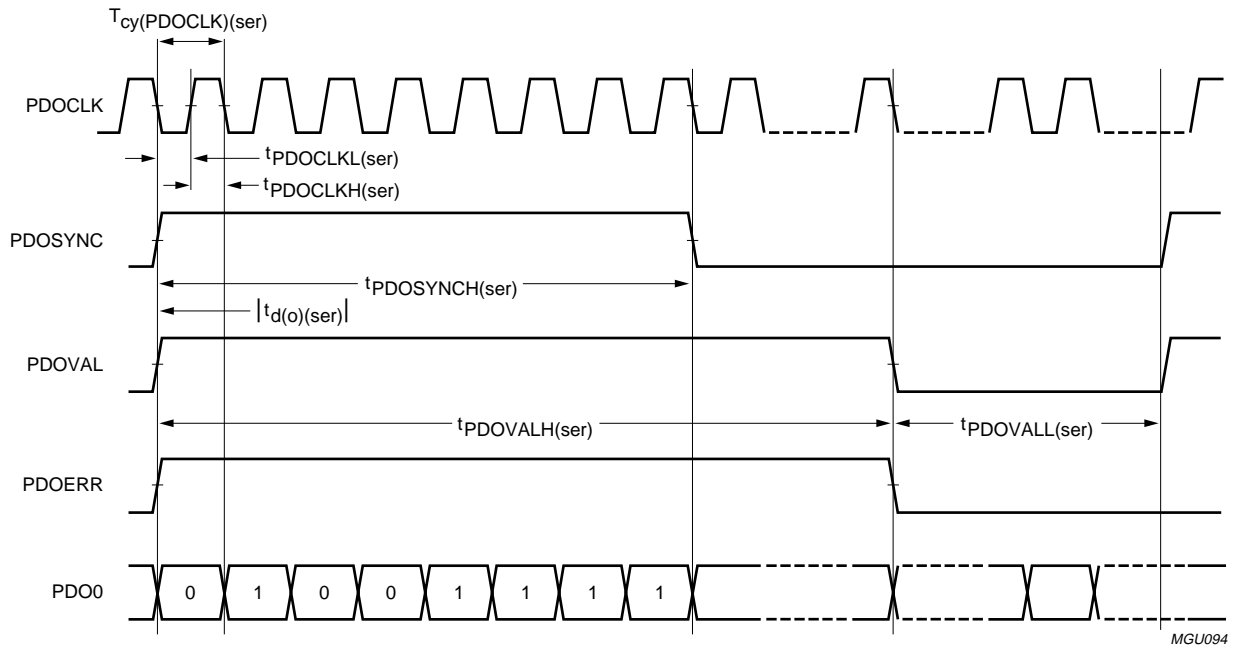


Fig.13 Transport stream interface timing (serial output format).

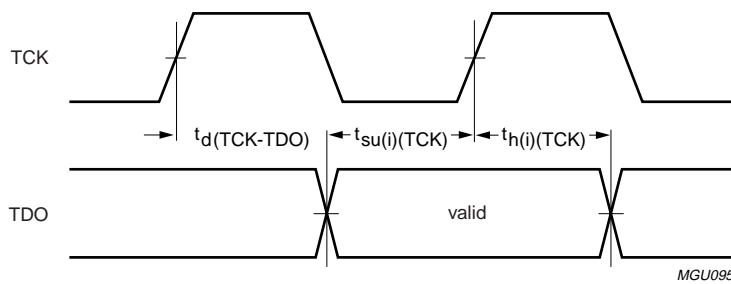
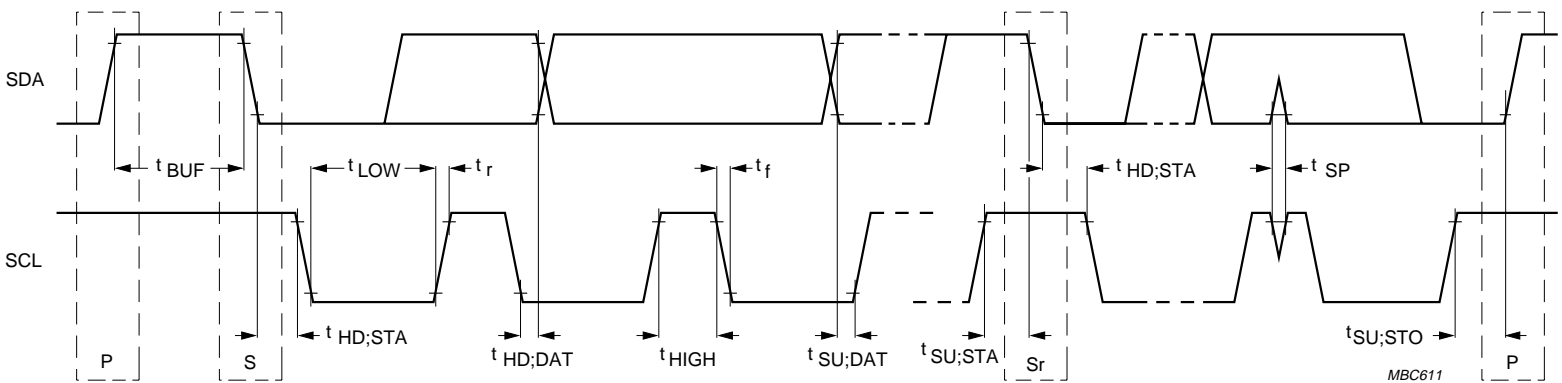


Fig.14 JTAG I/O timing.

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P = STOP condition.
S = START condition.
Sr = repeated START condition.

Fig.15 I²C-bus timing diagram.

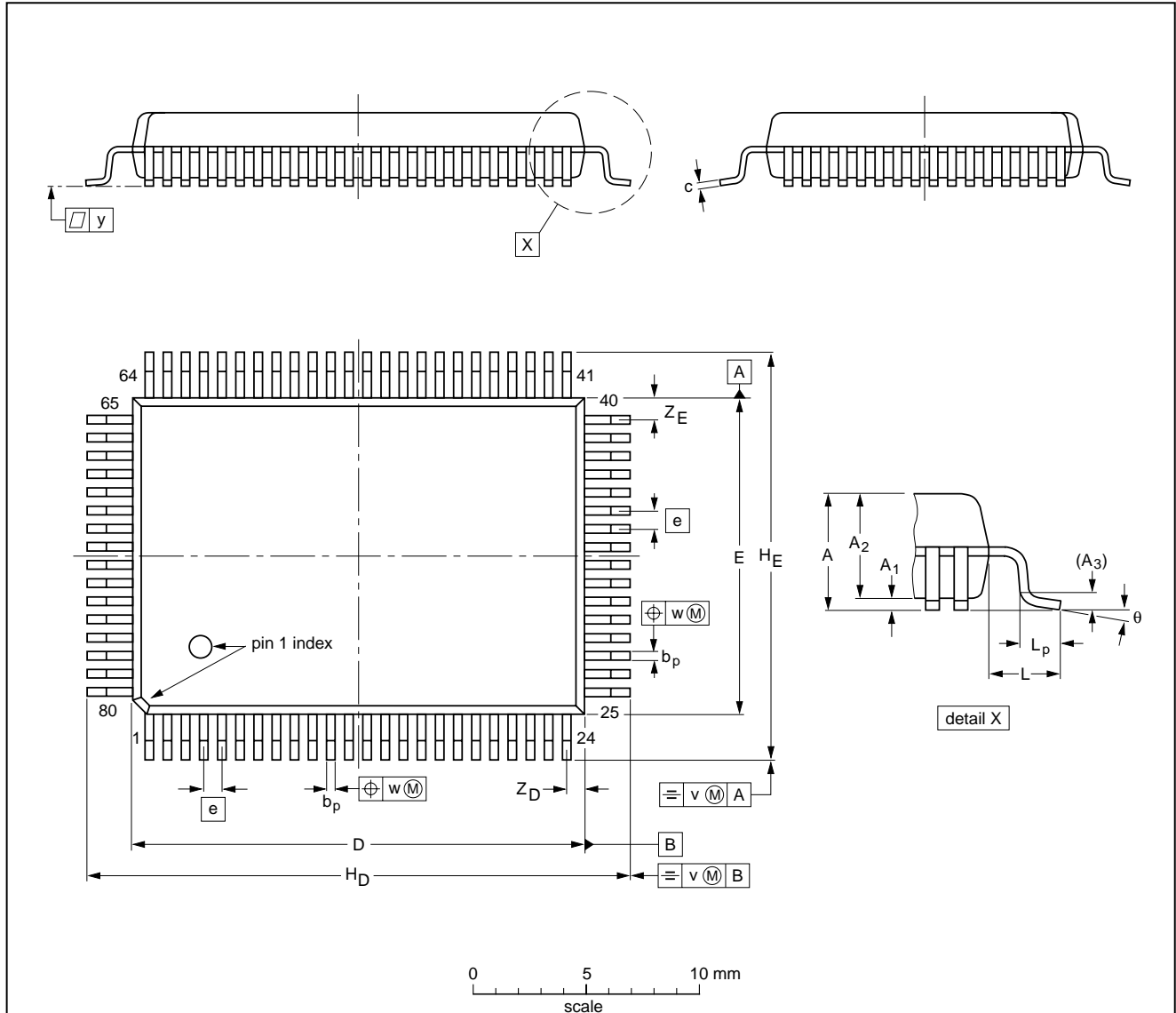
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PACKAGE OUTLINE

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm

SOT318-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	3.2	0.25 0.05	2.90 2.65	0.25	0.45 0.30	0.25 0.14	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-2		MO-112				97-08-04 99-12-27

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS ⁽¹⁾
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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