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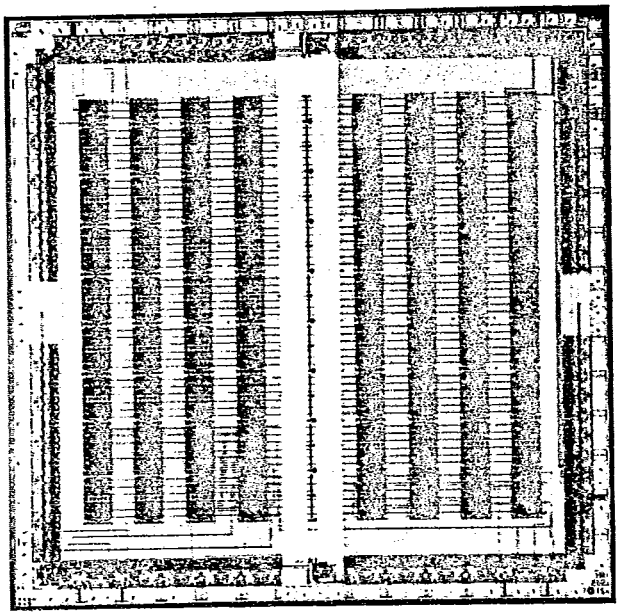
THOMSON SEMICONDUCTEURS

TSC06
TSC12
TSC17

T-42-11-15

ADVANCE INFORMATION



BIPOLAR MACRO ARRAYS

Two standard electrical interface environments have evolved for digital integrated circuits, TTL and ECL. TTL compatible products such as LS, FAST, CMOS, NMOS, etc., represent the majority of digital ICs in use today. However, ECL products are necessary for applications requiring the highest available switching performance. Interfacing these two incompatible environments has usually required dedicated level translation circuits as few logic ICs can operate in both environments simultaneously.

The TSC Bipolar MACRO ARRAYS exceed present offerings in compatibility, user friendliness, flexibility and performance. One comprehensive macro library and one set of industry standard CAD software tools support the entire family of arrays. The user may input a design in a variety of ways, from submitting a logic schematic to inputting a complete CAD design file via a remote terminal. Each array can be configured to operate in a TTL and/or ECL environment and all array pins can be configured as inputs or outputs providing maximum design flexibility. The internal macro logic is implemented with high performance series gated ECL circuits. These MACRO ARRAY features give the user a custom design solution with lower risk, lower cost and shorter design cycle than a full custom integrated circuit.

- TSC06 : 748 gates, TSC12 : 1338 gates, TSC17 : 1712 gates
- Typical internal equivalent gate delay : 0.8 ns
- Typical ECL I/O buffer pair delay : 2.0 ns
- Typical TTL I/O buffer pair delay : 8.0 ns
- All I/O cells may be configured as input, output, or bidirectional pins.
- True 10K ECL compatible interface
- Optional 2 kΩ on-chip pulldown resistor for direct wiring of ECL.
- True LS-TTL compatible interface including 8 mA or 16 mA outputs and three-state or open collector output options.
- High performance, oxide-isolated, 2 layer metalization process technology.
- Temperature range : −55 to + 125°C
- Identical macro library for all three arrays.
- Complete set of VAX/VMS and workstation CAD tools for the entire family.
- Commercial, Industrial and full MIL-STD-883C level B screening available.

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THOMSON COMPONENTS

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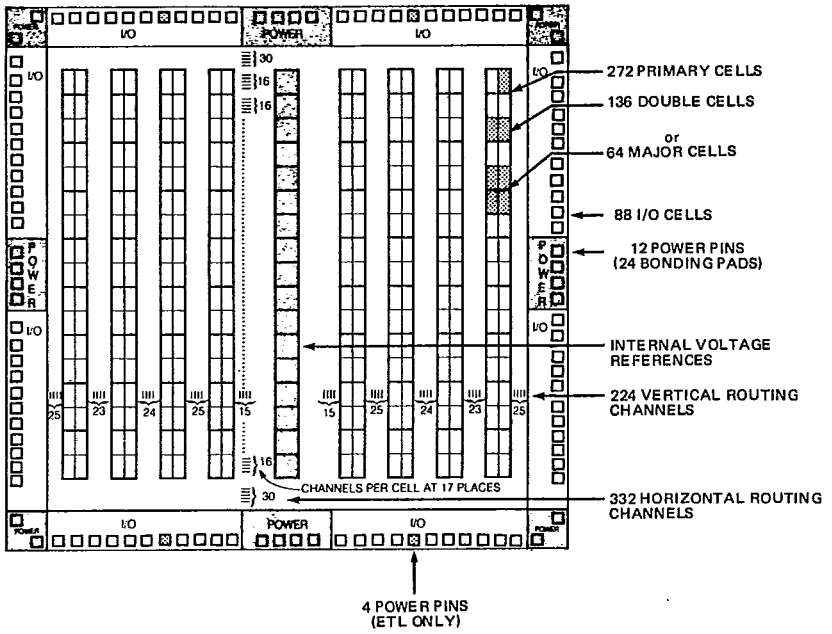
FIGURE 1



INTERFACE MODE

Each bipolar MACRO ARRAY can be designed to operate in either a TTL, ECL or combined TTL and ECL interface environment. Prior to generating a custom logic design on the arrays, the user selects the array size and the array interface mode. Selection of the interface mode determines the fixed metal pattern for all power busing and the assignment of supply voltages to package pins. The mode selection also determines which group of I/O Macros will be used. Selection of macros for primary, double, or major macro functions is not affected by the interface mode or array size. The ECL and TTL modes do not restrict the number of I/O's available or location. The ETL mode is restricted in that ECL I/O's and TTL I/O's are available on two sides respectively. In addition, four ECL I/O locations are eliminated because additional power pins are necessary. The number of available I/O's for each mode is listed below.

POWER

The power supply pins are located at the corners and centers of array periphery. Each power pin ties to two adjacent building pads. The number and assignment of supply voltages to the power pins depends on the interface mode. The power buses for internal array and I/O buffers are separated. This allows for improved array and system performance. The internal ARRAY is referenced to ECL power supply levels in both the ECL and DUAL interface mode and to TTL power levels in the TTL interface mode.

Interface mode	Number of I/O's		
	TSC06	TSC12	TSC17
ECL	52	72	88
TTL	52	72	88
DUAL		ECL 32 TTL 30	ECL 40 TTL 44

Mode	4–5.2 V	0 V	5.0 V
ECL	X	X	
TTL		X	X
DUAL	X	X	X

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THE TSC BIPOLAR MACRO ARRAYS

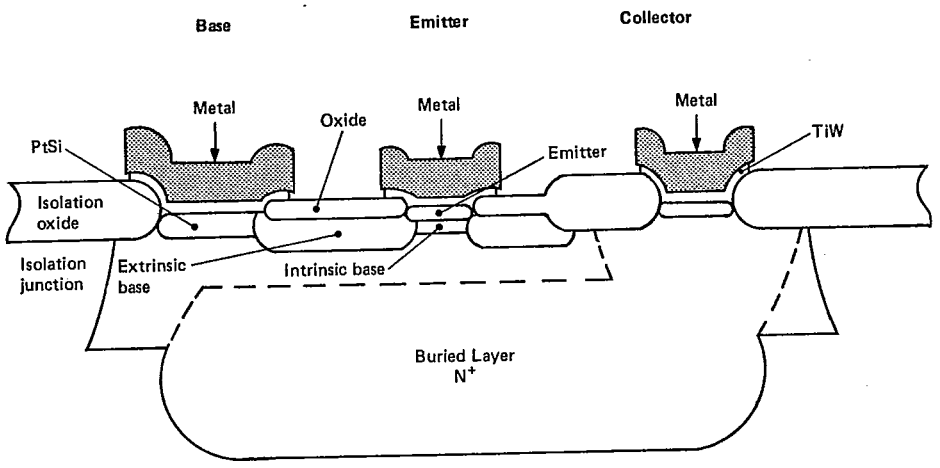
	TSC06	TSC12	TSC17
Primary cells	108	210	272
I/O cells	52	72	88
Max. Equivalent Gates (1)	748	1338	1712
Typical Array power	750 mW	1.5 mW	2.0 mW

(1) - Assumes that all array cells are utilized at an average of 5 equivalent, 2-input gates per primary cell and 4 equivalent gates per I/O cell.

PROCESS DESCRIPTION

The TSC bipolar MACRO ARRAYS are fabricated on THOMSON SEMICONDUCTEURS' HBIP2 high performance two metal process.

This technology provides improved speed power products over convention junction isolated product.

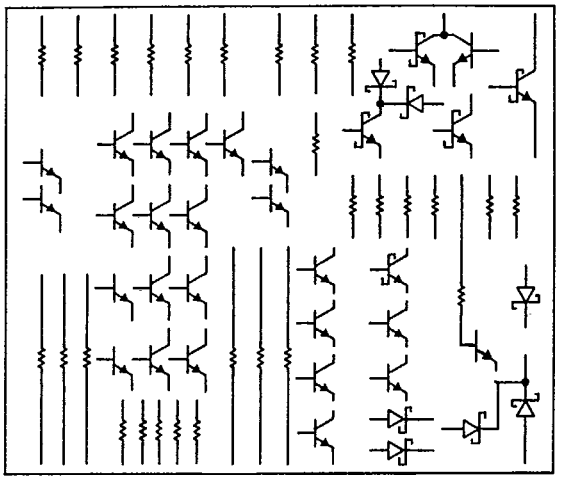


I/O MACRO CELLS

I/O macro cells are located around the periphery of the array. Each I/O cell has the required components to operate in either a ECL or TTL mode as an input or output. The I/O cell contains 28 transistors, 7 schottky diodes and 28 resistors. A schematic representation is shown in figure 2.

All signals to and from array must pass through an I/O cell for level translation and/or current drive capability. Each I/O location has a fixed bonding pad location allowing for single input and single output macros.

FIGURE 2



PRIMARY CELLS

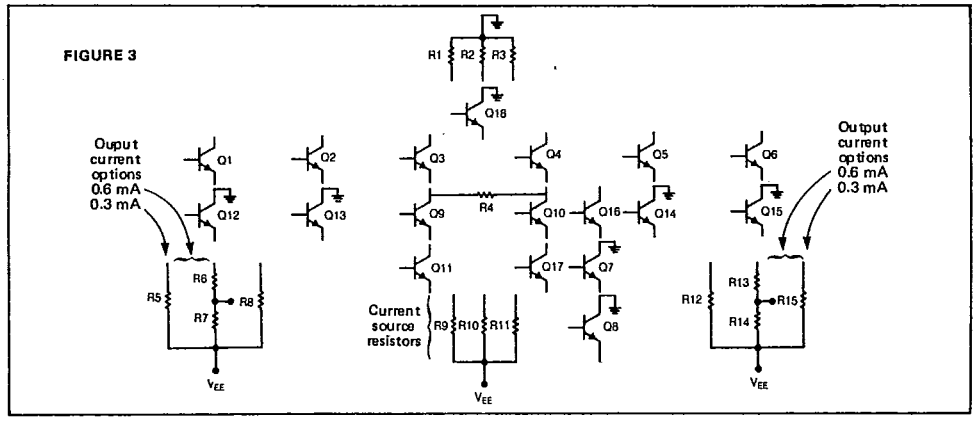
A primary cell is the basic logic building block in the internal array. Each primary cell contains 18 transistors and 15 resistors. A schematic representation is shown in figure 3. Logic functions are formed using first level metal interconnects. To incorporate more complex functions, adjacent cells are combined to form double cell or four symmetrical cells are combined to form a major cell.

All internal logic is configured with ECL logic structures using series gating. Other internal signals use one set of ECL logic levels. Some competing products use upper and lower logic levels which increases design risk.

The primary cell inputs can only be driven by an I/O cell or another primary cell and not from the external environment. Three drive levels are available from each primary output by paralleling resistors on the emitter follower : 0.300 mA and 0.600 mA. The outputs cannot be used as off-chip output drivers.

This primary cell has an increased component density over competing array product. This allows for more efficient utilisation of available cell locations.

FIGURE 3



PRIMARY CELL

CELL LIBRARY

I/O MACROS : to assist the designer in secreting the appropriate I/O macro, they have been given symbolic names which indicates logic function, fanout capability and interface mode :

First character : I for Input macro
O for Ouput macro
Second character : A number indicating logic function
Third character : Fanout capability (N-Normal, F-Fast)
Fourth character : Interface mode
(E-ECL, T-TTL, D-DUAL)

I/O macro	Macro description
I 1ND	TTL input LATCH
I 1NE	ECL input LATCH
I 1NT	TTL input LATCH
I 2ND	TTL input buffer/converter
I 2NE	ECL input buffer/converter
I 2NT	TTL input buffer/converter
I 3ND	TTL chip enable
I 3NT	TTL chip enable
I 4NE	ECL latch clock input
O INT	TTL bidirectional buffer
O 2ND	TTL output with LATCH
O 2NE	ECL output with LATCH
O 2NT	TTL output with LATCH
O 3ND	3 input OR with TTL output
O 3NE	3 input OR with ECL output
O 3NT	3 input OR with TTL output
O 4ND	3 input NOR with TTL output
O 4NE	4 input NOR with ECL output
O 4NT	4 input NOR with ECL output
O 5ND	2 input AND with TTL output
O 5NE	2 input AND with ECL output
O 5NT	2 input AND with TTL output
O 6ND	2 input NAND with TTL output
O 6NE	2 input NAND with ECL output
O 6NT	2 input NAND with TTL output

INTERNAL MACROS : The designer uses the same internal macros regardless of the interface mode. These macros have mnemonic names to assist the designer in the selection of macro function.

First character : define the logic function
AR - combined AND/OR
D - D Flip Flop
L - Latch
M - Mux
N - Inverter
R - OR
X - Exclusive OR
Second character : Inverter specifics about logic function.
Last character : Defines fanout ability.
N-Fanout up to 6 (0.3 mA)
F-Fanout up to 10 (0.6 mA).

ogic macro	Macro description
AR1N	3 input OR-AND
AR2N	2 wide 3-input active low AND-OR/NOR
AR3N	3 input OR-AND/NAND with 3 active low enable
AR4N	3 wide active low AND-OR/NOR
F1N	Positive edge D flip-flop with asynchronous reset
F2N	Positive edge D flip-flop with asynchronous set and reset
L1N	Negative clock transparent LATCH with reset
L2N	Positive clock transparent LATCH with reset
L3N	2 bit LATCH with asynchronous reset and active low enable
M1N	2 to 1 MUX with OR select and active low enable
M2N	2 to 1 MUX with OR select and active high enable
M3N	4 to 1 MUX
M4N	4 to 1 MUX with active low enable
M5N	DUAL 2 to 1 MUX
M7N	DUAL 2 to 1 MUX with common select
NR2N	4 input OR/NOR
NR2N	DUAL 3 input OR - 3 input NOR
NR4N	6 input OR/NOR
NR5N	DUAL 3 input NOR with 2 common input
NR7N	7 input OR-NOR
NR8N	12 input OR-NOR
R1N	DUAL 3 input OR
R2N	DUAL 3 input OR with 2 common inputs
X1N	3 input OR-exclusive OR/NOR
X2N	2 input OR-exclusive OR with active low
X3N	4 input ODD parity checker
X4N	4 input exclusive OR/NOR
X5N	2 input NOR-exclusive OR/NOR.

A.C. PERFORMANCE

The cell library provides the maximum delay time for worst case technology, 25°C ambient and $V_{CC} = -5.2$ V. Worst case performance can be calculated using the formula provided in the design manual or the CAD system.
The CAD system provides the designer with both a prerouting and routed A.C performance simulation. The prerouting simulation is based upon statistical loading estimates based upon fanout.
The designer can also calculate the typical and best case performance by multiplying worst case performance by 0.5 and 0.7 respectively.
The designer will be able to select the speed power products of an internal macro. Each function, where possible, will be released using a 0.300 mA and 0.600 mA source current. By doubling the power, the designer is able to obtain a 30 % performance improvement.
Table 1 provides a summary of typical performances for selected internal and I/O logic functions. The internal macros performance does not vary based upon interface mode.

TABLE 1 – TYPICAL TIMING DELAYS

INTERNAL MACRO (1)	TYPICAL DELAY
3 Input gate	1.8 ns
3 Input AND/OR	2.0 ns
Flip-flop	2.7 ns
Latch	2.2 ns
Mux	2.0 ns
INPUT MACRO (1)	
Latch (ECL)	3.9 ns
Latch (TTL)	4.2 ns
Buffer (ECL)	2.2 ns
Buffer (TTL)	2.7 ns
OUTPUT MACRO (2)	
Latch (ECL)	3.5 ns
Latch (TTL)	8.4 ns
Buffer (ECL)	2.1 ns
Buffer (TTL)	8.1 ns

(1) FANOUT = 3, routing metal 2.5 mm
(2) ECL load 50 Ω to – 2 V,
TTL load = 300 Ω.

PACKAGING OPTIONS

Package Type	Leads	TSC06	TSC12	TSC17
Ceramic DIP	28	X		
	40	X	X	
	48	X	X	
	64	X	X	X
Plastic DIP	28	X		
	40	X		
	48	X		
	64	X		
Leadless Ceramic Chip Carrier	68	X	X	X
	84		X	X
Pin Grid Array	68	X	X	X
	84		X	X

Other packages available on request.

QUALITY LEVELS

In addition to the standard quality procedures for commercial grade product, THOMSON SEMICONDUCTEURS offers a variety of extended temperature ranges and high reliability screening levels for the TSC MACRO Arrays. All extended screening is performed at THOMSON SEMICONDUCTEURS' Military and Spatial Division facility in France, which is completely equipped with state-of-the-art assembly, electrical test and environmental stress equipment. The Military and Spatial Division is dedicated to performing quality control and reliability assurance for all THOMSON SEMICONDUCTEURS integrated circuits for military and space applications.

AVAILABLE SCREENING LEVELS

Level	Description
Standard	Commercial Temp. Range 0° to+ 70°C Industrial Temp. Range –40° to+ 85°C Military Temp. Range –55° to+ 125°C
D	Standard Level with Burn-in
B/B	Full MIL-STD-883C, Class B Screening
G/B	MIL-STD-883C Without Constant Acceleration or Temp. Test, PDA < 10 %.

CAD SYSTEM

All of the THOMSON SEMICONDUCTEURS Array Products are supported by a fully automated VAX/VMS based CAD System. The CAD System provides a complete set of industry standard design, layout and verification tools to ensure fast, error-free design of the TSC MACRO ARRAYS. The CAD System resides at THOMSON SEMICONDUCTEURS Design Center and is accessed with a Tektronix 4109 (or equivalent) graphics terminal.

The CAD System can also accept verified netlists from a variety of popular engineering workstations, including Daisy® , Valid® , Mentor®, and IBM PC-XT®- based workstations that are equipped with the TSC Series Macro library. The key components of the THOMSON SEMICONDUCTEURS CAD System are :

Schematic Capture	SDS®
Netlist Extraction	SDS®
Logic Simulation	HILO®
Timing Analysis	HILO®
Fault Grading	HILO®
Tester Program Interface	HILO®
Automatic Placement and Routing	GARDS®
Interactive Placement and Routing	GARDS®
Design Rule Checking	GARDS®
Automatic Mask Generation	GARDS®

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Design entry is easily accomplished with the SDS menu driven software and a graphics terminal (Tek 4109). The SDS generated logic schematic is converted to a netlist and checked for logic design rule violations (excessive fanout, for instance). The netlist is then automatically converted to HILO simulation format.

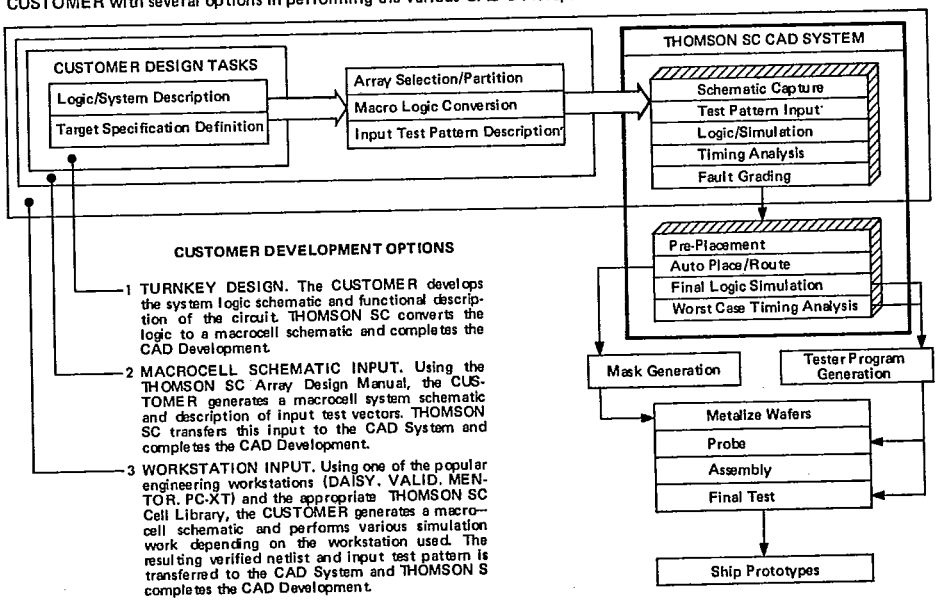
The HILO simulation program performs logic simulation based on the user defined input test pattern and timing analysis using pre-routing statistical load capacitances for delay calculations. HILO also can be used to perform fault grade analysis of the input test pattern.

The GARDS program is used to automatically place and route the array's cell logic as described in the SDS netlist. GARDS also has an interactive mode that allows cell or I/O preplacement and manual routing to optimize critical paths if necessary. After placement and routing is completed, HILO timing analysis can be performed again to determine worst case critical path delays using the actual interconnect length and fanout capacitances.

When the array design work is completed on the CAD System, the HILO simulation output is automatically converted to a tester program tape and the GARDS place and route file is converted to a graphics data base for mask generation. These two data bases are then sent to the factory for prototype generation.

DESIGN DEVELOPMENT PROCEDURE

The design of an array option is a joint development effort involving THOMSON SEMICONDUCTEURS and the CUSTOMER. THOMSON SEMICONDUCTEURS offers a very flexible interface to the CAD System, providing the CUSTOMER with several options in performing the various CAD Development Procedures as shown below :



CUSTOMER DEVELOPMENT OPTIONS

1 TURNKEY DESIGN. The CUSTOMER develops the system logic schematic and functional description of the circuit. THOMSON SC converts the logic to a macrocell schematic and completes the CAD Development.

2 MACROCELL SCHEMATIC INPUT. Using the THOMSON SC Array Design Manual, the CUSTOMER generates a macrocell system schematic and description of input test vectors. THOMSON SC transfers this input to the CAD System and completes the CAD Development.

3 WORKSTATION INPUT. Using one of the popular engineering workstations (DAISY, VALID, MENTOR, PC-XT) and the appropriate THOMSON SC Cell Library, the CUSTOMER generates a macrocell schematic and performs various simulation work depending on the workstation used. The resulting verified netlist and input test pattern is transferred to the CAD System and THOMSON S completes the CAD Development.