ANALOG DEVICES

High Speed 8-Bit Monolithic A/D Converter

AD9002

T-51-10-08

1.1 Scope.

This specification covers the requirements for an 8-bit, high speed, analog-to-digital converter. The AD9002 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the ECL compatible output latches.

1.2 Part Number.

The complete part number is as follows:

Device	Part Number
−1	AD9002S(X)/883B
−2	AD9002T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
E	E-28A	28-Contact LCC
Q	Q-28	28-Pin Ceramic DIP

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

Supply Voltage ($-V_S$)	−6.0 V
Power Dissipation	1.2 W
Digital Input Voltage	$-V_S$ to 0 V
Reference Input Voltage ($+V_{REF}$, $-V_{REF}$)[1]	−3.5 V to +0.1 V
Differential Reference Voltage	2.1 V
Reference Midpoint Current	±4 mA
Digital Output Current	20 mA
ENCODE to $\overline{\text{ENCODE}}$ Differential Voltage	4.0 V
Analog Input Voltage	$-V_S$ to +0.5 V
Junction Temperature[2]	+175°C
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range (Case)	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

NOTES
[1]$+V_{REF} \geq -V_{REF}$ under all circumstances.
[2]Maximum Junction temperature should not exceed +175°C.

1.5 Thermal Characteristics.

Thermal Resistance θ_{JA} = 56°C/W for Q-28
θ_{JC} = 20°C/W for Q-28
θ_{JA} = 69°C/W for E-28A
θ_{JC} = 23°C/W for E-28A

AD9002 – SPECIFICATIONS

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Test	Symbol	Device	Design Limits @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Sub Group 8	Sub Group 9	Test Conditions[1]	Units
Input Bias Current	I_B	All	100	100						A_{IN} = 0 V	µA max
			100		200					$-55°C \le T_A \le +125°C$ A_{IN} = 0 V	
Reference Ladder Resistance	R_R	All	64	64							Ω min
			110	110							Ω max
0 V Input Current	I_{IN}	All	300	300	300					$-55°C \le T_A \le +125°C$	µA max
High Level Output Voltage	V_{OH}	All	−1.1	−1.1	−1.1					See Note 2 $-55°C \le T_A \le +125°C$	V min
Low Level Output Voltage	V_{OL}	All	−1.5	−1.5	−1.5					See Note 2 $-55°C \le T_A \le +125°C$	V max
Negative Supply Current (−5.2 V)	$-I_{CC}$		175	175						A_{IN} = 0 V, See Note 4	mA max
					200					A_{IN} = 0 V, See Note 4 $-55°C \le T_A \le +125°C$	
Conversion Rate		All	125			125					MSPS min
Encode Pulse Width (Low)	t_{PW} (L)	All	1.5			1.5				See Note 3	ns min
Encode Pulse Width (High)	t_{PW} (H)	All	1.5			1.5				See Note 3	ns min
Signal-to-Noise Ratio	SNR	All	46			46				Encode Rate = 125 MSPS RMS Signal to RMS Noise	dB min
Differential Linearity	DNL	−1	0.75				0.75	1.0		$-55°C \le T_A \le +125°C$	LSB max
		−2	0.5				0.5	0.75		$-55°C \le T_A \le +125°C$	
Integral Linearity	INL	−1	1.0				1.0	1.2		$-55°C \le T_A \le +125°C$	LSB max
		−2	0.5				0.5	1.2		$-55°C \le T_A \le +125°C$	
Top of Reference Ladder		All	14				14	17		$-55°C \le T_A \le +125°C$	LSB max
Bottom of Reference Ladder		All	10				10	12		$-55°C \le T_A \le +125°C$	mV max
High Level Input Voltage	V_{IH}	All	−1.1				−1.1	−1.1		See Note 2 $-55°C \le T_A \le +125°C$	V min
Low Level Input Voltage	V_{IL}	All	−1.5				−1.5	−1.5		See Note 2 $-55°C \le T_A \le +125°C$	V max
High Level Input Current	I_{IH}	All	150				150	150		$-55°C \le T_A \le +125°C$	µA max
Low Level Input Current	I_{IL}	All	120				120	120		$-55°C \le T_A \le +125°C$	µA max
Power Supply Rejection	PSRR	All	1.5				1.5			Measured at −5.2 V ±5%	mV/V max

Table 1. (Continued on next page)

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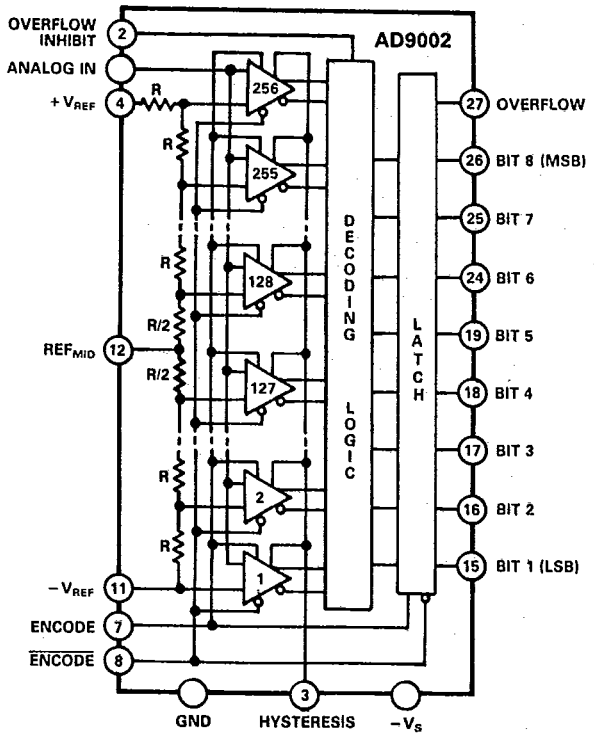
Test	Symbol	Device	Design Limits @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Sub Group 7	Sub Group 8	Sub Group 9	Test Conditions[1]	Units
Output Delay	t_{PD}	All	2.5						2.5	Measured from 50% Point of Rising ENCODE to 50% Point of LSB Transition; See Note 2	ns min
			5.5						5.5		ns max
Output Rise Time	t_R	All	3.0						3.0	Measured from 10% to 90% Points LSB Only; See Note 2	ns max
Output Fall Time	t_F	All	2.5						2.5	Measured from 10% to 90% Points LSB Only; See Note 2	ns max
In-Band Harmonics		All	48			48					dB min

NOTES
[1]V_{EE} = −5.2 V; $+V_{REF}$ = 0 V; $-V_{REF}$ = −2.0 V; digital outputs terminated to −2.0 V through 100 Ω or equivalent; T_A = +25°C, unless otherwise specified.
[2]Outputs terminated to −2.0 V through 100 Ω resistors or equivalent.
[3]ENCODE signal rise/fall times should be less than 10 ns for normal operation.
[4]Supply voltages should remain stable within ±5% for normal operation.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



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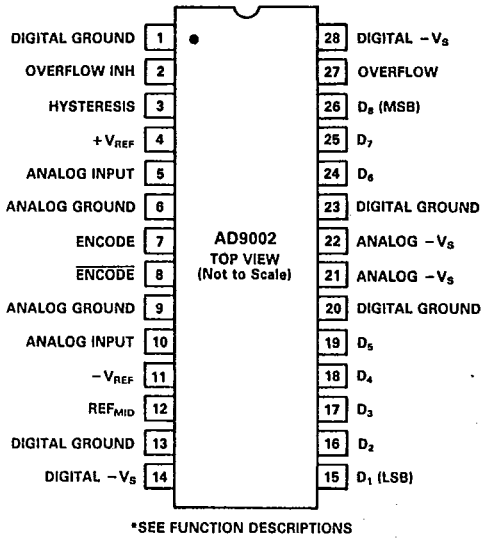
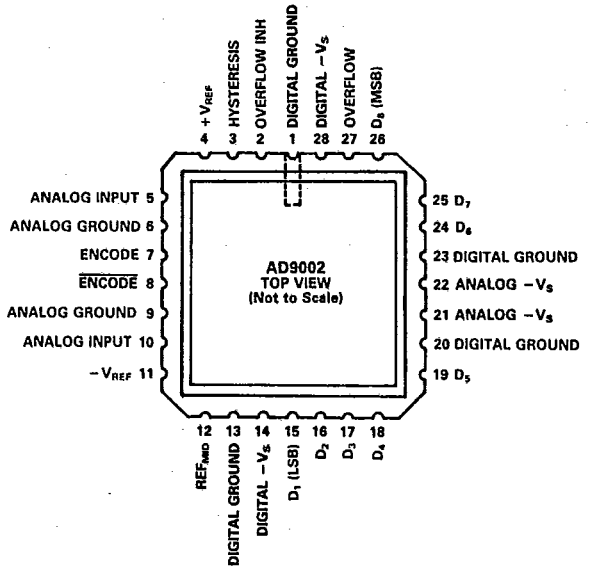
Pin Assignments

DIP (Q Package)



*SEE FUNCTION DESCRIPTIONS

LCC (E Package)

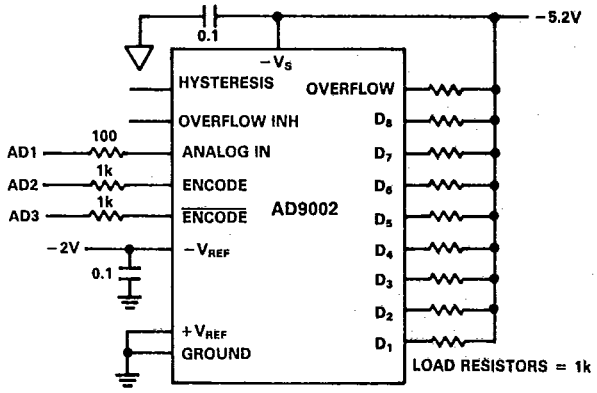


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group D57.

4.2.1 Life Test/Burn-In Circuit.

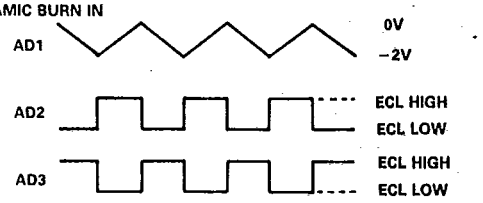
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



STATIC BURN IN

AD1 = 0V AD2 = ECL HIGH AD3 = ECL LOW

DYNAMIC BURN IN



ALL RESISTORS ±5%, Ω

ALL CAPACITORS ±20%, μF

ALL SUPPLIES ±5%

REV. A