

STRUCTURE

Silicon Monolithic Integrated Circuit

PRODUCT NAME

1ch Switching Regulator Controller

TYPE

BD9300F

FEATURES

PMW Switching Regulator Controller

Input Voltage Range: 3.6V~35V

●ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	36	V
Power Dissipation	Pd	450*	mW
Operating Temperature Range	Topr	−40~+85	Ĉ
Storage Temperature Range	Tstg	− 55~+125	Ĉ
Output Pin Current	lo	100**	mA
Output Pin Voltage	Vo	36	V
Junction Temperature	Tjmax	125	°C

^{*} Derating in done 4.5mW/°C for operating above Ta≥25°C (On 70.0mm×70.0mm×1.6mm board)

●OPERATING CONDITIONS (Ta=-40°C~+85°C)

Parameter	Symbol		11.24		
	Symbol	Min	Тур	Max	Unit
Supply Voltage	Vcc	3.6	12	35	V
Output Sink Current	10	_	_	30	mA
Output Pin Voltage	VO	_	_	35	٧
Timing Capacitance	СТ	33	_	1000	pF
Timing Resistance	RT	5		100	kΩ
Oscillator Frequency	Fosc	20	_	800	kHz

 $[\]bigstar$ This product is not designed for protection against radioactive rays.

Status of this document

^{**} Pd should not be exceeded

[★]The product described in this specification is a strategic product(and/or Service) subject to COCOM regulations. It should not be exported without Authorization from the appropriate government.

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

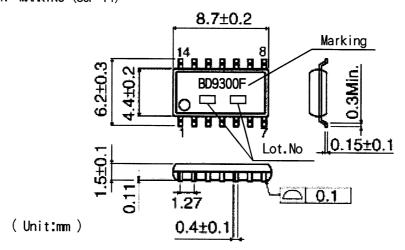
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• ELECTORICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C Vcc=12V, CT=200pF, RT=20k Ω)

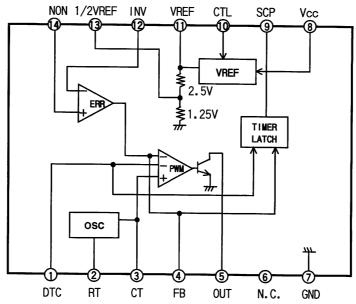
CELEGICITIONE GIVINOTETTOTTOO	(0111000 0	therwise		, 1a-23 C	VCC-12V,	C1=200pr, N1=20K32)
Parameter	Symbol	Limit			Unit	Condition
	Symbol	Min	Тур	Max	Unit	Condition
(ERROR AMPLIFIER BLOCK)						
Output Voltage	VREF	2.475	2.500	2.525	V	IREF=1mA
Line Regulation	VDLI	-	1.5	20	mV	Vcc=3.6~35V, IREF=1mA
Load Regulation	VDLD	-	0.5	20	mV	IREF=0~1mA
1/2 VREF Voltage	1/2VREF	1.212	1.25	1.288	٧	
[OSCILLATION BLOCK]				-		
Oscillation Frequency	FOSC	165	220	275	kHz	
Threshold Voltage Of Charging	V0SC+		1.95	_	٧	
Threshold Voltage Of Discharging	VOSC-	-	1.45	_	٧	
Frequency Drift	FDV0	_	1	_	%	Vcc=3.6~35V
[PROTECTION CIRCUIT BLOCK]						·
Threshold Voltage	VIT	1.5	1.8	2.1	٧	
SCP Source Current	Iscp	_	7	11	uA	
[DEAD TIME CONTROL INPUT]						
Input Threshold Voltage High	VtH	2.05	_	-	ν	Duty Cycle=0%
Input Threshold Voltage Low	VtL	_	_	1.35	ν	Duty Cycle=100%
Input Bias Current	Ibd		0.1	1	uA	DTC=1.5V
Latch Mode Source Current	Idtc	200	500	_	uA	DTC=0V
[UNDER VOLTAGE LOCK OUT BLOCK]						•
Threshold Voltage	VUT	_	2.8	_	V	
(ERROR AMPLIFIER BLOCK)						
Input Bias Current	IIB	_	0.1	1	uA	
Open Loop Gain	AV	_	85	_	dB	Null AMP
Max. Output Voltage	VOH	2.3	2.5	_	٧	
Min. Output Voltage	VOL	_	0.7	0.9		
Output Sink Current	101	0.1	1	_	mA	VFB=1.25V
Output Source Current	100	40	70	_	uA	VFB=1.25V
(OUTPUT BLOCK)						
Saturation Voltage	VSAT	_	1.0	1.4	٧	10=30mA
Leak Current	ILEAK	_	_	10	uA	OUT=35V
[CONTROL BLOCK]						
CTL ON Voltage	VON	2			V	
CTL OFF Voltage	VOFF	_	_	0.7	٧	
CTL SINK current	ICTL		57	90	uA	VCTL=5V
(DEVICE)						
Stand-by Current	ISTB	_	0	10	uA	VCTL=0V .
Average Supply Current	ICC		1.2	2.4		RT=VREF

●PHYSICAL DIMENSION • MARKING (SOP-14)



ROHM

BLOCK DIAGRAM



*Please refer to Technical note concerning application circuit, and etc.

● PIN NO. & FUNCTION TABLE

Pin No.	Pin Name	Function
1	DTC	Dead time control voltage input
2	RT	Connect to external resister setting operating frequency
3	СТ	Connect to external capacitor setting operating frequency
4	FB	Error amp output
5	OUT	PWM output (OPEN Collector)
6	N. C.	-
7	GND	Ground
8	Vcc	Power input
9	SCP	Connect to external capacitor setting short circuit protection timing. (Connect to GND when no use)
10	CTL	Control voltage input
11	VREF	Reference voltage output
12	INV	Error amp inverting input
13	1/2VREF	1/2Reference voltage output
14	NON	Error amp non inverting input



NOTES FOR USE

1. Operation supply voltage range

The circuit functionality is guaranteed within operation of ambient temperature range, as long as it is within operation supply voltage range. The standard electrical characteristic values are guaranteed at the test circuit voltage of VCC=12V. They cannot be guaranteed at other voltages. However, the variation will be small.

2. Grounding

It is recommended that every capacitor (bypass and another capacitors) is grounded to PIN7 using single-point connections.

3. FB Terminal

The FB terminal is for phase margin of the DC/DC system. A capacitor and a resistor or an only capacitor placed between the FB terminal and the INV terminal. The values of the capacitor and the resistor shall be adjusted according to the output current and the output capacitor value. The output may be oscillating if the value of capacitor is not sufficient, also the transient response may become insufficient if the value is too large. Therefore, the value of the capacitor and the resistor shall be adequately set up based on the condition of the temperature, and so on. Since the FB terminal also detects output short condition compulsorily applying an external voltage onto the FB terminal must not be performed because it may activate the timer latch protection circuit.

4. OUT Terminal

Since the IC may possibly be destroyed if a current exceeding its absolute maximum rating is input, be sure to locate a current limiting resistor. The resistance value shall be determined with a sufficient margin based on the input voltage (VCC), the VBE of the external transistor and output SAT voltage (VSAT).

5. VCC Terminal

For reduce the influence of switching noise, bypass capacitor is connected between VCC and GND.

6. Electromagnetic Fields

The IC is susceptible to strong electromagnetic fields and may cause malfunction. Therefore, caution should be used when placing it on the PCB.

7. Miscellaneous

This product is produced with strict quality control, but can be destroyed if used beyond absolute maximum ratings. Furthermore, the failure mode cannot be defined (e.g. short mode or open mode), if the device is used above the absolute maximum ratings, a fuse is recommended.

8. Application Design

When designing the external circuit, included adequate margins, including not only steady state but also transient characteristics.

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