SONY CXK541000J -25/30/35

262144-word × 4-bit High Speed CMOS Static RAM *Preliminary*

Description

CXK541000J is a 1048576 bits high speed CMOS static RAM organized as 262144 words by 4 bits and operates from a single 5V supply.

This device is suitable for use in high speed and low power applications.

32 pin SOJ (Plastic)

Features

- Fast access time (Access time)
  - CXK541000J-25 25ns (Max.)
  - CXK541000J-30 30ns (Max.)
  - CXK541000J-35 35ns (Max.)
- Low power consumption (operation) : 350mW (Typ.)
- Single +5V power supply: 5V ± 10%
- Fully static memory ····· No clock or timing strobe required.
- Equal access and cycle time.
- Separated data input and output: three-state output
- Directly TTL compatible: All inputs and outputs
- High density: 400 mil 32 pin SOJ plastic package

Function

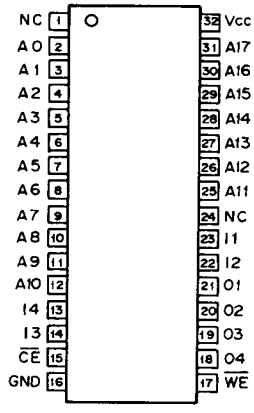
262144-word × 4-bit static RAM

Structure

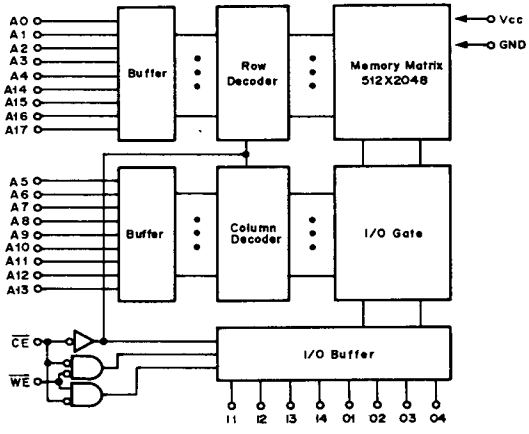
Silicon gate CMOS IC

Pin Configuration

(Top View)



Block Diagram



Pin Description

Symbol	Description
A0 to A17	Address input
I1 to I4	Data input
O1 to O4	Data output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5 * to +7.0	V
Input voltage	V_{IN}	−0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$	−0.5 * to Vcc+0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	−10 to +85	℃
Storage temperature	Tstg	−55 to +150	℃
Soldering temperature•time	Tsolder	260•10	℃•sec

* V_{CC}, V_{IN}, $V_{I/O}$=+7.5V Max. for pulse width less than10ns.
  V_{CC}, V_{IN}, $V_{I/O}$=−3.5V Min. for pulse width less than10ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	Data Output	Vcc Current
H	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	Read	Data out	Icc
L	L	Write	High Z	Icc

× : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.5	V
Input low voltage	V_{IL}	−0.5 *	—	0.8	V
Input rise time	tr	—	5	100	ns
Input fall time	tf	—	5	100	ns

* V_{IH}=+7.0V Max. for pulse width less than 10ns.
  V_{IL}=−3.0V Min. for pulse width less than 10ns.

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Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ. *	Max.	Unit
Input leak current	I_{LI}	V_{IN}=GND to Vcc Vcc=5.5V	−1	—	1	µA
Output leak current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=GND to Vcc	−1	—	1	µA
Average operating current	I_{CC}	Cycle=Min, Duty=100% I_{OUT}=0mA	—	70	120	mA
Standby current	I_{SB1}	$\overline{CE}$ ≧ Vcc−0.2V, V_{IN} ≧ Vcc−0.2V or V_{IN} ≦ 0.2V	—	—	2	mA
	I_{SB2}	$\overline{CE}$=V_{IH}, V_{IN}=V_{IH}/V_{IL}, min. cycle	—	15	30	mA
Output high voltage	V_{OH}	I_{OH}=−4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=8.0mA	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	6	pF
Output capacitance	C_{OUT}	V_{OUT}=0V	—	10	pF

Note) This parameter is sampled and is not 100% tested.

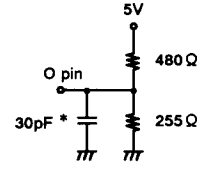
AC characteristics

• AC test conditions

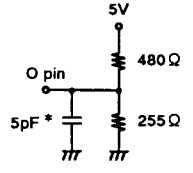
(Vcc=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig

** for t_{LZ}, t_{HZ}, tow, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	-25		-30		-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE}$)	t_{CO}	—	25	—	30	—	35	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	5	—	5	—	5	—	ns
Chip disable to output in high Z	t_{HZ}*	0	15	0	15	0	15	ns
Chip enable to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	25	—	30	—	35	ns

* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

• Write cycle

Item	Symbol	-25		-30		-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	18	—	20	—	20	—	ns
Chip enable to end of write	t_{CW}	18	—	20	—	20	—	ns
Data to write time overlap	t_{DW}	12	—	15	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	18	—	18	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	2	—	2	—	2	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	15	0	15	0	15	ns

* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

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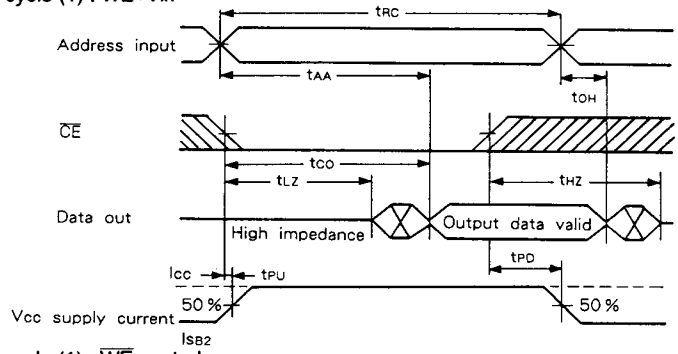
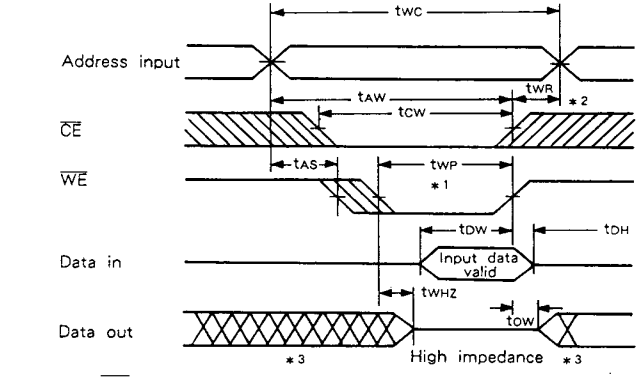
Timing Waveform

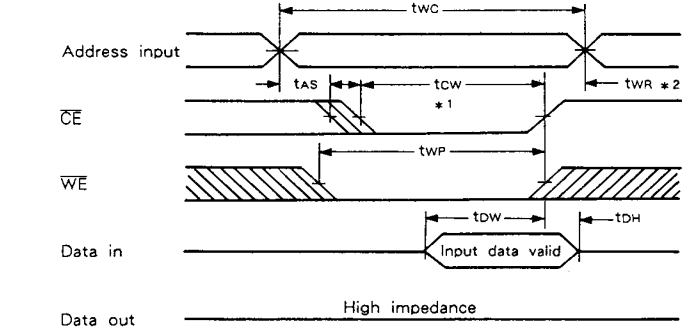
• Read cycle (1) : $\overline{WE}$=V_{IH}



• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



*1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.

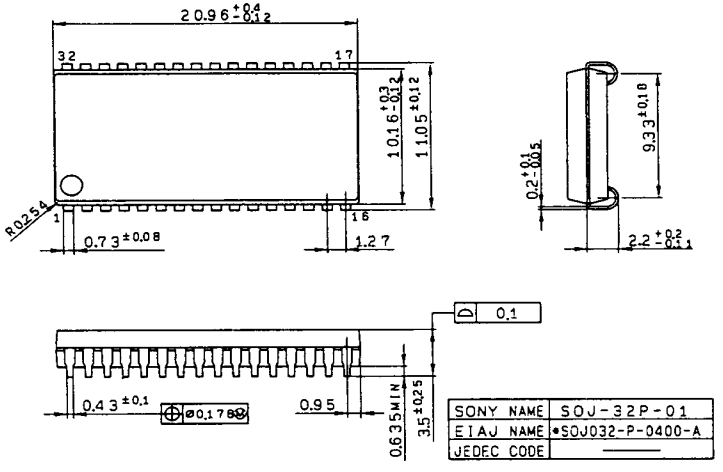
*2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.

*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

Package Outline

Unit : mm

32pin SOJ (Plastic) 400mil 1.3g



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