D470

Low-Power – High-Speed Octal CMOS Driver with Serial Interface

FEATURES

- Up to ± 22 Volt Output Range
- Low Propagation Delays (< 200 ns)
- Any combination of 8 Outputs
- TTL and CMOS Compatible
- Independent Output Voltages
- ESDS Protection > ±4000 V

BENEFITS

- Devices Can Be Chained For System Expansion
- Master Reset To All Drivers
- Simple Interfacing
- Reduced Parts Count
- Increased Versatility

APPLICATIONS

- Automotive and Avionics Systems
- ATE
- Serial Data Acquisition and Process control
- Communication Systems
- Display Drivers

DESCRIPTION

The D470 is a CMOS driver array configured as eight power buffers for use in serial input applications. By combining high output current capability (I_{OPEAK} = 200 mA) and low propagation delays (t_{PR} < 150 ns) the D470 is ideally suited for driving discrete devices in automotive, ATE, and process control applications.

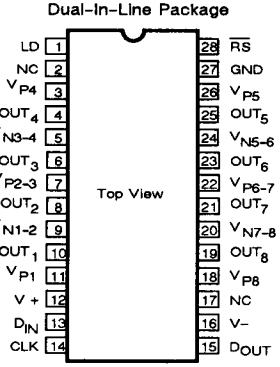
This device loads data serially into the input shift register with each clock pulse. The state of the shift register can be latched via LOAD (LD) at any point into an address register which holds the logic bits to control each individual driver. A $\overline{RS}$ pin resets all the latches which in turn reset the power buffers. A serial data output terminal D_{OUT} allows chaining of power drivers for larger matrix systems. The output voltages may be made independent or equal to V+ and V– for added flexibility.

The D470 is built on Siliconix' high voltage silicon gate process to achieve high voltage ratings and high output current capability. An epitaxial layer prevents latchup.

Packaging for the D470 consists of the 28-pin CerDIP, plastic DIP, and PLCC. Performance grades available are military, A suffix (–55 to 125°C) and industrial, D suffix (–40 to 85°C).

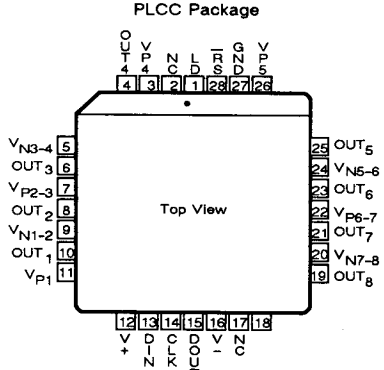
PIN CONFIGURATION

Dual-In-Line Package



Order Numbers:
CerDIP: D470AK, D470AK/883
Plastic: D470DJ

PLCC Package



Order Number: D470DN

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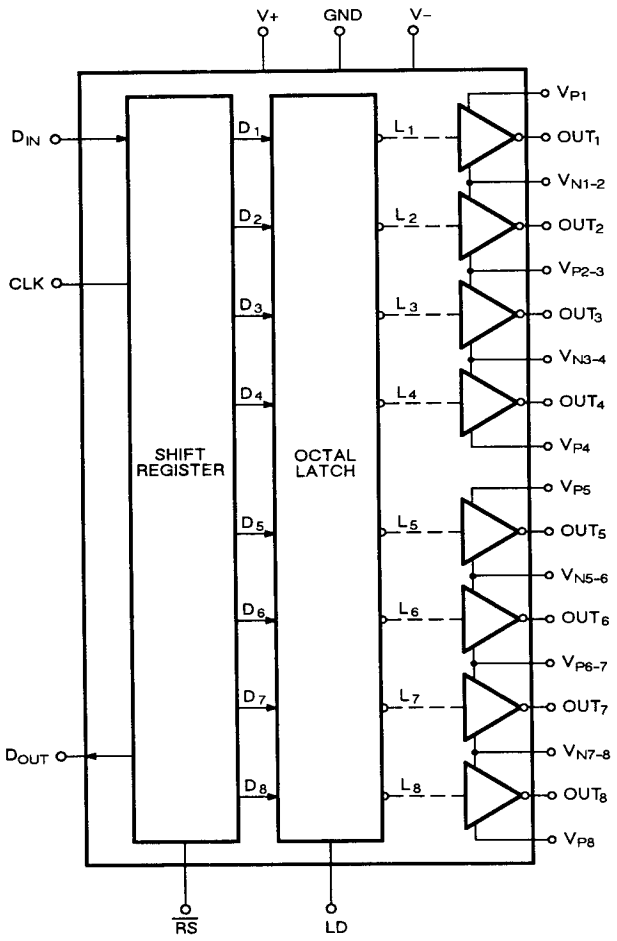
FUNCTIONAL BLOCK DIAGRAM



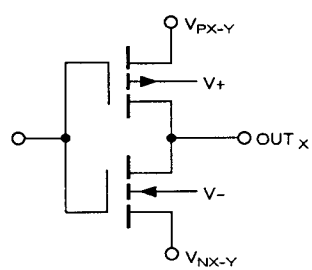
TRUTH TABLE

$\overline{RS}$	CLK*	D_{IN}	D_1	D_n
1	↑	0	0	D_{n-1}
1	↑	1	1	D_{n-1}
1	↓	X	D_1	D (NO CHANGE)
0	X	X	0	0

LD*	D_1	L_1	OUT_1
↑	0	1	V_{N1-2}
↑	1	0	V_{P1}
↓	D_1	L_1	(NO CHANGE)

* CLK and LD are level sensitive inputs.

OUTPUT STRUCTURE



Preliminary

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44 V

GND to V- ..... 25 V

Digital Inputs, V_{PX-Y}, V_{NX-Y}[1] ... (V-) -2 V to (V+) + 2 V
or 30 mA, whichever occurs first

Continuous Current (Any Terminal) ..... 30 mA

Current, I_{OS} (Pulsed 1 ms 10% duty cycle) ..... 200 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
28-Pin CerDIP** ..... 1200 mW
28-Pin Plastic*** ..... 625 mW
28-Pin PLCC**** ..... 450 mW

* All leads welded or soldered to PC Board.
** Derate 16 mW/°C above 75°C.
*** Derate 8.3 mW/°C above 75°C.
**** Derate 6 mW/°C above 75°C.

1 Signals exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, GND = 0 V, V_{IN} = 2.4 V, 0.8 V[d]	LIMITS 1=25°C 2=125,85°C 3=-55,-40°C TEMP	TYP[c]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
DRIVER									
Output Voltage HIGH	V_{OH}	I_O = -5 mA	1,3 2		14.6 14.4		14.6 14.4		V
		I_O = -30 mA	1,3 2		11 9		11 9		
Output Voltage LOW	V_{OL}	I_O = 5 mA	1,3 2			-14.6 -14.4		-14.6 -14.4	
		I_O = 30 mA	1,3 2			-11 -9		-11 -9	
Output Source Current	I_{OS+}	V_O = -15 V Pulsed	1,3 2		200 150		200 150		mA
		V_O = 0 V Pulsed	1,3 2		175 125		175 125		
Output Sink Current	I_{OS-}	V_O = 15 V Pulsed	1,3 2			-125 -100		-125 -100	
		V_O = 0 V Pulsed	1,3 2			-125 -100		-125 -100	
LOGIC INPUT									
Input Current with V_{IN} LOW	I_{IL}	V_{IN} Under Test = 0.8 V All Other = 2.4 V	1,2		-1	1	-1	1	µA
Input Current with V_{IN} HIGH	I_{IH}	V_{IN} Under Test = 2.4 V All Other = 0.8 V	1,2		-1	1	-1	1	

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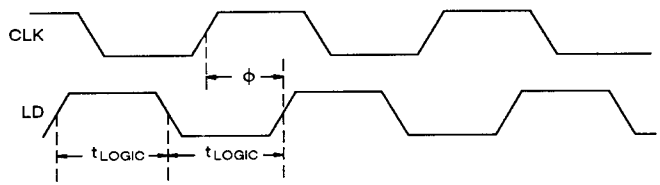
ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, GND = 0 V, V_{IN} = 2.4 V, 0.8 V [d]	LIMITS 1=25°C 2=125,85°C 3=−55,−40°C		A SUFFIX −55 to 125°C		D SUFFIX −40 to 85°C		UNIT
			TEMP	TYP [c]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
LOGIC OUTPUT									
Output Voltage LOW (D_{OUT})	V_{OL}	I_O = 3.2 mA	1,2			0.4		0.4	V
Output Voltage HIGH (D_{OUT})	V_{OH}	I_O = −80 µA	1,2		2.4		2.4		V
DYNAMIC									
Pulse Width for Logic Inputs	t_{LOGIC}	(D_{IN}, LD, CLK, $\overline{RS}$)	1 2		80 150		80 150		ns
Propagation Delay (Rise)	t_{PR}	V_{IN} = LD, C_L = 500 pF 50% of V_{IN} to 50% of V_O	1 2			150 200		250 200	ns
Propagation Delay (Fall)	t_{PF}		1 2			200 250		200 250	ns
Data Setup Time	t_{DW}		1,2		50		50		ns
SUPPLY									
Positive Supply Current	I+	V+ = 16.5 V, V− = −16.5 V V_{IN} = 0 or 5 V	1,2			100		100	µA
Negative Supply Current	I−		1,2		−1		−1		µA
Ground Current	I_{GND}		1,2		−100		−100		µA

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. V_{IN} = input voltage to perform proper function.

INPUT TIMING REQUIRMENTS



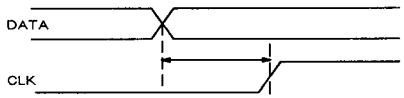
ϕ = for CLK and LD inputs of the same frequency
The recommended phase delay of LD from CLK is 1/2 t_{LOGIC} to t_{LOGIC}

t_{LOGIC}(MIN) : 80 ns at 25°C
150 ns at 125°C

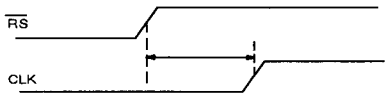
V+ = +15 V
V− = −15 V
GND = 0 V

INPUT TIMING REQUIRMENTS (Cont'd)

SHIFT REGISTER SETUP

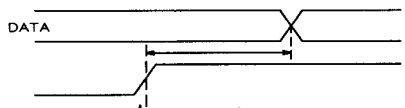


DATA TO CLK ↑ 30 ns at 25 °C
50 ns at 125 °C



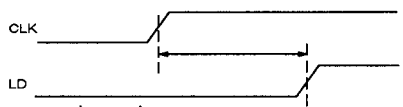
RS ↑ TO CLK ↑ 30 ns at 25 °C
50 ns at 125 °C

SHIFT REGISTER HOLD

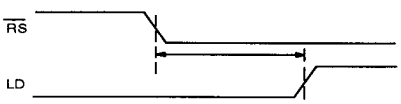


DATA FROM CLK ↑ 30 ns at 25 °C
50 ns at 125 °C

ADDRESS REGISTER SETUP

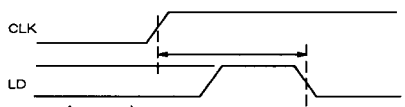


CLK ↑ TO LD ↑ 30 ns at 25 °C
50 ns at 125 °C

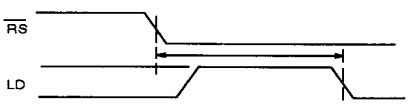


RS ↓ TO LD ↑ 30 ns at 25 °C
50 ns at 125 °C

ADDRESS REGISTER ENABLE



CLK ↑ TO LD ↓ 100 ns at 25 °C
150 ns at 125 °C



RS ↓ TO LD ↓ 100 ns at 25 °C
150 ns at 125 °C

V+ = +15 V, V− = − 15 V, GND = 0 V
INPUTS ARE 0 V TO 3 V

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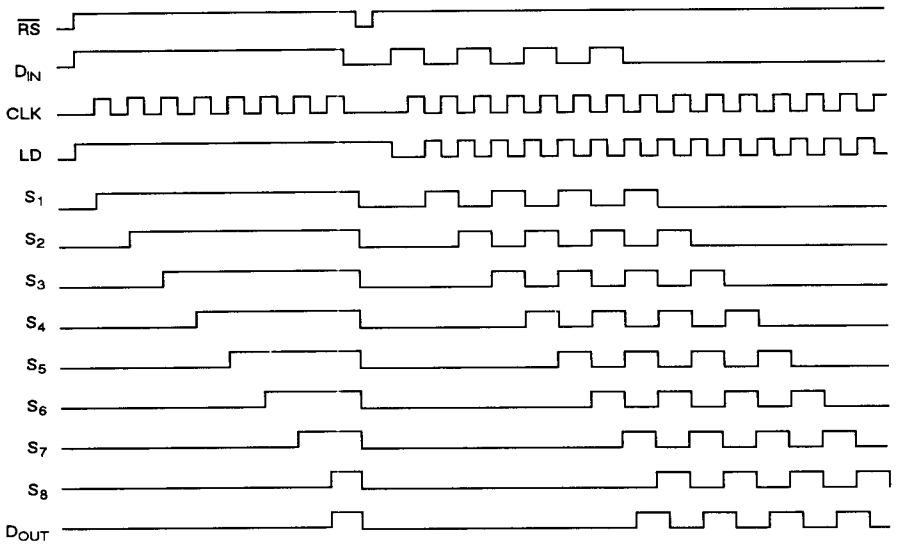
TIMING DIAGRAM



$S_1 - S_8$ and D_{OUT} are expected output with the drain connected high.
The sources require pull-downs of 1 kΩ .

PIN DESCRIPTION

SYMBOL	DESCRIPTION
LD	Logic LOAD DATA Input. When HIGH it loads the contents of the shift register into the octal latch.
NC	No Connection
V_{PX-Y}	Positive power supply voltage common to buffers X and Y.
OUT_X	Buffer X output
V_{NX-Y}	Negative Power Supply Voltage, common to buffers X and Y.
V+	Positive Supply Voltage
D_{IN}	Serial Data Input. TTL Compatible for V+ = +4.5 V up to +22 V.
CLK	Clock. The d-type master-slave flip-flops that make the shift register are updated during the positive transitions of the clock.
D_{OUT}	Serial Data Output. TTL compatible output levels. Can be used to chain several devices.
V-	Negative Supply Voltage.
GND	Digital Ground.
$\overline{RS}$	$\overline{RESET}$. When LOW this input clears the contents of the shift register to an all zeroes state.