DG400-405
Low-Power – High-Speed CMOS Analog Switches

Siliconix incorporated

FEATURES

- ±15 V Input Range
- ON Resistance < 35 Ω
- Fast Switching Action
  t_{ON} < 150 ns
  t_{OFF} < 100 ns
- Ultra Low Power Requirements (P_D < 35 μW)
- TTL, CMOS Compatible

BENEFITS

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

APPLICATIONS

- High Performance Audio and Video Switching
- Sample and Hold Circuits
- Battery Operation

DESCRIPTION

The DG400 family of monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (< 35 μW) with high speed (t_{ON} < 150 ns), the DG400 series is ideally suited for portable and battery powered industrial and military applications.

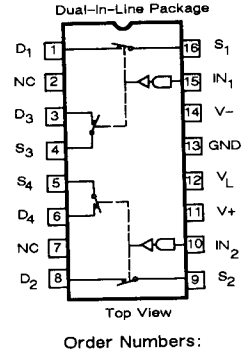
Built on the Siliconix proprietary high voltage silicon gate process to achieve high voltage rating and superior switch ON/OFF performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. ON resistance is very flat over the full ±15 V analog range, rivaling JFET performance without the inherent dynamic range limitations.

The six devices in this series are differentiated by the type of switch action as shown in the functional block diagrams. Package options include the 16-pin plastic, CerDIP and LCC package. Performance grades include industrial, D suffix (-40 to 85°C), and military, A suffix (-55 to 125°C). Additionally, the DG403 and DG405 are available in the narrow body surface mount package, SO-16.

FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE

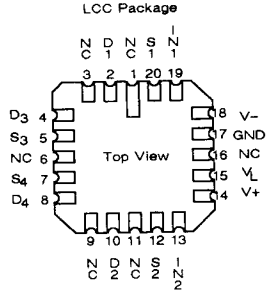
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG405AK
DG405AK/883
Plastic: DG405DJ

LCC Package



Order Number:
DG405AZ

DG405

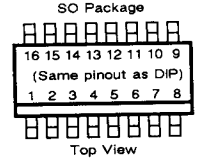
Two DPST Switches per Package

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 " ≤ 0.8 V
Logic " 1 " ≥ 2.4 V

SO Package

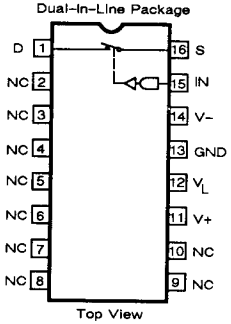


Top View

Order Number:
DG405DY

FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE (Cont'd)

Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG400AK
DG400AK/883
Plastic: DG400DJ

DG400

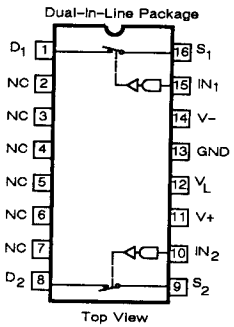
One SPST Switch per Package

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 " $\leq$ 0.8 V
Logic " 1 " $\geq$ 2.4 V

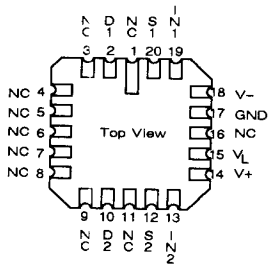
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG401AK
DG401AK/883
Plastic: DG401DJ

.CC Package



Order Number:
DG401AZ

DG401

Two SPST Switches per Package

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 " $\leq$ 0.8 V
Logic " 1 " $\geq$ 2.4 V

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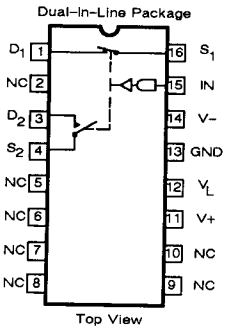
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG402AK
DG402AK/883
Plastic: DG402DJ

DG402

One SPDT Switch per Package

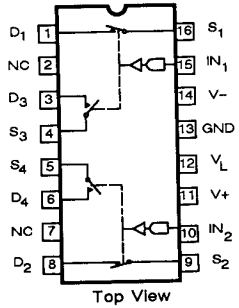
Truth Table

LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

Logic " 0 " $\leq$ 0.8 V
Logic " 1 " $\geq$ 2.4 V

FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE (Cont'd)

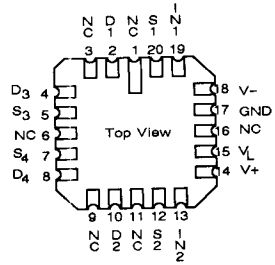
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG403AK
DG403AK/883
Plastic: DG403DJ

Leadless Chip Carrier



Order Number:
DG403AZ

DG403

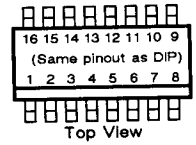
Two SPDT Switches per Package

Truth Table

LOGIC	SWITCH 1 SWITCH 2	SWITCH 3 SWITCH 4
0	OFF	ON
1	ON	OFF

Logic " 0 " $\leq$ 0.8 V
Logic " 1 " $\geq$ 2.4 V

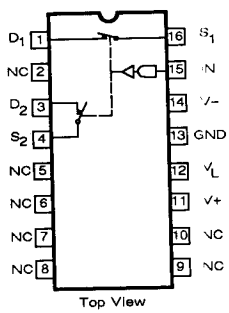
SO Package



Top View

Order Number:
DG403DY

Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG404AK
DG404AK/883
Plastic: DG404DJ

DG404

One DPST Switch per Package

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 " $\leq$ 0.8 V
Logic " 1 " $\geq$ 2.4 V

ABSOLUTE MAXIMUM RATINGS

V+ to V- 44V
GND to V- 25V
V_L to V- ..... (GND - 0.3 V) to 44 V
Digital Inputs[1] V_S, V_D ..... (V-) -2 V to (V+ plus 2 V)
..... or 30 mA, whichever occurs first
Current (Any Terminal) Continuous ..... 30 mA
Current, S or D (Pulsed 1 ms 10% duty) ..... 100 mA
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 450 mW
16-Pin CerDIP*** ..... 900 mW
20-Pin LCC**** ..... 750 mW
16-Pin SO***** ..... 600 mW

* All leads welded or soldered to PC board.
** Derate 6 mW/°C above 75°C
*** Derate 12 mW/°C above 75°C
**** Derate 10 mW/°C above 75°C
***** Derate 7.6 mW/°C above 75°C

[1] Signals on Sx, Dx or INx exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, V_L = 5 V, GND = 0 V, V_{IN} = 2.4V, 0.8 V [e]	LIMITS 1=25°C 2=125,85°C 3=-55,-40°C TEMP	TYP [d]	A SUFFIX -55 to 125°C MIN [b]	A SUFFIX -55 to 125°C MAX [b]	D SUFFIX -40 to 85°C MIN [b]	D SUFFIX -40 to 85°C MAX [b]	UNIT
SWITCH									
Analog Signal Range [c]	V_{ANALOG}				-15	15	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V+ = 13.5 V, V- = -13.5 V, I_S = -10 mA, V_D = ±10 V	1 2,3	20		35 45		45 55	Ω
Delta Drain-Source ON Resistance	$\Delta r_{DS(ON)}$	V+ = 16.5 V, V- = -16.5 V, I_S = -10 mA, V_D = 5, 0, -5 V	1 2,3	3.0		3.0 5.0		3.0 5.0	Ω
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5 V, V- = -16.5 V, V_D = -15.5 V, V_S = 15.5 V	1 2	-.01	-0.25 -20	0.25 20	-0.50 -20	0.50 20	nA
	$I_{D(OFF)}$	V+ = 16.5 V, V- = -16.5 V, V_D = 15.5 V, V_S = -15.5 V	1 2	-.01	-0.25 -20	0.25 20	-0.50 -20	0.50 20	nA
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5 V, V- = -16.5 V, V_D = V_S = ±15.5 V	1 2	-0.04	-0.4 -40	0.4 40	-1.0 -40	1.0 40	nA
INPUT									
Input Current with V_{IN} LOW	I_{IL}	V_{IN} Under Test = 0.8 V, All Other = 2.4 V	1,2	.005	-1.0	1.0	-1.0	1.0	µA
Input Current with V_{IN} HIGH	I_{IH}	V_{IN} Under Test = 2.4 V, All Other = 0.8 V	1,2	.005	-1.0	1.0	-1.0	1.0	µA
DYNAMIC									
Turn-ON Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF, See Figure 1A	1	100		150		150	ns
Turn-OFF Time	t_{OFF}	R_L = 300 Ω, C_L = 35 pF, See Figure 1A	1	60		100		100	ns
Break-Before-Make Time Delay	t_D	R_L = 300 Ω, C_L = 35 pF, DG402/DG403	1	20	10.0		10.0		ns
Charge Injection	Q	C_L = 10,000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	1	60		100		100	pC
Off Isolation		R_L = 100 Ω, C_L = 5 pF, f = 1 MHz	1	72					dB
Crosstalk [f] (Channel-to-Channel)		Any Other Channel Switches, R_L = 100 Ω, C_L = 5 pF, f = 1 MHz	1	90					dB
Source-OFF Capacitance	$C_{S(OFF)}$	V_S = 0 V, f = 1 MHz	1	12					pF
Drain-OFF Capacitance	$C_{D(OFF)}$	V_S = 0 V, f = 1 MHz	1	12					pF
Drain and Source ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	V_S = 0 V, f = 1 MHz	1	39					pF

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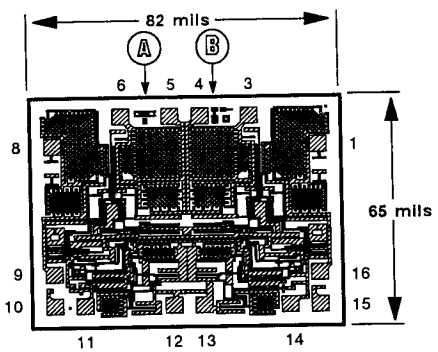
ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, V_L = 5 V, GND = 0 V, V_{IN} = 2.4V, 0.8 V [e]	LIMITS 1=25°C, 2=125,85°C, 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
SUPPLY									
Positive Supply Current	I+	V+ = 16.5 V, V- = -16.5 V, V_{IN} = 0.0 or 5.0 V	1 2,3	0.01		1 5		1 5	µA
Negative Supply Current	I-		1 2,3	-0.01	-1 -5		-1 -5		
Logic Supply Current	I_L		1 2,3	0.01		1 5		1 5	
Ground Current	I_{GND}		1 2,3	-0.01	-1 -5		-1 -5		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. Crosstalk performance is improved to 110 dB (typ.) with LCC package.

DIE TOPOGRAPHY

DG400



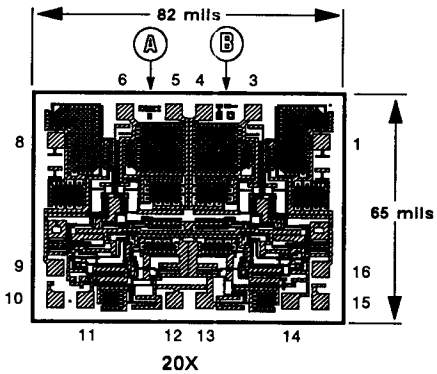
20X

Pad No.	Function
1	D
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	V+
12	V_L
13	GND
14	V-
15	IN
16	S

CSHCA/B
2 Capacitors
2 Resistors
8 P-channel enhancement MOSFETs
10 N-channel enhancement MOSFETs
2 Diodes

DIE TOPOGRAPHY (Cont'd)

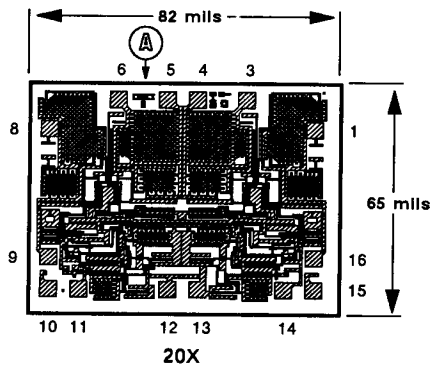
DG401



Pad No.	Function
1	D_1
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	D_2
9	S_2
10	IN_2
11	V+
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

CSHCA/B
4 Capacitors
4 Resistors
16 P-channel enhancement MOSFETs
20 N-channel enhancement MOSFETs
4 Diodes

DG402

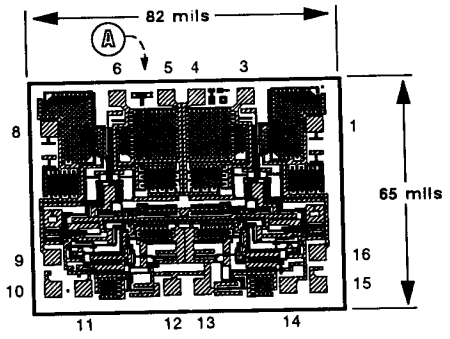


Pad No.	Function
1	D_1
2	NC
3	D_2
4	S_2
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	V+
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

CSHCA
2 Resistors
4 Capacitors
11 P-channel enhancement MOSFETs
15 N-channel enhancement MOSFETs
2 Diodes

5

DG403

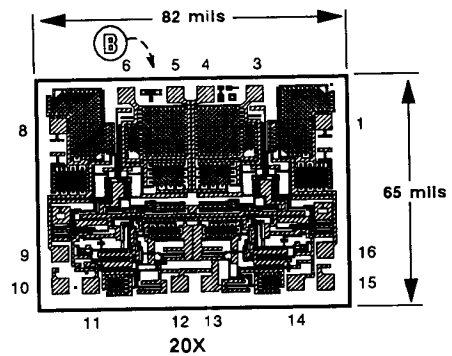


20X

CSHCA
8 Capacitors
4 Resistors
22 P-channel enhancement MOSFETs
30 N-channel enhancement MOSFETs
4 Diodes

Pad No.	Function
1	D_1
2	NC
3	D_3
4	S_3
5	S_4
6	D_4
7	NC
8	D_2
9	S_2
10	IN_2
11	V+
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

DG404



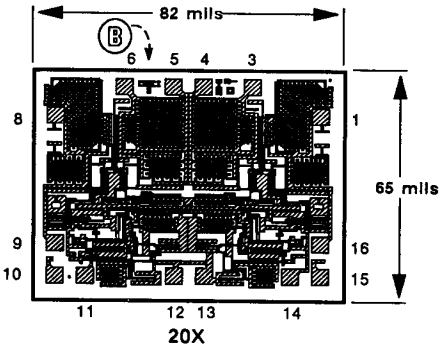
20X

CSHCB
2 Resistors
4 Capacitors
11 P-channel enhancement MOSFETs
15 N-channel enhancement MOSFETs
2 Diodes

Pad No.	Function
1	D_1
2	NC
3	D_2
4	S_2
5	NC
6	NC
7	NC
8	NC
9	NC
10	NC
11	V+
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

DIE TOPOGRAPHY (Cont'd)

DG405

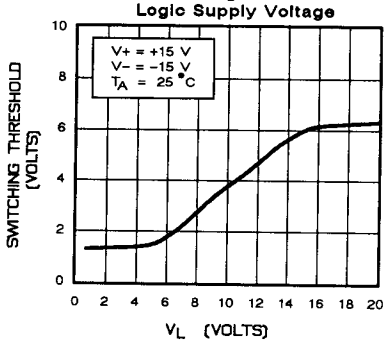


CSHCB
8 Capacitors
4 Resistors
22 P-channel enhancement MOSFETs
30 N-channel enhancement MOSFETs
4 Diodes

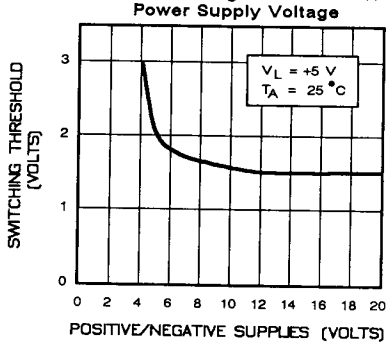
Pad No.	Function
1	D_1
2	NC
3	D_3
4	S_3
5	S_4
6	D_4
7	NC
8	D_2
9	S_2
10	IN_2
11	V+
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

TYPICAL CHARACTERISTICS

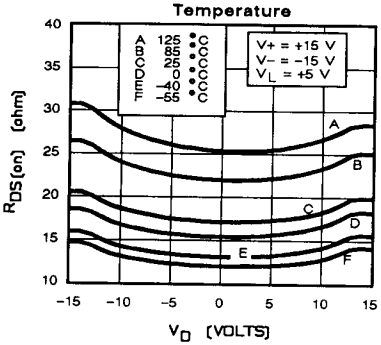
Input Switching Threshold vs. Logic Supply Voltage



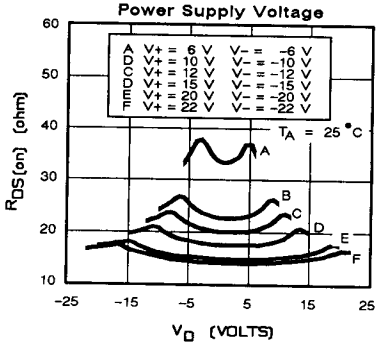
Input Switching Threshold vs. Power Supply Voltage



$r_{DS(ON)}$ vs. V_D and Temperature



$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



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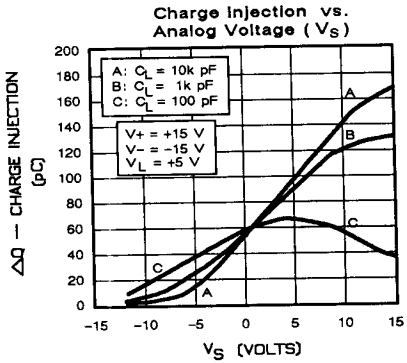
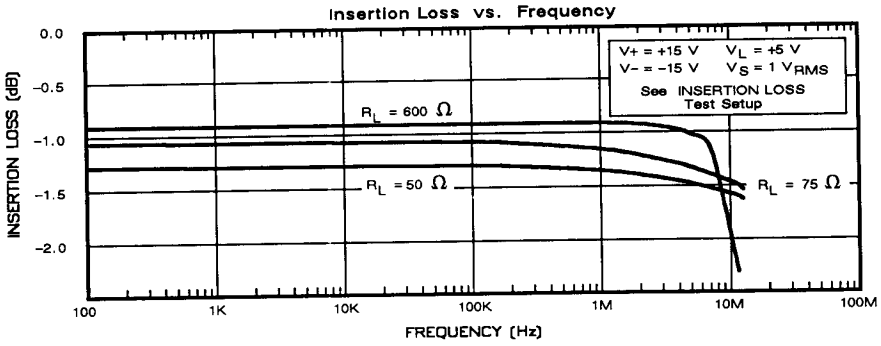
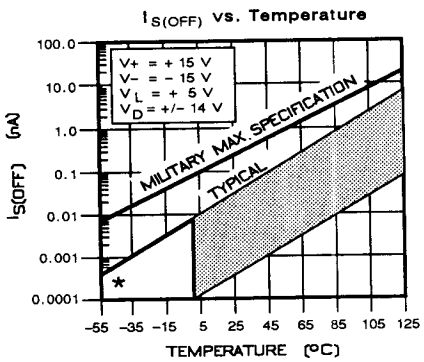
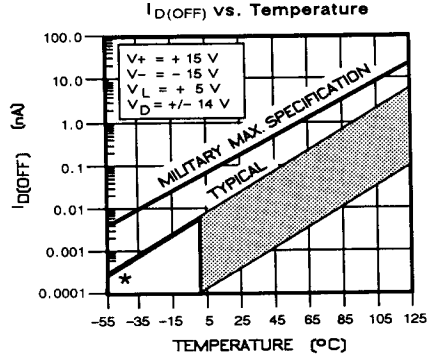
TYPICAL CHARACTERISTICS (Cont'd)



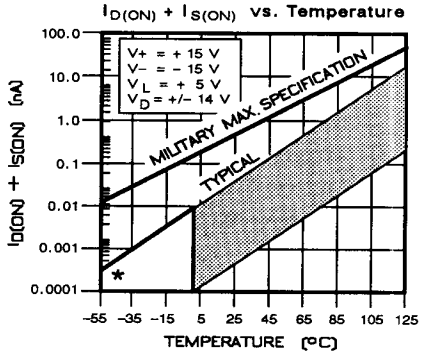


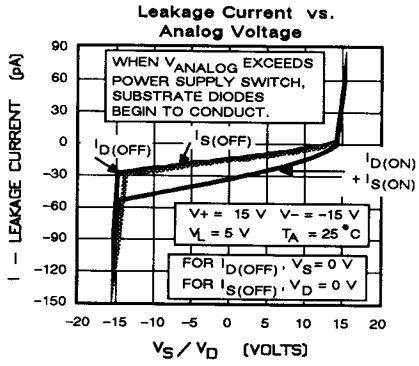


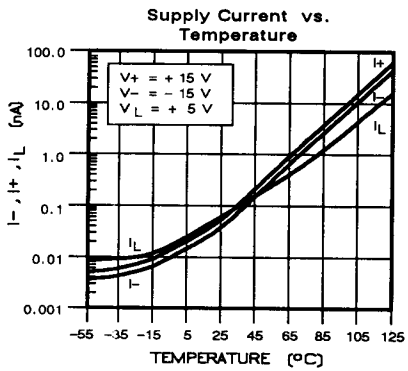


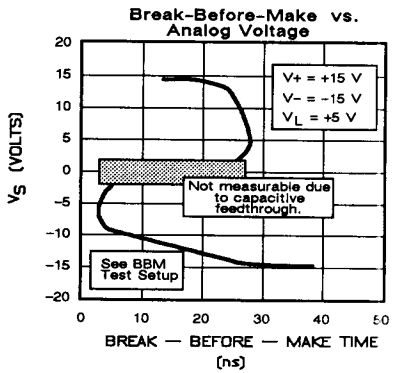
* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

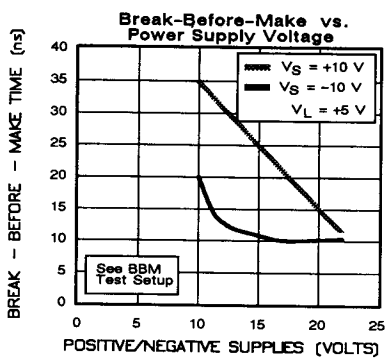
TYPICAL CHARACTERISTICS (Cont'd)







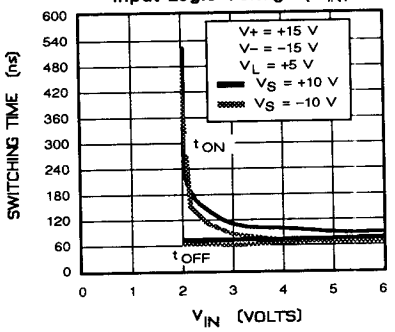




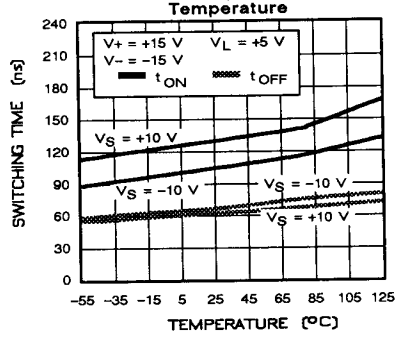
* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

TYPICAL CHARACTERISTICS (Cont'd)

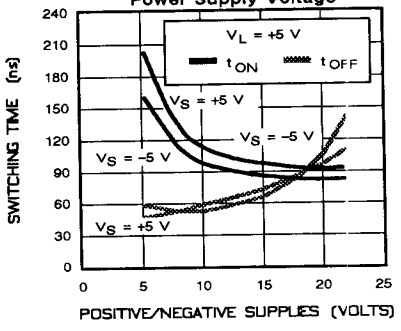
Switching Time vs. * Input Logic Voltage (V_{IN})



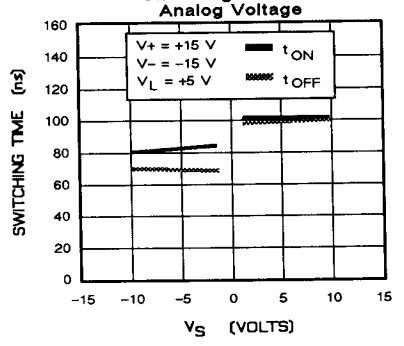
Switching Time vs. * Temperature



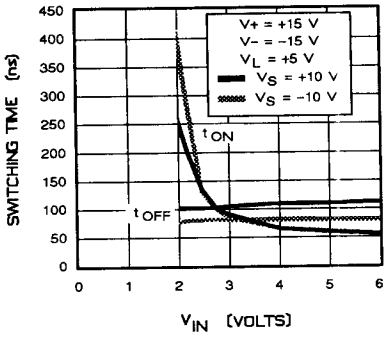
Switching Time vs. * Power Supply Voltage



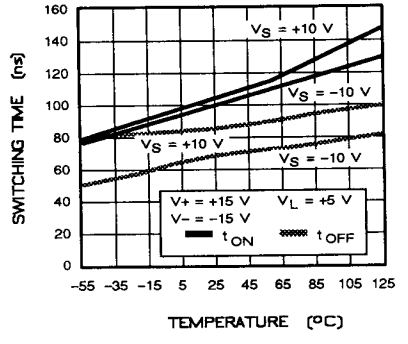
Switching Time vs. * Analog Voltage



Switching Time vs. ** Input Logic Voltage (V_{IN})



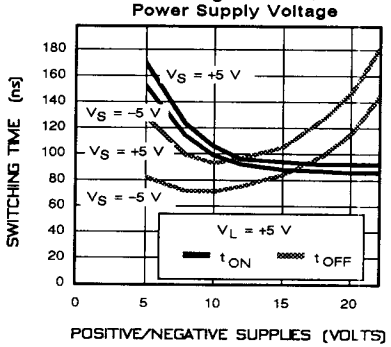
Switching Time vs. ** Temperature



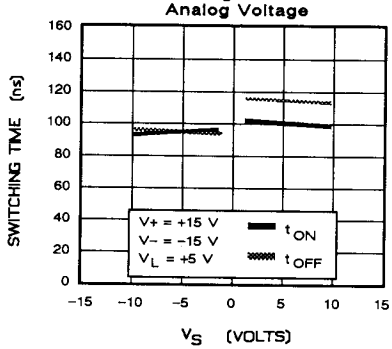
* REFER TO FIGURE 1A FOR TEST CONDITIONS
** REFER TO FIGURE 1B FOR TEST CONDITIONS

TYPICAL CHARACTERISTICS (Cont'd)

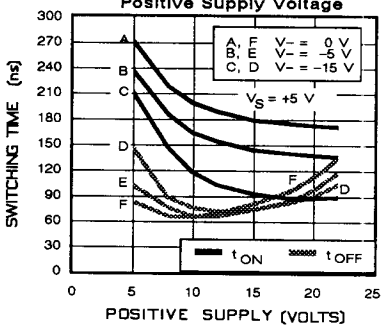
Switching Time vs. **
Power Supply Voltage



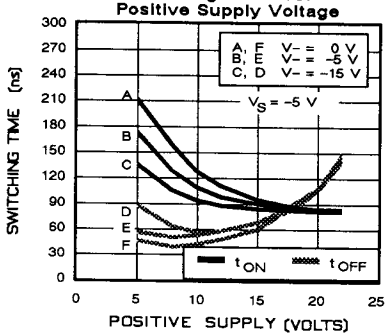
Switching Time vs. **
Analog Voltage



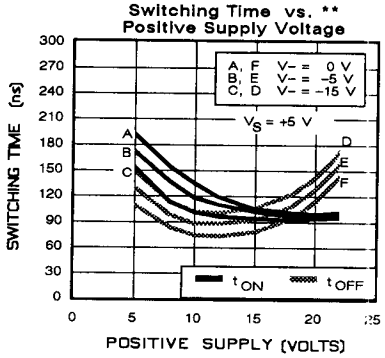
Switching Time vs. *
Positive Supply Voltage



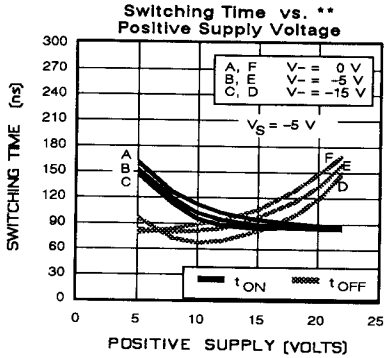
Switching Time vs. *
Positive Supply Voltage



Switching Time vs. **
Positive Supply Voltage



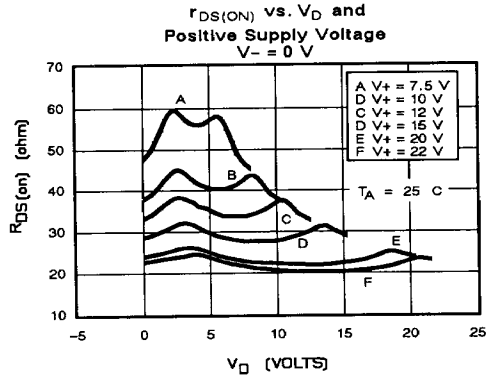
Switching Time vs. **
Positive Supply Voltage



* REFER TO FIGURE 1A FOR TEST CONDITIONS
** REFER TO FIGURE 1B FOR TEST CONDITIONS

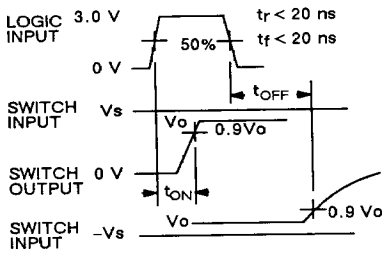
5

TYPICAL CHARACTERISTICS (Cont'd)

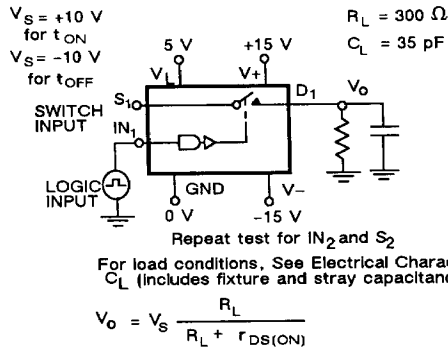


SWITCHING TIME TEST CIRCUIT

Vo is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense control

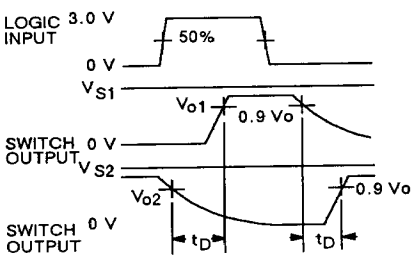


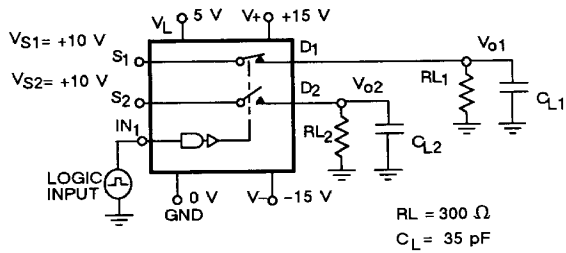
For load conditions, See Electrical Characteristics
C_L (includes fixture and stray capacitance)

$$V_o = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

Figure 1

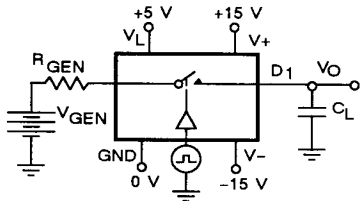
BREAK-BEFORE-MAKE TEST CIRCUIT

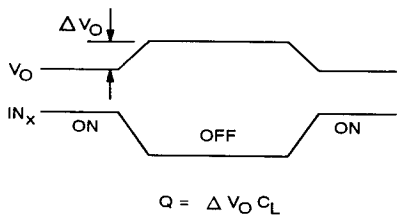




(includes fixture and stray capacitance)

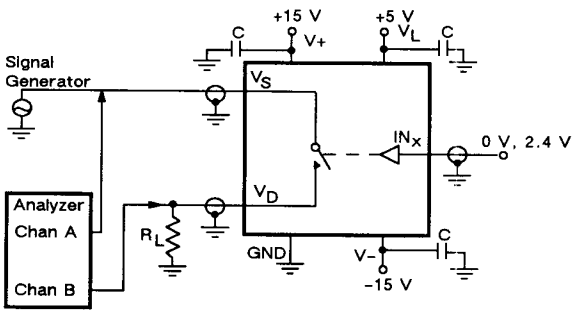
CHARGE INJECTION TEST CIRCUIT





$$Q = \Delta V_O C_L$$

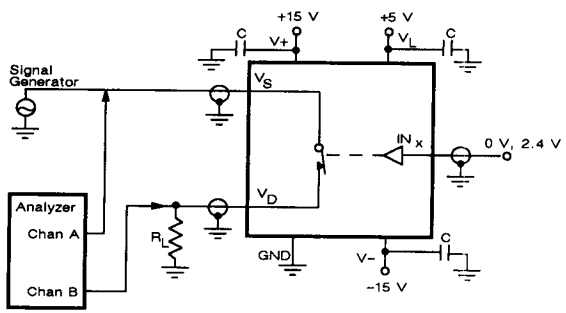
OFF ISOLATION TEST CIRCUIT



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

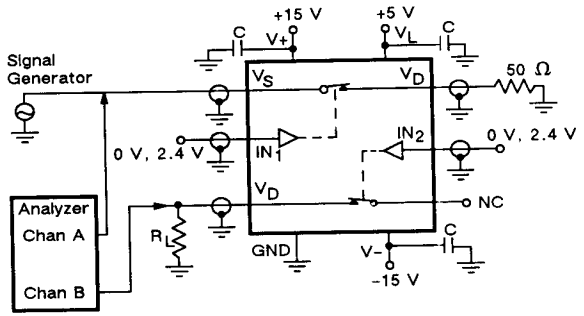
$$\text{OFF ISOLATION} = 20 \log \frac{V_D}{V_S}$$

INSERTION LOSS TEST CIRCUIT



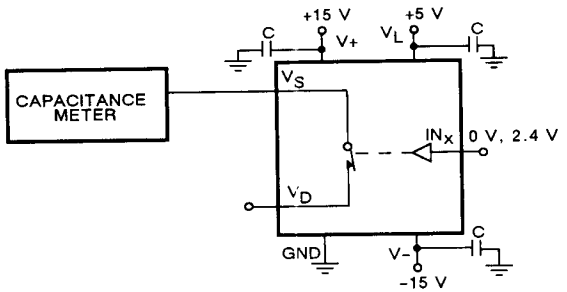
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

CROSSTALK TEST CIRCUIT



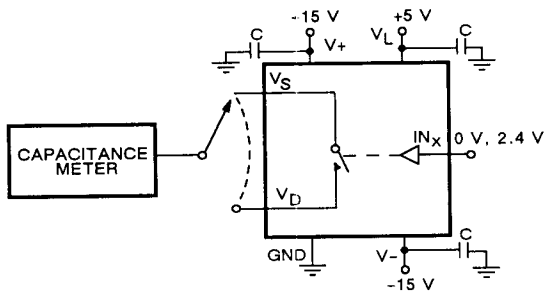
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

SOURCE/DRAIN ON CAPACITANCE



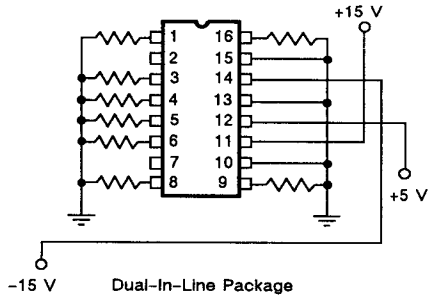
METER
HP4192A Impedance Analyzer or equivalent

SOURCE/DRAIN OFF CAPACITANCE

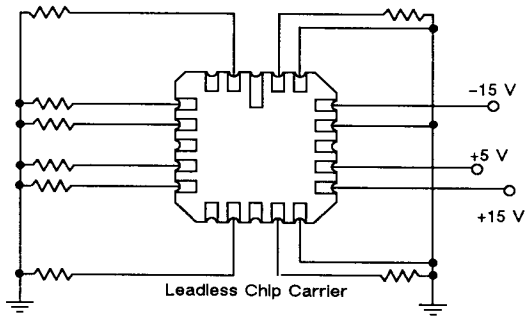


METER
HP4192A Impedance Analyzer or equivalent

BURN-IN CIRCUITS

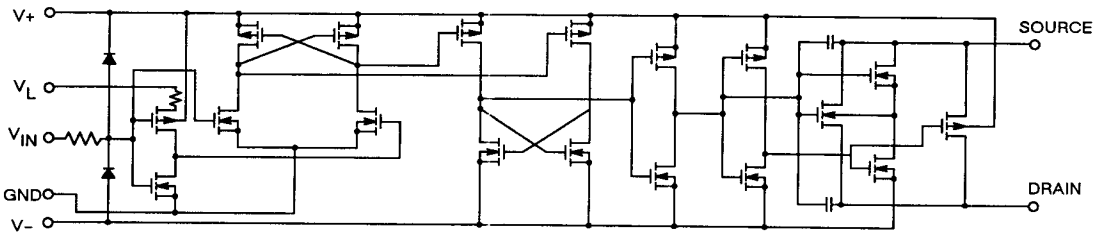


Note: All Resistors are 10 kΩ unless otherwise specified



Note: SO Package is the same as the DIP

SCHEMATIC DIAGRAM (Typical Channel)



PIN DESCRIPTION

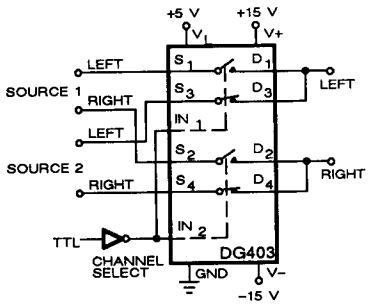
SYMBOL	DESCRIPTION
S	An Analog Channel Input or Output
D	An Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply Voltage
V-	Negative Supply Voltage
GND	Digital Ground
V_L	Logic Supply Voltage

APPLICATIONS

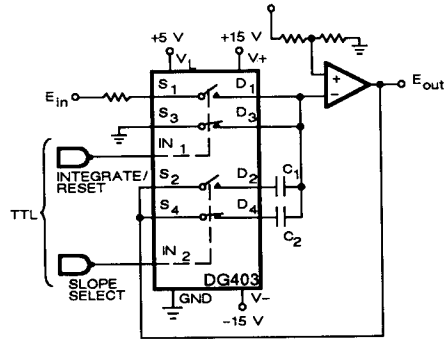
Stereo Source Selectors:
A single logic signal controls the status of all four switches of the device, simplifying stereo source switching. The low on-resistance (< 35 Ω) minimizes total harmonic distortion.

Dual Slope Integrators:
The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2. Another one selects E_{in} or discharges the capacitor in preparation for the next integration cycle.

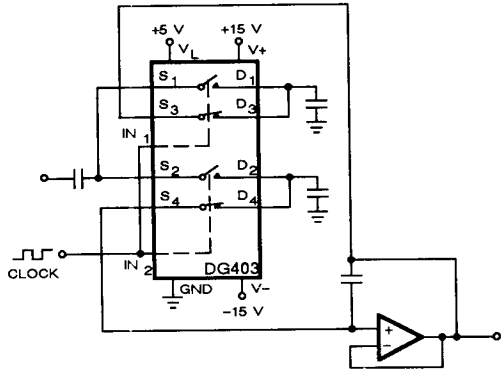
Band-Pass Switched Capacitor Filter:
Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.



Stereo Source Selector



Dual Slope Integrator



Band-Pass Switched Capacitor Filter