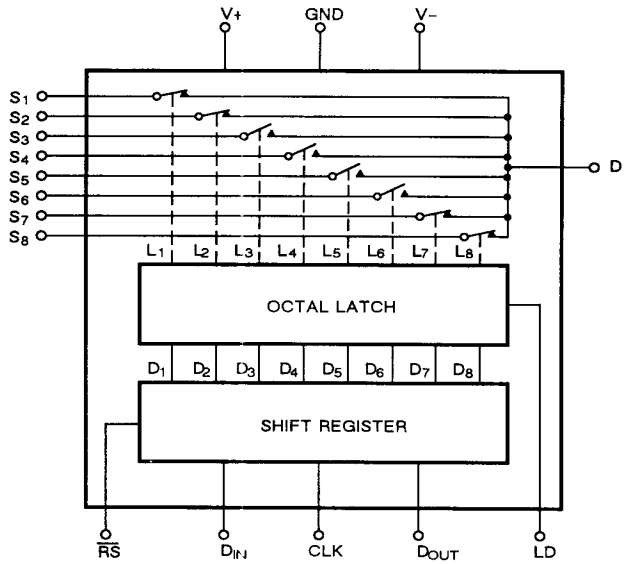
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLES

$\overline{RS}$	CLK*	D_{IN}	D_1	D_N
1	↑	0	0	D_{N-1}
1	↑	1	1	D_{N-1}
1	↓	X	D_1	D_N (NO CHANGE)
0	X	X	0	0

LD*	D_N	L_N	SW_N
↑	0	0	OFF
↑	1	1	ON
↓	D_N	L_N	(NO CHANGE)

*CLK and LD Inputs are Level Triggered

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44 V

GND to V- ..... 25 V

Digital Inputs V_S, V_D[1] ..... (V-) -2 V to (V+)+ 2 V
..... or 30 mA, whichever occurs first

Continuous Current (Any Terminal) ..... 30 mA

Current, S or D (Pulsed 1 ms, 10% duty cycle) .. 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
18-Pin CerDIP** ..... 600 mW
18-Pin Plastic DIP*** ..... 470 mW

* All leads welded or soldered to PC Board.
** Derate 9.2 mW/°C above 75°C.
*** Derate 16.5 mW/°C above 25°C.

1 Signals on Sx, Dx, or INx exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V, GND = 0 V, V_{IN} = 2.0 V, 0.8 V [e]	LIMITS 1=25°C, 2=125,85°C, 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
SWITCH									
Analog Signal Range [c]	V_{ANALOG}				-15	15	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = ±10 V, V+ = 13.5 V, V- = -13.5 V	1,3 2			75 100		75 100	Ω
Delta Drain-Source ON Resistance	$\Delta r_{DS(ON)}$	$\frac{\Delta r_{DS(ON)} = r_{DS(ON)\ MAX} - r_{DS(ON)\ MIN}}{r_{DS(ON)\ AVG}}$	1			10		10	%
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5 V, V- = -16.5 V, V_D = -14 V, V_S = 14 V	1 2		-1 -20	1 20	-1 -20	1 20	nA
	$I_{D(OFF)}$	V+ = 16.5 V, V- = -16.5 V, V_D = 14 V, V_S = -14 V	1 2		-10 -200	10 200	-10 -200	10 200	
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	V+ = 16.5 V, V- = -16.5 V, V_S = V_D = ±14 V	1 2		-20 -500	20 500	-20 -500	20 500	
INPUT									
Input Current with V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V, all other = 2.0 V	1 2		-1 -5	1 5	-1 -5	1 5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} under test = 2.0 V, all other = 0.8 V	1 2		-1 -5	1 5	-1 -5	1 5	
OUTPUT									
Output Voltage with V_{IN} Low – SO	V_{OL}	V_{IN} under test = 0.8 V, all other = 2.4 V	1,2			0.4		0.4	V
DYNAMIC									
Pulse Width for Logic	t_{LOGIC}	(D_{IN}, LD, CLK, $\overline{RS}$) See Figure	1 2		80 150		80 150		ns
Transition Time	t_{TRAN}	R_L = 1 MΩ, C_L = 35 pF, V_{S1} = 10 V, V_{S2} = -10 V, 50% of V_{LD} to 90% of V_D See Figure	1 2			200 250		200 250	
Data Setup Time	t_{DW}		1		50		50		
Break-Before-Make	t_{BREAK}	R_L = 1 kΩ, C_L = 35 pF, V_{S1} = V_{S2} = 10 V, 90% of V_D to 90% of V_D See Figure	1 2		10 20		10 20		
Turn-ON Time	t_{ON}	50% of LD, $\overline{RS}$ to 90% of V_D, R_L = 1 kΩ, C_L = 35 pF See Figure 1A	1 2			200 250		200 250	
Turn-OFF Time	t_{OFF}		1 2			150 200		150 200	

Preliminary

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, GND = 0 V, V_{IN} = 2.0 V, 0.8 V [e]	LIMITS 1=25°C 2=125,85°C 3=−55,−40°C		A SUFFIX −55 to 125°C		D SUFFIX −40 to 85°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
DYNAMIC (Cont'd)									
Charge Injection	Q	V_S = 0 V, C_L = 1000 pF	1	40					pC
OFF Isolation		R_L = 50Ω, C_L = 5 pF, f = 1 MHz	1	−65					dB
Source-OFF Capacitance	$C_{S(OFF)}$	V_{gen} = 0 V, R_{gen} = 0Ω, f = 1 MHz	1	7					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		1	55					
Drain and Source ON Capacitance	$C_{S(ON)}$ + $C_{D(ON)}$		1	200					
SUPPLY									
Positive Supply Current	I+	V+ = 16.5 V, V− = −16.5 V, V_{IN} = 0 or 5 V	1,2,3			100		100	µA
Negative Supply Current	I−		1,2,3		−1		−1		
Ground Current	I_{GND}		1,2,3		−100		−100		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.

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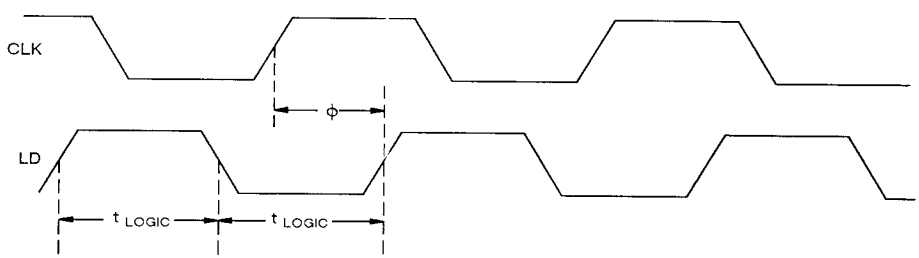
INPUT TIMING REQUIRMENTS



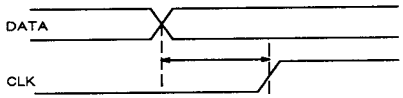
ϕ = for CLK and LD inputs of the same frequency
The recommended phase delay of LD from CLK is 1/2 t_{LOGIC} to t_{LOGIC}

t_{LOGIC}(MIN) : 80 ns at 25°C
150 ns at 125°C

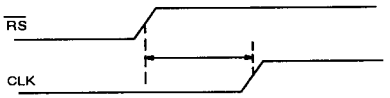
V+ = +15 V
V− = −15 V
GND = 0 V

INPUT TIMING REQUIRMENTS (Cont'd)

SHIFT REGISTER SETUP



DATA TO CLK ↑ 30 ns at 25 °C
50 ns at 125 °C

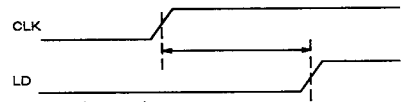


RS ↑ TO CLK ↑ 30 ns at 25 °C
50 ns at 125 °C

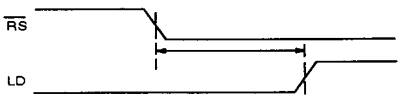
SHIFT REGISTER HOLD

DATA FROM CLK ↑ 30 ns at 25 °C
50 ns at 125 °C

ADDRESS REGISTER SETUP

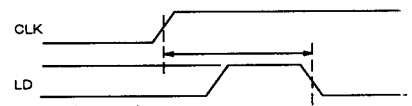


CLK ↑ TO LD ↑ 30 ns at 25 °C
50 ns at 125 °C

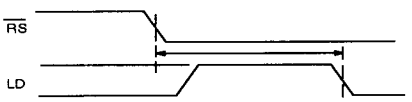


RS ↓ TO LD ↑ 30 ns at 25 °C
50 ns at 125 °C

ADDRESS REGISTER ENABLE



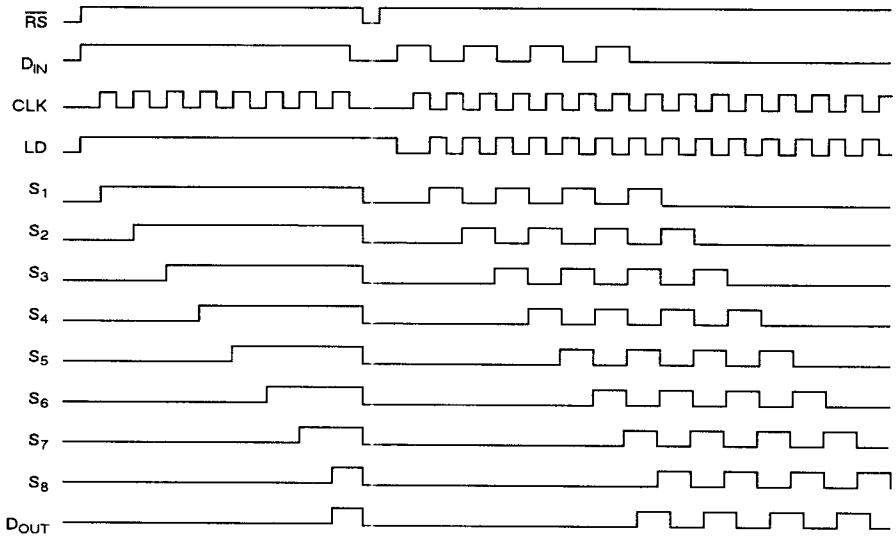
CLK ↑ TO LD ↓ 100 ns at 25 °C
150 ns at 125 °C



RS ↓ TO LD ↓ 100 ns at 25 °C
150 ns at 125 °C

V+ = +15 V, V− = - 15 V, GND = 0 V
INPUTS ARE 0 V TO 3 V

TIMING DIAGRAM



$S_1 - S_8$ and D_{OUT} are expected output with the drain connected high.
The sources require pull-downs of 1 kΩ .

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