80C51PX

CMOS Piggy Back for MHS 80C51/C52/C154/C154D

Introduction

The MHS 80C51PX are piggy back devices for all the MHS microcontrollers 80C51, 80C52, 83C154 and 83C154D.

That piggy back devices represent an efficient tool which allows designers to do the most realistic software evaluation in a short time without additional hardware. The EPROM containing the software is plugged in the socket on the top of the device. Thus, successive versions of software can be evaluated and the optimum solution found by using real time evaluation and by reducing the turn-around time of development.

The piggy back may then be replaced by an MHS microcontroller with on-chip program memory without any re-design of the board, since MHS 80C51PX are pin-to-pin compatible with MHS microcontrollers.

- 80C51P4 : Piggy back for MHS 80C51 (4 K bytes of ROM)
- 80C51P8 : Piggy back for MHS 80C52 (8 K bytes of ROM)
- 80C51P16 : Piggy back for MHS 83C154 (16 K bytes of ROM)
- 80C51P32 : Piggy back for MHS 83C154D (32 K bytes of ROM)

Features

- Fully static design
- F = 0 to 12 MHz
- Vcc = 5 V ± 10 %
- High Performance CMOS Process
- Temperature Range : Commercial
- Each 80C51PX is compatible with the associated MHS micro controller

Interface

Figure 1. Block Diagram

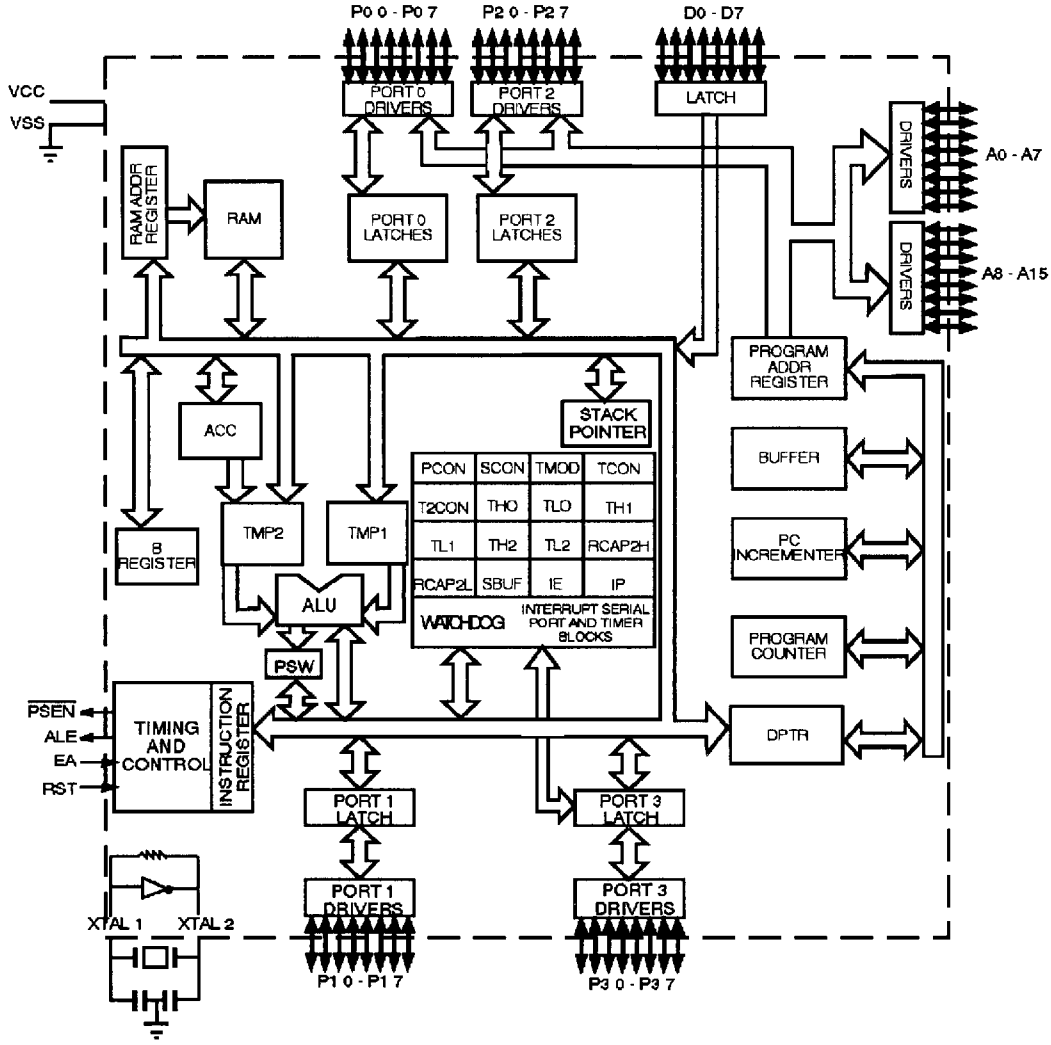
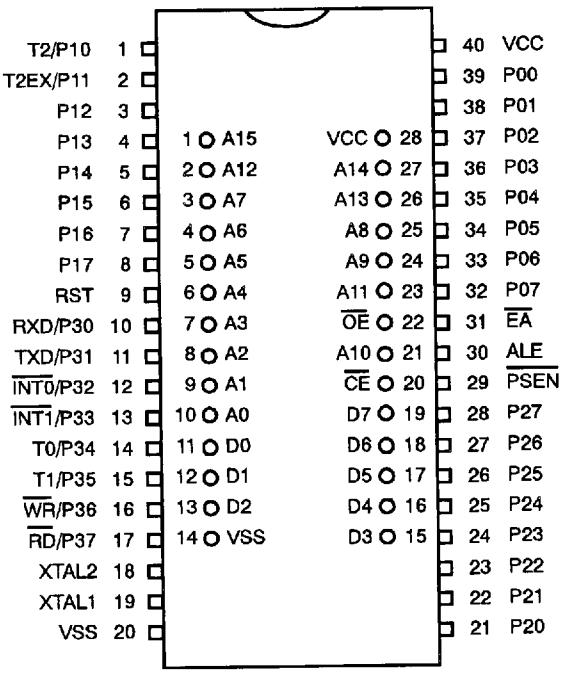


Figure 2. Pin Configuration



Diagrams are for reference only. Package sizes are not to scale.

Pin Description

The pin configuration of the bottom of the MHS 80C51PX is the same as for the associated MHS microcontroller (Dual In Line package).

For the top of the piggy back the pin configuration depends on the version.

Table 1 : How to choose 80C51PX.

PIGGY BACK	MCU	EPROM
80C51P4	80C51	27C64*
80C51P8	80C52	27C64
80C51P16	83C154	27C128
80C51P12	83C154D	27C256

* Only 4 k bytes are used.

The table 1 shows how to choose the right version of the MHS 80C51PX. Table 2 shows the pin configuration of the top of the device.

When used on piggy back, EPROMs are always in Read mode. So the following top pins have to be at Vcc :

– pin 1 on 80C51P4, P8, P16 and P32 (VPP)

– pin 27 on 80C51P4, P8 and P16 (PGM)

That means the EPROM must be chosen exclusively according to the piggy back version used.

Figure 3. Top Pin Configuration.

P4	P8	P16	P32
VCC	VCC	VCC	VCC
A12	A12	A12	A12
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O0	O0	O0	O0
O1	O1	O1	O1
O2	O2	O2	O2
GND	GND	GND	GND

P4	P8	P16	P32
VCC	VCC	VCC	VCC
VCC	VCC	VCC	A14
NC	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
A11	A11	A11	A11
OE	OE	OE	OE
A10	A10	A10	A10
CE	CE	CE	CE
O7	O7	O7	O7
O6	O6	O6	O6
O5	O5	O5	O5
O4	O4	O4	O4
O3	O3	O3	O3

Status of External Pins During Idle Mode

	BOTTOM PINS						TOP PINS			
PROGRAM MEMORY	ALE	PSEN	PORT0	PORT1	PORT2	PORT3	CE	OE	A0-A15	D0-D7
INTERNE	1	1	DATA	DATA	DATA	DATA	1	1	ADDRESS	FLOAT
EXTERNE	1	1	FLOAT	DATA	ADDRESS	DATA	1	1	ADDRESS	FLOAT

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in *figure 3*. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in *figure 4*. There is no requirement on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

Figure 4. Crystal Oscillator

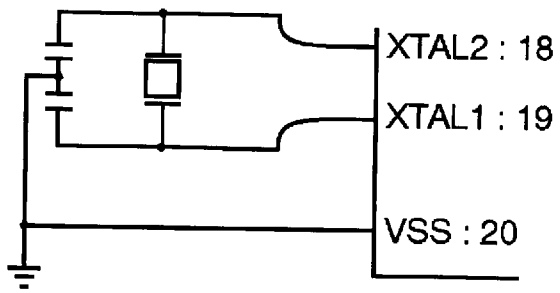
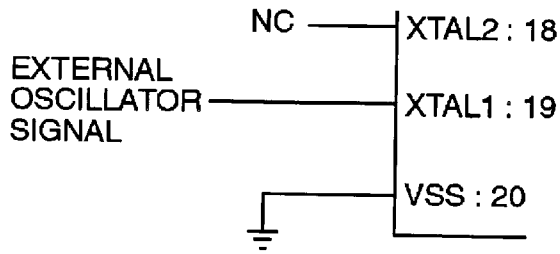


Figure 5. External Drive Configuration



Internal Program Memory Access

Fetches from EPROM program memory use 12 to 15 bit-address. So the on-chip Program Memory can be up to 32K bytes.

The signal $\overline{OE}$ enables datas output on pins D0-D7.

The $\overline{CE}$ allows the EPROM power control.

The control pins $\overline{CE}$ and $\overline{OE}$ are logically inactive under following conditions :

- during external RAM accesses (MOVX inst.)

- if EA = 0 or if the program counter contains an address greater than on-chip program memory capacity :

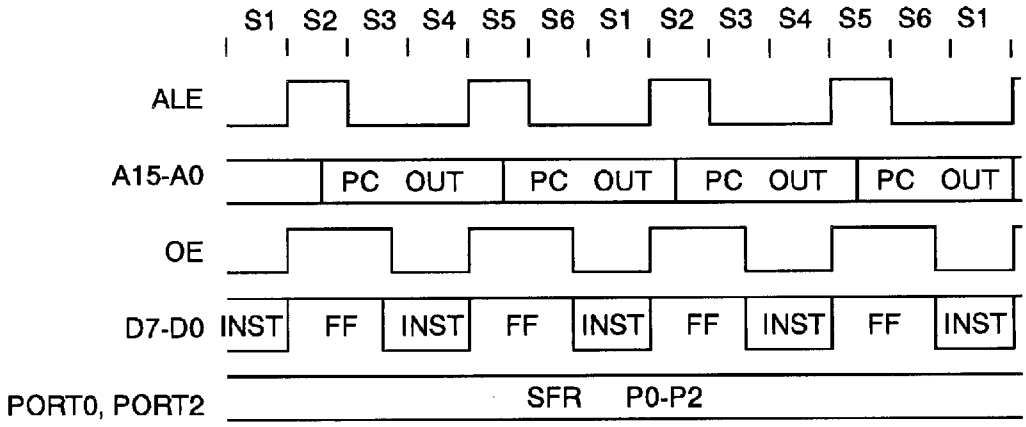
4K on 80C51P4
8K on 80C51P8
16K on 80C51P16
32K on 80C51P32

Datas pins D0-D7 are pulled high by internal pull-up.

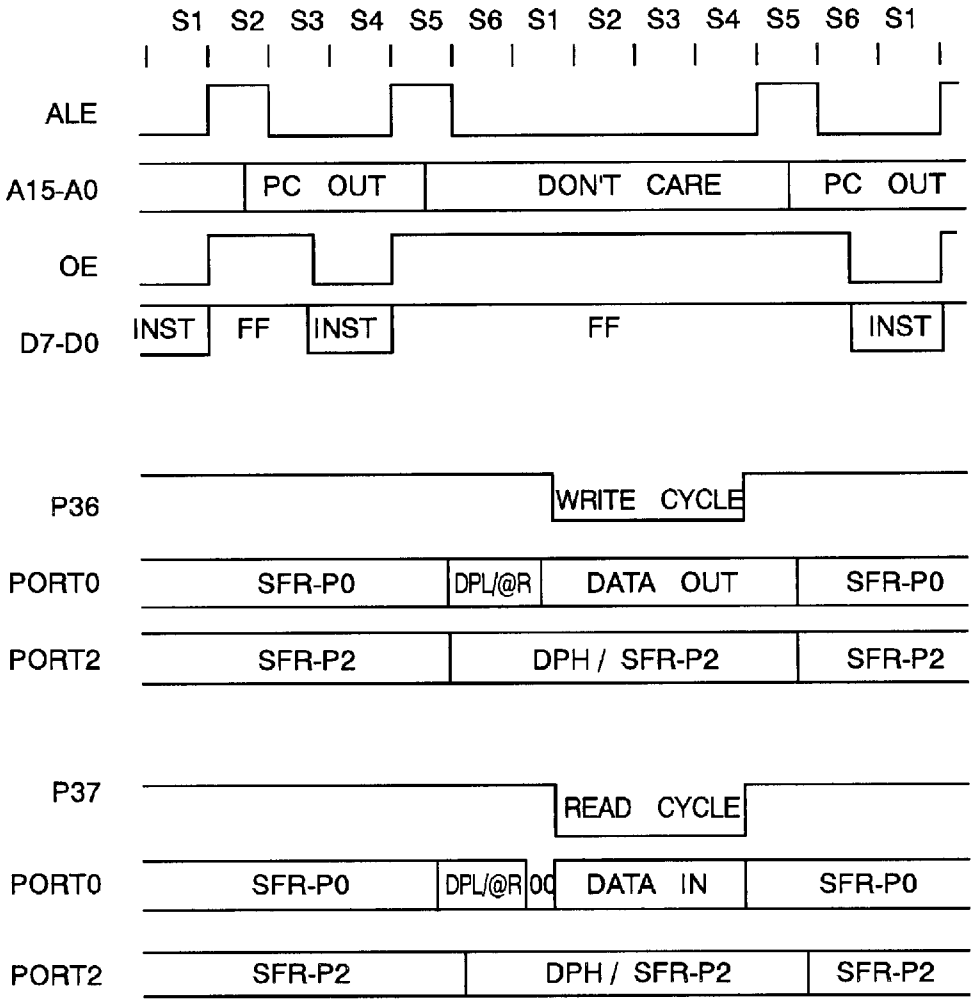
They will sink current (IIL) when externally pulled low by reading "0" from EPROM.

Figure 6.

INTERNAL PROGRAM MEMORY READ CYCLE – without MOVX instruction



INTERNAL PROGRAM MEMORY READ CYCLE – with MOVX instruction



Electrical Characteristics

Absolute Maximum Ratings

Operating Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... –65°C to 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 mW(1)
(1) This value is based on the maximum allowable die temperature and the thermal resistance of the package.

**** Notice***

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Characteristics

T_A = 0°C to 70°C ; VCC = 5 V ± 10 % ; VSS = 0 V ; F = 12 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 VCC – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 VCC + 0.9	VCC + 0.5	V	
VIH1	Input High Voltage XTAL and RST	0.7 VCC	VCC + 0.5	V	
VOL	Output Low Voltage Ports 1, 2, 3, A0–A15		0.45	V	IOL = 1.6 mA (Note 3)
VOL1	Output Low Voltage Port0, ALE, PSEN		0.45	V	IOL = 3.2 mA (Note 3)
VOL2	Output Low Voltage OE, CE		0.45	V	IOL = 2.0 mA (Note 3)
VOH	Output High Voltage Ports 1, 2, 3, A0–A15, OE, CE	0.9 VCC		V	IOH = – 10 µA
		0.75VCC		V	IOH = – 25 µA
		2.4		V	IOH = – 60 µA
VOH1	Output High Voltage Port0, Ale, Psen	0.9VCC		V	IOH = – 40 µA
		0.75VCC		V	IOH = – 150 µA
		2.4		V	IOH = – 400 µA
IIL	Logical 0 Input Current Ports 1, 2, 3, D0–D7		– 50	UA	VIN = 0.45 V
ILI	Input Leakage Current Port0, ALE, PSEN		± 10	UA	0.45 < VIN < VCC
ITL	Logical 1 To 0 Transition Current Ports 1, 2, 3		– 650	UA	VIN = 2V
RRST	Rst Pulldown Resistor	50	150	KΩ	
CIO	Capacitance of IO Buffers		10	PF	FC = 1MHz, TA = 25°C
ICC	Power Supply Current Active Mode 12 MHz Idle Mode 12 MHz		28 8	MA MA	(Notes 1, 2)

Note 1 : See figures 7 to 9 for ICC test conditions.

Note 2 : Operating ICC is mesured with all output pins disconnected ;

XTAL1 driven with TCLCH, TCLCL = 5 ns, VIL = VSS + 0.5 V, VIH = 5 V -0.5 V ; XTAL2 N.C. ; EA = RST = PORT 0 = VCC ; D0 -D7 disconnected ;

ICC would be slightly higher if a crystal oscillator is used.

Idle ICC is mesured with all output pins disconnected ; XTAL1 driven with TCLCH, TCLCL = 5 ns, VIL = VSS + 0.5 V, VIH = 5 V -0.5 V ; XTAL2 N. C. ; Port 0 = VCC ; EA = RST = VSS ; D0-D7 disconnected.

Note 3 : Capacitance loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V0L of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and 2 pins when these pins make 1 to 0 transitions during bus operations.

In the worst cases (capaciting loading 100pF), the noise pulse on the ALE line may exceed 0.45 V with maxi V0L peak 0.6 V.A Schmitt Trigger use is not necessary.

Figure 7. ICC Test Condition, Idle Mode. All other pins are disconnected.

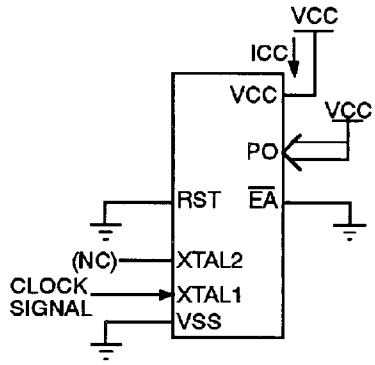


Figure 8. ICC Test Condition, Active Mode. All other pins are disconnected.

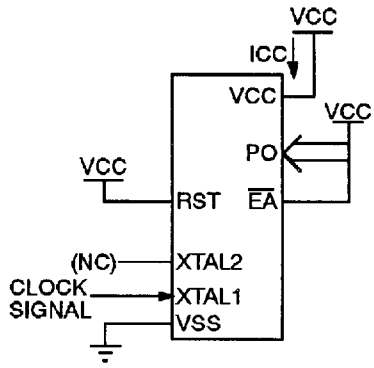
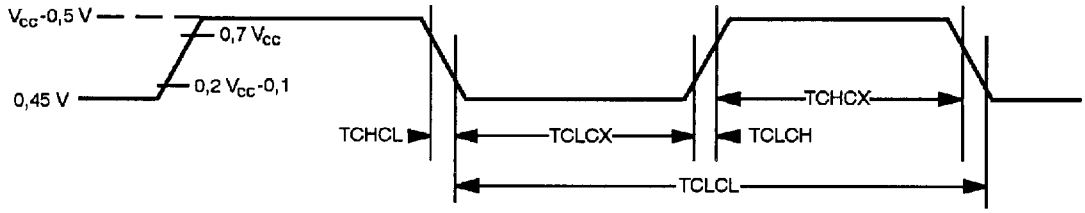


Figure 9. Clock Signal Waveform for ICC Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.



External Clock Drive Characteristics (XTAL 1)

SYMBOL	PARAMETER	VARIABLE CLOCK FREQ = 0 to 12 MHz		UNIT
		MIN	MAX	
TCLCL	Oscillator Period	83		ns
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

AC Parameters

TA = 0 to +70°C ; VSS = 0 V ; VCC = 5 V ± 10 % ; 0 to 12 MHz
(Load Capacitance for PORT 0, ALE and PSEN = 100 pf ; Load Capacitance for all other outputs = 80 pf)

External Program Memory Characteristics

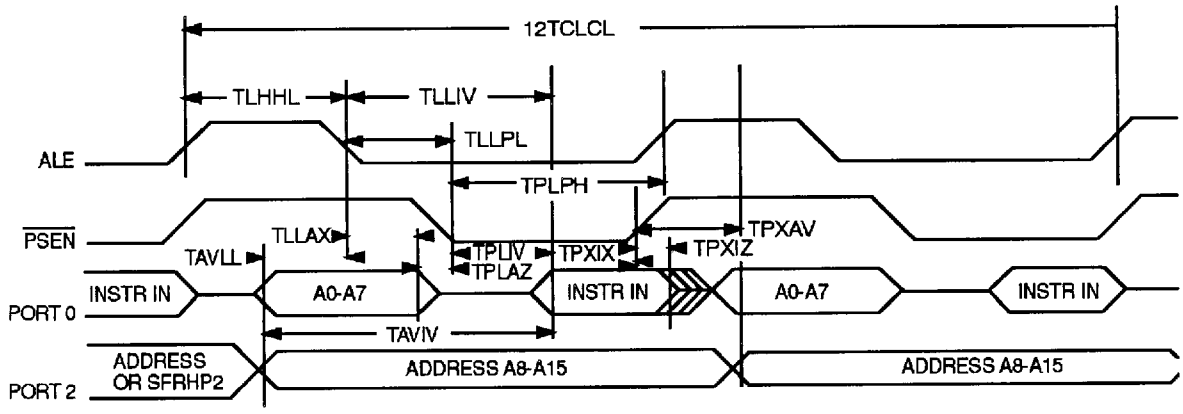
SYMBOL	PARAMETER	0 TO 12 MHz	
		MIN	MAX
TLHLL	ALE pulse width	2TCLCL-40	
TAVLL	Address Valid to ALE	TCLCL-40	
TLLAX	Address Hold After ALE	TCLCL-30	
TLLIV	ALE to Valid instr in		4TCLCL-100
TLLPL	ALE to PSEN	TCLCL-30	
TPLPH	PSEN Pulse Width	3TCLCL-45	
TPLIV	PSEN to Valid Instr IN		3TCLCL-105
TPXIX	Input Instr Hold After PSEN	0	
TPXIZ	Input Inst Float After PSEN		TCLCL-25
TPXAV	PSEN to Address Valid	TCLCL-8	
TAVIV	Address to Valid Instr In		5TCLCL-105
TPLAZ	PSEN Low to Address Float		10

External Data Memory Characteristics

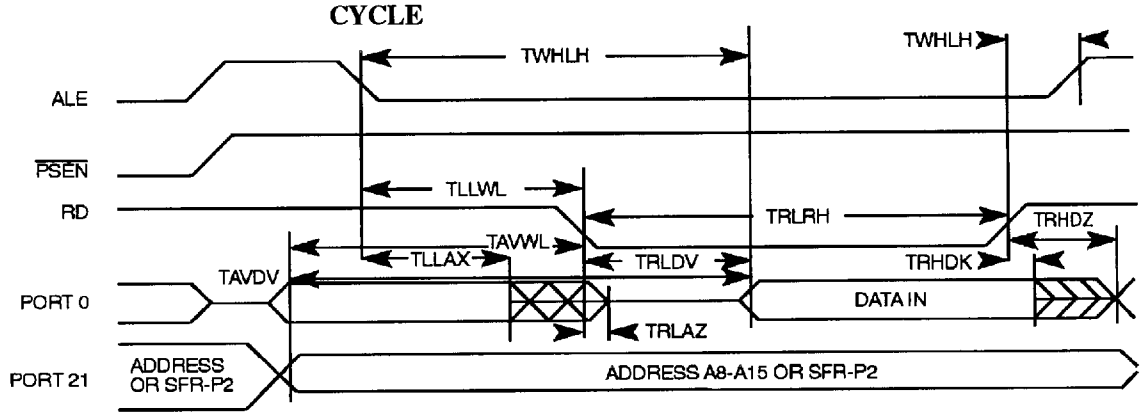
SYMBOL	PARAMETER	0 TO 12 MHz	
		MIN	MAX
TRLRH	RD Pulse Width	6TCLCL-100	
TWLWH	WR Pulse Width	6TCLCL-100	
TLLAX	Data Addr. Hold After ALE	TCLCL-35	
TRLDV	RD to Valid Data In		5TCLCL-165
TRHDX	Data Hold After RD	0	
TRHDZ	Data Float After RD		2TCLCL-60
TLLDV	ALE to Valid Data In		8TCLCL-150
TAVDV	Address to Valid Data In		9TCLCL-165
TLLWL	ALE to WR or RD	3TCLCL-50	3TCLCL+50
TAVWL	Address to WR or RD	4TCLCL-130	
TQVWX	Data Valid to WR Transition	TCLCL-50	
TQVWH	Data Set-Up to WR High	7TCLCL-150	
TWHQX	Data Hold After WR	TCLCL-50	
TRLAZ	RD Low to Address Float		0
TWHLH	RD or WR High to ALE High	TCLCL-40	TCLCL+40

AC Timing Diagrams

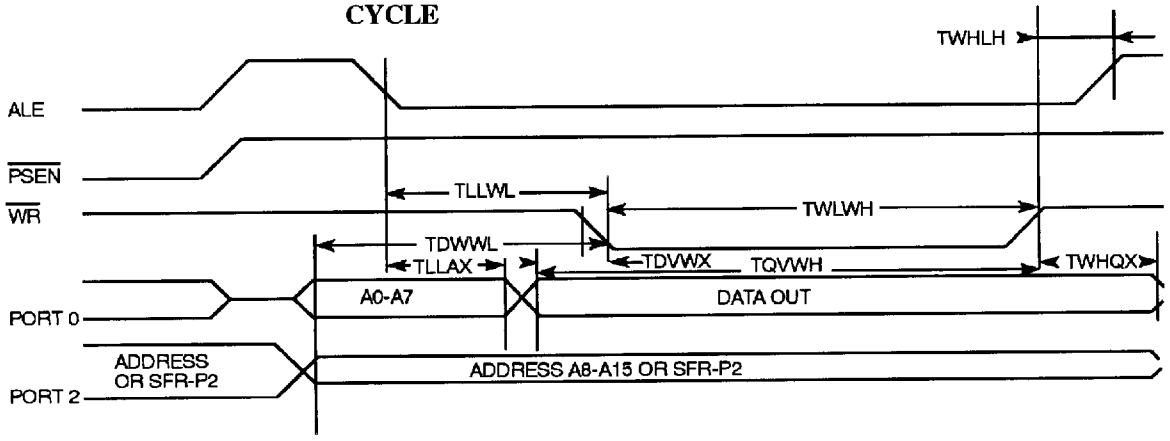
EXTERNAL PROGRAM MEMORY CYCLE



EXTERNAL DATA MEMORY READ CYCLE

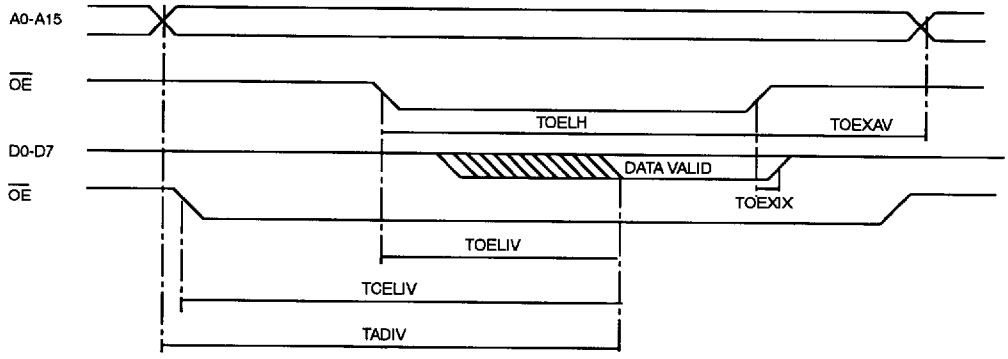


EXTERNAL DATA MEMORY WRITE CYCLE



Internal Program Memory Characteristics

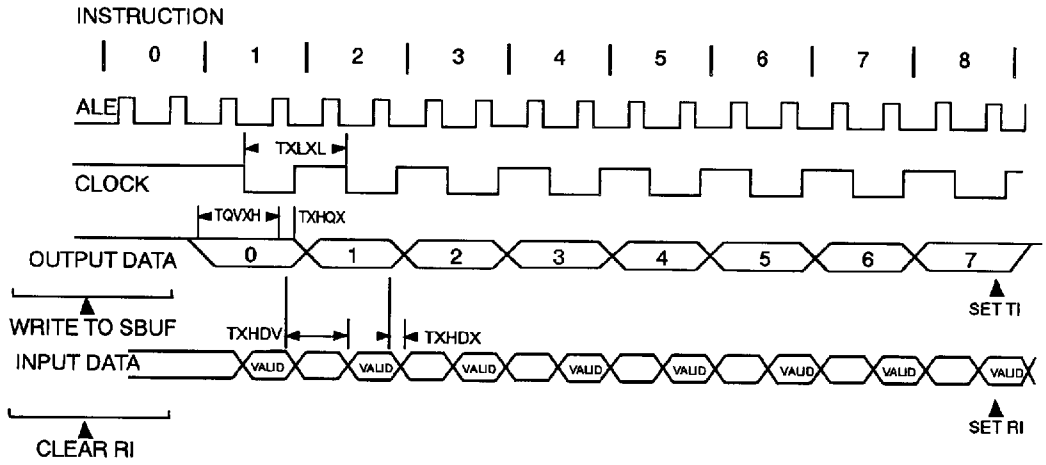
SYMBOL	PARAMETER	MIN	MAX	UNITS
TOELH	OE Pulse Width	3TCLCL-45		NS
TOELIV	OE Low to Valid Instr. In		3TCLCL-105	NS
TOEXIX	Input Instr. Hold after OE	0		NS
TOEXAV	OE to Address Valid	TCLCL-8		NS
TCELIV	CE Low to Valid Instr. In		5TCLCL-105	NS
TADIV	Address to Valid Instr. In		5TCLCL-105	NS



Serial Port Timing – Shift Register Mode

TA = 0 to 70°C ; VSS = 0 V ; VCC = 5 V ± 10 % ; 0 to 12 MHz

SYMBOL	PARAMETER	0 TO 12 MHz	
		MIN	MAX
TXLXL	Serial part clock cycle time	12TCLCL	
TQVHX	Output data setup to clock rising edge	10TCLCL-133	
TXHQX	Output data hold after clock rising edge	2TCLCL-117	
TXHDX	Input data hold after clock rising edge	0	
TXHDV	Clock rising edge to input data valid		10TCLCL-133



Explanation of the AC Symbol

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal is a list of all the characters and what they stand for.

Example :

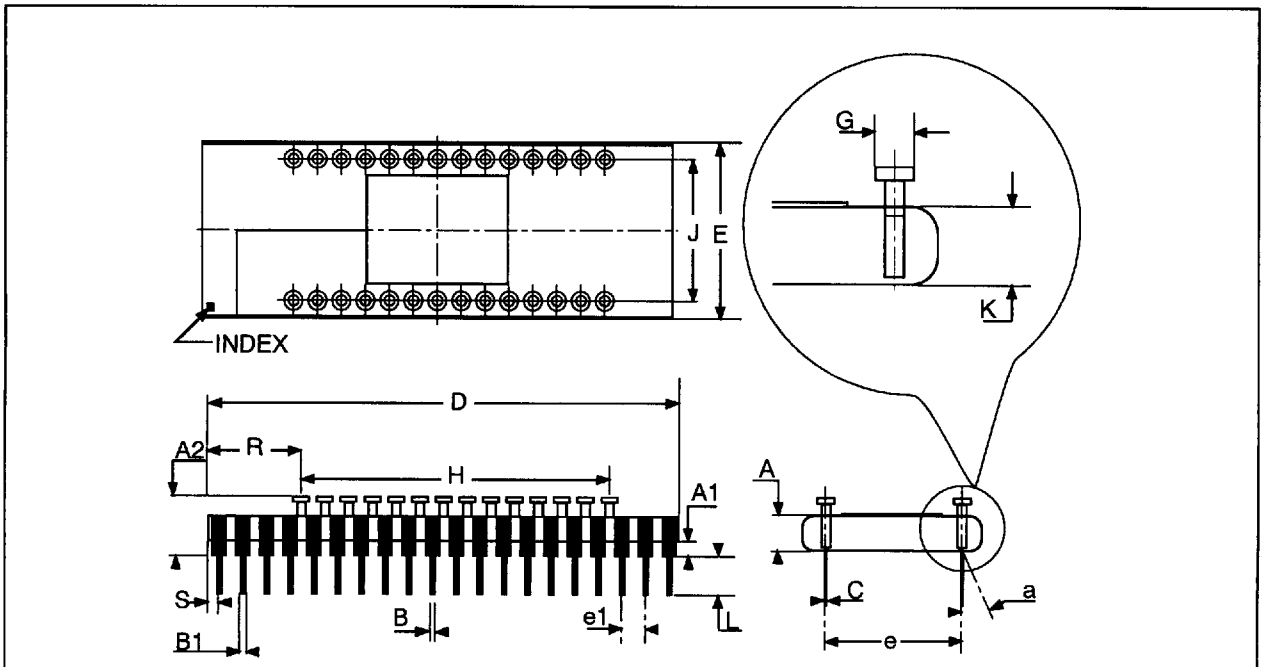
TAVLL = Time for Address Valid to ALE low.

TLLPL = Time for ALE low to $\overline{\text{PSEN}}$ low.

A : Address.	Q : Output data.
C : Clock.	R : READ signal.
D : Input data.	T : Time.
H : Logic level HIGH	V : Valid.
I : Instruction (program memory contents).	W : WRITE signal.
L : Logic level LOW, or ALE.	X : No longer a valid logic level.
P : PSEN.	Z : Float.

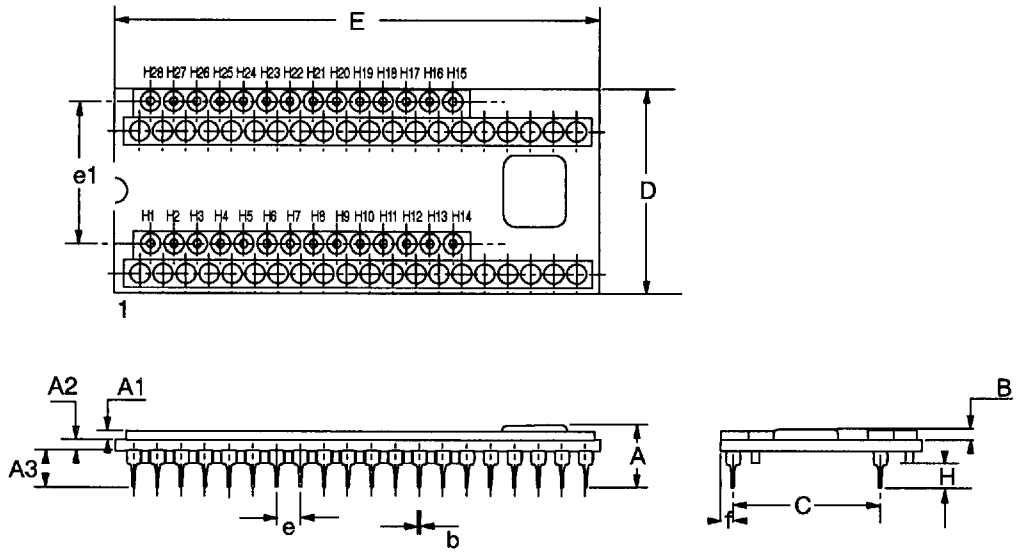
Packaging

Ceramic



	MM		INCH	
A	2.72	3.45	.107	.136
A1	1.02	1.52	.040	.060
A2	6.20	7.76	.244	.305
B	0.39	0.53	.015	.020
B1	0.92	1.12	.036	.044
C	0.23	0.35	.690	.730
D	49.51	51.01	1.95	2.00
E	18.75	19.25	.738	.757
G	1.83 REF		.072 REF	
H	32.67	33.67	1.29	1.31
J	15.04	15.44	.592	.607
K	2.47	3.13	.097	.123
L	3.18	4.44	.125	.175
R	8.32	–	.327	–
S	0.45	–	.017	–
a	0°	15°	0°	15°
e	14.94	15.54	.588	.612
el	2.54 BSC		.100 BSC	

40 LDS Chip on Board



	MM		INCH	
	MIN	MAX	MIN	MAX
A	7.3	7.7	.288	.303
A1	1.6	2	.063	.079
A2	1.5	1.7	.059	.067
A3	3.7	4	.146	.157
C	15	15.5	.590	.610
D	20.5	21.5	.807	.846
E	51.5	52.5	2.027	2.067
H	2.8	3	.110	.118
e	2.5	2.6	.098	.102
e1	15	15.5	.590	.610
f	1.3	1.7	.051	.067
B	1.8	2.1	.071	.083
b	0.48 TYP		0.019 TYP	

80C51PX

Ordering Information