MirrorBit Quick Reference Guide

July 2003

The following document refers to Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

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MirrorBit Quick Reference Guide, Fall 2002

3.0 Volt-only MirrorBit™ Flash Memory

Density	Ordering Part Number[1]					Voltage Supply	V_{IO}[4]	Page Mode	Organization	Additional Features, Sector Size/Count[5]
	Device Number	Sector	Access Times (ns)[2]	Package (Pin/Ball Count)[3]	Temp. Range					
16 Mbit	Am29LV017M	U	70, 90, 120	E (40), F (40), WC (48)	I	2.7–3.6 V	NA	N	2 M x 8	CFI. Sector size (kB): (32)64
16 Mbit	Am29LV116M	T, B	70, 90, 120	E (40), F (40)	I	2.7–3.6 V	NA	N	2 M x 8	CFI. Sector sizes (kB): 16,(2)8,32,(15)64
16 Mbit	Am29LV160M	T, B	70, 90, 120	E (48), F (48), WC (48), PC (64)	I	2.7–3.6 V	NA	N	1 M x 16, 2 M x 8	CFI. Sector sizes (kB): 16,(2)8,32,(15)64
32 Mbit	Am29LV033M	U	90R	E (40), F (40), WM (48)	I	3.0–3.6 V	3.0–3.6 V	Y	4 M x 8	CFI. Sector size (kB): (64)64
			101R			2.7–3.6 V				
			112R			1.65–3.6 V				
			120R			1.65–3.6 V				
			101			2.7–3.6 V	2.7–3.6 V			
			112			1.65–3.6 V				
			120			1.65–3.6 V				
32 Mbit	Am29LV320M	H, L	90R	E (56), F (56), PC (64)	I	3.0–3.6 V	3.0–3.6 V	Y	2 M x 16, 4 M x 8	SecSi Sector, WP#/ACC, CFI. Sector size (kB): (64)64
			101R			2.7–3.6 V				
			112R			1.65–3.6 V				
			120R			1.65–3.6 V				
			101			2.7–3.6 V	2.7–3.6 V			
			112			1.65–3.6 V				
			120			1.65–3.6 V				
		T, B	90R	E (48), WM (48), PC (64)	I	3.0–3.6 V	NA			SecSi Sector, WP#/ACC, CFI. Sector sizes (kB): (8)8,(63)64
			100R			2.7–3.6 V				
			110R			1.65–3.6 V				
			120R			1.65–3.6 V				
			100			2.7–3.6 V				
			110			1.65–3.6 V				
			120			1.65–3.6 V				
64 Mbit	Am29LV065M	U	90R	E (48), F (48), WH (63)	I	3.0–3.6 V	3.0–3.6 V	Y	8 M x 8	SecSi sector, ACC, CFI. Sector size (kB): (128)64
			101R			2.7–3.6 V				
			112R			1.65–3.6 V				
			120R			1.65–3.6 V				
			101			2.7–3.6 V	2.7–3.6 V			
			112			1.65–3.6 V				
			120			2.7–3.6 V				
64 Mbit	Am29LV640M (continued on next page)	U	90R	WH (63), PC (64)	I	3.0–3.6 V	3.0–3.6 V	Y	4 M x 16	SecSi sector, ACC, CFI. Sector size (kW): (128)32
			101R			2.7–3.6 V				
			112R			1.65–3.6 V				
			120R			1.65–3.6 V				
			101			2.7–3.6 V	2.7–3.6 V			
			112			1.65–3.6 V				
			120			1.65–3.6 V				
64 Mbit		H, L	90R	E (56), F (56), PC (64)	I	3.0–3.6 V	3.0–3.6 V	Y	4 M x 16, 8 M x 8	SecSi sector, WP#/ACC, CFI. Sector size (kB): (128)64
			101R			2.7–3.6 V				
			112R			1.65–3.6 V				
			120R			1.65–3.6 V				
			101			2.7–3.6 V	2.7–3.6 V			
			112			1.65–3.6 V				
			120			1.65–3.6 V				

Notes:

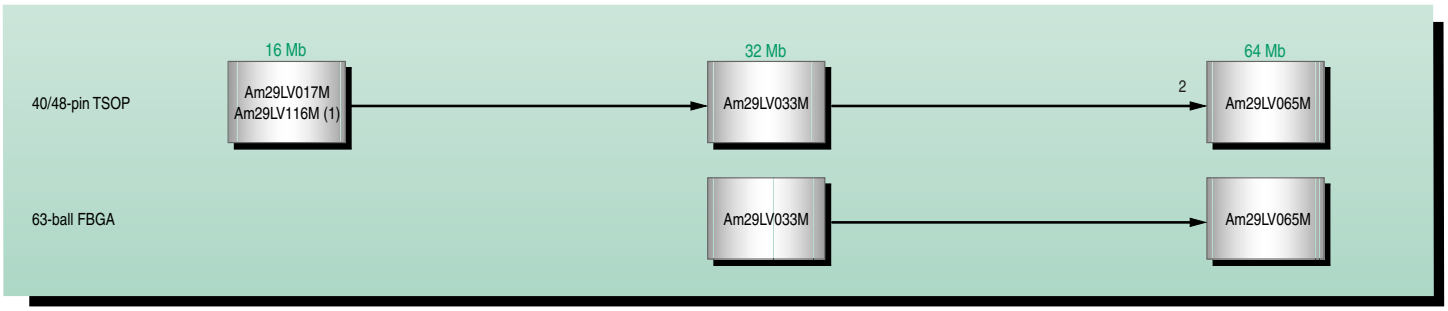
1. *Contact an AMD representative for availability. See individual data sheets for details. Some features may be pending, and specifications may be subject to change.*
2. *Access times are as follows: 90/90R = 90 ns, 101/101R = 100 ns, 112R/112 = 110 ns, 120R/120 = 120 ns.*
3. *Pin/ball count is provided in parenthesis for information only, and is not included in the actual ordering part number.*
4. *On 32 and 64 Mbit MirrorBit products, V_{IO} controls voltage levels on the DQ inputs and outputs only.*
5. ***Features:** WP# = Write protect input. ACC = Programming acceleration input. SecSi Sector = Secured Silicon (unique/random ID). CFI = Common Flash Interface.*
   ***Sector Size/Count:** Sector counts are given in parentheses. kW= kilowords, kB = kilobytes, Mb = megabits.*

Density	Ordering Part Number[1]					Voltage Supply	V_{IO}[4]	Page Mode	Organization	Additional Features, Sector Size/Count[5]
	Device Number	Sector	Access Times (ns)[2]	Package (Pin/Ball Count)[3]	Temp. Range					
64 Mbit	Am29LV640M (continued from previous page)	T, B	90R	E (48), WH (63), PC (64)	I	3.0–3.6 V	NA	Y	4 M x 16, 8 M x 8	SecSi sector, WP#/ACC, CFI. Sector sizes (kB): (8)8,(127)64
			100R			2.7–3.6 V				
			110R			1.65–3.6 V				
			120R			1.65–3.6 V				
			100			2.7–3.6 V				
			110			1.65–3.6 V				
			120			1.65–3.6 V				
64 Mbit	Am29LV641M	H, L	90R	E (48), F (48)	I	3.0–3.6 V	3.0–3.6 V	Y	4 M x 16	SecSi sector, WP#, ACC, CFI. Sector size (kW): (128)32
			101R			2.7–3.6 V				
			112R			1.65–3.6 V				
			120R			1.65–3.6 V				
			101			2.7–3.6 V	2.7–3.6 V			
			112			1.65–3.6 V				
			120			1.65–3.6 V				
128 Mbit	Am29LV128M	H, L	93R	E (56), F (56), PC (64)	I	3.0–3.6 V	3.0–3.6 V	Y	8 M x 16, 16 M x 8	WP#/ACC, CFI. Sector size (kB): (256)64
			98R			1.65–3.6 V				
			103R			3.0–3.6 V				
			108R			1.65–3.6 V				
			113R			3.0–3.6 V				
			118R			1.65–3.6 V				
			123R			3.0–3.6 V				
			128R			1.65–3.6 V				
			103			2.7–3.6 V	2.7–3.6 V			
			108			1.65–3.6 V				
			113			2.7–3.6 V				
			118			1.65–3.6 V				
			123			2.7–3.6 V				
			128			1.65–3.6 V				
256 Mbit	Am29LV256M	H, L	93R	E (56), F (56), PG (64)	I	3.0–3.6 V	3.0–3.6 V	Y	16 M x 16, 32 M x 8	WP#/ACC, CFI. Sector size (kB): (512)64
			98R			1.65–3.6 V				
			103R			3.0–3.6 V				
			108R			1.65–3.6 V				
			113R			3.0–3.6 V				
			118R			1.65–3.6 V				
			123R			3.0–3.6 V				
			128R			1.65–3.6 V				
			103			2.7–3.6 V	2.7–3.6 V			
			108			1.65–3.6 V				
			113			2.7–3.6 V				
			118			1.65–3.6 V				
			123			2.7–3.6 V				
			128			1.65–3.6 V				

Notes:

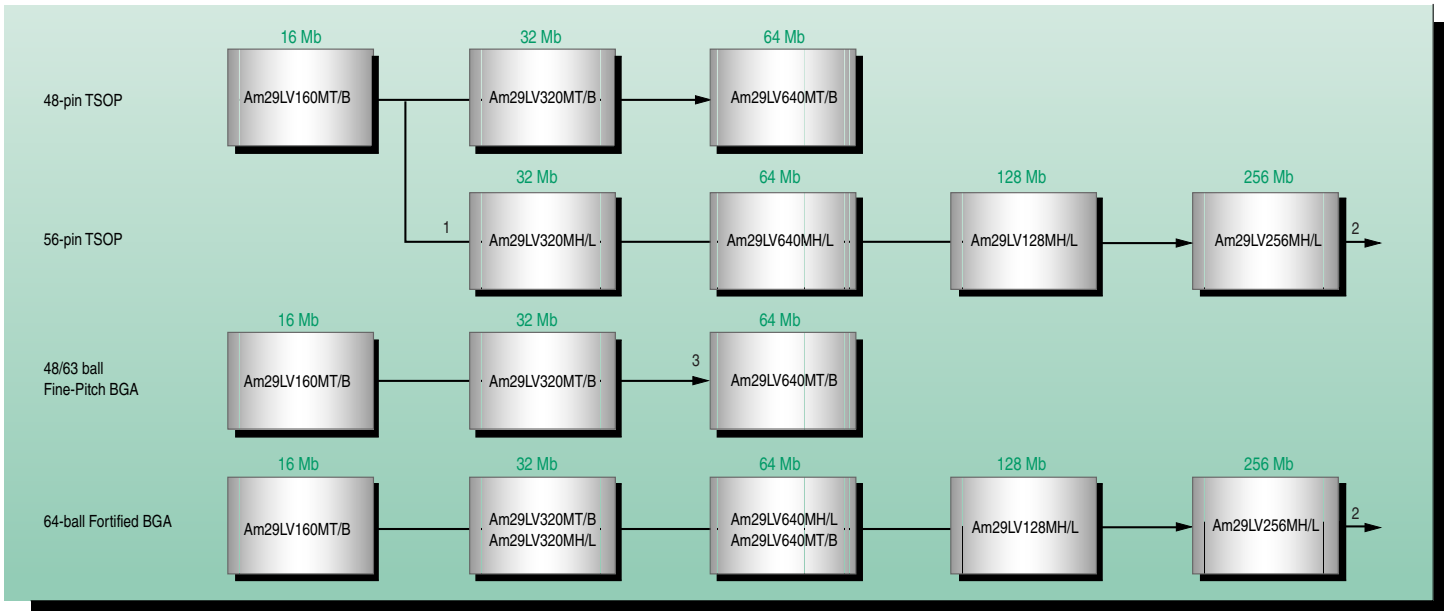
1. *Contact an AMD representative for availability. See individual data sheets for details. Some features may be pending, and specifications may be subject to change.*
2. *Access times are as follows: 90/90R = 90 ns, 101/101R = 100 ns, 112R/112 = 110 ns, 120R/120 = 120 ns.*
3. *Pin/ball count is provided in parenthesis for information only, and is not included in the actual ordering part number.*
4. *On 32 and 64 Mbit MirrorBit products, V_{IO} controls voltage levels on the DQ inputs and outputs only. On 128 and 256 Mbit MirrorBit products, V_{IO} controls voltage levels on all controls, data, and address inputs and outputs.*
5. ***Features:** WP# = Write protect input. ACC = Programming acceleration input. SecSi Sector = Secured Silicon (unique/random ID). CFI = Common Flash Interface.*
   ***Sector Size/Count:** Sector counts are given in parentheses. kW= kilowords, kB = kilobytes, Mb = megabits.*

MirrorBit Package Migration (x8 only)



Notes: *1. Am29LV116M has boot sectors; all other devices shown have uniform sectors. 2. 40- to 48-pin migration.*

MirrorBit Package Migration (x8/x16, x16 only)



Notes: *T/B = Top or bottom boot sector WP# protection. H/L = Top or bottom uniform sector WP# protection. U = Uniform sectors without WP# protection. (1) 48- to 56-pin migration. (2) MirrorBit products in these packages will include 512 Mbit and 1 Gbit devices. (3) 48- to 63-ball migration.*

AMD

MirrorBit Drop-in Compatibility

Density	MirrorBit Device	TSOP	FBGA	Conventional Flash Device
16 Mbit	Am29LV160M	E (48), F (48)	WC (48)	Am29LV160D
			PC (64)	Am29DL163D[1]
	Am29LV017M	E (40), F (40)	WC (48)	Am29LV017D
	Am29LV116M	E (40), F(40)		Am29LV116D
32 Mbit	Am29LV320MT/B	E (48)	WM (48)	Am29LV320D
			PC (64)	Am29DL323D/G
	Am29LV320MH/L	E (56), F (56)		Am29LV320D[1]
			PC (64)	Am29DL323D/G[1]
	Am29LV033M	E (40), F (40)	WC (48)	Am29LV033C
64 Mbit	Am29LV640MU		WH (63), PC (64)	Am29LV640D
	Am29LV640T/B	E (48)	WH (63), PC (64)	Am29DL640G
	Am29LV640H/L	E (56), F (56)	PC (64)	Am29DL640G[1,2,3]
	Am29LV641MH/L	E (48), F (48)		Am29LV641D
	Am29LV065MU	E (48), F (48)	WH (63)	Am29LV065D
128 Mbit	Am29LV128M		PC (64)	Am29LV642D

Notes: *1. Sector architecture differences. 2. 48-pin to 56-pin TSOP migration. 3. MirrorBit supports V_{IO}; DL640 does not support V_{IO}.*