REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes to conditions in Table I, addition of Test condition 2 in Figure 4. Editorial changes throughout.	96-11-13	Thomas M. Hess

REV																			
SHEET																			
REV	A	A	A	A	A	A	A												
SHEET	15	16	17	18	19	20	21												

REV STATUS OF SHEETS															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
95-12-28

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, CMOS, PROGRAMMABLE PERIPHERAL INTERFACE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-95819**

SHEET 1 OF 21

DESC FORM 193
JUL 94

5962-E033-97

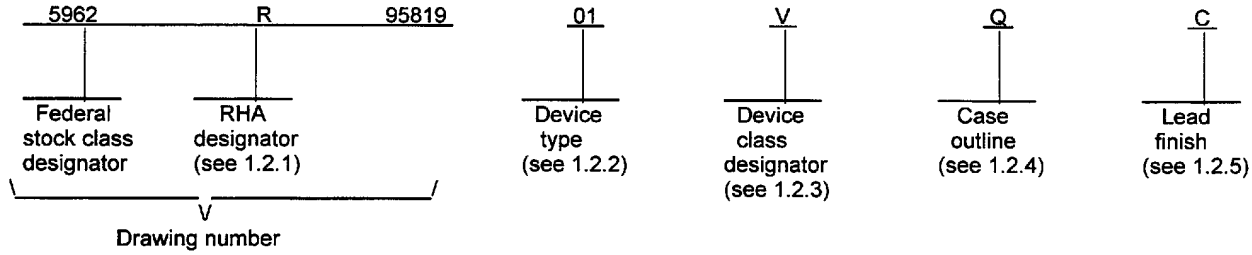
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0024943 5T0

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	82C55ARH	Radiation hardened,CMOS programmable peripheral interface

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	CDIP2-T40	40	Dual-in-line package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD})	+7.0 V dc
Input or output voltage range	V_{SS} -0.3 V dc to V_{DD} +0.3 V dc
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature (T_J)	+175°C
Lead temperature (soldering 10 seconds) (T_S)	+300 °C
Thermal resistance junction-to-case (θ_{JC}):	
Case outline X	6°C/W
Thermal resistance junction-to-ambient (θ_{JA}):	
Case outline X	40°C/W
Maximum power dissipation (P_D): 2/	
Case outline X	1.25 W

1.4 Recommended operating conditions.

Operating supply voltage range (V_{DD})	4.5 V dc to +5.5 V dc
Operating temperature range (T_A)	-55°C to +125°C
Input low voltage range (V_{IL})	0 V dc to +0.8 V dc
Input high voltage range (V_{IH})	V_{DD} -1.5 V dc to V_{DD}
Radiation features	
Total dose	> 100 k Rads(Si)
Transient upset	> 10^8 RAD(Si)/sec 3/
Single event upset	> 50 MEV/(mg/cm^2) 3/
Single event latchup	> 50 MEV/(mg/cm^2) 3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ If device power exceeds package power dissipation capability provide heat sinking or derate linearly (the derating is based on Θ_{JA}) at a rate of 25 mW/°C.
3/ Guaranteed by process or design, but not tested.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TTL output high voltage	V_{OH1}	V_{DD} = 4.5 V, I_O = -2.5 mA, V_{IN} = 0 V, 4.5 V	1,2,3	All	3.0		V
CMOS output high voltage	V_{OH2}	V_{DD} = 4.5 V, I_O = -100 µA V_{IN} = 0 V, 4.5 V	1,2,3	All	V_{DD}-0.4		V
Output low voltage	V_{OL}	V_{DD} = 4.5 V, I_O = 2.5 mA, V_{IN} = 0 V, 4.5 V	1,2,3	All		0.4	V
Input leakage current	I_{IL} or I_{IH}	V_{DD} = 5.5 V, V_{IN} = 0 V, 4.5 V	1,2,3	All	-1.0	1.0	µA
Output leakage current	I_{OZL} or I_{OZH}	V_{DD} = 5.5 V, V_{IN} = 0 V, 4.5 V	1,2,3	All	-10	10	µA
Input current bus hold high	I_{BHH}	V_{DD} = 4.5 V or 5.5 V, V_{IN} = 3.0 V 2/ Ports A,B,C	1,2,3	All	-800	-60	µA
Input current bus hold low	I_{BHL}	V_{DD} = 4.5 V or 5.5 V, V_{IN} = 1.0 V 3/ Port A	1,2,3	All	60	800	µA
Standby power supply current	I_{DDSB}	V_{IN} = GND or V_{DD} V_{DD} = 5.5 V, I_O = 0 mA,	1,2,3	All		20	µA
Darlington drive voltage	V_{DAR}	V_{DD} = 4.5 V, I_O = -2.0 mA, V_{IN} = GND or V_{DD}	1,2,3	All	3.9		V
Input capacitance	C_{IN}	See 4.4.1c V_{DD} = Open, f = 1 Mhz, All measurements referenced to device ground	4	All		10	pF
I/O capancitance	$C_{I/O}$	See 4.4.1c V_{DD} = Open, f = 1 Mhz, All measurements referenced to device ground	4	All		20	pF
Functional tests		See 4.4.1b V_{DD} = 4.5 V and 5.5 V, V_{IN} = GND or V_{DD}, f = 1 MHz	7,8	All			
Noise immunity functional test 4/		See 4.4.1b V_{DD} = 5.5 V, V_{IN} = GND or V_{DD} - 1.5 V and V_{DD} = 4.5 V, V_{IN} = 0.8 V or V_{DD}	7,8	All			

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
READ							
Address stable before $\overline{RD}$	t_{AVRL}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	0		ns
Address stable after $\overline{RD}$	t_{RHAX}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	0		ns
$\overline{RD}$ pulse width	t_{RLRH}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	250		ns
Data valid from $\overline{RD}$	t_{RLDV}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All		200	ns
Data float after $\overline{RD}$	t_{RHDX}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 2	9,10,11	All	10		ns
Time between $\overline{RD}$s and/or $\overline{WR}$s	t_{RWHRWL}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	300		ns
WRITE							
Address stable before $\overline{WR}$	t_{AVWL}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	0		ns
Address stable after $\overline{WR}$	t_{WHAX}	V_{DD} = 4.5, 5.5 V See figure 4, Ports A and B Test Condition 1	9,10,11	All	20		ns
		V_{DD} = 4.5, 5.5 V See figure 4, Port C Test Condition 1	9,10,11	All	100		ns
$\overline{WR}$ pulse width	t_{WLWH}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	100		ns
Data valid to $\overline{WR}$ high	t_{DVWH}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	100		ns
Data valid after $\overline{WR}$ high	t_{WHDX}	V_{DD} = 4.5, 5.5 V See figure 4, Ports A and B Test Condition 1	9,10,11	All	30		ns
		V_{DD} = 4.5, 5.5 V See figure 4, Port C Test Condition 1	9,10,11	All	100		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
OTHER TIMINGS							
$\overline{WR}$ = 1 to output	t_{WHPV}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All		350	ns
Peripheral data before RD	t_{PVRL}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	0		ns
Peripheral data after $\overline{RD}$	t_{RHPX}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	0		ns
$\overline{ACK}$ pulse width	t_{KLKH}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	200		ns
$\overline{STB}$ pulse width	t_{SLSH}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	100		ns
Peripheral data before STB high	t_{PVSH}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	20		ns
Peripheral data after STB high	t_{SHPX}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All	50		ns
$\overline{ACK}$ = 0 to output	t_{KLPV}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All		175	ns
$\overline{ACK}$ = 1 to output float	t_{KHPZ}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 2	9,10,11	All	10		ns
$\overline{WR}$ = 1 to $\overline{OBF}$ = 0	t_{WHOL}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All		150	ns
$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1	t_{KLOH}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All		150	ns
$\overline{STB}$ = 0 to IBF = 1	t_{SLIH}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All		150	ns
$\overline{RD}$ = 1 to IBF = 0	t_{RHIL}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All		150	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
OTHER TIMINGS							
$\overline{RD}$ = 0 to INTR = 1	t_{RLNL}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All		200	ns
$\overline{STB}$ = 1 to INTR = 1	t_{SHNH}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All		150	ns
$\overline{ACK}$ = to INTR = 1	t_{KHNH}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All		150	ns
$\overline{WR}$ = 0 to INTR = 0	t_{WLNL}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 1	9,10,11	All		200	ns
RESET pulse width	t_{RSHRSL}	V_{DD} = 4.5, 5.5 V See figure 4 5/ Test Condition 1	9,10,11	All	500		ns
Data float after $\overline{RD}$ 6/	t_{RHDX}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 2	9,10,11	All		75	ns
$\overline{ACK}$ = 1 to output float 6/	t_{KHPZ}	V_{DD} = 4.5, 5.5 V See figure 4 Test Condition 2	9,10,11	All		250	ns

1/ Devices supplied to this drawing will meet all levels M, D, L, R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ I_{BHH} should be measured after raising V_{IN} and then lowering to 3.0 V.

3/ I_{BHL} should be measured after lowering V_{IN} to V_{SS} and then raising to 0.8 V.

4/ For V_{IH}(V_{DD} = 5.5 V)and V_{IL} (V_{DD} = 4.5 V) each of the following groups is tested separately with all other inputs using V_{IH} = 2.5 V, V_{IL} = 0.4: PA, PB, PC control pins (pins 5,6,8,9,35,36).

5/ Period of initial RESET pulse after power-on must be least 50 µs. Subsequent RESET pulses may be 500 ns minimum.

6/ These parameters, are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design changes which would affect these characteristics.

Device type	01		
Case outline	Q		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	PA3	21	PB3
2	PA2	22	PB4
3	PA1	23	PB5
4	PA0	24	PB6
5	$\overline{RD}$	25	PB7
6	$\overline{CS}$	26	V_{DD}
7	GND	27	D7
8	A1	28	D6
9	A0	29	D5
10	PC7	30	D4
11	PC6	31	D3
12	PC5	32	D2
13	PC4	33	D1
14	PC0	34	D0
15	PC1	35	RESET
16	PC2	36	$\overline{WR}$
17	PC3	37	PA7
18	PB0	38	PA6
19	PB1	39	PA5
20	PB2	40	PA4

FIGURE 1. Terminal connections.

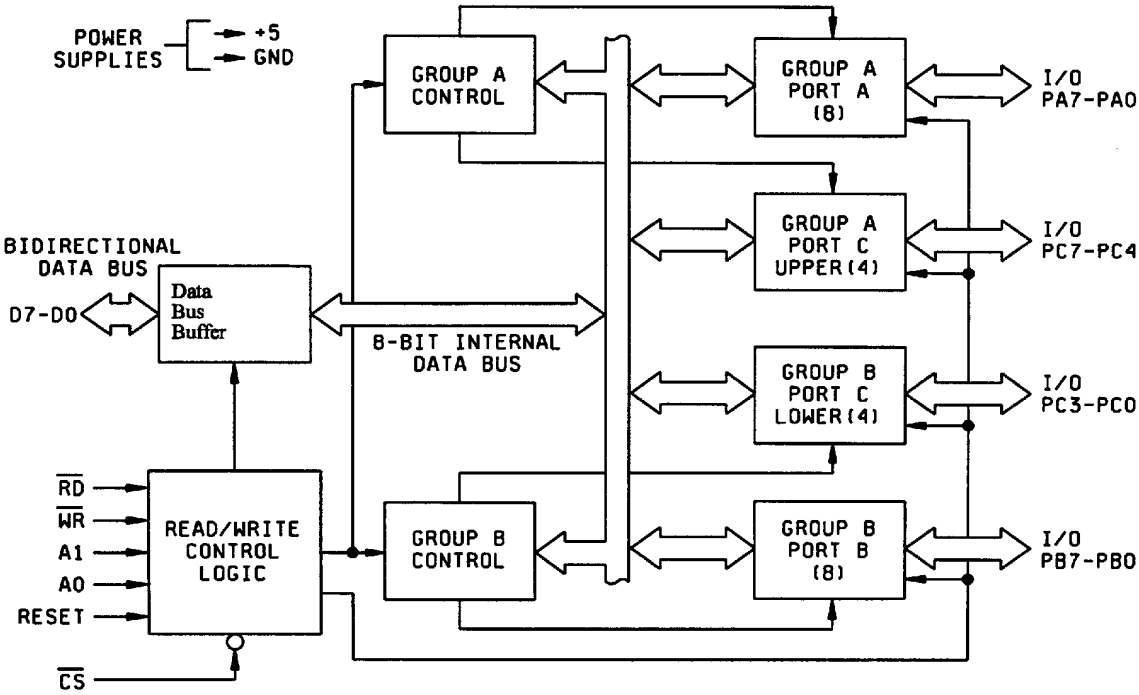
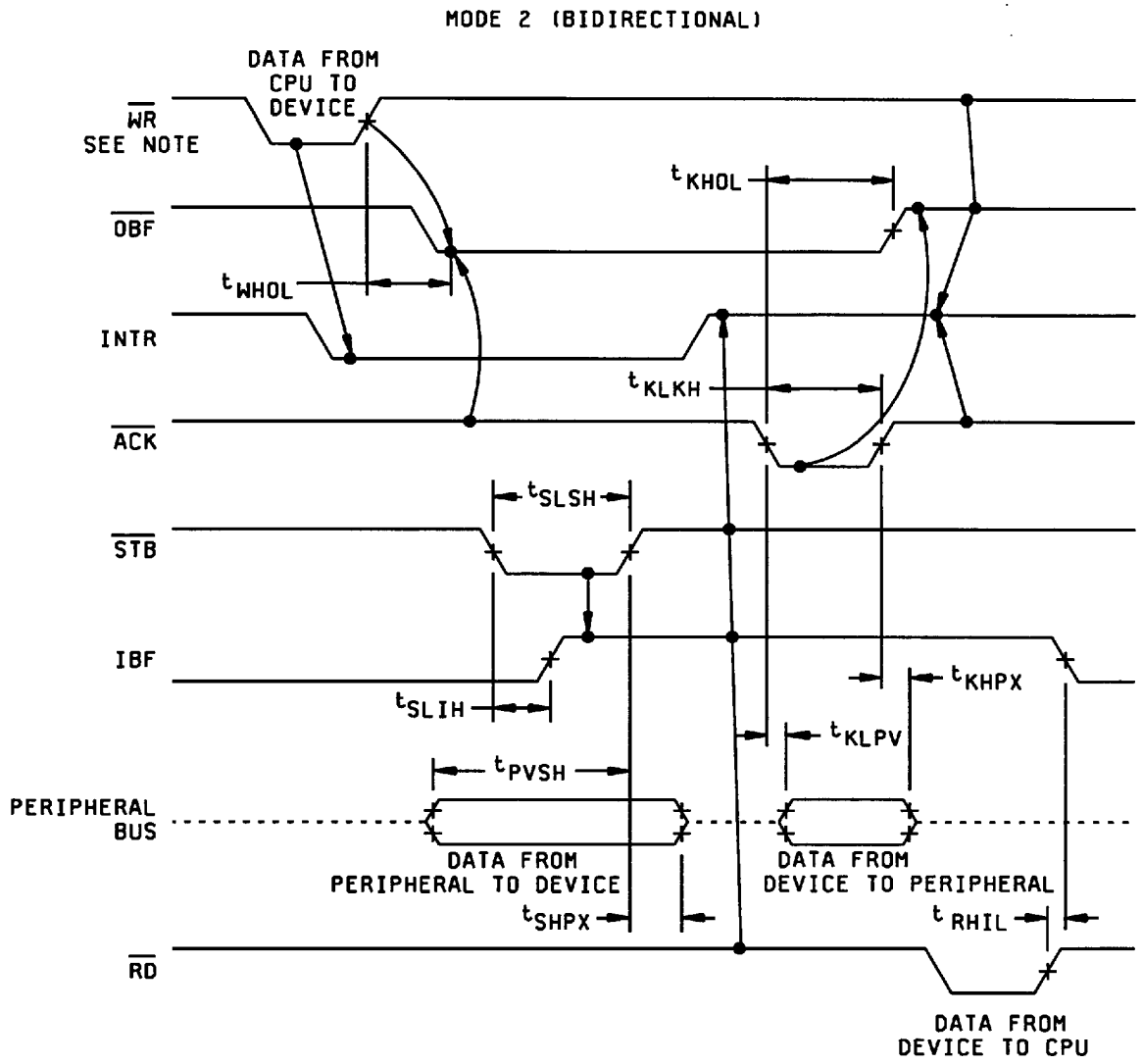


FIGURE 2. Block diagram.

Pin	Symbol	Pin	Symbol
1	V_{DD}	21	V_{DD}
2	V_{DD}	22	V_{DD}
3	V_{DD}	23	V_{DD}
4	V_{DD}	24	V_{DD}
5	V_{DD}	25	V_{DD}
6	V_{DD}	26	V_{DD}
7	GND	27	V_{DD}
8	V_{DD}	28	V_{DD}
9	V_{DD}	29	V_{DD}
10	V_{DD}	30	V_{DD}
11	V_{DD}	31	V_{DD}
12	V_{DD}	32	V_{DD}
13	V_{DD}	33	V_{DD}
14	V_{DD}	34	V_{DD}
15	V_{DD}	35	V_{DD}
16	V_{DD}	36	V_{DD}
17	V_{DD}	37	V_{DD}
18	V_{DD}	38	V_{DD}
19	V_{DD}	39	V_{DD}
20	V_{DD}	40	V_{DD}

Note: V_{DD} = 5.5 V

FIGURE 3. Radiation exposure circuit.



Note:
1. Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.

FIGURE 4. Timing waveforms.

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		REVISION LEVEL A	SHEET 12

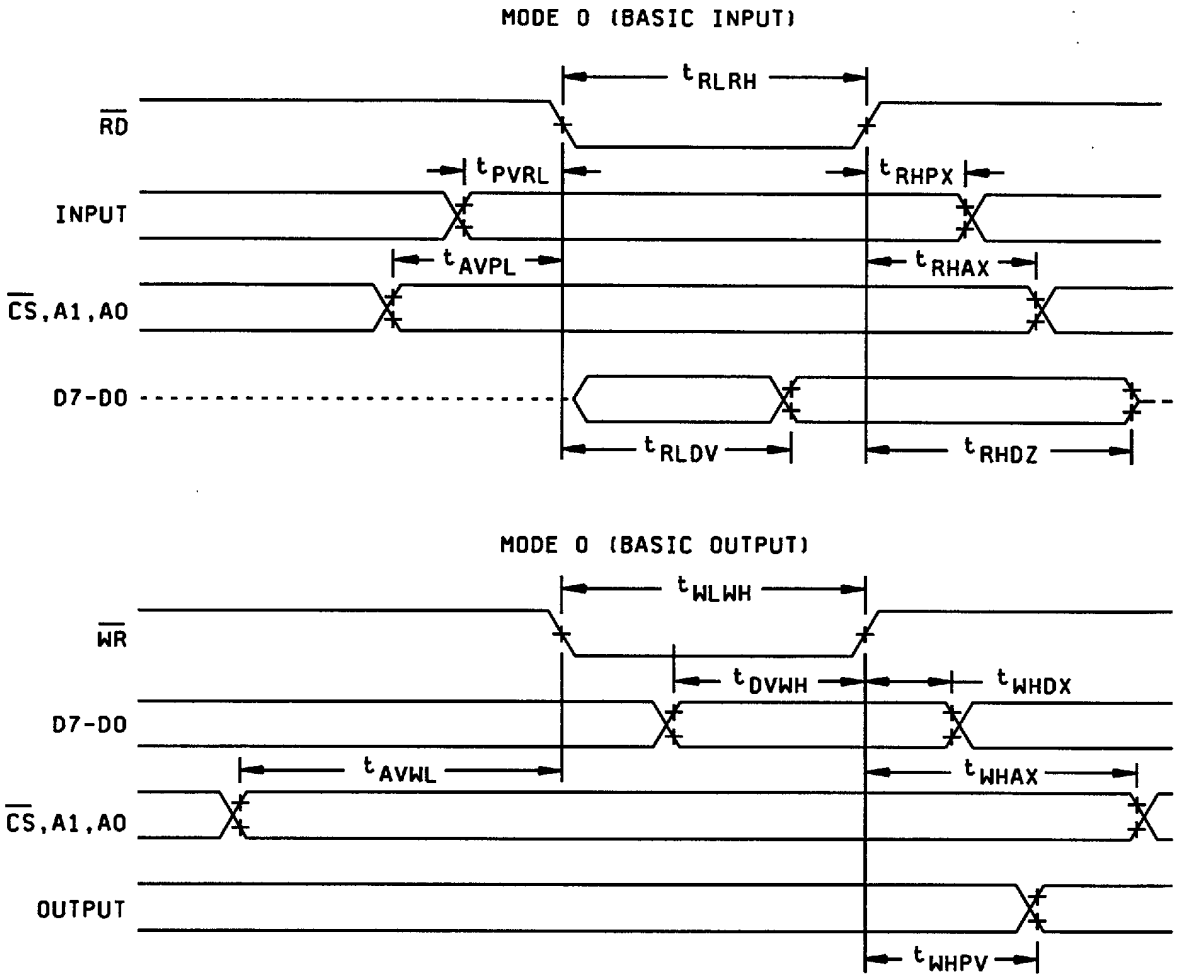
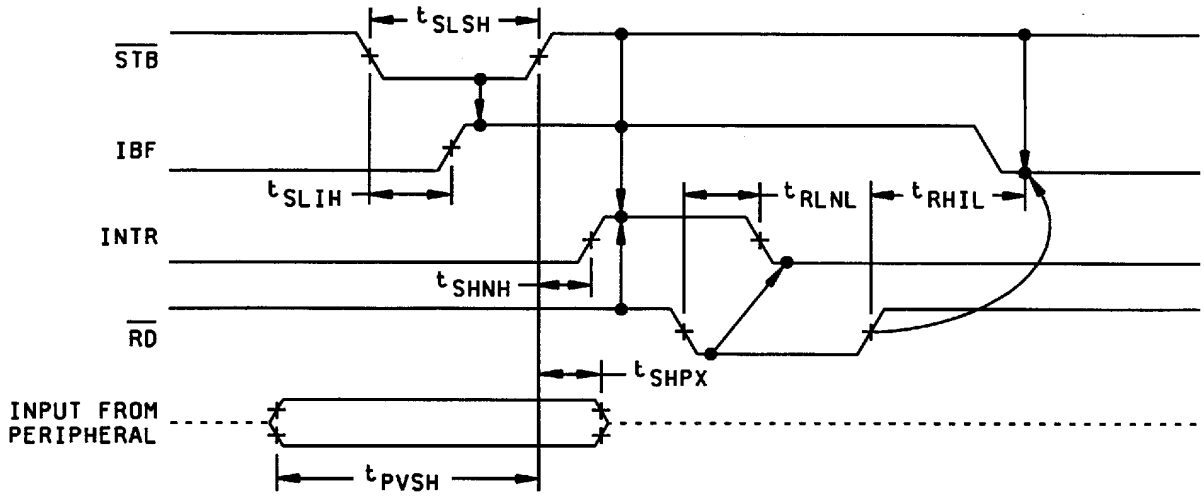
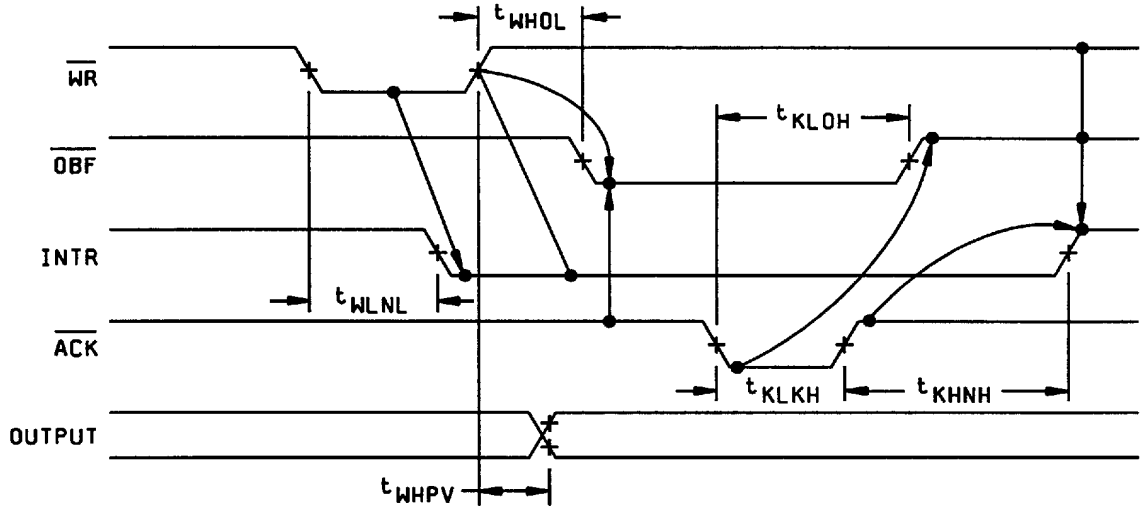


FIGURE 4. Timing waveforms. - Continued

MODE 1 (STROBED INPUT)



MODE 1 (STROBED OUTPUT)



Note:
1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The users needs to send OBF to the perifpheral device, generate an ACK from the peripheral device and then latch data inot the peripheral device on the rising edge of OBF.

FIGURE 4. Timing waveforms. - Continued

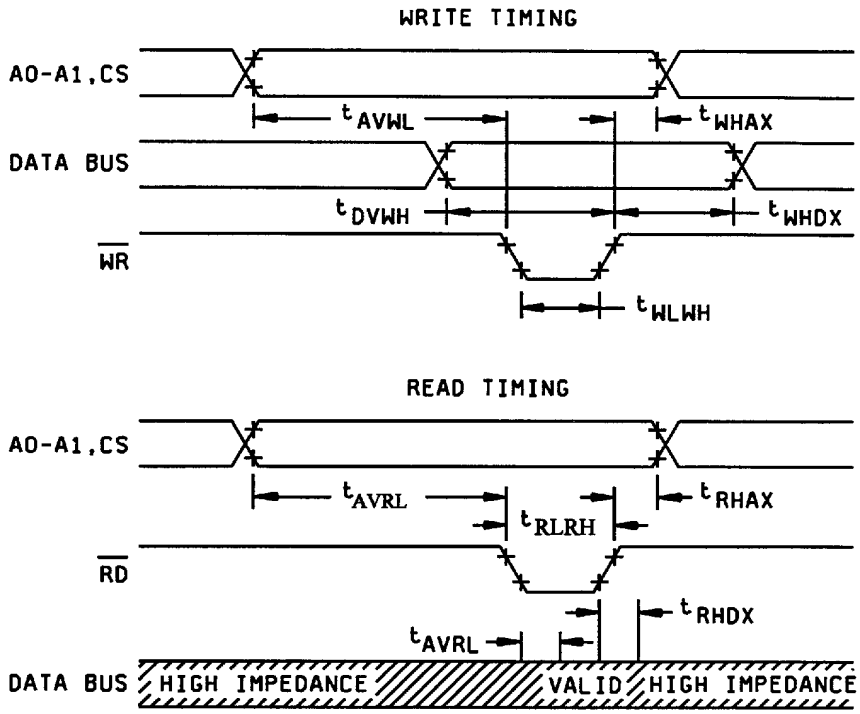
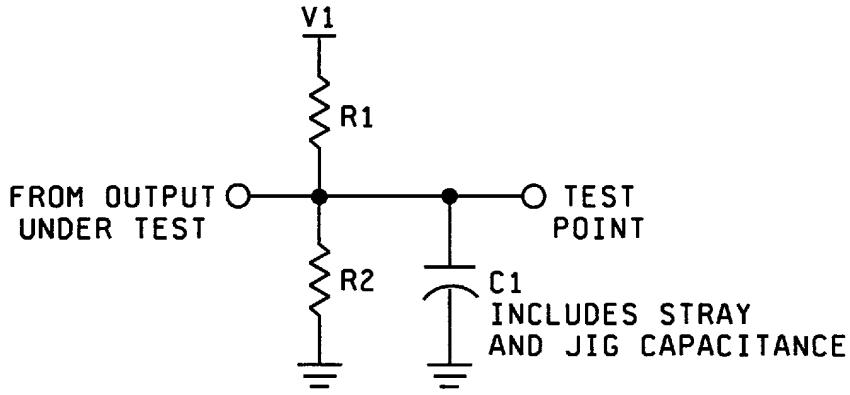
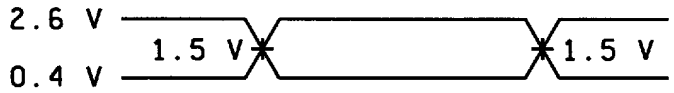


FIGURE 4. Timing waveforms. - Contined

AC TEST CIRCUIT



AC TESTING INPUT, OUTPUT WAVEFORM



Note: Input rise and fall times are driven at 1 V/ns.

Test Conditions	V_1	R_1	R_2	C_1
1	1.7 v	523 Ω	Open	150 pF
2	V_{DD}	2000 Ω	1690 Ω	50 pF

FIGURE 4. Timing waveforms. - Contined

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535, or as modified in the device manufacturers approved quality management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535, or as specified in QM plan including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN} and $C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9 1/ 10,11	1,2,3,7, 1/ 8,9,10,11	1,2,3, 2/3/ 7,8,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8, 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8,9,10,11	1,2,3,7,8,9, 10,11	1,2,3,7, 3/ 8,9,10,11
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1and 7.
2/ PDA applies to subgroups 1,7 and deltas.
3/ Delta limits as specified in Table !!B herein shall be required when specified and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in delta parameters (+25°).

Parameter	Symbol	Delta limits
Standby power supply current	I_{CCSB}	±10 µA
Input leakage current	I_{IH}, I_{IL}	±200 nA
Low level output voltage	V_{OL}	±80 mV
CMOS High level output voltage	V_{OH}	±150 mV
Output leakage current	I_{OZL}, I_{OZH}	± 2 µA
TTL output high voltage	V_{OH1}	± 600 mV

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-I-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (See 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.4). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows:

Pin symbol	Type	Description
PA0-7	I/O	Port A: General purpose I/O port. Data direction and mode is determined by the contents of the control word.
PB0-7	I/O	Port B: General purpose I/O port. See port A.
PC0-3	I/O	Port C(Lower): Combination I/O port and control port associated with port B. See port A.
PC4-7	I/O	Port C (Upper): Combination I/O port and control port associated with Port A. See port A.
D0-7	I/O	Bidirectional data bus: Three-state data bus enabled as an input when $\overline{CS}$ and $\overline{WR}$ are low and as an ouput when CS and RD are low.
V_{DD}	P	V_{DD}: The +5 V power supply pin. A 0.1 µF capacitor between pins 26 and 7 is recommended for decoupling.
GND		Ground.
$\overline{CS}$	I	Chip select: A "low" on this input pin enables the communication between the device and the CPU.
$\overline{RD}$	I	Read: A "low" on this input pin enables the device to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the device.
$\overline{WR}$	I	Write: A "low" on this input pin enables the CPU to write data or control words into the device.
A0 and A1	I	Port select 0 and Port select 1: These input signals, in conjuction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A0 and A1).
RESET	I	Reset: A "high" on this input clears the control register and all ports (A,B,C) are set to the input mode. "Bus hold" devices internal to the devicae will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400 µA.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.8 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-11-13

Approved sources of supply for SMD 5962-95819 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962R9581901QQC	34371	HS1-82C55ARH-8
5962R9581901VQC	34371	HS1-82C55ARH-Q

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Harris Semiconductor P.O. Box 883 Melbourne, FL 32902-0883

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.