



DRAM

4 MEG x 4 DRAM

3.3V, EDO PAGE MODE

AVAILABLE IN MILITARY SPECIFICATIONS

- MIL-STD-883
- SMD Planned

FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +3.3V $\pm 0.3V$ power supply
- Low power, 1mW standby; 150mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$ -BEFORE- $\overline{RAS}$ (CBR) HIDDEN
- 2,048-cycle (11 row-, 11 column-addresses)
- Extended Data-Out (EDO) PAGE access cycle
- 5V-tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS

- Timing
 - 60ns access (Contact Factory)
 - 70ns access
 - 80ns access

- Packages

Ceramic SOJ	ECJ	No. 505
Ceramic LCC	EC	No. 212
Ceramic Gull Wing	ECG	No. 603

MARKING

KEY TIMING PARAMETERS

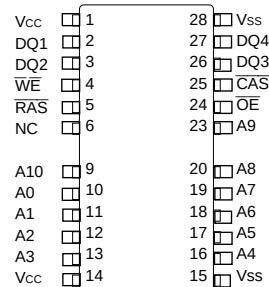
SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-6	110ns	60ns	30ns	30ns	15ns	12ns
-7	130ns	70ns	35ns	35ns	18ns	15ns
-8	150ns	80ns	40ns	40ns	20ns	20ns

GENERAL DESCRIPTION

The AS4LC4M4 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x4 configuration. The AS4LC4M4 $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle, regardless of $\overline{OE}$.

PIN ASSIGNMENT (Top View)

24/28-Pin



A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. An EARLY WRITE occurs when $\overline{WE}$ is taken LOW prior to $\overline{CAS}$ falling. A LATE WRITE or READ-MODIFY-WRITE occurs when $\overline{WE}$ falls after $\overline{CAS}$ was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of $\overline{OE}$. During LATE WRITE or READ-MODIFY-WRITE cycles, $\overline{OE}$ must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping $\overline{OE}$ LOW, no write will occur, and the data-outputs will drive read data from the accessed location.

The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE

FAST PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The FAST PAGE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE of operation.



EDO PAGE MODE

The AS4LC4M4E8 provides EDO PAGE MODE which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after $\overline{\text{CAS}}$ returns HIGH. EDO allows $\overline{\text{CAS}}$ precharge time (t_{CP}) to occur without the output data going invalid. This elimination of $\overline{\text{CAS}}$ output control allows pipeline READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{\text{CAS}}$. EDO-PAGE-MODE DRAMs operate similarly to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after $\overline{\text{CAS}}$ goes HIGH during READs, provided $\overline{\text{RAS}}$ and $\overline{\text{OE}}$ are held LOW. If $\overline{\text{OE}}$ is pulsed while

$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are LOW, data will toggle from valid data to High-Z and back to the same valid data. If $\overline{\text{OE}}$ is toggled or pulsed after $\overline{\text{CAS}}$ goes HIGH while $\overline{\text{RAS}}$ remains LOW, data will transition to and remain High-Z (refer to Figure 1). $\overline{\text{WE}}$ can also perform the function of disabling the output devices under certain conditions, as shown in Figure 2.

During an application, if the DQ outputs are wire OR'd, $\overline{\text{OE}}$ must be used to disable idle banks of DRAMs. Alternatively, pulsing $\overline{\text{WE}}$ to the idle banks during $\overline{\text{CAS}}$ high time will also High-Z the outputs. Independent of $\overline{\text{OE}}$ control, the outputs will disable after t_{OFF} , which is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

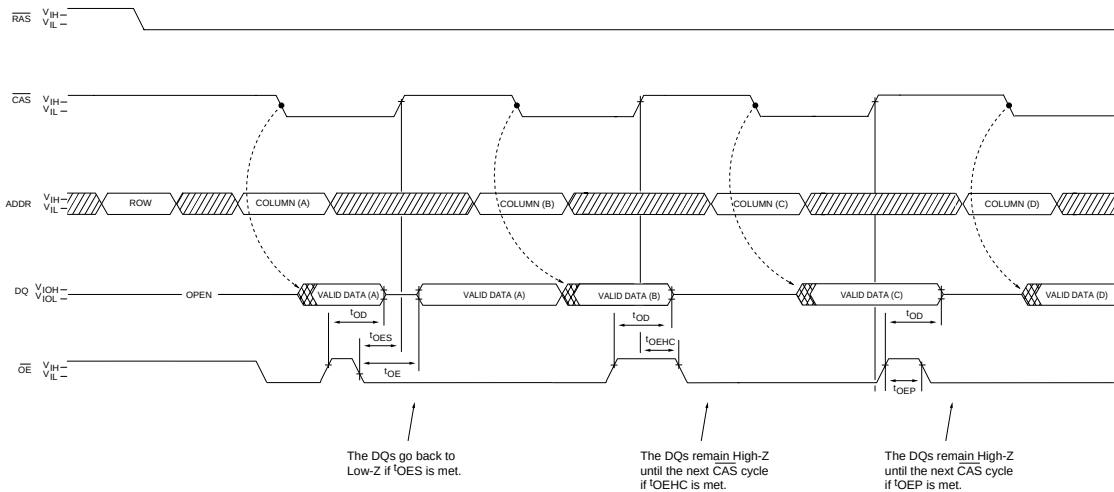


Figure 1
OUTPUT ENABLE AND DISABLE



REFRESH

Preserve correct memory cell data by maintaining power and executing a $\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ refresh cycle ($\overline{\text{RAS}}$ ONLY, CBR, or HIDDEN) so that all 2,048 combinations of $\overline{\text{RAS}}$ addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{\text{RAS}}$ addressing.

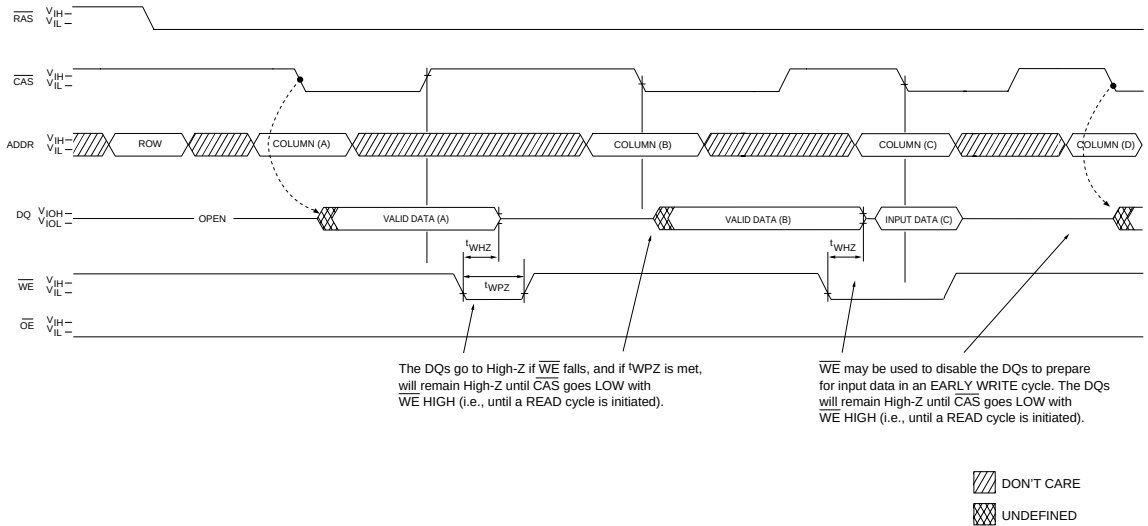
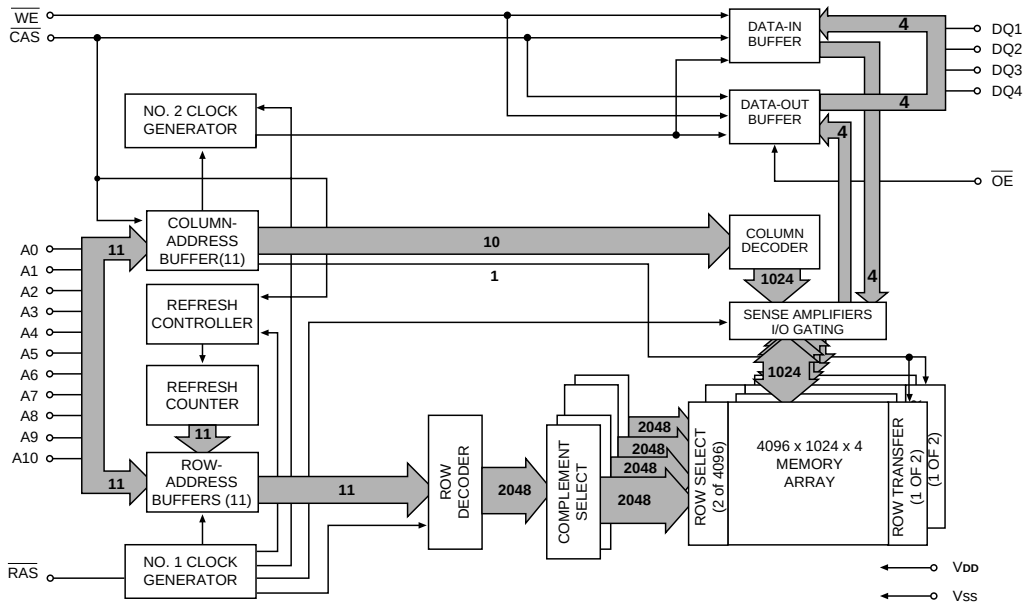


Figure 2
 $\overline{\text{WE}}$ CONTROL OF DQs



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DATA-IN/OUT
						t _R	t _C	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
	Any Cycle	L	L→H	H	L	n/a	n/a	Data-Out
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
CBR REFRESH		H→L	L	H	X	X	X	High-Z

**ABSOLUTE MAXIMUM RATINGS***

Voltage on V_{CC} pin Relative to V_{SS} -1V to +4.6V
 Voltage on NC, Inputs or I/O pins
 Relative to V_{SS} -1V to +5.5V
 Operating Temperature, T_A (ambient) .. T_A(MIN) = -55°C
 T_C(MAX) = 125°C
 Storage Temperature -55°C to +150°C
 Power Dissipation 1W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	V _{IH}	2.0	V _{CC} +1	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	V _{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ 5.5V V _{CC} = 3.6V (All other pins not under test = 0V) (NC pins not tested)	I _I	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V) V _{CC} =3.6V	I _{OZ}	-10	10	μA	
OUTPUT LEVELS Output High Voltage (I _{OUT} = -2mA)	V _{OH}	2.4		V	
Output Low Voltage (I _{OUT} = 2mA)	V _{OL}		0.4	V	

PARAMETER/CONDITION	SYM	MAX			UNITS	NOTES
		-6	-7	-8		
STANDBY CURRENT: (TTL) (RAS = CAS = V _{IH})	I _{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = other inputs = V _{CC} -0.2V)	I _{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, address cycling: ^t RC = ^t RC [MIN])	I _{CC3}	120	110	100	mA	3, 4, 12
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS = V _{IL} , CAS, address cycling: ^t PC = ^t PC [MIN])	I _{CC4}	110	100	90	mA	3, 4, 12
REFRESH CURRENT: RAS ONLY Average power supply current (RAS cycling, CAS = V _{IH} : ^t RC = ^t RC [MIN])	I _{CC5}	120	110	100	mA	3, 12
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, address cycling: ^t RC = ^t RC [MIN])	I _{CC6}	120	110	100	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C _{I1}	7	pF	2
Input Capacitance: RAS, CAS, WE, OE	C _{I2}	7	pF	2
Input/Output Capacitance: DQ	C _{IO}	8	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	t _{AA}		30		35		40	ns	
Column-address set-up to CAS precharge during write	t _{ACH}	15		15		20		ns	
Column-address hold time (referenced to RAS)	t _{AR}	45		55		60		ns	
Column-address setup time	t _{ASC}	0		0		0		ns	
Row-address setup time	t _{ASR}	0		0		0		ns	
Column-address to WE delay time	t _{AWD}	55		65		65		ns	20
Access time from CAS	t _{CAC}		15		20		20	ns	14
Column-address hold time	t _{CAH}	10		15		15		ns	
CAS pulse width	t _{CAS}	12	10,000	15	10,000	20	10,000	ns	
CAS hold time (CBR REFRESH)	t _{CHR}	10		15		15		ns	5
CAS to output in Low-Z	t _{CLZ}	0		0		0		ns	
Data output hold after next CAS LOW	t _{COH}	5		5		5		ns	
CAS precharge time	t _{CP}	10		10		10		ns	15
Access time from CAS precharge	t _{CPA}		35		40		40	ns	
CAS to RAS precharge time	t _{CRP}	5		5		5		ns	
CAS hold time	t _{CSH}	50		55		60		ns	
CAS setup time (CBR REFRESH)	t _{CSR}	5		5		10		ns	5
CAS to WE delay time	t _{CWD}	35		40		45		ns	20
Write command to CAS lead time	t _{CWL}	15		15		20		ns	
Data-in hold time	t _{DH}	10		12		15		ns	21
Data-in hold time (referenced to RAS)	t _{DHR}	40		56		55		ns	
Data-in setup time	t _{DS}	0		0		0		ns	21
Output disable	t _{OD}	0	15	0	15		20	ns	
Output Enable	t _{OE}		15		20		20	ns	22
OE hold time from WE during READ-MODIFY-WRITE cycle	t _{OEH}	10		12		15		ns	
OE HIGH hold from CAS HIGH	t _{OEHC}	10		10		10		ns	
OE HIGH pulse width	t _{OEP}	10		10		10		ns	
OE LOW to CAS HIGH setup time	t _{OES}	5		5		5		ns	

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($V_{CC} = +3.3V \pm 0.3V$)

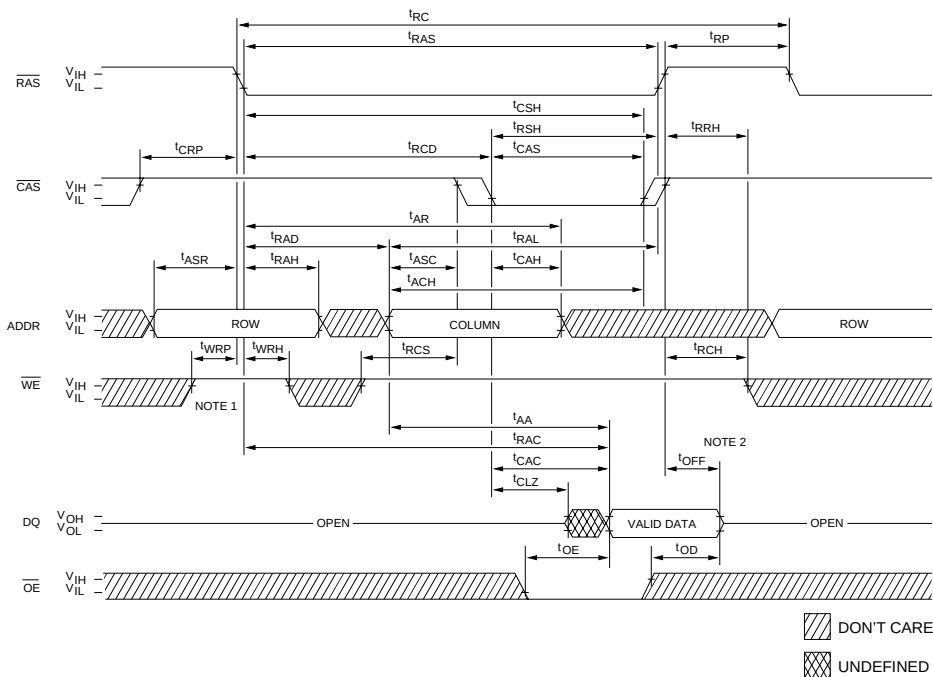
AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	20	ns	
OE setup prior to RAS during HIDDEN REFRESH cycle	t_{ORD}	0		0		0		ns	19
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	30		35		40		ns	
EDO-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	75		85		90		ns	
Access time from RAS	t_{RAC}		60		70		80	ns	13
RAS to column-address delay time	t_{RAD}	15	30	15	35	15	40	ns	17
Row-address hold time	t_{RAH}	10		10		10		ns	
Column-address to RAS lead time	t_{RAL}	30		35		40		ns	
RAS pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
RAS pulse width (EDO PAGE MODE)	t_{RASP}	60	100,000	70	100,000	80	100,000	ns	
Random READ or WRITE cycle time	t_{RC}	110		130		150		ns	
RAS to CAS delay time	t_{RCD}	16	45	16	50	20	60	ns	16
Read command hold time (referenced to CAS)	t_{RCH}	0		0		0		ns	18
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period (2,048 cycles)	t_{REF}		32		32		32	ms	
RAS precharge time	t_{RP}	40		50		60		ns	
RAS to CAS precharge time	t_{RPC}	5		5		5		ns	
Read command hold time (referenced to RAS)	t_{RRH}	0		0		0		ns	18
RAS hold time	t_{RSH}	13		15		15		ns	
READ WRITE cycle time	t_{RWC}	150		180		200		ns	
RAS to WE delay time	t_{RWD}	80		90		105		ns	20
Write command to RAS lead time	t_{RWL}	15		15		20		ns	
Transition time (rise or fall)	t_T	2	30	2	30	2	30	ns	
Write command hold time	t_{WCH}	10		12		15		ns	
Write command hold time (referenced to RAS)	t_{WCR}	40		56		60		ns	
WE command setup time	t_{WCS}	0		0		0		ns	20
Output disable delay from WE	t_{WHZ}	0	14	0	16	0	20	ns	
Write command pulse width	t_{WP}	10		12		15		ns	
WE pulse to disable at CAS HIGH	t_{WPZ}	10		12		15		ns	
WE hold time (CBR REFRESH)	t_{WRH}	10		10		10		ns	24
WE setup time (CBR REFRESH)	t_{WRP}	10		10		10		ns	24



NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{CC} = +3.3V$; $f = 1\text{ MHz}$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of $100\mu s$ is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the $\overline{REF}$ refresh requirement is exceeded.
8. AC characteristics assume $t_T = 2.5ns$.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. Column address changed once each cycle.
12. Measured with a load equivalent to two TTL gates, $100pF$ and $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
13. Assumes that $t_{RCD} < t_{RCD}(\text{MAX})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
14. Assumes that $t_{RCD} \geq t_{RCD}(\text{MAX})$.
15. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for t_{CP} .
16. Operation within the $t_{RCD}(\text{MAX})$ limit ensures that $t_{RAC}(\text{MAX})$ can be met. $t_{RCD}(\text{MAX})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{MAX})$ limit, then access time is controlled exclusively by t_{CAC} , provided t_{RAD} is not exceeded.
17. Operation within the $t_{RAD}(\text{MAX})$ limit ensures that $t_{RAC}(\text{MIN})$ and $t_{CAC}(\text{MIN})$ can be met. $t_{RAD}(\text{MAX})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\text{MAX})$ limit, then access time is controlled exclusively by t_{AA} , provided t_{RCD} is not exceeded.
18. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
19. $t_{OFF}(\text{MAX})$ defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL} . It is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
20. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY WRITE cycles. t_{RWD} , t_{AWD} and t_{CWD} apply to READ-MODIFY-WRITE cycles. If $t_{WCS} \geq t_{WCS}(\text{MIN})$, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{WCS} < t_{WCS}(\text{MIN})$ and $t_{RWD} \geq t_{RWD}(\text{MIN})$, $t_{AWD} \geq t_{AWD}(\text{MIN})$ and $t_{CWD} \geq t_{CWD}(\text{MIN})$, the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$ -controlled) cycle. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not applicable in a LATE WRITE cycle.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
22. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, $\overline{WE}$ must be pulsed during $\overline{CAS}$ HIGH time in order to place I/O buffers in High-Z.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = \text{LOW}$ and $\overline{OE} = \text{HIGH}$.
24. t_{WTS} and t_{WTH} are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverses of t_{WRP} and t_{WRH} in the CBR REFRESH cycle.

READ CYCLE



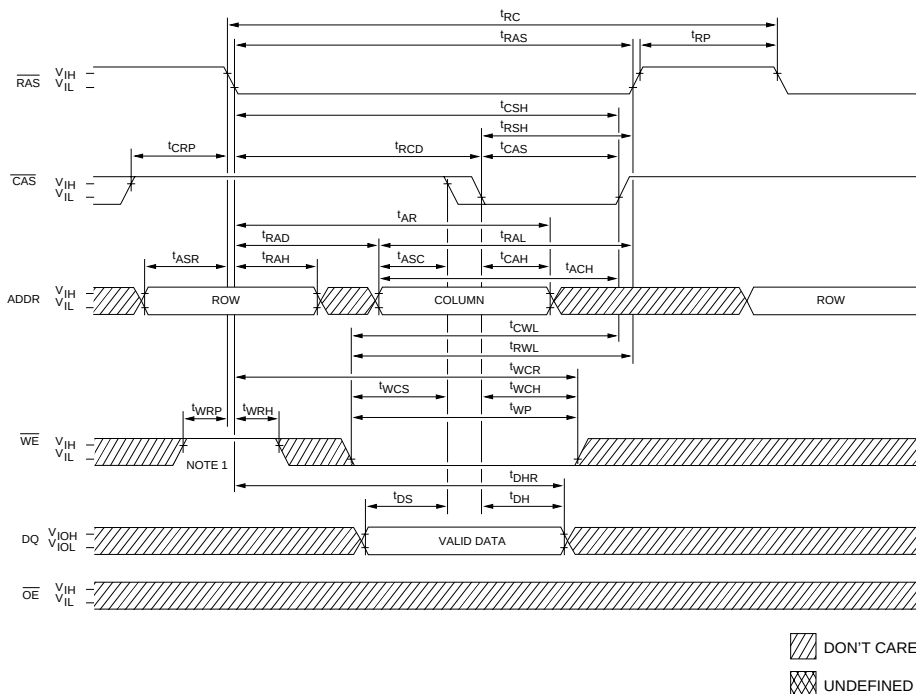
- NOTE:**
1. Although $\overline{\text{WE}}$ is a "don't care" at $\overline{\text{RAS}}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{\text{WE}}$ HIGH for ${}^t\text{WRP}$ and ${}^t\text{WRH}$. This design implementation will facilitate compatibility with future EDO DRAMs.
 2. ${}^t\text{OFF}$ is referenced from rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^t AA		30		35		40	ns
^t ACH	15		15		20		ns
^t AR	45		50		60		ns
^t ASC	0		0		0		ns
^t ASR	0		0		0		ns
^t CAC		15		20		20	ns
^t CAH	10		15		15		ns
^t CAS	12	10,000	15	10,000	20	10,000	ns
^t CLZ	0		0		0		ns
^t CRP	5		5		5		ns
^t CSH	50		55		60		ns
^t OD	0	15	0	15		20	ns
^t OE		15		20		20	ns
^t OFF	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^t RAC		60		70		80	ns
^t RAD	15	30	15	35	15	40	ns
^t RAH	10		10		10		ns
^t RAL	30		35		40		ns
^t RAS	60	10,000	70	10,000	80	10,000	ns
^t RC	110		130		150		ns
^t RCD	16	45	16	50	20	60	ns
^t RCH	0		0		0		ns
^t RCS	0		0		0		ns
^t RP	40		50		60		ns
^t RRH	0		0		0		ns
^t RSH	10		12		15		ns
^t WRH	10		10		10		ns
^t WRP	10		10		10		ns

EARLY WRITE CYCLE



NOTE: 1. Although $\overline{\text{WE}}$ is a "don't care" at $\overline{\text{RAS}}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{\text{WE}}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

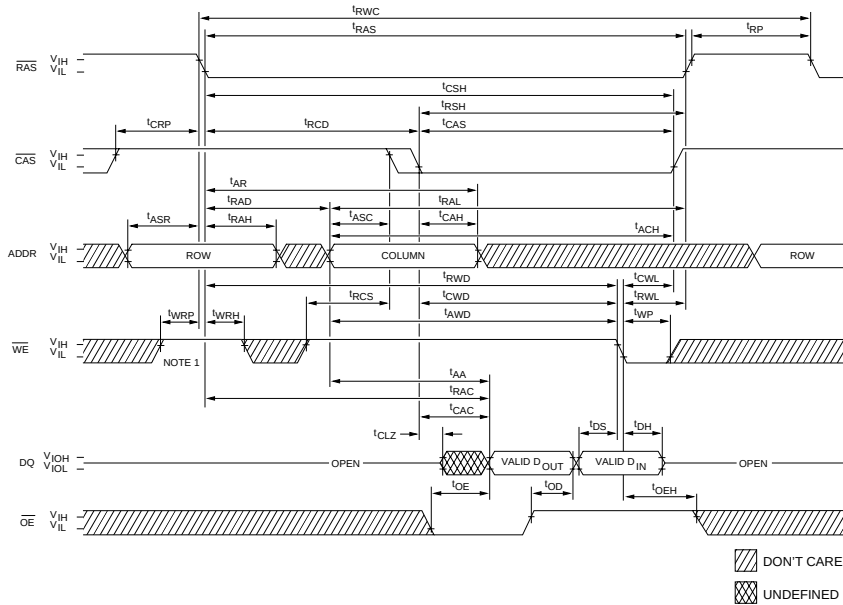
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^t ACH	15		15		20		ns
^t AR	45		55		60		ns
^t ASC	0		0		0		ns
^t ASR	0		0		0		ns
^t CAH	10		15		15		ns
^t CAS	12	10,000	15	10,000	20	10,000	ns
^t CRP	5		5		5		ns
^t CSH	50		55		60		ns
^t CWL	15		15		20		ns
^t DH	10		12		15		ns
^t DHR	40		50		55		ns
^t DS	0		0		0		ns
^t RAD	15	30	15	35	15	40	ns
^t RAH	10		10		10		ns

	-6		-7		-8		
<i>SYM</i>	<i>MIN</i>	<i>MAX</i>	<i>MIN</i>	<i>MAX</i>	<i>MIN</i>	<i>MAX</i>	<i>UNITS</i>
^t RAL	30		35		40		ns
^t RAS	60	10,000	70	10,000	80	10,000	ns
^t RC	110		130		150		ns
^t RCD	16	45	16	50	20	60	ns
^t RP	40		50		60		ns
^t RSH	13		15		0		ns
^t RWL	15		15		20		ns
^t WCH	10		12		15		ns
^t WCR	40		50		60		ns
^t WCS	0		0		0		ns
^t WP	10		12		15		ns
^t WRH	10		10		10		ns
^t WRP	10		10		10		ns



READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE cycles)



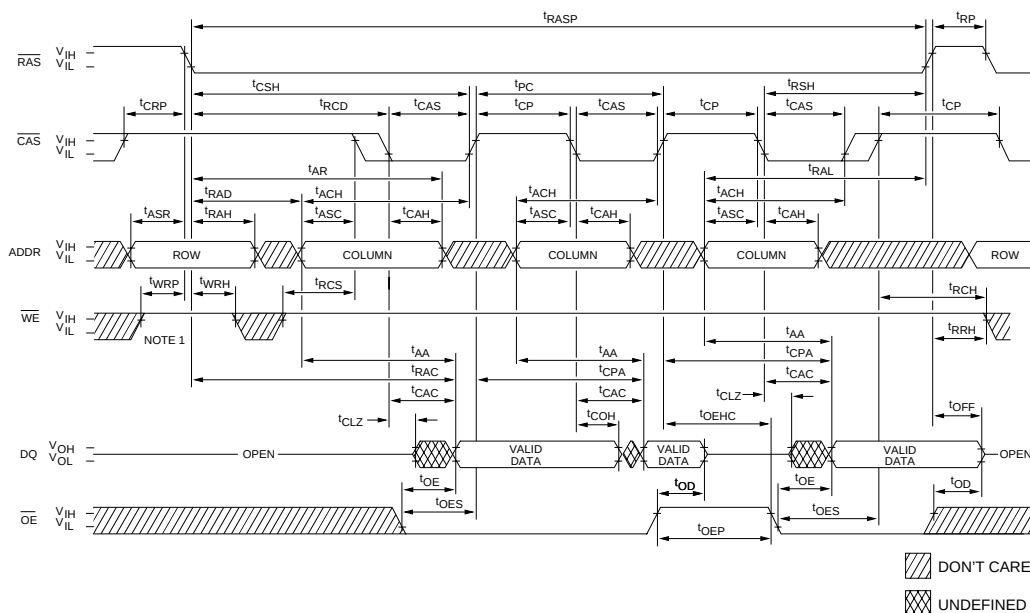
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t_{AA}		30		35		40	ns
t_{ACH}	15		15		20		ns
t_{AR}	45		55		60		ns
t_{ASC}	0		0		0		ns
t_{ASR}	0		0		0		ns
t_{AWD}	55		65		65		ns
t_{CAC}		15		20		20	ns
t_{CAH}	10		15		15		ns
t_{CAS}	12	10,000	15	10,000	20	10,000	ns
t_{CLZ}	0		0		0		ns
t_{CRP}	5		5		5		ns
t_{CSH}	50		55		60		ns
t_{CWD}	35		40		45		ns
t_{CWL}	15		15		20		ns
t_{DH}	10		12		15		ns
t_{DS}	0		0		0		ns
t_{OD}	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t_{OE}		15		20		20	ns
t_{OEH}	10		12		15		ns
t_{RAC}		60		70		80	ns
t_{RAD}	15	30	15	35	15	40	ns
t_{RAH}	10		10		10		ns
t_{RAL}	30		35		40		ns
t_{RAS}	60	10,000	70	10,000	80	10,000	ns
t_{RCD}	16	45	16	50	20	60	ns
t_{RCS}	0		0		0		ns
t_{RP}	40		50		60		ns
t_{RSH}	13		15		15		ns
t_{RWC}	150		180		200		ns
t_{RWD}	80		90		105		ns
t_{RWL}	15		15		20		ns
t_{WP}	10		12		15		ns
t_{WRH}	10		10		10		ns
t_{WRP}	10		10		10		ns

EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although $\overline{\text{WE}}$ is a "don't care" at $\overline{\text{RAS}}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{\text{WE}}$ HIGH for ${}^t\text{WRP}$ and ${}^t\text{WRH}$. This design implementation will facilitate compatibility with future EDO DRAMs.

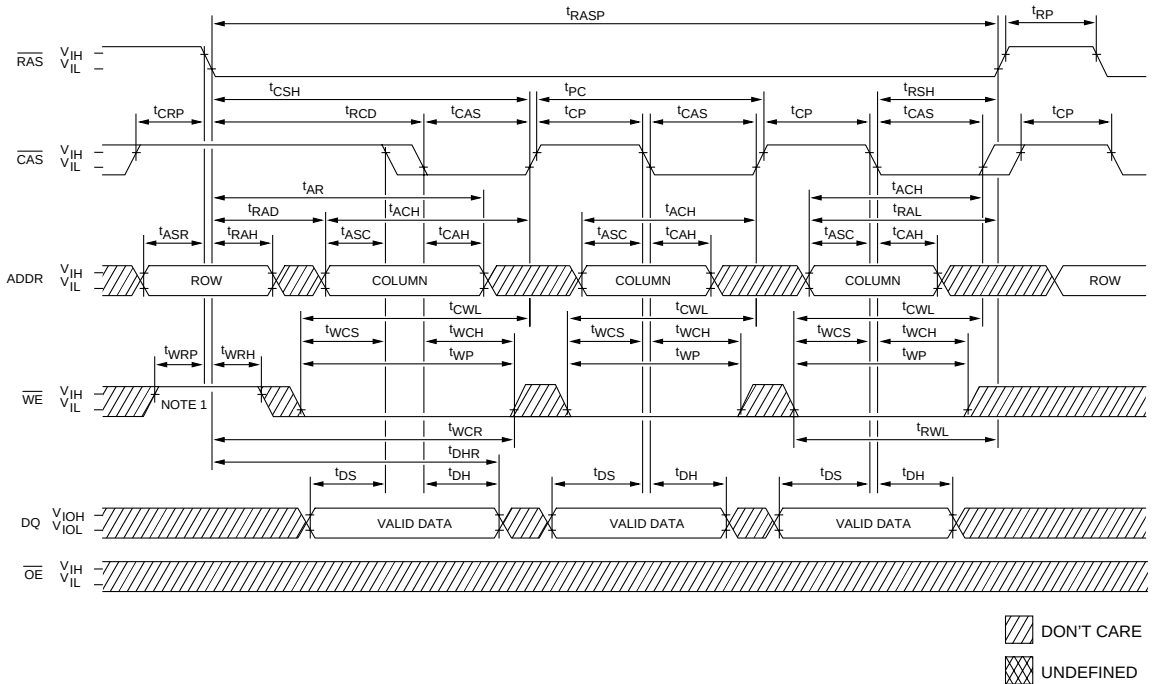
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^t AA		30		35		40	ns
^t ACH	15		15		20		ns
^t AR	45		55		60		ns
^t ASC	0		0		0		ns
^t ASR	0		0		0		ns
^t CAC		15		20		20	ns
^t CAH	10		15		15		ns
^t CAS	12	10,000	15	10,000	20	10,000	ns
^t CLZ	0		0		0		ns
^t COH	5		5		5		ns
^t CP	10		10		10		ns
^t CPA		35		40		40	ns
^t CRP	5		5		5		ns
^t CSH	50		55		60		ns
^t OD	0	15	0	15	0	20	ns
^t OE		15		20		20	ns
^t OEHC	10		10		10		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^t OEP	10		10		10		ns
^t OES	5		5		5		ns
^t OFF	0	15	0	15	0	20	ns
^t PC	30		35		40		ns
^t RAC		60		70		80	ns
^t RAH	15	30	15	35	15	40	ns
^t RAH	10		10		10		ns
^t RAL	30		35		40		ns
^t RASP	60	100,000	70	100,000	80	100,000	ns
^t RCD	16	45	16	50	20	60	ns
^t RCH	0		0		0		ns
^t RCS	0		0		0		ns
^t RP	40		50		60		ns
^t RRH	0		0		0		ns
^t RSH	13		15		15		ns
^t WRH	10		10		10		ns
^t WRP	10		10		10		ns



EDO-PAGE-MODE EARLY-WRITE CYCLE



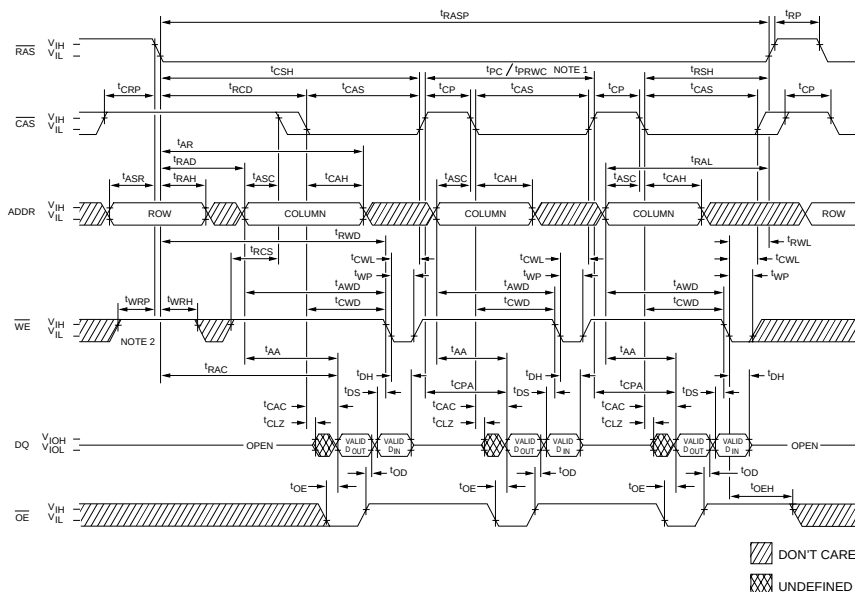
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t_{ACH}	15		15		20		ns
t_{AR}	45		55		60		ns
t_{ASC}	0		0		0		ns
t_{ASR}	0		0		0		ns
t_{CAH}	10		12		15		ns
t_{CAS}	12	10,000	15	10,000	20	10,000	ns
t_{CP}	10		10		10		ns
t_{CRP}	5		5		5		ns
t_{CSH}	50		55		60		ns
t_{CWL}	15		15		20		ns
t_{DH}	10		12		15		ns
t_{DHR}	40		50		55		ns
t_{DS}	0		0		0		ns
t_{PC}	30		35		40		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t_{RAD}	15	30	15	35	15	40	ns
t_{RAH}	10		10		10		ns
t_{RAL}	30		35		40		ns
t_{RASP}	60	100,000	70	100,000	80	100,000	ns
t_{RCD}	16	45	16	50	20	60	ns
t_{RP}	40		50		60		ns
t_{RSH}	13		15		15		ns
t_{RWL}	15		15		20		ns
t_{WCH}	10		12		15		ns
t_{WCR}	40		50		60		ns
t_{WCS}	0		0		0		ns
t_{WP}	10		12		15		ns
t_{WRH}	10		10		10		ns
t_{WRP}	10		10		10		ns

EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE: 1. t_{PC} is for LATE WRITE cycles only.

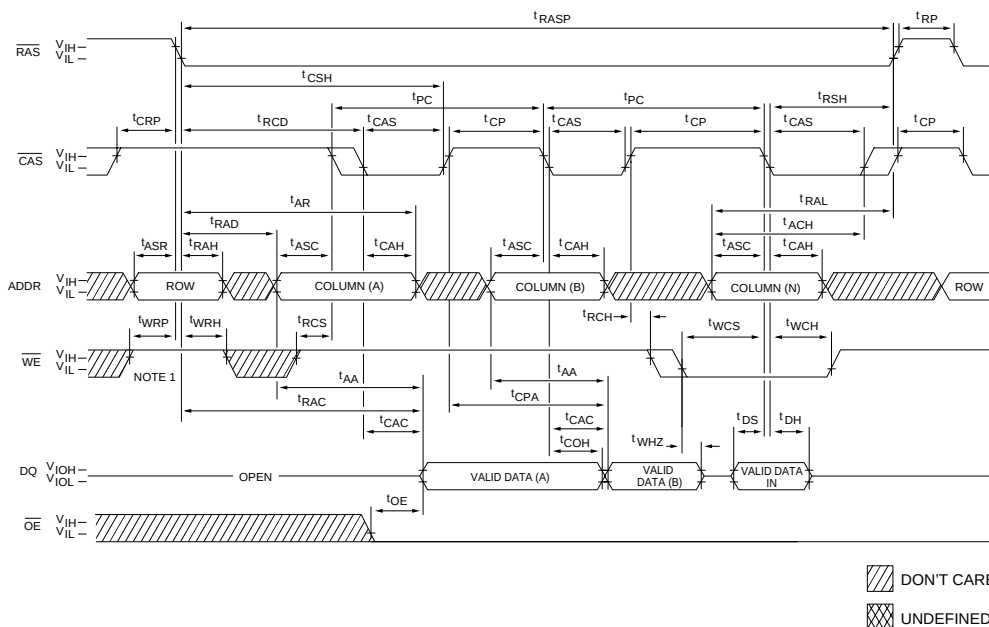
2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
1AA		30		35		40	ns
1AR	45		55		60		ns
1ASC	0		0		0		ns
1ASR	0		0		0		ns
1AWD	55		65		65		ns
1CAC		15		20		20	ns
1CAH	10		15		15		ns
1CAS	12	10,000	15	10,000	20	10,000	ns
1CLZ	0		0		0		ns
1CP	10		10		10		ns
1CPA		35		40		40	ns
1CRP	5		5		5		ns
1CSH	50		55		60		ns
1CWD	35		40		45		ns
1CWL	15		15		20		ns
1DH	10		12		15		ns
1DS	0		0		0		ns
1OD	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^t OE		15		20		20	ns
^t OEH	10		12		15		ns
^t PC	30		35		40		ns
^t PRWC	75		85		90		ns
^t RAC		60		70		80	ns
^t RAD	15	30	15	35	15	40	ns
^t RAH	10		10		10		ns
^t RAL	30		35		40		ns
^t RASP	60	100,000	70	100,000	80	100,000	ns
^t RCD	16	45	16	50	20	60	ns
^t RCS	0		0		0		ns
^t RP	40		50		60		ns
^t RSR	13		15		15		ns
^t RWD	80		90		105		ns
^t RWL	15		15		20		ns
^t WP	10		12		15		ns
^t WRH	10		10		10		ns
^t WRP	10		10		10		ns

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Pseudo READ-MODIFY-WRITE)



☐ DON'T CARE

UNDEFINED

NOTE: 1. Although $\overline{\text{WE}}$ is a "don't care" at $\overline{\text{RAS}}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{\text{WE}}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

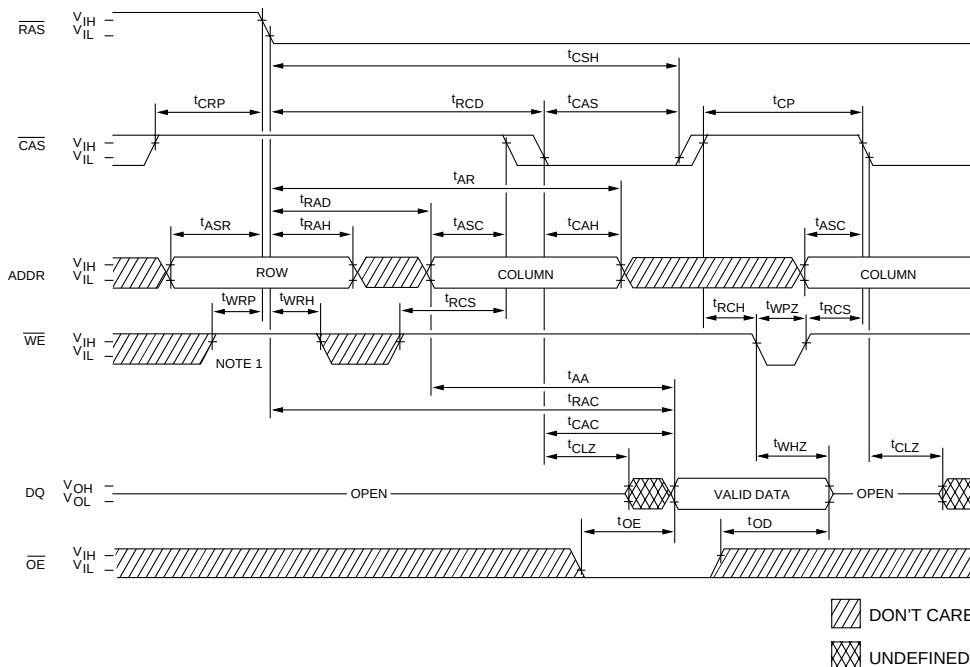
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		30		35		40	ns
tACH	15		15		20		ns
tAR	45		55		60		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		20		20	ns
tCAH	10		15		15		ns
tCAS	12	10,000	15	10,000	20	10,000	ns
tCOH	5		5		5		ns
tCP	10		10		10		ns
tCPA		35		40		40	ns
tCRP	5		5		5		ns
tCSH	50		55		60		ns
tDH	10		12		15		ns
tDS	0		0		0		ns
tOE		15		20		20	ns

	-6		-7		-8		
<i>SYM</i>	<i>MIN</i>	<i>MAX</i>	<i>MIN</i>	<i>MAX</i>	<i>MIN</i>	<i>MAX</i>	<i>UNITS</i>
^t PC	30		35		40		ns
^t RAC		60		70		80	ns
^t RAD	15	30	15	35	15	40	ns
^t RAH	10		10		10		ns
^t RAL	30		35		40		ns
^t RASP	60	100,000	70	100,000	80	100,000	ns
^t RCD	16	45	16	50	20	60	ns
^t RCH	0		0		0		ns
^t RCS	0		0		0		ns
^t RP	40		50		60		ns
^t RSH	13		15		15		ns
^t WCH	10		12		15		ns
^t WCS	0		0		0		ns
^t WHZ	0	13	0	15	0	15	ns
^t WRH	10		10		10		ns
^t WRP	10		10		10		ns



READ CYCLE (with $\overline{\text{WE}}$ -controlled disable)

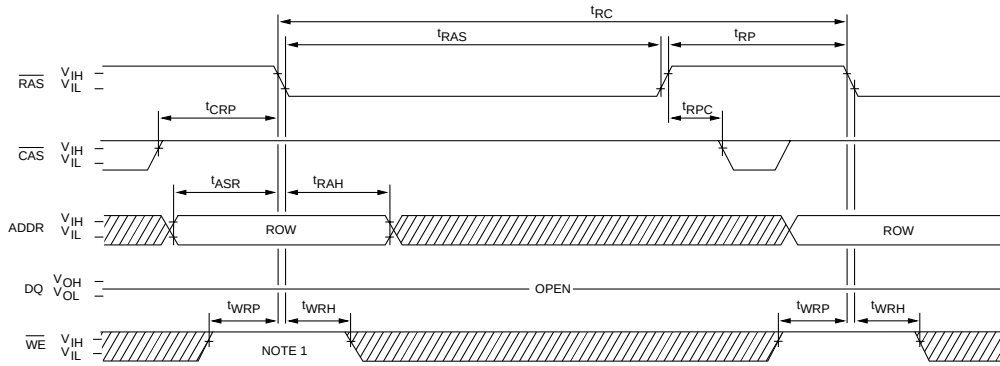
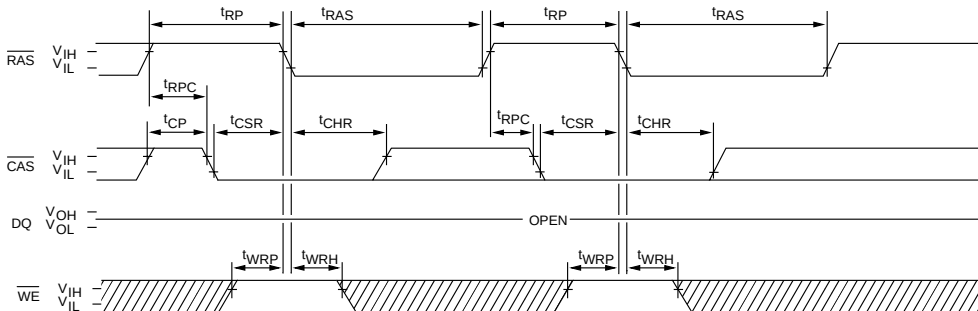


NOTE: 1. Although $\overline{\text{WE}}$ is a "don't care" at $\overline{\text{RAS}}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{\text{WE}}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t_{AA}		30		35		40	ns
t_{AR}	45		55		60		ns
t_{ASC}	0		0		0		ns
t_{ASR}	0		0		0		ns
t_{CAC}		15		20		20	ns
t_{CAH}	10		15		15		ns
t_{CAS}	12	10,000	15	10,000	20	10,000	ns
t_{CLZ}	0		0		0		ns
t_{CP}	10		10		10		ns
t_{CRP}	5		5		5		ns
t_{CSH}	50		55		60		ns
t_{OD}	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t_{OE}		15		20		20	ns
t_{RAC}		60		70		80	ns
t_{RAD}	15	30	15	35	15	40	ns
t_{RAH}	10		10		10		ns
t_{RCD}	16	45	16	50	20	60	ns
t_{RCH}	0		0		0		ns
t_{RCS}	0		0		0		ns
t_{WHZ}	0	14	0	16	0	20	ns
t_{WPZ}	10		12		15		ns
t_{WRH}	10		10		10		ns
t_{WRP}	10		10		10		ns

**RAS-ONLY REFRESH CYCLE****CBR REFRESH CYCLE**
(Addresses and $\overline{OE}$ = DON'T CARE)

DON'T CARE

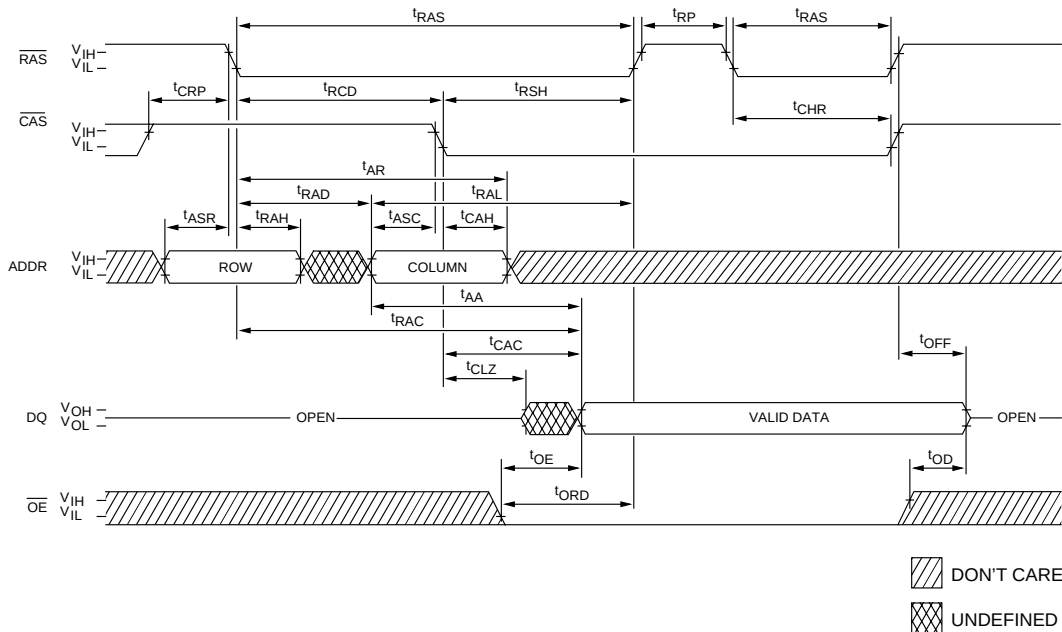
UNDEFINED

NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for t_{WRP} and t_{WRH} . This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t_{ASR}	0		0		0		ns
t_{CHR}	10		15		15		ns
t_{CP}	10		10		10		ns
t_{CRP}	5		5		5		ns
t_{CSR}	5		5		10		ns
t_{RAH}	10		10		10		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t_{RAS}	60	10,000	70	10,000	80	10,000	ns
t_{RC}	110		130		150		ns
t_{RP}	40		50		60		ns
t_{RPC}	5		5		5		ns
t_{WRH}	10		10		10		ns
t_{WRP}	10		10		10		ns

**HIDDEN REFRESH CYCLE**²⁴
(WE = HIGH; OE = LOW)**TIMING PARAMETERS**

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{AA}		30		35		40	ns
t _{AR}	45		55		60		ns
t _{ASC}	0		0		0		ns
t _{ASR}	0		0		0		ns
t _{CAC}		15		20		20	ns
t _{CAH}	10		15		15		ns
t _{CHR}	10		15		15		ns
t _{CLZ}	0		0		0		ns
t _{CRP}	5		5		5		ns
t _{OD}	0	15	0	15	0	20	ns
t _{OE}		15		20		20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
t _{OFF}	0	15	0	15	0	20	ns
t _{ORD}	0		0		0		ns
t _{RAC}		60		70		80	ns
t _{RAD}	15	30	15	35	15	40	ns
t _{RAH}	10		10		10		ns
t _{RAL}	30		35		40		ns
t _{RAS}	60	10,000	70	10,000	80	10,000	ns
t _{RCD}	16	45	16	50	20	60	ns
t _{RP}	40		50		60		ns
t _{RSH}	13		15		15		ns



ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.

