CTI

CT2525/26/27
MIL-STD-1553
SINGLE PACKAGE SOLUTION

ADVANCE INFORMATION

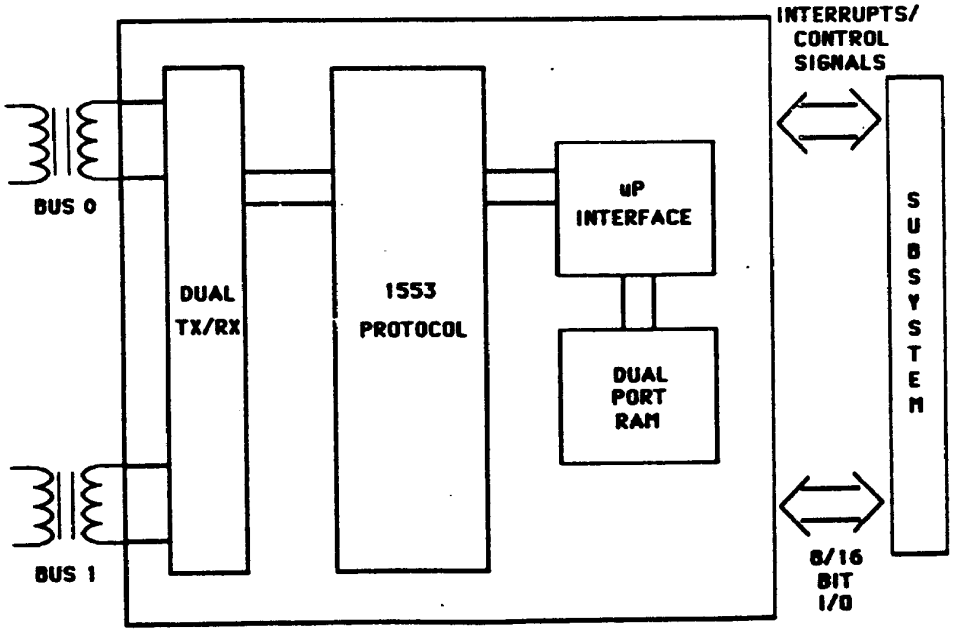
MARCONI CIRCUIT TECHNOLOGY
MIL-STD 1772 CERTIFIED

GENERAL DESCRIPTION

The CT2525 provides a complete one package interface between the MIL-STD-1553 bus and all microprocessor systems. The hybrid provides all data buffers and control registers to function as a Bus Controller or Remote Terminal. Control of the hybrid by the subsystem is through simple I/O port commands. Internal hybrid logic removes all critical timing imposed on a typical subsystem, thereby simplifying the implementation of this interface.

FEATURES

- Incorporates transceivers, Protocol and sub-system Interface components into a single Hybrid Package
- Functions as a Remote Terminal or Bus Controller
- Interfaces to uP as a simple peripheral unit
- Available with several options for transceivers: ± 15V, ± 12V and + 5V only
- Provides Fully Buffed Dual Port RAM storage for transmit and receive sub-addresses



CT2525

CT2525/26/27

SINGLE HYBRID PROTOCOL/SUBSYSTEM INTERFACE

Key Features

*Functional Superset of CT1800

*Downward compatible with existing base of CT1800 designs.

*Incorporates Transceivers, Protocol and Interface Hybrids into a single package.

*Functions as a Remote Terminal or Bus Controller.

General

The CT2525 provides a complete interface between the MIL-STD-1553 bus and any microprocessor system. Functioning as a superset of the CT1800 interface, the hybrid separates the bus from the subsystem. The hybrid provides all data buffers and control registers necessary to implement RT and BC functions. Internal arbitration and data transfer control circuitry eliminates subsystem response requirements. All data written into or read from this interface are double buffered on a message basis. Only valid and complete receive messages are transferred into the receive RAM.

The CT2525 supports all 15 mode codes and all types of data transfers allowed by MIL-STD-1553B. All circuitry (excluding transceiver drivers) are CMOS which results in very low power requirements.

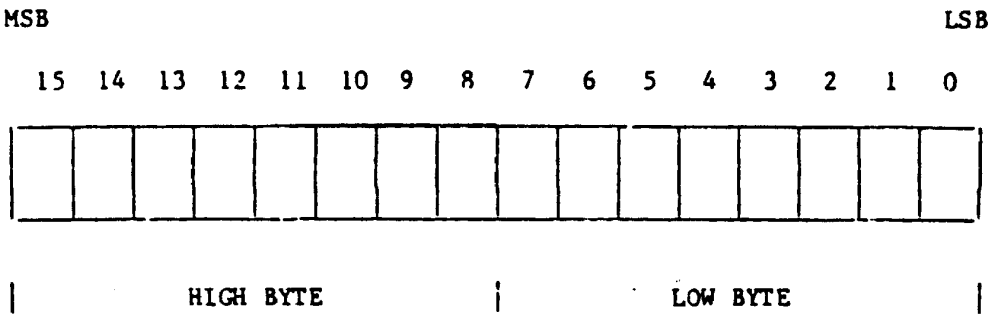
Interfacing to the subsystem is simplified through the use of tri-stated input/output buffers onto the subsystem bus. Control signals basically consist of four address lines, a device select input, read strobe, write strobe and several interrupts, the use of which are optional. Hybrid is accessed as a memory mapped I/O port of a microprocessor. Valid transmission and reception of data are indicated to the subsystem through the use of interrupts. This frees up the system processor from actively monitoring the port unitl a valid message is received.

Operation Register

This register contains information provided by the subsystem to control the hybrid. The register sets up the mode of operation for the hybrid (BC or RT) and selects the available options (BUS Select and Auto-Retry). This register also provides software control of the DBCACC, SER REQ, and SSERR bits of the status word. Following power-up or reset, bit 7 of this register will be set high. This bit is the busy bit of the status word. The subsystem reads and writes to this register under I/O commands. The I/O transfer functions defined by this register are executed by either of the two Execute Commands.

The register contains information for reading or writing data to the Internal RAM. The Internal RAM is divided into transmit or receive sections. In general, data is written to the transmit section and read from the receive section. However, either section may be read from or written to via the T/R bit in this register.

OPERATION REGISTER



1. RESET TO $FF80_H$

2. ADDRESS CODE = 0000_B (16 BIT MODE)
   0000_B (LOW BYTE, 8 BIT MODE)
   0001_B (HIGH BYTE, 8 BIT MODE)

BIT	NAME	FUNCTIONS
0–4	SA BITS	SUBADDRESS BITS Define SUBADDRESS MESSAGE BLOCK in INTERNAL RAM. BIT / SUBADDRESS BIT 0 — SA 0 (LSB) 1 — SA 1 2 — SA 2 3 — SA 3 4 — SA 4 (MSB) These bits correspond directly to 1553B definition in command word. Although SUBADDRESSES 00000_B AND 11111_B are illegal in 1553B, message blocks specified by them are both READABLE and WRITABLE by the SUBSYSTEM. They are not accessable from the 1553B BUS.

OPERATION REGISTER

BIT	NAME	FUNCTION
5	T/$\overline{R}$ BIT	TRANSMIT/RECEIVE BIT points INPUT/OUTPUT OPERATION to either the TRANSMIT SECTION or RECEIVE SECTION of the INTERNAL RAM.
6	I/$\overline{O}$ BIT	INPUT/OUTPUT BIT DEFINES DIRECTION OF DATA TRANSFER 1. SET HIGH: INPUT OPERATION Data currently loaded in the input FIFO BUFFER is moved to the specified message block (SUBADDRESS) in the INTERNAL RAM. If EXECUTE with RPT OPTION COMMAND is used, previously loaded data (i.e. data for which a load operation was previously executed) will be loaded to a new message block. Between 1 and 32 data words must be loaded in the input FIFO BUFFER when using an EXECUTE command with this bit set. 2. SET LOW: OUTPUT OPERATION When set low the execute operation will transfer a complete block of data (32 words) to the output FIFO buffer from the specified subaddress of internal RAM.
7	BUSY BIT	RTU BUSY HIGH = BUSY LOW = NOT BUSY MASTER RESET SETS BIT HIGH

OPERATION REGISTER

BIT	NAME	FUNCTION
8	RT/$\overline{BC}$	Remote Terminal/Bus Controller Bit. This line when set high, causes the hybrid to function as a Remote Teminal. When set low, it will function as a Bus Controller.
9	Transaction/$\overline{Test}$	Transaction/Test Mode Bit. When this bit is set high, normal transactions will be handled eg.. BC to RT, RT to BC. If this bit is set low and an I/O command trigger is issued, the self test will be performed for the MIL-STD-1553 protocol chip.
10	$\overline{LT\ Local}$	Loop Test Local Bit. This signal selects the self test path. When this signal is low, the internal digital path is selected. When set high, the external path including transceivers is selected.
11	Bus Select	Bus Select. When this signal is high Bus 1 is selected. When low, the opposite bus, Bus 0 is selected.

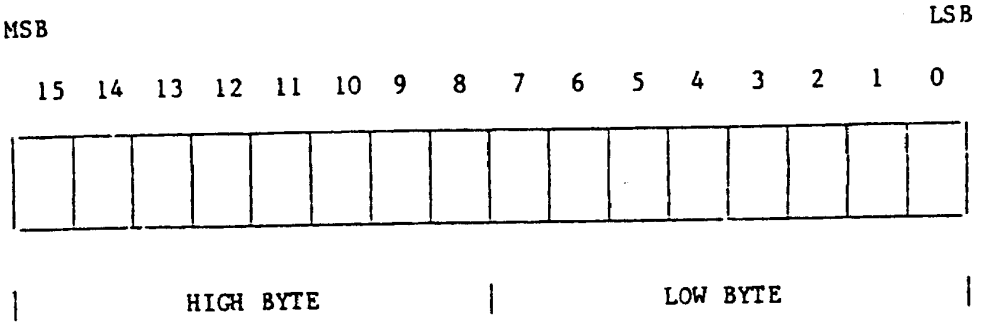
OPERATION REGISTER

BIT	NAME	FUNCTION
12	Normal/$\overline{\text{RT-RT}}$	Normal/RemoteTerminal-Remote Terminal Bit. When this signal is high, BC to RT and RT to BC transfers as performed. When this signal is low, RT to RT transfers are performed. Two command words are needed and two status words will be returned.
13	$\overline{\text{SERV REQ}}$/ Auto-Retry (LSB)	Service Request/Auto-Retry (LSB) Bit. RT Mode: A low in this bit will cause the service request bit in the status word to be set. BC Mode: This is the LSB of the Auto-Retry options. See table below.
14	$\overline{\text{SERR}}$/ Auto-Retry (MSB)	Subsystem Error/Auto-Retry (MSB) Bit. RT Mode: A low in this bit will cause the Subsystem Error Bit in the status word to be set.

OPERATION REGISTER

BIT	NAME	FUNCTION
14	$\overline{\text{SERR}}$/ Auto-Retry (MSB)	BC Mode: This is the MSB of the Auto-Retry options. Auto-Retry Options MSB LSB BUS 0 0 0 1 Sec. 1 0 PRI, Sec. 1 1 PRI, Sec.,Sec.
15	$\overline{\text{DBCACC}}$/Auto-Retry Bus	Dynamic Bus Control Accept/ Auto-Retry Bus. Bit. RT Mode: This bit should be held low if a subsystem is able to accept control of the bus if offered. BC Mode: This bit should be held high if an invalid transfer is to be retryed according to the selected auto-retry option listed above.

RT Command Word Register



1. RESET TO 0000_H

2. ADDRESS CODE = 0100_B (16 BIT MODE)
   0100_B (LOW BYTE, 8 BIT MODE)
   0101_B (HIGH BYTE, 8 BIT MODE)

BIT	NAME	FUNCTION
0-4	WC/MC FIELD	WORD COUNT/ MODE CODE FIELD 1. FOR DATA TRANSFERS WC/MC = WORD COUNT NOTE: 00000_B = 32 WORDS 2. FOR MODE COMMANDS WC/MC = MODE CODE SPECIFICATION
5-9	SA/M FIELD	SUBADDRESS/MODE FIELD When DATA transfers, this field is the SUBADDRESS field in the INTERNAL RAM. However when field is 00000_B or 11111_B it specifies that the command is a MODE COMMAND.

RT Command Word Register

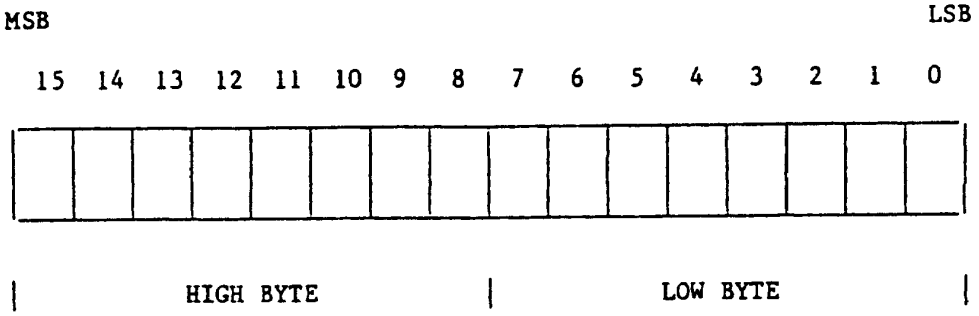
BIT	NAME	FUNCTION
10	TX/$\overline{RX}$	TRANSMIT/RECEIVE BIT
11-15	RTAD	RTU ADDRESS FIELD This field will contain only the HARD WIRED RTU ADDRESS or the BROADCAST ADDRESS (11111_B) if the RTU is enabled to receive BROADCAST COMMANDS. Reception of BROADCAST COMMANDS is enabled by a HIGH on the BCSTEN1 and BCSTEN0 input signal pins of the protocol front end.

RECEIVE COMMAND REGISTER (RCV CMD)

The RECEIVE COMMAND REGISTER contains the last valid receive command received by the RTU. It is a doubled buffer version of the COMMAND WORD REGISTER. This maximizes the time provided to the subsystem for reading the receive command before any new command can overwrite it.

Generally, the subsystem would read this register after the GOOD BLOCK interrupt issued.

RECEIVE COMMAND REGISTER (RCV CMD)



1. RESET TO 0000_H

2. ADDRESS CODE = 0010_B (16 BIT MODE)
   0010_B (LOW BYTE, 8 BIT MODE)
   0011_B (HIGH BYTE, 8 BIT MODE)

BIT	NAME	FUNCTION
0-4	WC FIELD	WORD COUNT FIELD NOTE: 00000_B = 32 WORDS
5-9	SA FIELD	SUBADDRESS FIELD NOTE: NEVER 00000_B OR 11111_B
10	$TX/\overline{RX}$	TRANSMIT/RECEIVE BIT ALWAYS SET LOW (0)
11-15	RTAD	RTU ADDRESS FIELD This field will contain only the HARD WIRED RTU ADDRESS or the BROADCAST ADDRESS (11111_B) if the RTU is enabled to receive BROADCAST COMMANDS. Reception of BROADCAST COMMANDS is ENABLED by a HIGH on BCSTEN1 and BCSTEN 0 input signal pins of the PROTOCOL FRONT END.

SUBSYSTEM INTERFACE SIGNALS

SIGNAL NAME	FUNCTION
A0-A3	INPUT ADDRESS A0 = LSB A3 = MSB These four signals provide the address codes that control the operation of the interface.
$\overline{DS}$	$\overline{DEVICE\ SELECT}$ Used in conjunction with the address signals. The input/output interface data bus will remain tri-stated and no operation will be executed when this signal is high, regardless of the state of the address signals. $\overline{DS}$ = LOW (0) INTERFACE SELECTED $\overline{DS}$ = HIGH (1) INTERFACE NOT SELECTED
DB0-DBF	I/O DATA BUS Data bus for all SUBSYSTEM READ and WRITE OPERATIONS. 16 BIT MODE: DB0 = LSB; DBF = MSB 8 BIT MODE: DB0/DBB = LSB; DB7/DBF = MSB When used in 8 BIT MODE the data bus must be connected as follows: DB0 TO DB8 DB1 TO DB9 DB2 TO DBA DB3 TO DBB DB4 TO DBC DB5 TO DBD DB6 TO DBE DB7 TO DBF

SUBSYSTEM INTERFACE SIGNALS (CONT'D)

SIGNAL NAME	FUNCTION
16/$\overline{8}$	PROGRAMS INTERFACE FOR 8 BIT OR 16 BIT DATA BUSES 16/ $\overline{8}$ = LOW (0) 8 BIT MODE 16/ $\overline{8}$ = HIGH (1) 16 BIT MODE
$\overline{\text{MASTER RESET}}$	SYSTEM RESET When low resets all registers and INPUT/OUTPUT buffers. Minimum Low Time for reset = .5usec.
$\overline{\text{WT}}$	WRITE STROBE Must GO LOW together with $\overline{\text{DS}}$ to perform a WRITE OPERATION. NOTE: $\overline{\text{RD}}$ MUST BE HIGH
$\overline{\text{RD}}$	READ STROBE Must GO LOW together with $\overline{\text{DS}}$ to perform a READ OPERATION. NOTE: $\overline{\text{WT}}$ STROBE MUST BE HIGH.
INTERRUPTS	Refer to DISCRETE INTERRUPT TABLE

NON-REGISTER OPERATIONAL COMMANDS

There are five operational commands that are not register read or write operations. These commands are summerized in the table below. The two execute operations are dependent on the contents of the OPERATION register. The address codes for all the operational commands are summarized in the 8 bit and 16 bit I/O OPERATIONAL tables.

NON-REGISTER OPERATIONAL COMMANDS

OPERATION	FUNCTION
RESET	RESET INPUT/OUTPUT BUFFERS This command clears both the input and output FIFO buffers. The BUFF EF flag will go low indicating the output buffer is empty.
READ OUTPUT DATA BUFFER	READ OUTPUT FIFO READS the data moved from the INTERNAL RAM in response to an UNLOAD execute operation. The order of the data words corresponds to the same order that they would be received on the 1553B bus. That is, the first data word read is the first data word following the COMMAND word. In 8 bit mode the high byte is read first.
WRITE INPUT DATA BUFFER	WRITE INPUT FIFO WRITES the data that will be moved into the INTERNAL RAM in response to a LOAD execute operation. The order of the data words corresponds to the same order that they would be transmitted on the 1553B bus. That is, the first data word written is the first data word transmitted following the STATUS word. In 8 bit mode the high byte is written first.

NON-REGISTER OPERATION COMMANDS

OPERATION	FUNCTION
EXECUTE OP.	EXECUTES OPERATION SPECIFIED IN OPERATION REGISTER 1. I/$\overline{O}$ BIT HIGH Data currently in INPUT FIFO BUFFER is loaded into the INTERNAL RAM block specified by the T/R BIT and SUBADDRESS FIELD of the OPERATION REGISTER. INPUT BUFFER must have at least one data word. The DONE interrupt is pulsed when the operation is completed. 2. I/$\overline{O}$ BIT LOW An entire block of data (32 words) specified by the T/R and the SUBADDRESS field of the OPERATION REGISTER is unloaded from the INTERNAL RAM into the OUTPUT FIFO BUFFER. The BUFFER flag goes high when the first data word is moved into the OUTPUT BUFFER. The DONE interrupt is pulsed when the complete message has been moved.
EXECUTE OP. WITH RPT OPTION	EXECUTES OPERATION SPECIFIED IN OPERATION REGISTER WITH REPEAT OPTION. 1. I/$\overline{O}$ BIT HIGH Data previously written into the INPUT BUFFER is loaded into a new INTERNAL RAM block specified by the T/R and SUBADDRESS field of the OPERATION REGISTER. This operation allows a block of data loaded in the INPUT BUFFER to be repeatedly copied into multiple subaddresses of the INTERNAL RAM without the subsystem having to reload the data. The done interrupt is pulsed when the operation is completed. The intent of the operation is to minimize the time required to initialize the INTERNAL RAM. 2. I/O BIT LOW Operation identical to EXECUTE OP. WITHOUT RPT option.

16 BIT MODE I/O OPERATION'S

Operation	$\overline{RD}$	$\overline{WT}$	$\overline{DS}$	AD3	AD2	AD1	AD0
RT and BC Mode							
No Operation-I/O Bus Tri-Stated	x	x	1	x	x	x	x
Read Operation Register	P*	1	0	0	0	0	0
Write Operation Register	1	P	0	0	0	0	0
Execute Operation (Load/Unload RAM)	1	P	0	1	0	0	0
Execute Operation with Repeat	1	P	0	1	0	1	0
Read Output FIFO	P	1	0	1	1	1	0
Write Input FIFO	1	P	0	1	1	1	0
Reset Input FIFO	1	P	0	1	0	1	1
Reset Input FIFO	1	P	0	1	1	0	1
Reset Input and Output FIFO	1	P	0	1	1	0	0
RT Mode Only							
Read RT Command Word Register	P	1	0	0	1	0	0
Read Receive Command Register	P	1	0	0	0	1	0
Read SYNC Data Register	P	1	0	0	1	1	0
Write Vecto Word Register	1	P	0	0	1	1	0
BC Mode Only							
Read Status Word #1 Register	P	1	0	0	0	1	0
Read Status Word #2/RMD Register	P	1	0	0	1	1	0
Write Command Word #1 Register	1	P	0	0	0	1	0
Write Command Word #2/AMD Register	1	P	0	0	1	1	0
Trigger Transaction/ Trigger Test	1	P	0	1	0	0	1

*P = Active Low Strobe ⌐└

8 BIT MODE I/O OPERATION'S

Operation	$\overline{RD}$	$\overline{WT}$	$\overline{DS}$	AD3	AD2	AD1	AD0
BC and RT Mode							
No Operation-I/O Bus Tristated	x	x	1	x	x	x	x
Read Operation Reg. High Byte	P	1	0	0	0	0	1
Read Operation Reg. Low Byte	P	1	0	0	0	0	0
Write Operation Reg. High Byte	1	P	0	0	0	0	1
Write Operation Reg. Low Byte	1	P	0	0	0	0	0
Read Output FIFO (High Byte First)	P	1	0	1	1	1	0
Write Input FIFO (High Byte First)	1	P	0	1	1	1	0
Execute Operation (Load/Unload RAM)	1	P	0	1	0	0	0
Execute Operation with Repeat	1	P	0	1	0	1	0
Reset Input FIFO	1	P	0	1	0	1	1
Reset Output FIFO	1	P	0	1	1	0	1
Reset Input and Output FIFOS	1	P	0	1	1	0	0
RT Mode Only							
Read RT Command Word Reg. High Byte	P	1	0	0	1	0	1
Read RT Command Word Reg. Low Byte	P	1	0	0	1	0	0
Read Receive Command Reg. High Byte	P	1	0	0	0	1	1
Read Receive Command Reg. Low Byte	P	1	0	0	0	1	0
Read SYNC Data Reg. High Byte	P	1	0	0	1	1	1
Read SYNC Data Reg. Low Byte	P	1	0	0	1	1	0
Write Vector Word Reg. High Byte	1	P	0	0	1	1	1
Write Vector Word Reg. Low Byte	1	P	0	0	1	1	0
BC Mode Only							
Read Status Word #11 Reg. High Byte	P	1	0	0	0	1	1
Read Status Word #11 Reg. Low Byte	P	1	0	0	0	1	0
Read Status Word #12/RMD Reg. High Byte	P	1	0	0	1	1	1
Read Status Word #2/RMD Reg. Low Byte	P	1	0	0	1	1	0
Write Command Word #1 Reg. High Byte	1	P	0	0	0	1	1
Write Command Word #1 reg. Low Byte	1	P	0	0	0	1	0
Write Command Word #2/AMD Reg. High Byte	1	P	0	0	1	1	1
Write Command Word #2/AMD Reg. Low Byte	1	P	0	0	1	1	0
Trigger Transaction/Trigger Test	1	P	0	1	0	0	1

* P = Active Low Strobe ⌐⌐

Bus Controller Mode

The CT2525 is programmed into Bus Controller mode by setting the RT/BC bit in the Operation register to a logic zero. There are five 16-bit registers available in Bus Controller mode: the Operation register, Command Word 1 register, Command Word 2 / Associated Mode Data register, Status Word 1 register, and Status Word 2 / Returned Mode Data register.

In order to initiate a 1553B bus transfer, the Bus Controller derives most of the required information (i.e. RTU address or Broadcast command, transmit or receive command, sub-address or mode command, and word count or mode code) directly from the Command Word 1 register. Other options that must be selected are programmed by the state of various bits in the Operation register. These bits specify which 1553B bus is to be used, whether it is an RT-to-RT transfer, and which AUTO-RETRY option is to be used.

For all 1553B commands except Remote Terminal to Remote Terminal transfers, the NORMAL/RT-RT bit in the Operation register is set to a logic one. The command word to be transmitted on the 1553B bus is written into the Command Word 1 register.

If the command is a Mode Command that requires an associated data word, the data word is written into the Command Word 2 / Associated Mode Data register.

If a Remote Terminal to Remote Terminal transfer is to be implemented, the command word for the receiving Remote Terminal is written into the Command Word 1 register, the command word for the transmitting Remote Terminal is written into the Command Word 2 / Associated Mode Data register, and the NORMAL/RT-RT bit in the Operation register is set to a logic zero.

The transaction is initiated by the I/O write command TRIGGER TRANSACTION which begins the transfer by transmitting the command word from the Command Word 1 register onto the 1553B data bus.

Bus Controller to Remote Terminal Transfers

As the command word is being transmitted, the data block located in the transmit section of RAM at the sub-address specified by the command word is burst transferred to the XMIT FIFO. The block of data is then transmitted word by word onto the 1553B bus.

The status word returned by the Remote Terminal is loaded into the Status Word 1 register. The address field and the Busy bit of the status word are examined and, if the address matches the address of the command word and the Busy bit is not set, then the Bus Controller issues a VALID TRANSFER interrupt. If the address field of the returned status word is incorrect or if the Busy bit is set or if no status word is returned, then an INVALID TRANSFER interrupt is issued.

Remote Terminal to Bus Controller Transfers

The status word returned by the Remote Terminal is loaded into the Status Word 1 register. As the data words are received from the Remote Terminal, they are loaded into the RCV FIFO. After the entire message is received and validated, the block of data is burst transferred from the RCV FIFO into the receive section of RAM at the sub-address specified by the command word. If the address field of the status word matches the address field of the command word and the block of data has been successfully verified, then the VALID TRANSFER interrupt is issued; otherwise, an INVALID TRANSFER interrupt is issued.

Mode Commands

For mode commands that transfer a data word from the Bus Controller to the Remote Terminal, the data word is obtained from the Command Word 2 / Associated Mode Data register.

The status word returned by the Remote Terminal is loaded into the Status Word 1 register. For mode commands that transfer a data word from the Remote Terminal to the Bus Controller, the data word is loaded into the Returned Mode Data register.

In order to generate a VALID TRANSFER interrupt, the address field of the status word must match the address field of the command word. For mode commands that transfer a data word from the Remote Terminal to the Bus Controller, an additional requirement for a VALID TRANSFER interrupt is that one and only one data word must be returned by the Remote Terminal.

If the above criteria are not met, then an INVALID TRANSFER interrupt is issued.

Remote Terminal to Remote Terminal Transfers

The first command word is for the receiving Remote Terminal. The second command word, for the transmitting Remote Terminal, is obtained from the Command Word 2 / Associated Mode Data register.

The first status word returned, which is from the transmitting Remote Terminal, is loaded into the Status Word 1 register. As the data words are received from this Remote Terminal, they are loaded into the RCV FIFO. After the entire message is received and validated, the block of data is burst transferred from the RCV FIFO into the receive section of RAM at the sub-address specified by the Command Word 1 register. The status word returned from the receiving Remote Terminal is loaded into the Status Word 2 / Returned Mode Data register.

If both status words are returned with the correct address field and the busy bit not set, and the block of data has been successfully verified, then the VALID TRANSFER interrupt is issued; otherwise, an INVALID TRANSFER interrupt is issued.

Broadcast Transfers

For all Bus Controller to Remote Terminal data transfers, if the command word has the Broadcast address (11111 BIN), the Bus Controller performs as for a non-broadcast command except that the VALID TRANSFER interrupt will be issued only if a status word is NOT returned from any Remote Terminal. If a status word IS returned, an INVALID TRANSFER interrupt is issued.

For Remote Terminal to Remote Terminal transfers, if the first command word (for the receiving Remote Terminal) has the Broadcast address, the Bus Controller performs as for a non-broadcast transfer except that the VALID TRANSFER interrupt will be issued only if a status word is NOT returned from the receiving Remote Terminal and if the status word and data block from the transmitting Remote Terminal meet the same criteria as for a non-broadcast Remote Terminal to Remote Terminal transfer; otherwise, an INVALID TRANSFER interrupt is issued.

AUTO-RETRY OPERATION

In the event of an invalid 1553B transfer, a programmable AUTO-RETRY option is available for automatically repeating the transfer without subsystem intervention.

This function is controlled by three bits in the Operation register: AUTO-RETRY MSB, AUTO-RETRY LSB, and AUTO-RETRY OTHER BUS,

The AUTO-RETRY MSB and AUTO-RETRY LSB bits determine the number of times that the failed transfer will be re-executed as a result of continued failures.

The AUTO-RETRY OTHER BUS bit determines whether the secondary (redundant) 1553B data bus will be used during the retry attempts. If this bit is LOW, only the primary 1553B data bus (as selected by the BUS1/BUS0 bit in the Operation register) will be used. If this bit is HIGH, bus selection is sequenced as follows:

AUTO-RETRY		BUS SELECTION	
MSB	LSB	INITAL TRANSFER	RETRY ATTEMPTS
0	0	Primary	none
0	1	Primary	Secondary
1	0	Primary	Primary, Secondary
1	1	Primary	Primary, Secondary, Secondary

When an invalid transfer occurs during the AUTO-RETRY sequence, a RETRY interrupt is issued to the subsystem. An INVALID TRANSFER interrupt is issued only after failure of the last retry attempt.

Discrete Interrupts

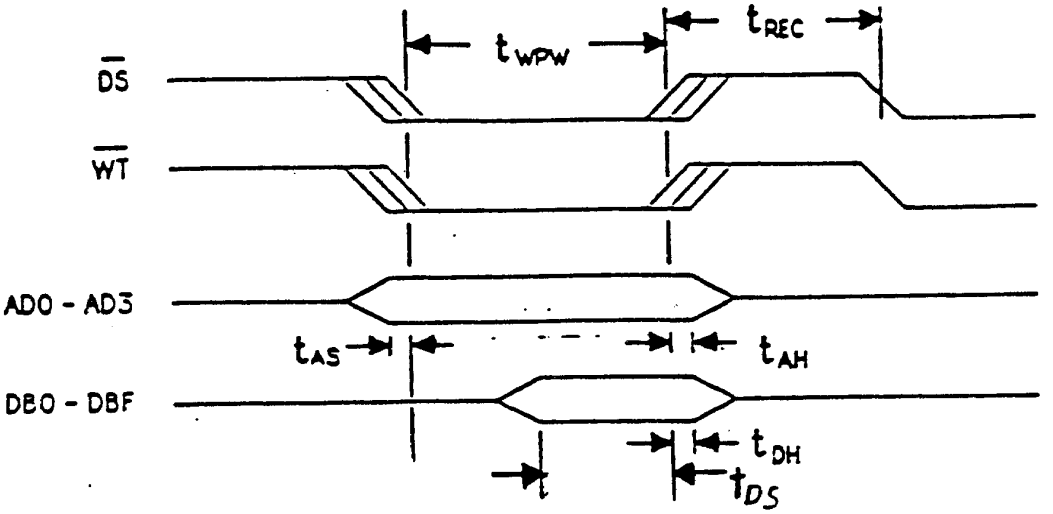
Four discrete interrupt output signals are available to the subsystem in BC mode. Any or all of these may be used depending on subsystem requirements. All of the interrupts are low going, 160 nSec (nom) wide pulse signals. The empty flag for the output buffer BUFFEF is also made available to the subsystem. When high, it indicates that the output buffer is not empty.

The interrupt functions are summarized in the table below.

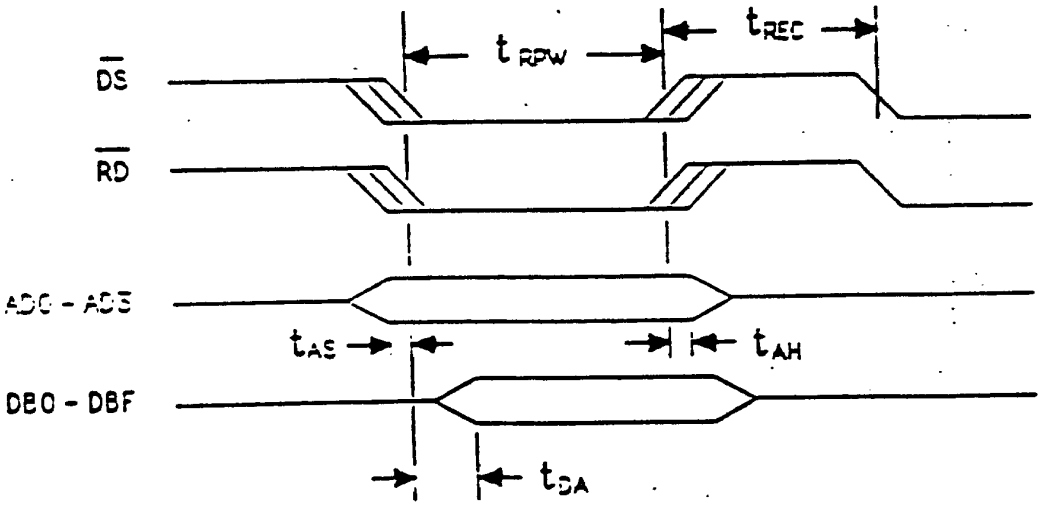
DISCRETE INTERRUPTS

NAME	FUNCTION
$\overline{\text{VALID TRANSFER}}$	Issued in response to a TRIGGER TRANSACTION I/O command. Indicates that the transaction has been completed SUCCESSFULLY.
$\overline{\text{INVALID TRANSFER}}$	Issued in response to a TRIGGER TRANSACTION I/O command. Indicates that the transaction has NOT been completed successfully.
$\overline{\text{RETRY}}$	Issued in response to a TRIGGER TRANSACTION I/O command. Indicates that the transaction has NOT been completed successfully and that another attempt will be made (AUTO-RETRY).
$\overline{\text{DONE}}$	Issued in response to an EXECUTE I/O command. For a RAM to OUTPUT FIFO transfer, it indicates that the complete 32 word message block (subaddress) has been loaded into the OUTPUT FIFO. For an INPUT FIFO to RAM transfer, it indicates that the full message (1 to 32 words) has been loaded into RAM.
$\overline{\text{BUFFEF}}$	This flag may be used to speed up the transfer of data from RAM to the subsystem. This flag will go HIGH when the first word is loaded into the OUTPUT FIFO. That word may be read at this time. Subsequent data words may be read each time this flag returns high. The OUTPUT FIFO is loaded internally at a rate of 0.5 uSec/word.

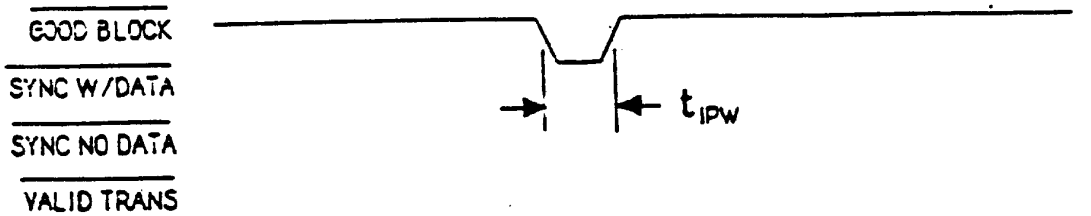
I/O Write Timing



I/O Read Timing



Output Interrupts

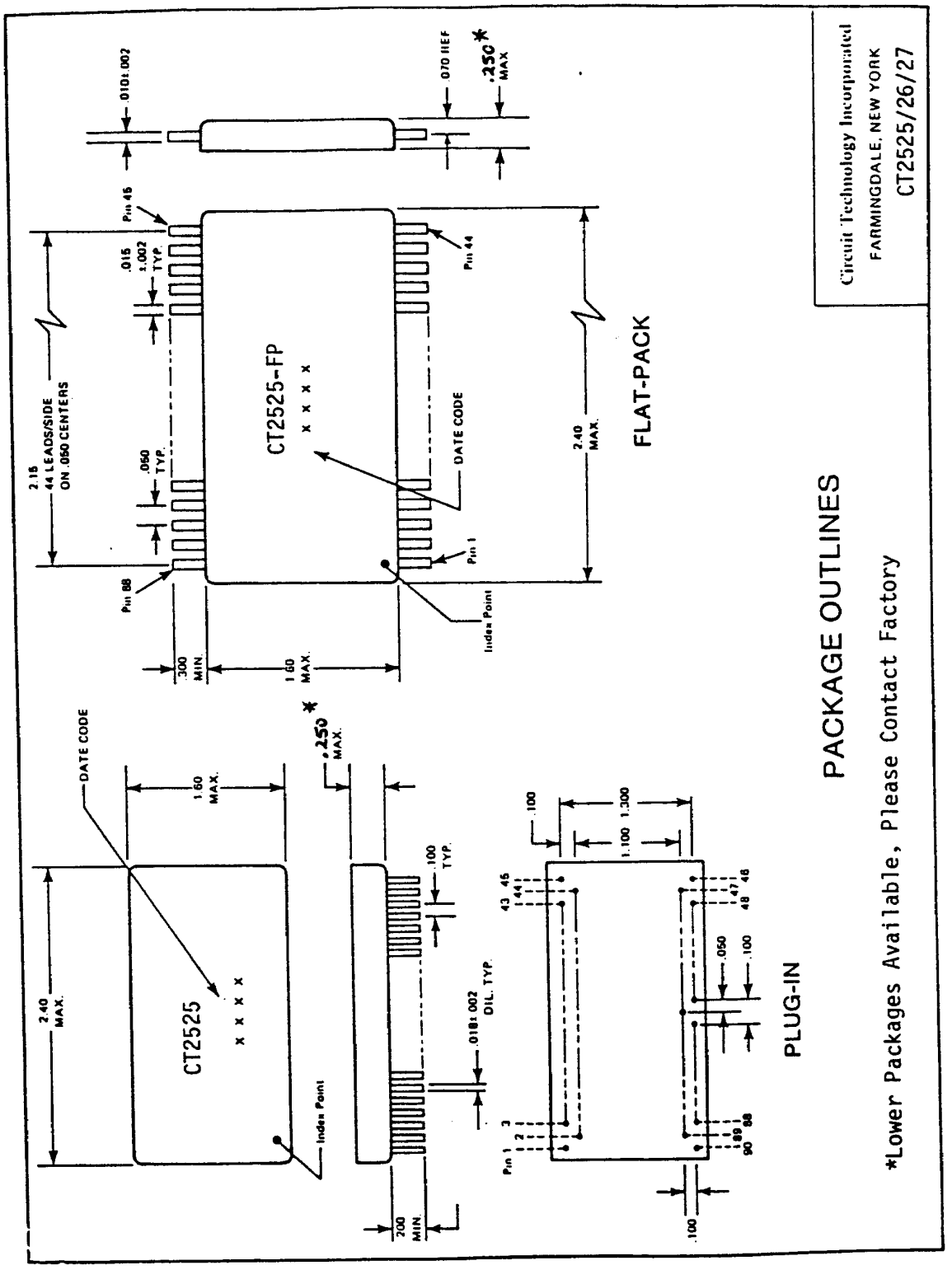


CT1800M/CT2525 Subsystem Interface Timing

AC ELECTRICAL CHARACTERISTICS
($-55°C \leq T_A \leq +125°C$) V_{cc} = +5.0 VOLTS ± 10%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{WPW}	WRITE PULSE WIDTH	50			nsec	1,2
t_{RPW}	READ PULSE WIDTH	50			nsec	3
t_{AS}	ADDRESS SET UP TIME	5			nsec	
t_{AH}	ADDRESS HOLD TIME	5			nsec	
t_{DS}	WRITE DATA SET UP TIME	5			nsec	
t_{DH}	WRITE DATA HOLD TIME	0			nsec	2
t_{DA}	READ DATA ACCESS TIME			50	nsec	
t_{IPW}	INTERRUPT PULSE WIDTH	140	160	180	nsec	
t_{REC}	RECOVERY TIME	100			nsec	

NOTES:
1. Write pulse width t_{WPW} is the time when both $\overline{DS}$ and $\overline{WT}$ are simultaneously low. Either $\overline{DS}$ or $\overline{WT}$ may go low or return high first.
2. Write hold time: t_{DH} = 0 for $t_{WPW} \geq 450$ nsec
   t_{DH} = 10 nsec for 50 nsec < t_{WPW} < 450 nsec.
3. Read pulse time t_{RPW} is the time where both $\overline{DS}$ and $\overline{RD}$ are simultaneously low. Either $\overline{DS}$ or $\overline{RD}$ may go low or return high first.



CIRCUIT TECHNOLOGY INC. 160 Smith St., Farmingdale, NY 11735 516-293-8686 TWX: 510-224-6555 CA: 213-374-7446

DS-1800/2.5M/12-85

C1553/2K/22

FUNCTIONAL DIAGRAM

CTI

CT2525/26/27
MIL-STD-1553
SINGLE PACKAGE SOLUTION

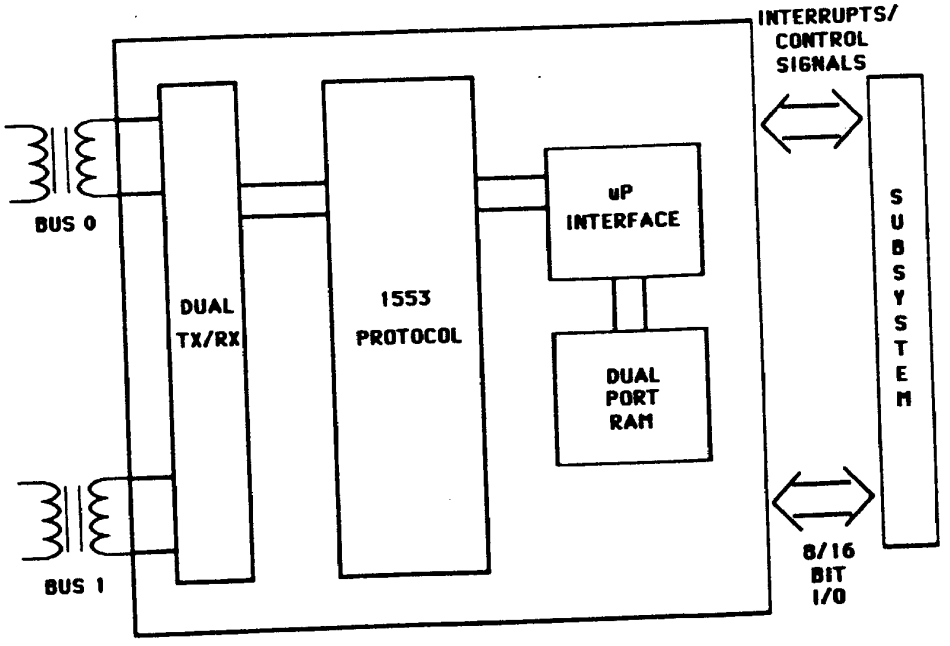
ADVANCE INFORMATION

GENERAL DESCRIPTION

The CT2525 provides a complete one package interface between the MIL-STD-1553 bus and all microprocessor systems. The hybrid provides all data buffers and control registers to function as a Bus Controller or Remote Terminal. Control of the hybrid by the subsystem is through simple I/O port commands. Internal hybrid logic removes all critical timing imposed on a typical subsystem, thereby simplifying the implementation of this interface.

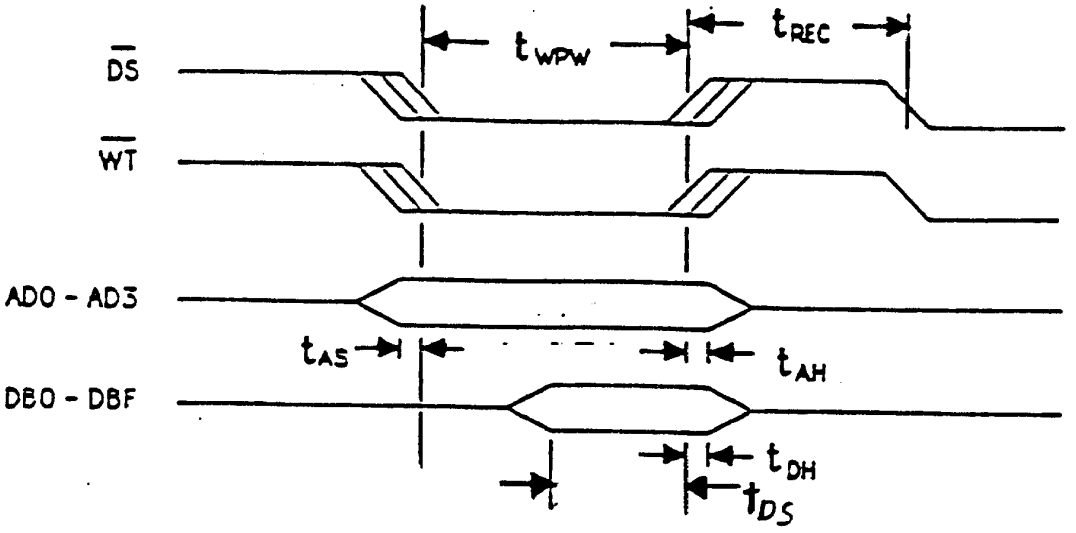
FEATURES

- Incorporates transceivers, Protocol and sub-system Interface components into a single Hybrid Package
- Functions as a Remote Terminal or Bus Controller
- Interfaces to uP as a simple peripheral unit
- Available with several options for transceivers: ± 15V, ± 12V and + 5V only
- Provides Fully Buffed Dual Port RAM storage for transmit and receive sub-addresses

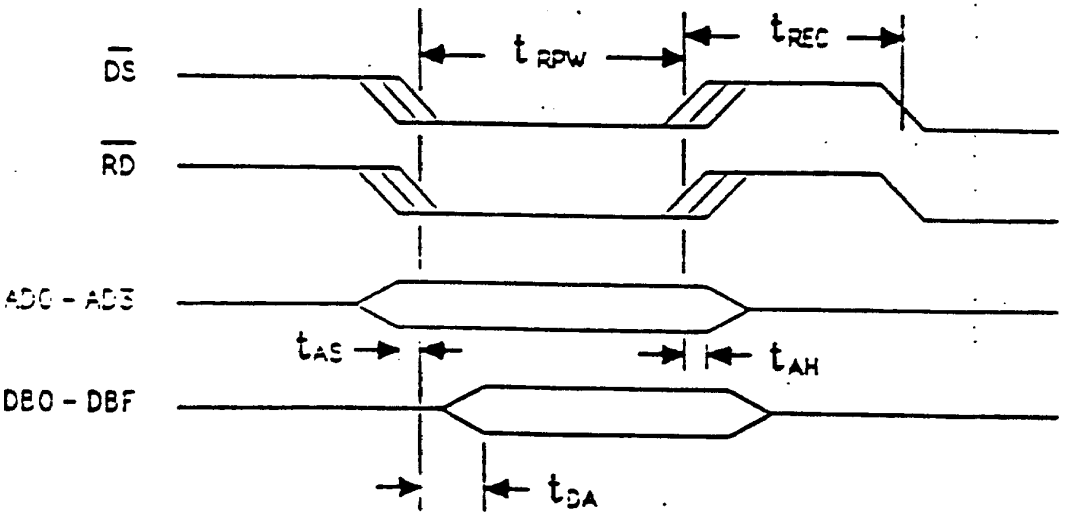


CT2525

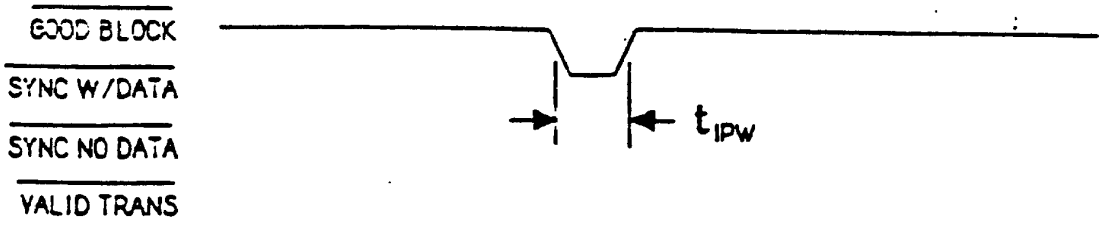
I/O Write Timing



I/O Read Timing



Output Interrupts



CT1800M/CT2525 **Subsystem Interface Timing**

C1553/1760/27
FUNCTIONAL DIAGRAM

CTI

Circuit Technology Incorporated

Main Office: Circuit Technology Incorporated, 160 Smith Street, Farmingdale, NY 11735 (516) 293-8686 TWX: 510-224-6555
Irvine, CA: Circuit Technology Incorporated, P.O. Box 18107, Irvine, CA 92713 (714) 559-1075
Manhattan Beach, CA: Circuit Technology Incorporated, P.O. Box 72, Manhattan Beach, CA 90266 (213) 374-7446
Newbury Park, CA: Circuit Technology Incorporated, P.O. Box 487, Newbury Park, CA 91320 (213) 991-5773
Minneapolis, MN: Circuit Technology Incorporated, 7216 Boone Avenue North, Minneapolis, MN 55428 (612) 535-7673
European Office: Circuit Technology, P.O. Box 133, Camberly, Surrey, GU16 5PY, United Kingdom 44-276-23684