DGP201A
Precision Monolithic Quad SPST CMOS Analog Switch

Siliconix incorporated

FEATURES

- ± 22 Volt Input Range
- 10 Ω Max $\Delta r_{DS(ON)}$ Any Combination Of Switches
- 0.25 nA Max At 25°C, ± 15 V
- 50 pC Max Charge Transfer Error
- Tested Δt_{ON} and $\Delta t_{OFF} \leq$ 50 ns

BENEFITS

- Fully Tested Around ± 10.8, ± 16.5 and ± 22 V Supplies
- Pin Compatible With DG201A – Simplifies Upgrades
- Simplifies Worst Case Analysis
- TTL Compatible

APPLICATIONS

- Precision Data Acquisition
- Automatic Test Equipment
- Radar Systems

DESCRIPTION

The DGP201A is a precision quad single-pole single-throw analog switch designed for critical applications requiring improved performance over that obtainable with the popular DG201A. Produced on an enhanced proprietary high voltage process, the DGP201A has been fully specified with input analog signals to ±22 V making it an ideal choice for high voltage applications or where the added margin of safety over traditional switches is of importance.

In addition to the low current leakage specifications, charge injection, $\Delta r_{DS(ON)}$, Δt_{ON} and Δt_{OFF} have been tested and guaranteed at various input voltages to assure worst case error analysis. An epitaxial layer prevents latchup.

Packaging for this device includes a 16-Pin CerDIP, plastic, and small outline options. Performance grades include military, A suffix (–55 to 125°C) and industrial, D suffix (–40 to 85°C) temperature ranges. Additionally, LCC packaging is available.

PIN CONFIGURATION AND FUNCTION BLOCK DIAGRAM

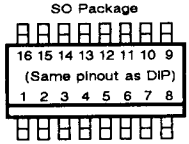
Four SPST Switches per Package

Truth Table

LOGIC	SWITCH
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

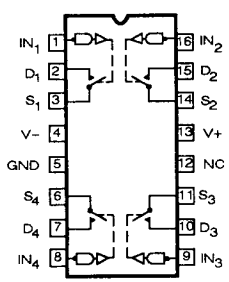
SO Package



Top View

Order Number:
DGP201ADY

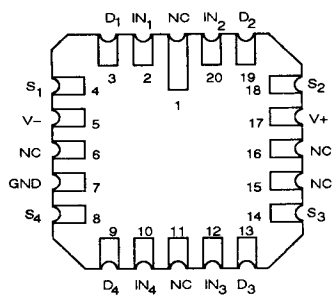
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DGP201AAK
DGP201AAK/883
Plastic: DGP201ADJ

Leadless Chip Carrier



Top View

Order Number:
DGP201AAZ/883

Siliconix has improved its high voltage metal gate CMOS process to allow for lower variation performance. Additionally, through dramatic improvements in automated testing technology, specifications and limits that were previously untestable are now 100% tested and specified on the DGP201A data sheet.

The data sheet specification tables are in a new format as well. The format is that of a military drawing, where all specifications are 100% tested, eliminating any uncertainty about what is actually tested. Many parameters that were previously listed as "typical" or "guaranteed by design" are now 100% tested with minimum and maximum values, so that a worst case design can be realized.

For example, charge transfer error (or charge injection) was listed only as a typical value in the DG201A data sheet, and no maximum value was guaranteed. A maximum limit of 50 pico Coulombs has been established on the data sheet, and this value is 100% tested. This allows the design engineer to design precision switching circuits, such as sample-and-hold amplifiers, with fixed limits for the charge compensation circuit.

The DGP201A also specifies certain parameters that have never been seen on a DG201A standard product data sheet in min/max or typical form. An important example of this is the variation of the switching time over all channels, which is specified with a maximum of 50 ns. The variation of "ON" resistance is similarly specified and 100% tested to be less than 10 ohms over six different drain voltage and source current conditions, over all four channels tested, resulting in 24 different readings. This specification is necessary for determining the worst-case distortion and signal level variation due to differences in channel resistance and ON resistance modulation effects.

Leakage currents are specified and tested to new lower limits at both room temperature and over the full temperature range. For example, the industrial range devices' leakages have been reduced from 100 nA (over temp) on the DG201A to 1 nA (over temp) on the DGP version. Additionally, the leakages are specified at the extremes of the operating ranges (e.g. ±16.5 V instead of ±15 V), where the leakages tend to be the highest. This is essential for designs where worst-case leakage must be well known, such as precision instruments and sample-and-hold amplifiers.

The operating range of the DGP201A is increased beyond that of the DG201A, up to ±22 V and down to ±10.8 V. This allows the switches to have guaranteed performance limits with power supplies as low as ±12 V (±10%).

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ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-[1]

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[1] V_S, V_D ..... (V-) - 2 V to (V+) + 2 V
..... or 30 mA, whichever occurs first

Continuous Current (Any Terminal) ..... 30 mA

Current, S or D (Pulsed 1 ms 10% duty) ..... 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*

16-Pin Plastic DIP** ..... 450 mW

16-Pin CerDIP*** ..... 900 mW

20-Pin LCC**** ..... 750 mW

16-Pin SO***** ..... 600 mW

* All leads welded or soldered to PC board.

** Derate 6 mW/°C above 75°C.

*** Derate 12 mW /°C above 75°C.

**** Derate 10 mW/°C above 75°C.

***** Derate 7.6 mW /°C above 75°C.

1 Signals on Sx, Dx, or INx exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, GND = 0 V, V_{IN} = 2.4 V, 0.8 V [e]		LIMITS 1=25°C 2=125,85°C 3=−55,−40°C TEMP	TYP [d]	A SUFFIX −55 to 125°C MIN [b]	A SUFFIX −55 to 125°C MAX [b]	D SUFFIX −40 to 85°C MIN [b]	D SUFFIX −40 to 85°C MAX [b]	UNIT
SWITCH										
Analog Signal Range [c]	V_{ANALOG}			1,2,3		−15	15	−15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V+ = 13.5 V, V− = −13.5 V, I_S = 1 mA, V_D = ±10.0 V		1,3 2	115		175 250		175 250	Ω
		V+ = 10.8 V, V− = 10.8 V, I_S = 1 mA, V_D = ±7.5 V, V_{IN} = 0.4 V		1,3 2	145		250 325		250 325	
		V+ = 22 V, V− = −22 V, I_S = 1 mA, V_D = ±15 V		1,3 2	85		125 225		125 225	
Delta Drain-Source ON Resistance	$\Delta r_{DS(ON)}$	V_D = +5, 0, −5 V, I_S = ±1 mA, V_{IN} = 0.8 V Worst Combination		1,3 2	5		10 15		10 15	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5 V, V− = −16.5 V	V_D = −15.5 V, V_S = −15.5 V	1 2	0.015	−0.25 −20	0.25 20	−0.25 −2	0.25 2	nA
			V_D = +15.5 V, V_S = +15.5 V	1 2	0.015	−0.25 −20	0.25 20	−0.25 −2	0.25 2	
		V+ = 22 V, V− = −22 V	V_D = −21 V, V_S = −21 V	1 2	0.15	−2 −200	2 200	−2 −20	2 20	
			V_D = +21 V, V_S = +21 V	1 2	0.15	−2 −200	2 200	−2 −200	2 200	
		V_D = −5 V, V_S = −5 V		2		−10	10	−2	2	
		V_D = +5 V, V_S = +5 V		2		−10	10	−2	2	
Source OFF Leakage Current	$I_{S(OFF)}$	V+ = 13.5 V, V− = −13.5 V	V_D = −12.5 V, V_S = +12.5 V	1 2	−0.01		0.25 10		0.25 1	
			V_D = +12.5 V, V_S = −12.5 V	1 2	−0.01	−0.25 −10		−0.25 −1		
		V+ = 16.5 V, V− = −16.5 V	V_D = −15.5 V, V_S = +15.5 V	1 2	0.015		0.25 10		0.25 1	
			V_D = +15.5 V, V_S = −15.5 V	1 2	−0.015	−0.25 −10		−0.25 −1		
		V+ = 22 V, V− = −22 V, V_{IN} = 3 V	V_D = −21 V, V_S = +21 V	1 2	0.15		1 100		1 10	
			V_D = +21 V, V_S = −21 V	1 2	−0.15	−1 −100		−1 −10		
		V_D = −5 V, V_S = +5 V		2			5		1	
		V_D = +5 V, V_S = −5 V		2		−5		−1		

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, GND = 0 V, V_{IN} = 2.4 V, 0.8 V [e]		LIMITS 1=25°C 2=125,85°C 3=−55,−40°C		A SUFFIX −55 to 125°C		D SUFFIX −40 to 85°C		UNIT
				TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
SWITCH (Cont'd)										
Drain OFF Leakage Current	$I_{D(OFF)}$	V+ = 13.5 V, V− = −13.5 V	V_D = −12.5 V, V_S = +12.5 V	1	0.01		0.25		0.25	nA
				2			10		1	
			V_D = +12.5 V, V_S = −12.5 V	1	−0.01	−0.25		−0.25		
				2		−10		−1		
		V+ = 16.5 V, V− = −16.5 V	V_D = −15.5 V, V_S = +15.5 V	1	0.015		0.25		0.25	
				2			10		1	
			V_D = +15.5 V, V_S = −15.5 V	1	−0.015	−0.25		−0.25		
				2		−10		−1		
		V+ = 22 V, V− = −22 V, V_{IN} = 3 V	V_D = −21 V, V_S = +21 V	1	0.15		1		1	
				2			100		10	
			V_D = +21 V, V_S = −21 V	1	−0.15	−1		−1		
				2		−100		−10		
		V_D = −5 V, V_S = +5 V		2			5		1	
		V_D = +5 V, V_S = −5 V		2		−5		−1		
INPUT										
Input current with V_{IN} HIGH	I_{IH}	V+ = 22 V, V− = −22 V, V_{IN} under test = 2.4 V		1	−0.005	−0.5	0.5	−0.5	0.5	µA
				2		−5	5	−5	5	
		V+ = 22 V, V− = −22 V, V_{IN} under test = 22 V		1	−0.005	−0.5	0.5	−0.5	0.5	
				2		−5	5	−5	5	
Input current with V_{IN} LOW	I_{IL}	V+ = 22 V, V− = −22 V, V_{IN} under test = 0 V		1	0.005	−0.5	0.5	−0.5	0.5	
				2		−5	5	−5	5	
DYNAMIC										
Turn-ON Time	t_{ON}	See Switching Time Test Circuits		1	450		600		600	ns
				2,3			800		800	
Turn-OFF Time	t_{OFF}			1	320		450		450	
				2,3			600		600	
Delta t_{ON}	Δt_{ON}	Worst Combination among channels of the t_{ON} measurements		1	30		50		50	
				2,3			100		100	
Delta t_{OFF}	Δt_{OFF}	Worst Combination among channels of the t_{OFF} measurements		1	30		50		50	
				2,3			100		100	
Charge Injection	Q	R_{gen} = 0 Ω, C_L = 10 nF	V_{gen} = 0 V	1	25		50		50	pC
			V_{gen} = ± 10 V	1	33		100		100	
Source OFF Capacitance [d]	$C_{S(OFF)}$	f = 1 MHz, V_S = 0 V		1	4.5					pF

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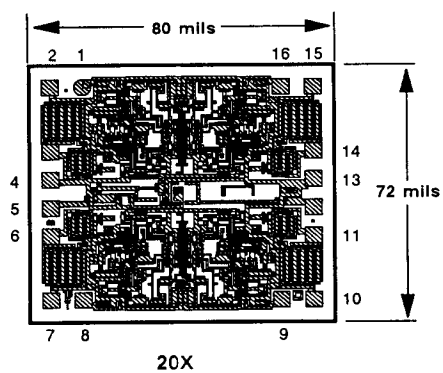
ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V− = −15 V, GND = 0 V, V_{IN} = 2.4 V, 0.8 V [e]	LIMITS 1=25°C 2=125,85°C 3=−55,−40°C TEMP	TYP [d]	A SUFFIX −55 to 125°C MIN [b]	A SUFFIX −55 to 125°C MAX [b]	D SUFFIX −40 to 85°C MIN [b]	D SUFFIX −40 to 85°C MAX [b]	UNIT
DYNAMIC (Cont'd)									
Drain OFF Capacitance [d]	$C_{D(OFF)}$	f = 1 MHz, V_S = 0 V	1	5.5					pF
Channel ON Capacitance [d]	$C_{D(ON)}$ + $C_{S(ON)}$	f = 1 MHz, V_S = 0 V	1	15					pF
Crosstalk (Channel-to-Channel)		R_L = 50 Ω C_L = 5 pF f = 1 MHz	1	95					dB
OFF Isolation		R_L = 50 Ω C_L = 5 pF f = 1 MHz	1	80					dB
SUPPLY									
Positive Supply Current	I+	V_{IN} = 0 or 5 V $V_\pm$ = ±16.5 V	1 2	0.8		1.5 2.5		1.5 2.5	mA
Negative Supply Current	I−	V_{IN} = 0 or 5 V $V_\pm$ = ±16.5 V	1 2	0.26	−1 −2		−1 −2		mA

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.

DIE TOPOGRAPHY



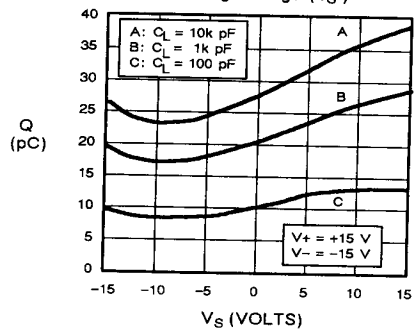
20X

ICMCB
8 Capacitors
9 Resistors
49 P-channel enhancement MOSFET
45 N-channel enhancement MOSFET

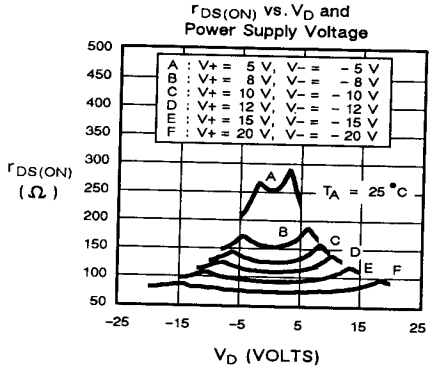
Pad No.	Function
1	Input 1
2	Drain 1
3	Source 1
4	V−
5	GND
6	Source 4
7	Drain 4
8	Input 4
9	Input 3
10	Drain 3
11	Source 3
13	V+ (Substrate)
14	Source 2
15	Drain 2
16	Input 2

TYPICAL CHARACTERSITICS

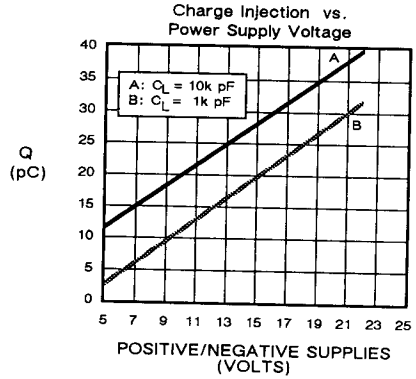
Charge Injection vs. Analog Voltage (V_S)



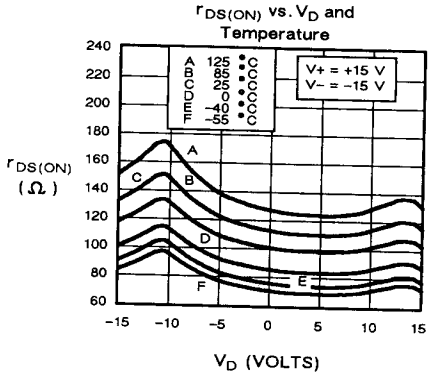
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



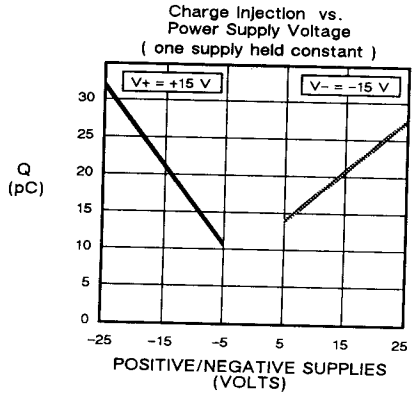
Charge Injection vs. Power Supply Voltage



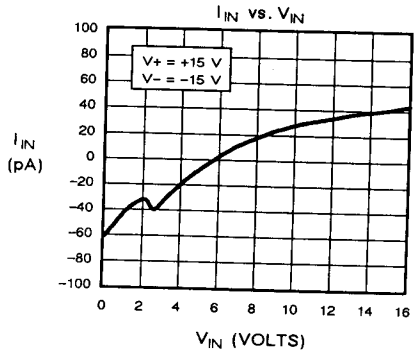
$r_{DS(ON)}$ vs. V_D and Temperature



Charge Injection vs. Power Supply Voltage (one supply held constant)



I_{IN} vs. V_{IN}



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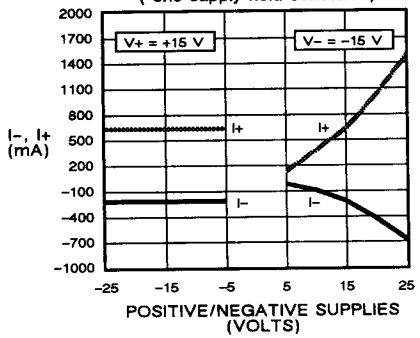
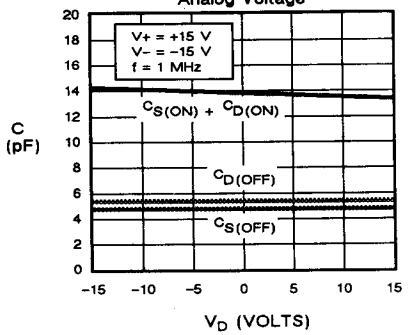
TYPICAL CHARACTERSITICS

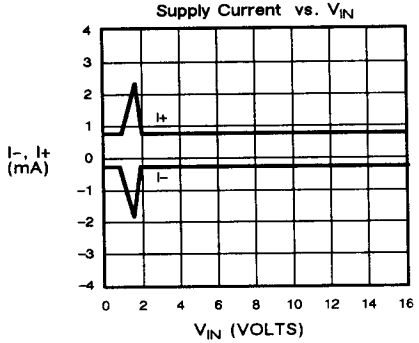
Supply Current vs. Supply Voltage
(one supply held constant)



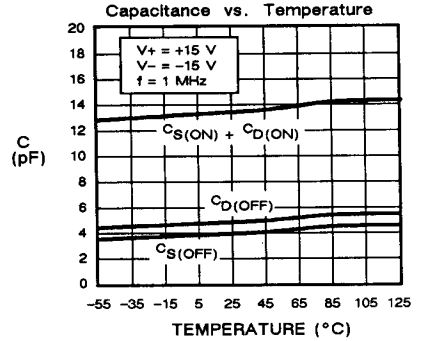
Capacitance vs. Analog Voltage



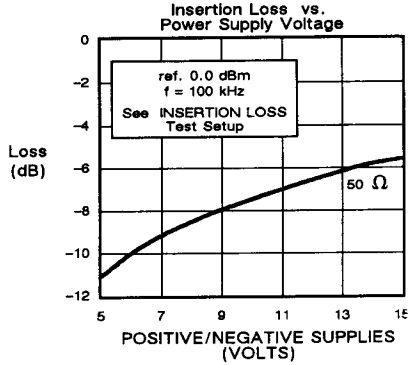
Supply Current vs. V_{IN}



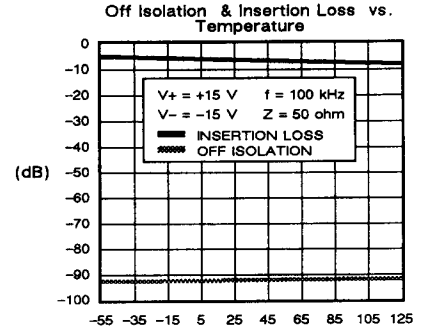
Capacitance vs. Temperature



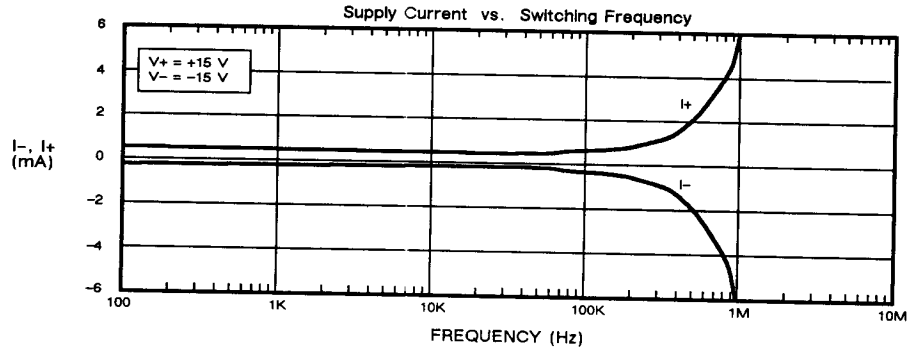
Insertion Loss vs. Power Supply Voltage

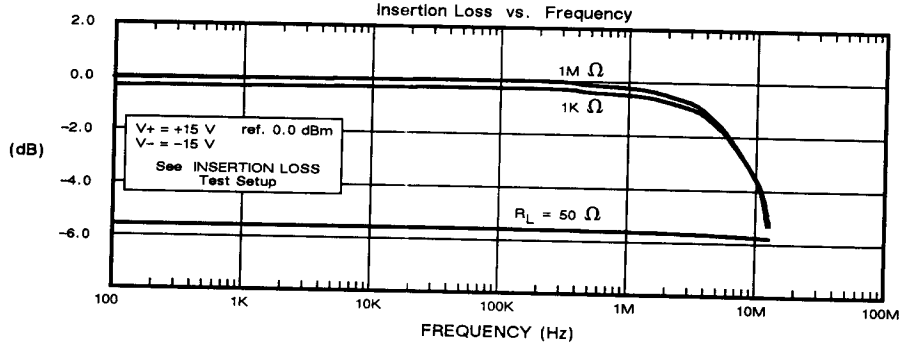


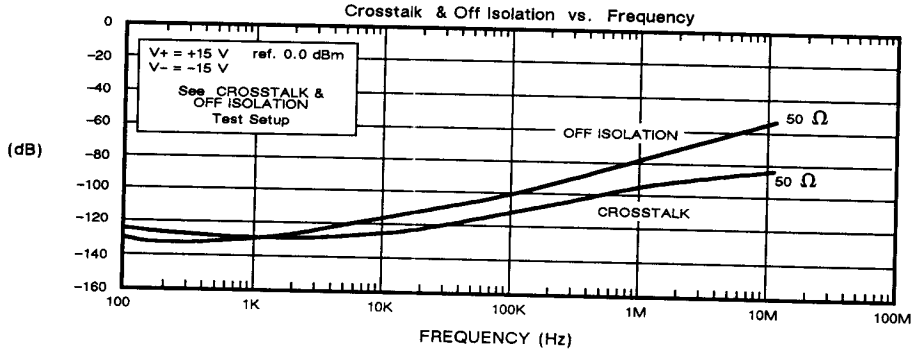
Off Isolation & Insertion Loss vs. Temperature



TYPICAL CHARACTERSITICS







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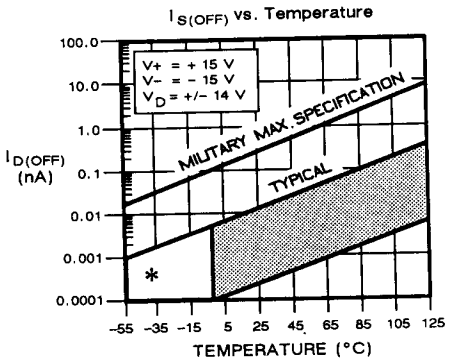
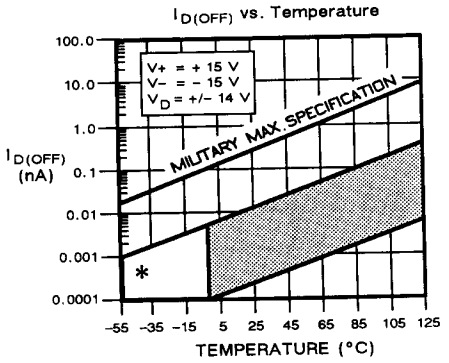
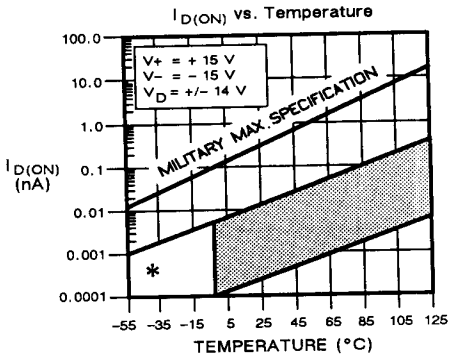
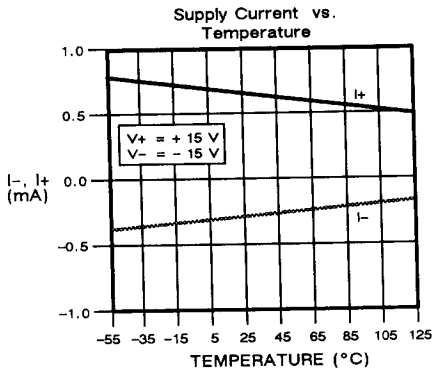
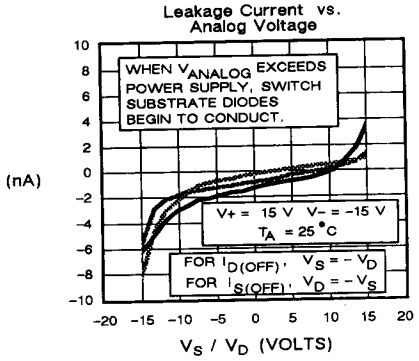
TYPICAL CHARACTERSITICS

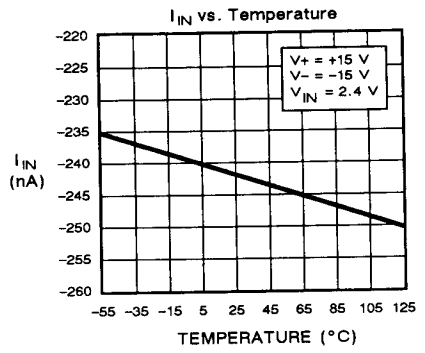








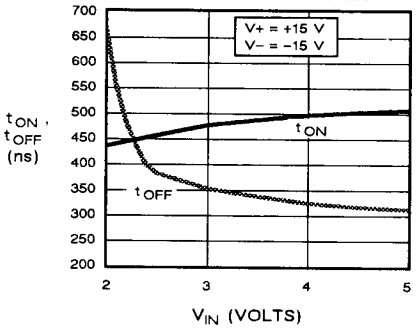




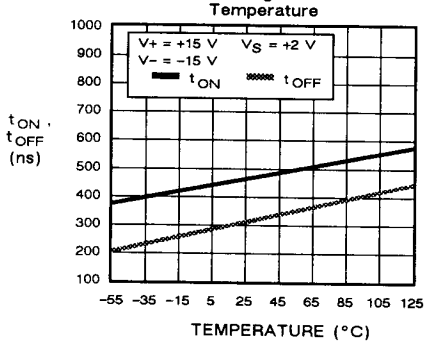
* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

TYPICAL CHARACTERSITICS

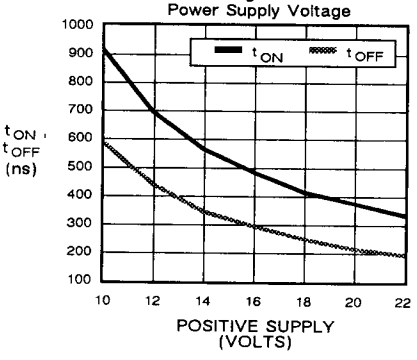
Switching Time vs. Input Logic Voltage (V_{IN})



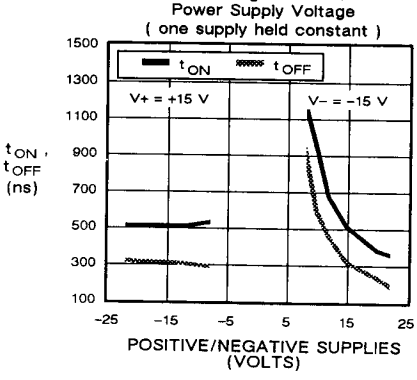
Switching Time vs. Temperature



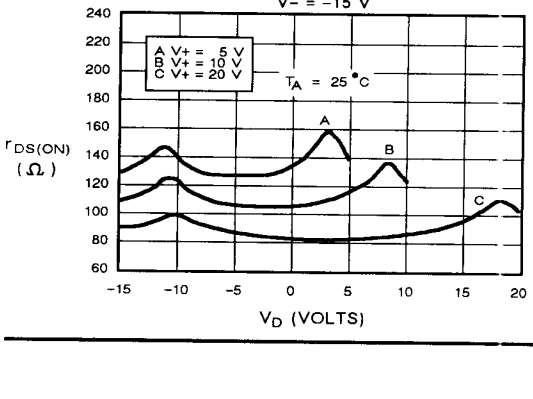
Switching Time vs. Power Supply Voltage



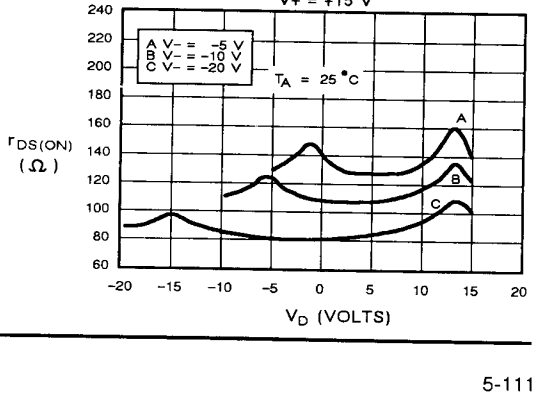
Switching Time vs. Power Supply Voltage (one supply held constant)



$r_{DS(ON)}$ vs. V_D and Positive Supply Voltage V− = −15 V

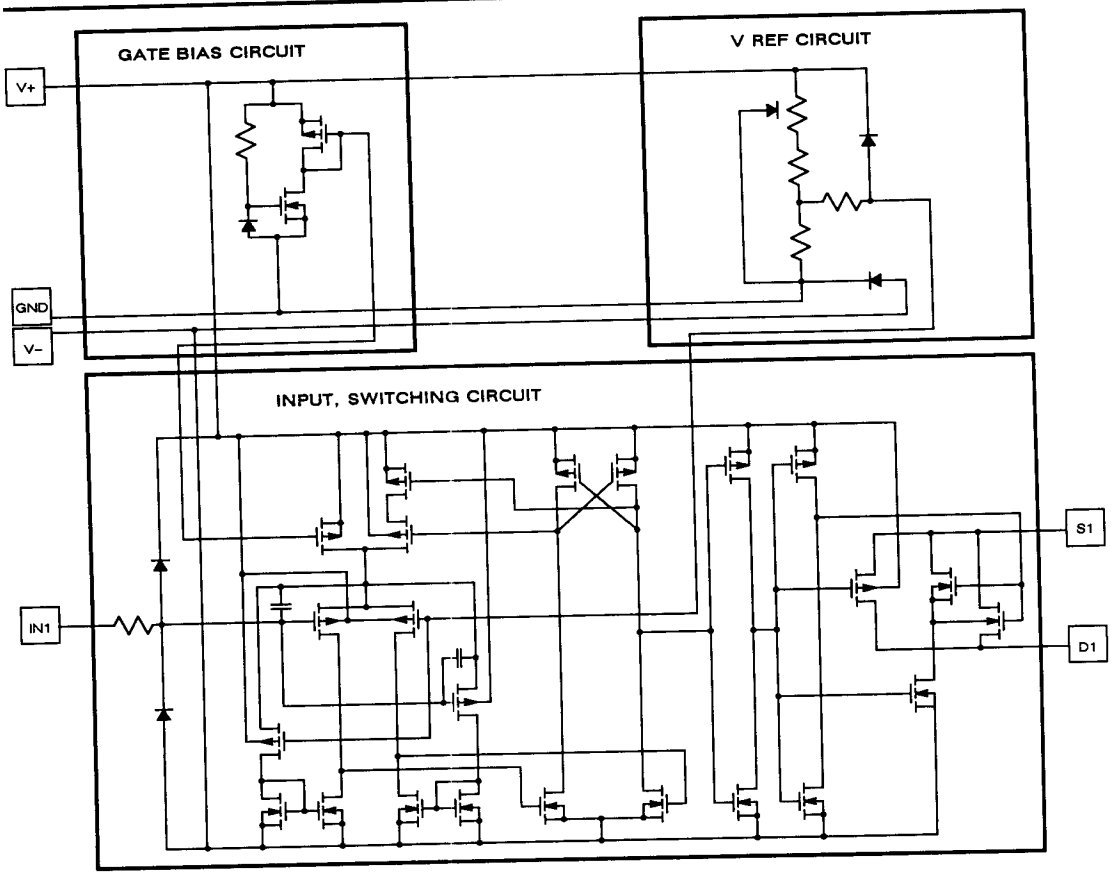


$r_{DS(ON)}$ vs. V_D and Negative Supply Voltage V+ = +15 V



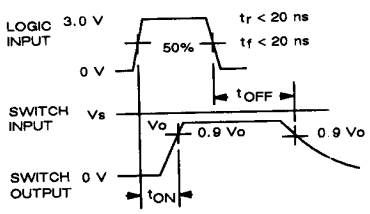
5

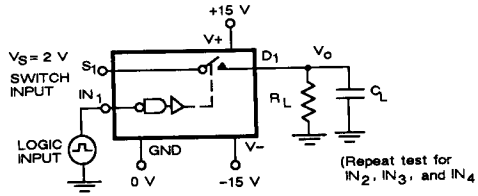
SCHEMATIC DIAGRAM (Typical Channel)



SWITCHING TIME TEST CIRCUITS

Vo is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

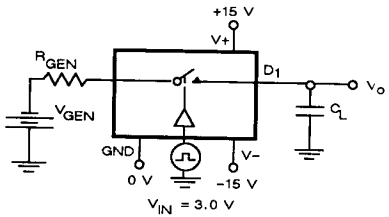


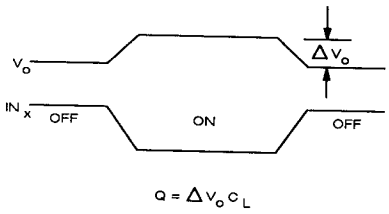


For load conditions, See Electrical Characteristics
C_L (includes fixture and stray capacitance)

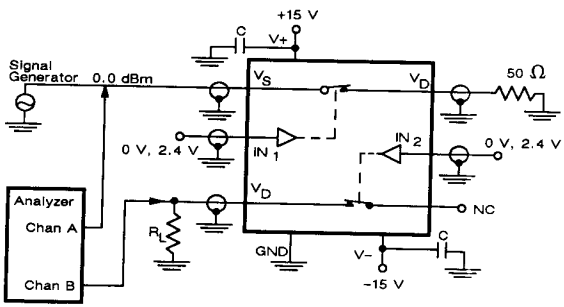
$$V_o = V_S \frac{R_L}{R_L + R_{DS(ON)}}$$

CHARGE INJECTION TEST CIRCUIT



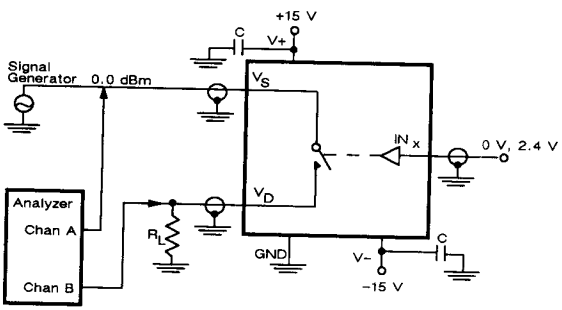


CROSSTALK TEST CIRCUIT



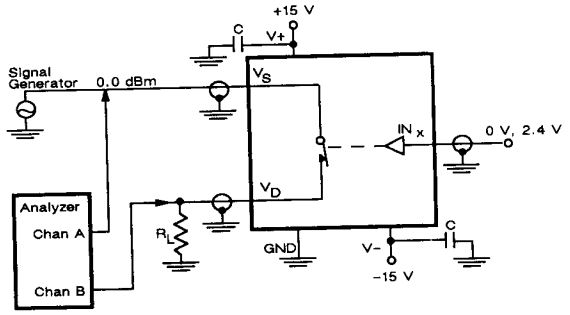
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

OFF ISOLATION TEST CIRCUIT



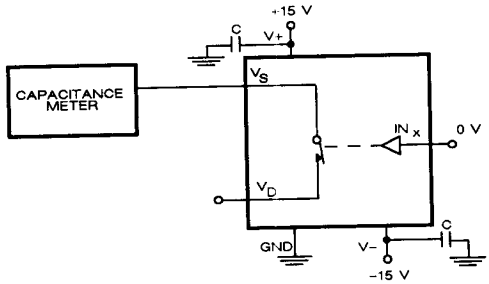
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

INSERTION LOSS TEST CIRCUIT



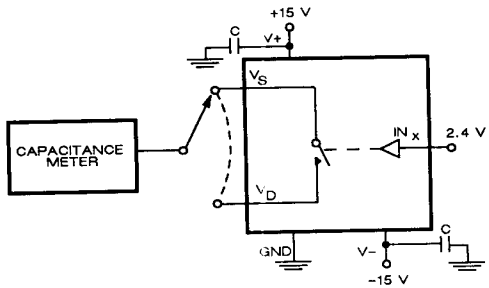
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

SOURCE/DRAIN ON CAPACITANCE



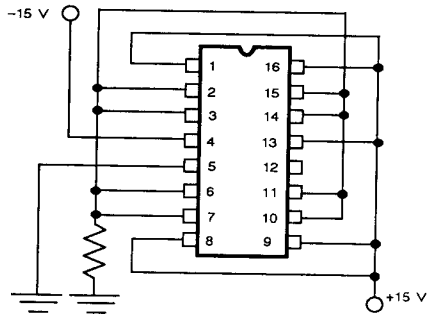
METER
BOONTON 72BD Capacitance Meter or equivalent

SOURCE/DRAIN OFF CAPACITANCE

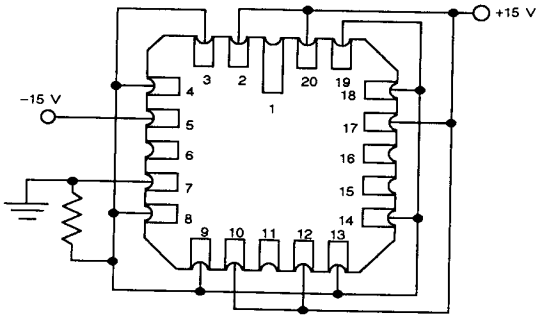


METER
BOONTON 72BD Capacitance Meter or equivalent

BURN-IN CIRCUIT



Note: All Resistors are 10 k Ω unless otherwise specified



Note: LCC package uses same circuit and conditions as the DIP

PIN DESCRIPTION

SYMBOL	DESCRIPTION
S	An Analog Channel Input or Output
D	An Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply Voltage
V−	Negative Supply Voltage
GND	Digital Ground
V_L	Logic Supply Voltage

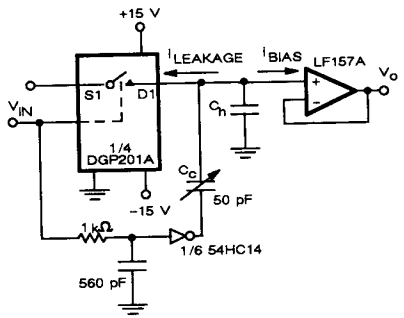
APPLICATION HINTS

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
5	−5	1.0/0.2	−5 to 5
10	−10	1.5/0.5	−10 to 10
15	−15	2.4/0.8	−15 to 15
22	−22	3.0/1.2	−22 to 22

APPLICATION HINTS (Cont'd)

Sample-and-Hold Circuit:

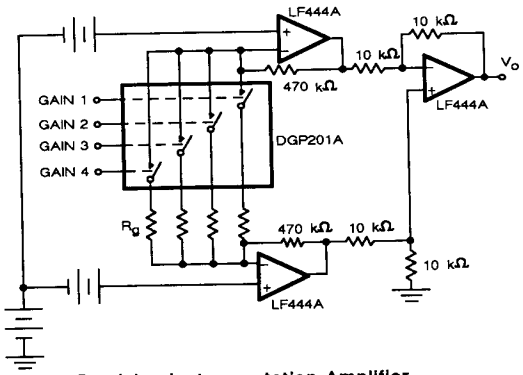
The DGP201A helps to reduce two common sources of error. First, its low charge injection reduces DC offset errors that would appear at the holding capacitor C_h. Second; its guaranteed low leakage current reduces the voltage drop rate during the holding period. When further charge injection is required, the Schmitt trigger (54HC14) and compensation capacitor C_C may be used to generate a charge of opposite polarity.



Sample-and-Hold Circuit

Precision Instrumentation Amplifier With Digitally Programmable Gains:

This instrumentation-quality differential amplifier can be designed for high gains. The input stages take advantage of the low leakage characteristics of the DGP201A to provide switching of the gain setting resistors (Rgx) without causing excessive DC offsets.



Precision Instrumentation Amplifier with Digitally Programmable Gains