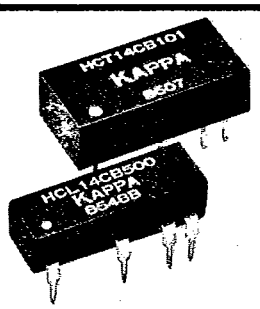
SERIES HCL14/HCT14 (14-PIN) 5-TAP

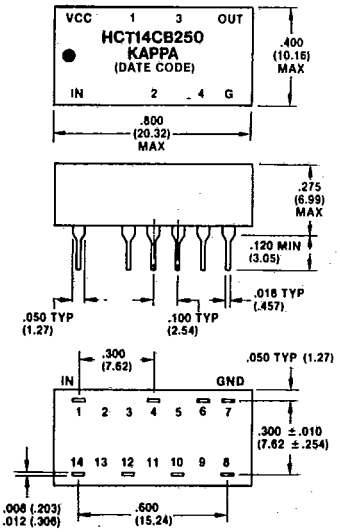
HCMOS DELAY LINES



FEATURES

- HCMOS logic interfaced
- Delays from 50 to 500 ns
- 5 equally-spaced taps
- Available in auto-insertable (HCL14) and standard (HCT14) packages
- Drives up to 10 LS TTL loads
- Compatible with standard LS TTL family

MARKINGS AND DIMENSIONS, in (mm)



RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage			4	5	6	V
V_{IH}	High-Level Input Voltage		4V	1.5			V
			5V	3.15			
			6V	4.2			
V_{IL}	Low-Level Input Voltage		4V	0		0.3	
			5V	0		0.9	V
			6V	0		1.2	
V_I	Input Voltage			0		V_{CC}	V
V_O	Output Voltage			0		V_{CC}	V
I_{IK}	Input Diode Current	$V_I<0$ or $V_I>V_{CC}$				±20	mA
I_{OK}	Output Diode Current	$V_O<0$ or $V_O>V_{CC}$				±20	mA
I_O	Continuous Output Current	$V_O=0$ to V_{CC}				±25	mA
T_A	Operating Free-Air Temperature			−40	+25	+85	°C

DC ELECTRICAL CHARACTERISTICS

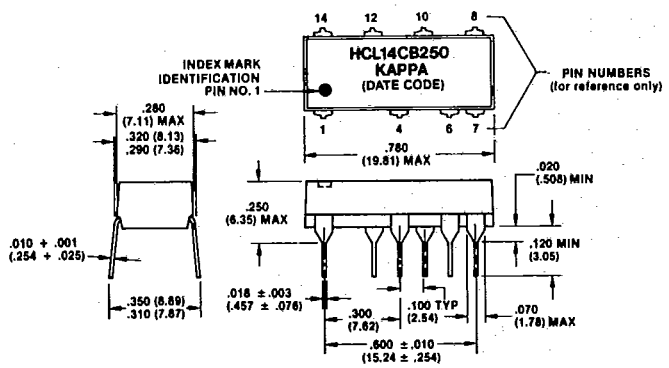
V_{OH}	High-Level Output Voltage	$V_I=V_{IH}$ or V_{IL}, $I_{OH}=-20\mu A$	4V	1.9			
			5V	4.4			
			6V	5.9			
		$V_I=V_{IH}$ or V_{IL}, $I_{OH}=4mA$	5V	3.84			V
		$V_I=V_{IH}$ or V_{IL}, $I_{OH}=5.2mA$	6V	5.34			
I_{OH}	High-Level Output Current	$V_I=V_{IH}$ or V_{IL}, $V_O=V_{CC}$	6V			5	μA
V_{OL}	Low-Level Output Voltage	$V_I=V_{IH}$ or V_{IL}, $I_{OL}=20\mu A$	4V			0.1	
			5V			0.1	
			6V			0.1	
		$V_I=V_{IH}$ or V_{IL}, $I_{OL}=4mA$	5V			0.4	V
		$V_I=V_{IH}$ or V_{IL}, $I_{OL}=5.2mA$	6V			0.4	
I_I	Input Current	$V_I=0$ to V_{CC}	6V			±1.0	μA
I_{CC}	Supply Current	$V_I=V_{CC}$ or 0, $I_O=0$	6V		5	10	mA
N	Fanout	$V_O=V_{OL}$ to V_{OH}, V_{CC} = min-to-max				10	LS TTL Loads

INPUT PULSE TEST CONDITIONS

E_{IN}	Pulse Voltage		3.1	3.2	3.3	V
T_{RI}	Pulse Risetime				2.0	ns
T_W	Pulse Width, in % of Total Delay Time		100			%
d	Duty Cycle			33.3	50	%

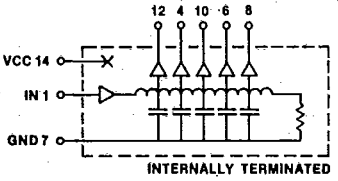
AC ELECTRICAL CHARACTERISTICS

T_{PLH}	Low-to-High Level Delay Time	$V_{CC}=TYP$, $T_A=TYP$, $E_{IN}=TYP$, $T_W=$ min, $d=T_{YP}$(1) (2) (4)		−5		+5	%
T_{RO}	Output Risetime	$V_{CC}=TYP$, $T_A=TYP$, $E_{IN}=TYP$, $T_W=$ min, $d=TYP$ (3) (4)			8		ns



Notes:

1. Delays measured at 1.5V level on leading edge only.
2. Delay tolerances: ±5% or ±2 ns, whichever is greater, referenced from input and guaranteed only under the following test conditions: $V_{CC}=TYP$, $T_A=TYP$, $E_{IN}=TYP$, $T_{RI}=$ max, $T_W=$ min, $P_{RR}=1MHz$ (or d/tw, whichever is less), R_L 1 megohm and C_L 2pf.
3. Risetime measured from 0.75V to 2.4V level.
4. Measured with no load on delay taps.
5. **Other delays also available upon request.**



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